PETRA IV.
NEW DIMENSIONS

DAMC-X3TIMER

Status report on the PETRA IV timing and synchronisation system developments

Hendrik Lippek *in behalf of the PETRA IV Timing & synchronisation project team (WP2.09)*
Hamburg 08.12.2021

HELMHOLTZ

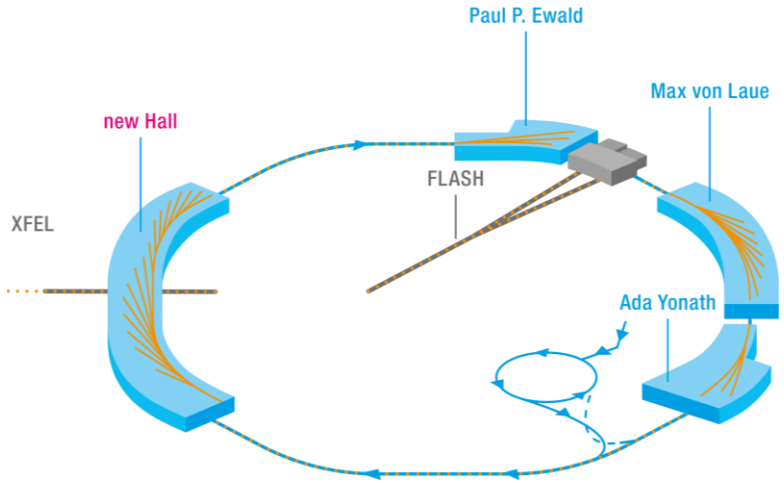
11th MTCA Workshop for Research and Industry

December 6-8, 2022
DESY - Hamburg

DESY.

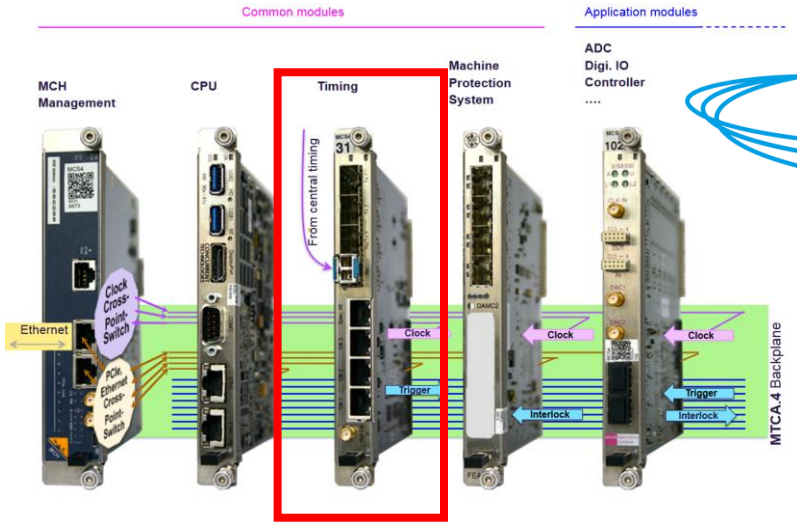
PETRA IV

Timeline & Scope



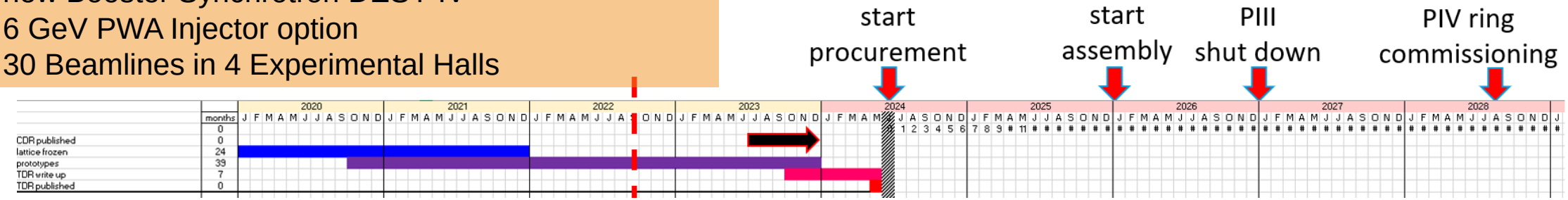
PETRA IV Highlights

- 4th Generation Light source
- low emittance: hor. 10-30 pm rad, vert. < 10 pm rad
- 500 MHz + 1.5GHz RF
- timing / brightness mode: 80 / 3840 Bunches
- new Booster Synchrotron DESY IV
- 6 GeV PWA Injector option
- 30 Beamlines in 4 Experimental Halls

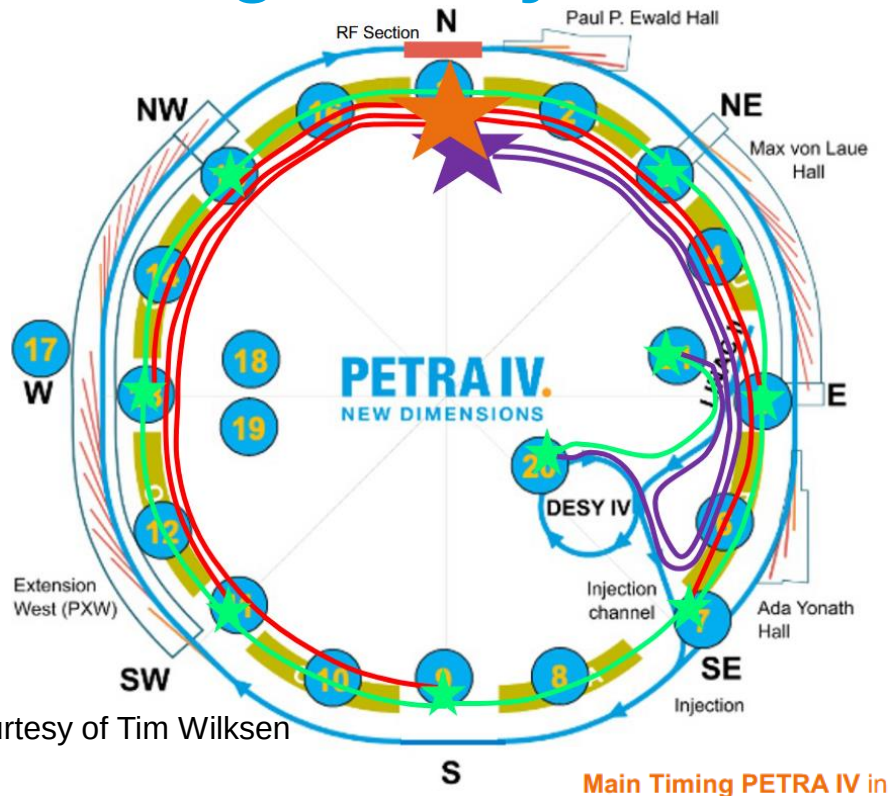


Timing System development for PETRA IV

- **MicroTCA.4 components will replace existing PETRA III hardware** for controls and diagnostics
- **Make use of experience from well-established Timing System concepts** as utilized at the FLASH and European XFEL facility
- **Keep the design flexible** to enhance functionality during life-cycle of PETRA IV

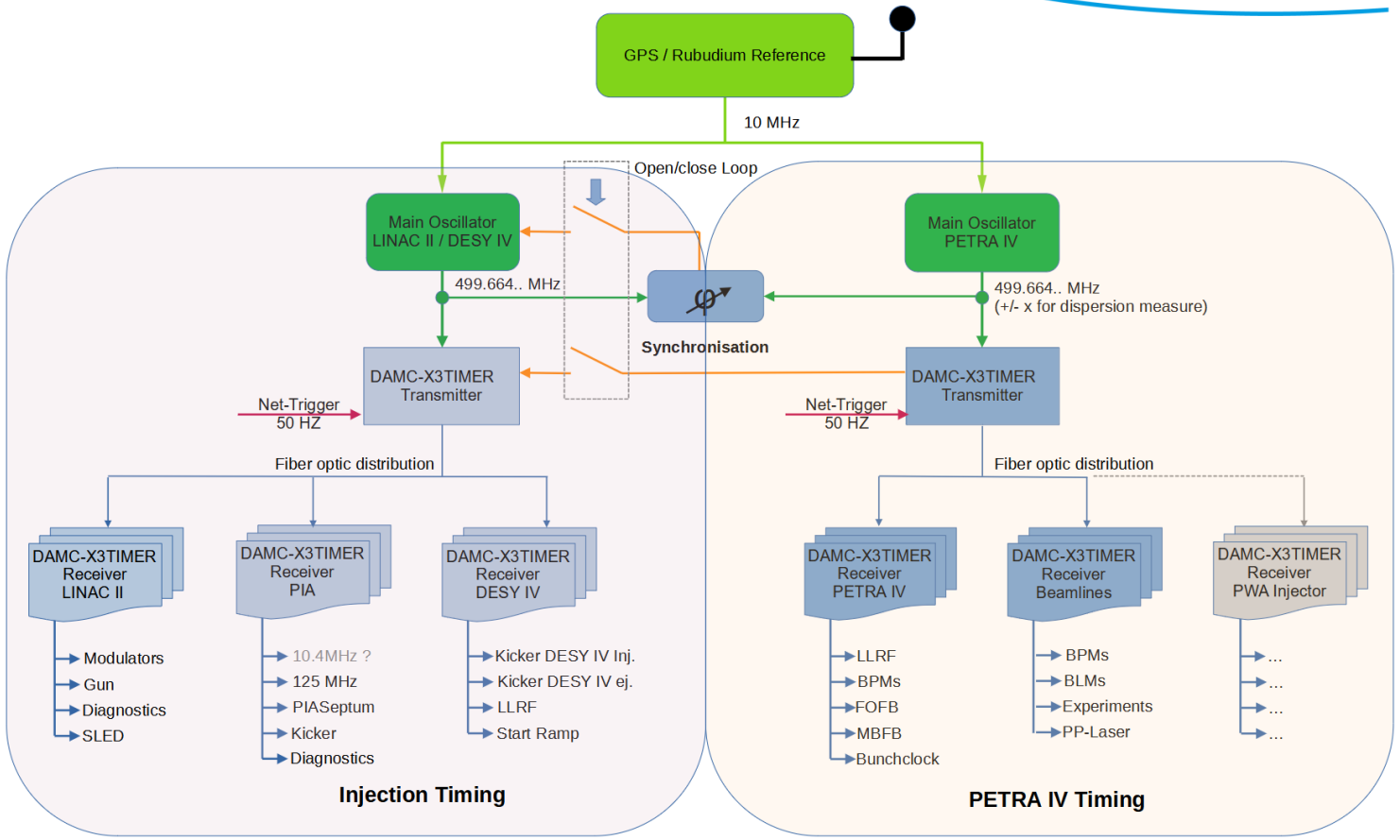


Timing and Synchronization System Design



Courtesy of Tim Wilksen

Main Timing PETRA IV in N Hall 1
Main Timing DESY IV in N Hall 1



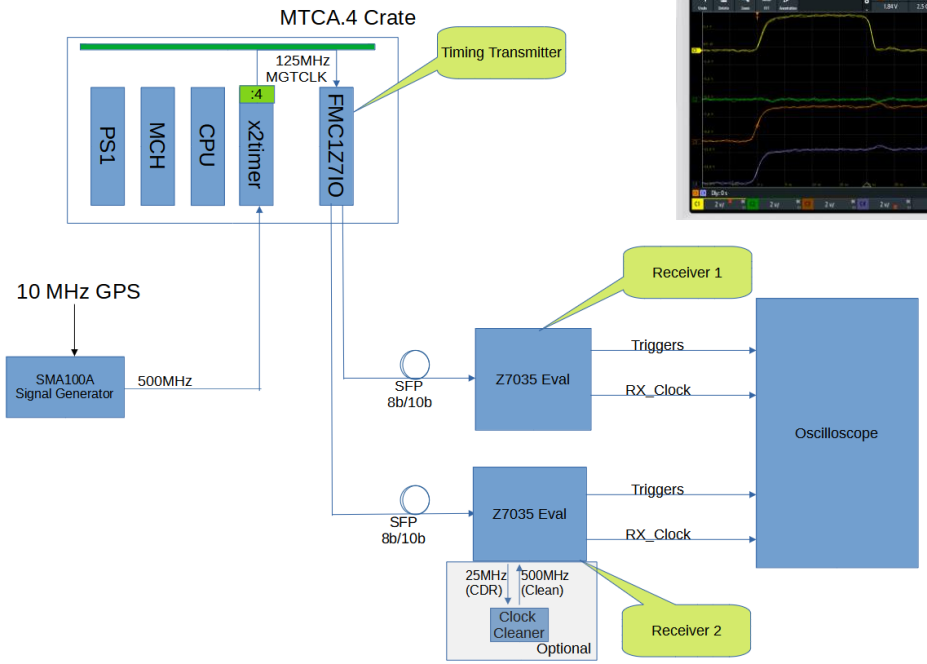
Key Requirements

- Distributing a continuous RF reference signal
- Provide low jitter clocks (e.g. for ADC sampling)
- Provide continuous timing signals & trigger events
- Provide beam-synchronous data as:
  - Timestamp / revolution counter
  - Beam mode / bunch pattern
  - bunch currents

- Common hardware for timing transmitter and receiver
- Dedicated fiber optic distribution with drift compensation
- Common timing system for accelerator and beamlines

Transmitter – Receiver lab setup

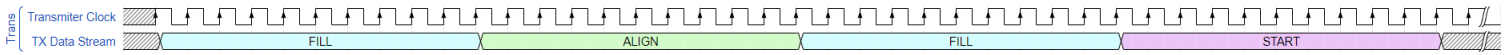
- Data transmission over MGT (GTX) transceivers
- Data rate is derived from RF-Input
- Receivers recover the clock from the data stream
- Alignment:
  - Alignment characters (K28.5) in the data
  - CDR phase is shifted towards the alignment character



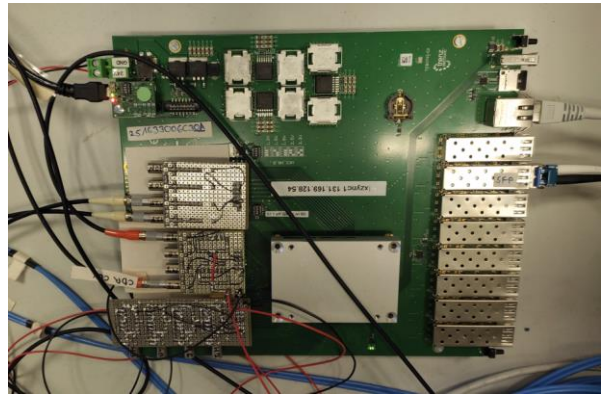
DAMC-FMC1Z7IO

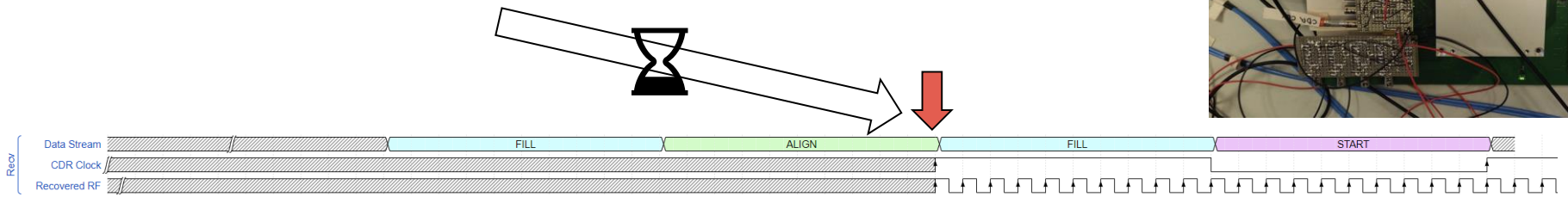
Special comma characters used in the protocol

Character	Name	Function	8b Data	10b Data	
D21.5	FILL	Idle filler	0xB5	101010 1010	101010 1010
K28.0	START	Start of a message packet	0x1C	001111 0100	110000 1011
K28.1	SYNC	Synchronisation	0x3C	001111 1001	110000 0110
K28.4	PROBE	Link delay measurement	0x9C	001111 0010	110000 1101
K28.5	ALIGN	GTP comma alignment	0xBC	001111 1010	110000 0101
K28.7	RES	Reserved	0xFC	001111 1000	110000 0111



TE0745 – Z7053 evalboard

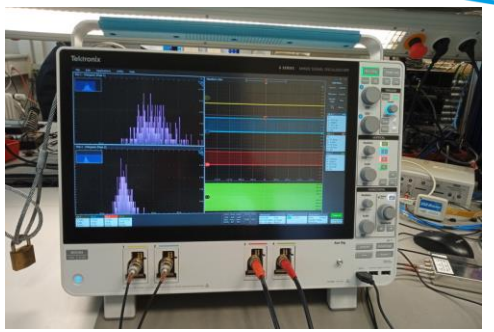




Clock jitter cleanup

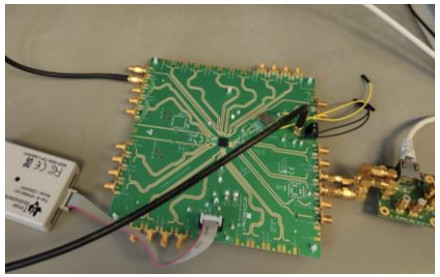
Test Setup

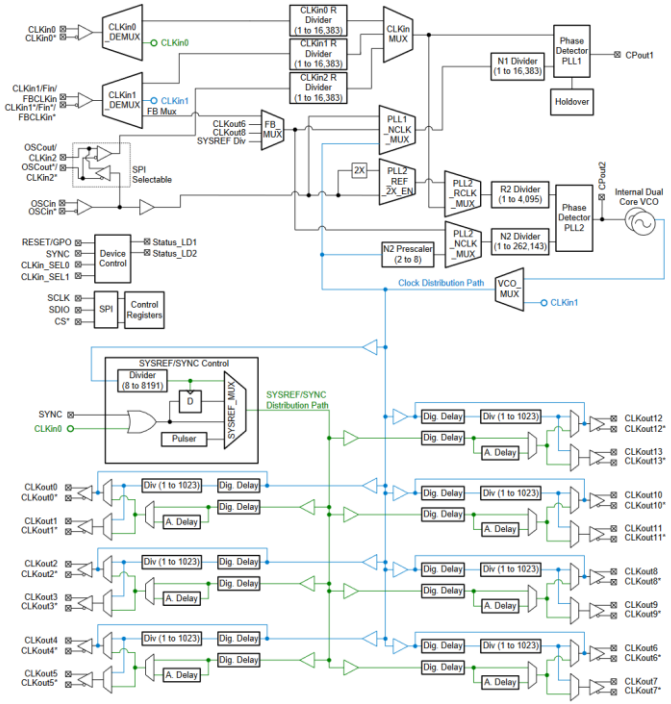
- RF-Generator (R&S SMA100A)
  - 500 MHz GPS stabilized
- MTCA 7-Slot Crate with 2 * X2Timer
  - (Transmitter, Receiver)
- Jitter cleaner Eval-Board (LMK04832)
- 50GS/s Oscilloscope with Jitter&Eye analysis



LMK04832 clock cleaner

- Dual loop PLL
  - PLL1 External custom VCXO -> 499.6643MHz +/-100ppm
  - PLL2 internal 2.5GHz VCO
- 3 Clock inputs (RF, CDR, Aux)
- internal output dividers
- output delays
- different output levels (LVDS, LVPECS, CMOS,..)

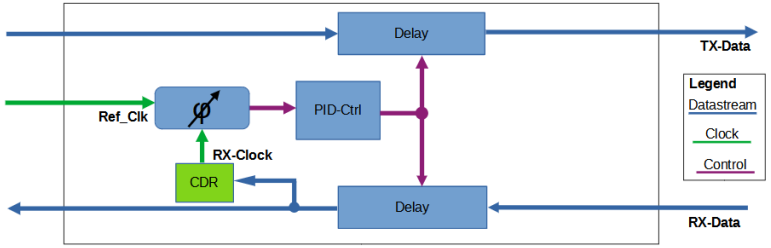




Option	Description	Jitter
No jitter cleaner	Clock from CDR (similar to X2Timer)	10-30ps
Single loop	LMK04832 and internal VCO loop only	1-3ps
Dual loop *	custom VCXO and internal VCO	< 1ps expected

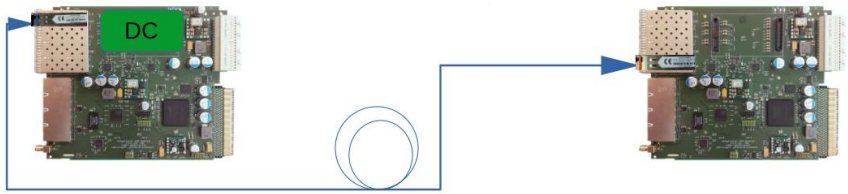
*VCXO samples for test ordered

Drift compensation



Active drift compensation on Transmitter side

- Detect phase differences between Ref_CLK and recovered clock (looped back on receiver)
- Sets delays to keep the phase relation constant
- separate module option to keep Receiver BoM cost low
  - receivers or applications with no critical drift requirements
- Standard transmission over separate fibers for RX and TX
- Fibers (also of a pair) have not the same propagation delay
- Tested also with BiDi Transceivers (dual wavelength, single fiber)



Measurement

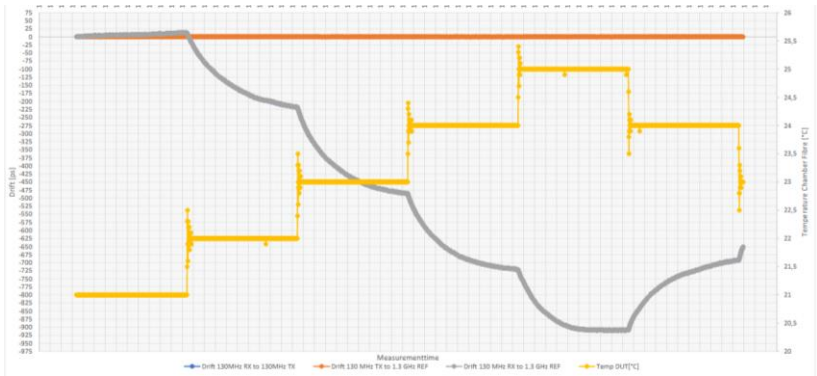
Test-Setup:

- 2 x2timers &
- 1km fiber
- tested in climate chamber

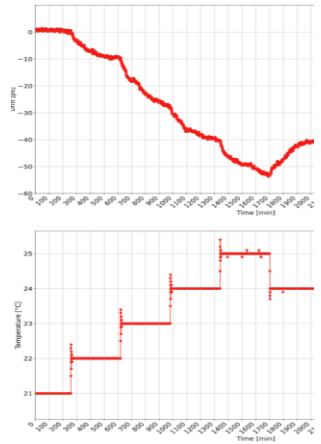
Results:

- No compensation -> ~250 ps/°K
- 2 fibers -> 15 ps/°K
- BiDi-SFP -> ~5 ps uncertainty (without drift over temperature)

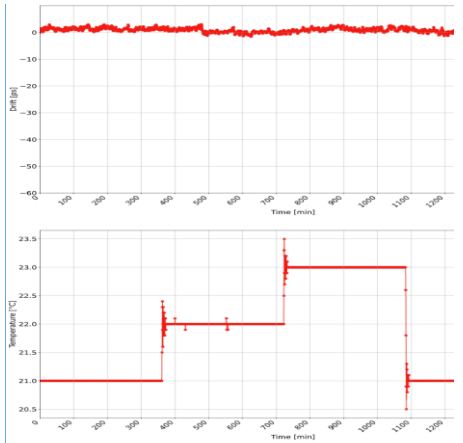
No compensation



Standard 2 fibers



BiDi single fiber SFP

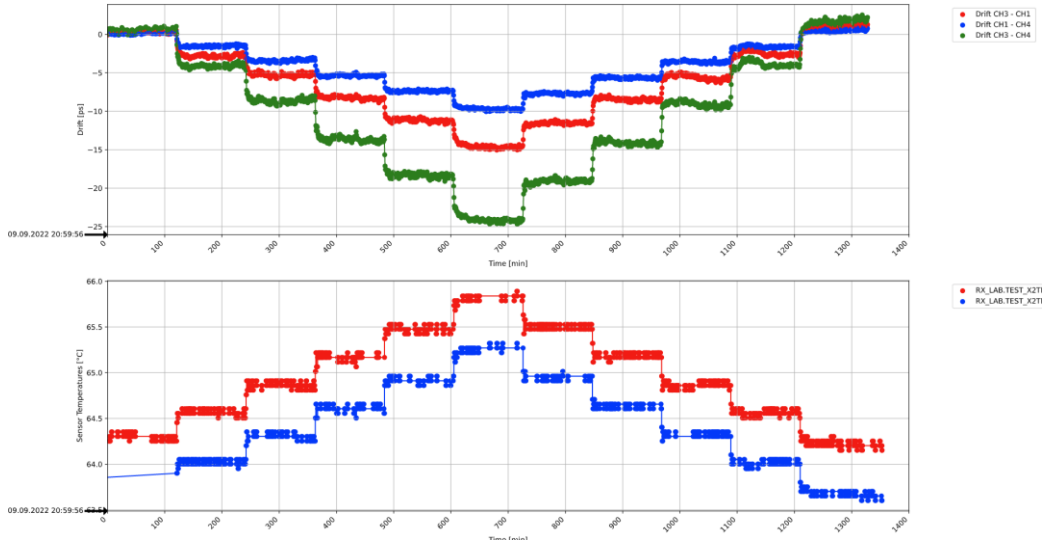


Courtesy of Michael Pawelzik

Thermal considerations and measures

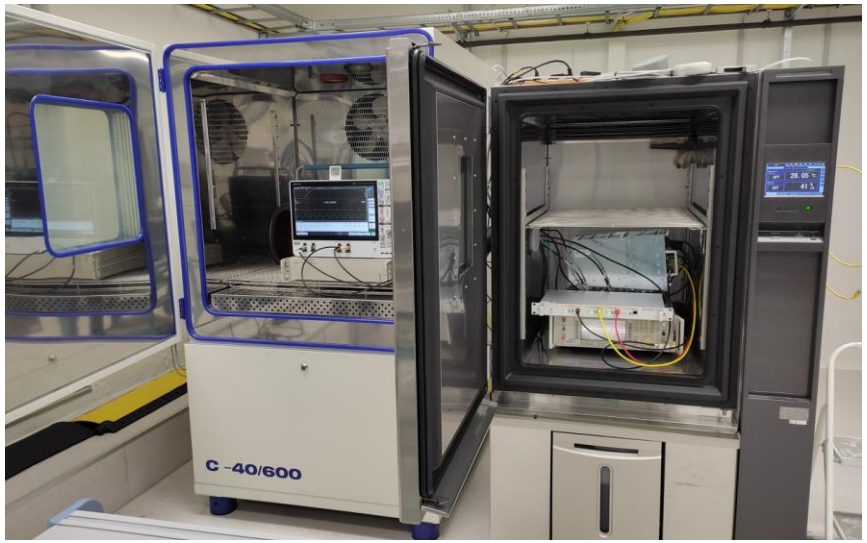
Considerations

- Thermal drifts in the compensation loop are compensated well
- There is still **drift in the out of loop components**
  - Dividers
  - Crosspoint-Switches
  - FPGA
- Temperature changes by MTCA **Fan activities** have a big influence on AMC temperature and component drifts



Measures

- Room / Rack / Crate level
  - temperature & humidity controlled electronics room
  - Use water-cooled Racks for constant temperature & best heat dissipation
  - Set Crate to **steady air stream** configuration



- PCB level
  - Reduce amount of critical components
    - LMK04832 contains also divider, delay and multiplexer
  - Place critical components close together (or on separate PCB)
  - Active thermal stabilization
    - **local temperature regulation** (with FETs or Peltier)
    - Metal (Copper) cover for thermal conduction
    - equip-option to keep BoM cost low for non drift-critical requirements

DAMC-X3TIMER Block Design

Front Panel

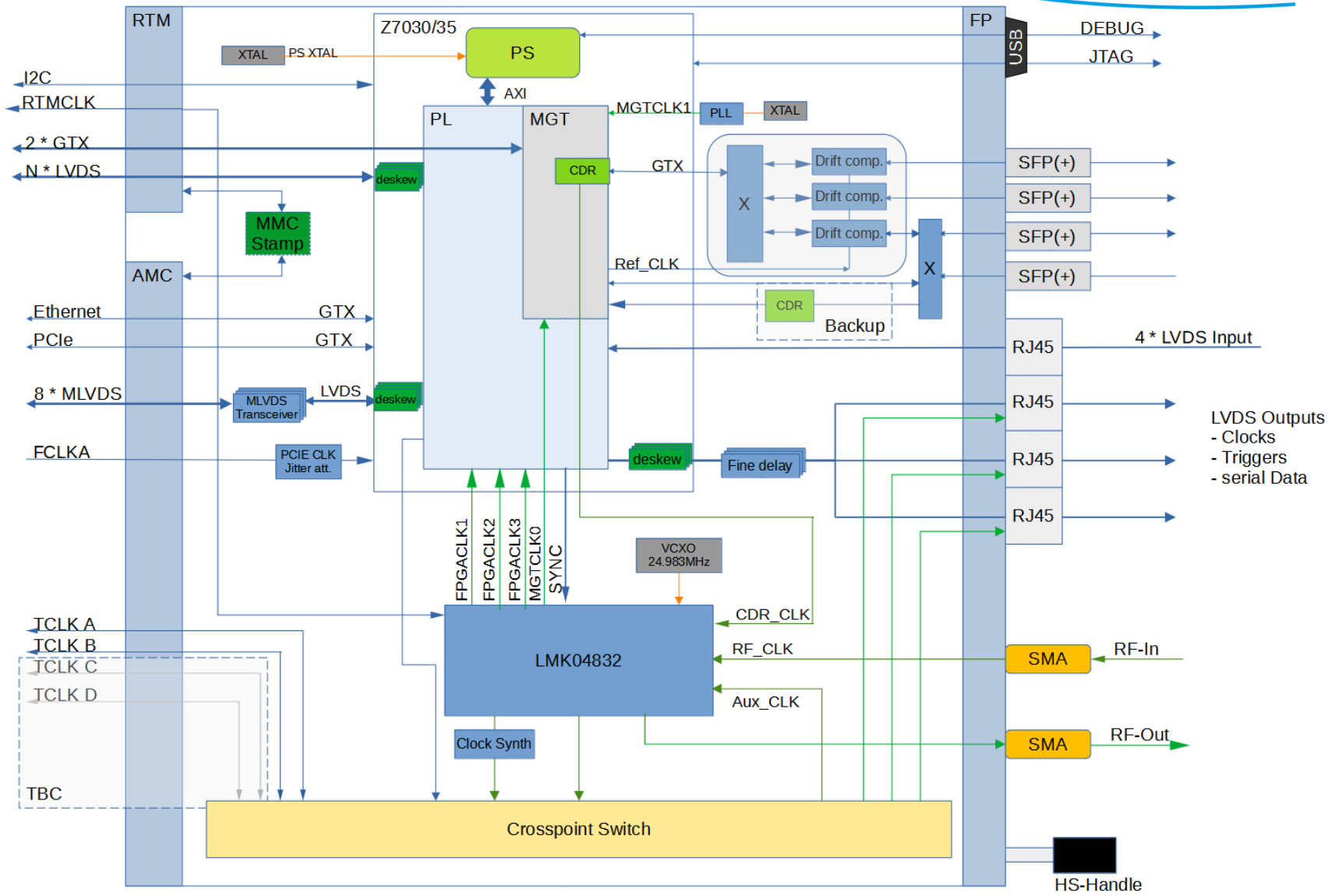
- SFP(+) –> timing signal distribution
- RF-Input
- RF-Output
- LVDS Output (RJ45)
- Synchronous RS232 Output
- LVDS Input (Sync signal, Trigger)
- USB (Debug/JTAG)

AMC - Backplane

- PCIe
- Ethernet
- TCLK A/B (C/D tbd.)
- Port 17-20 Trigger/Clock
- IPMI to MMC

RTM Zone 3 (Class D1.1)

- MGT lanes
- LVDS Trigger / Clocks
- I2C to MMC
- I2C for configuration

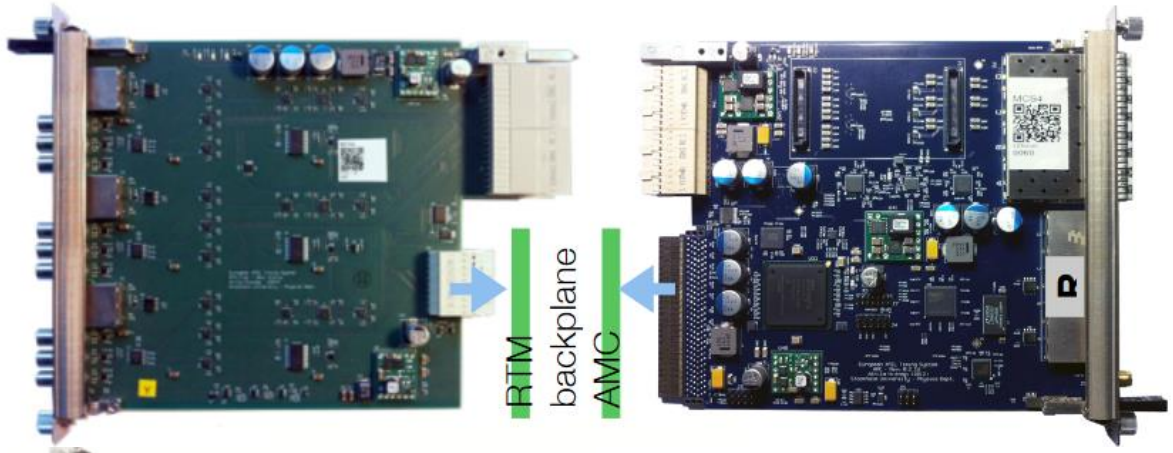


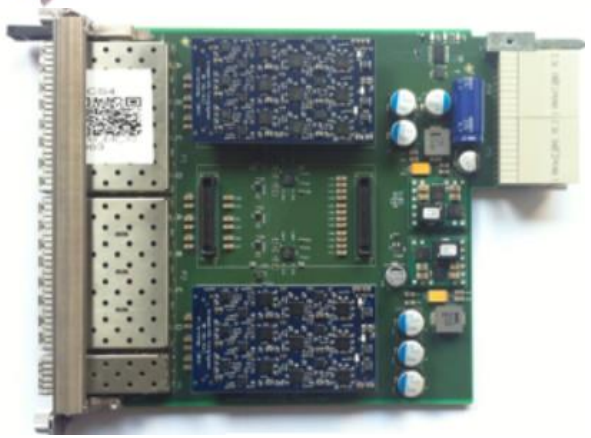
Planned RTM modules

Zone 3 (RTM-Connector)

RTM Class D1.1

- 42 LVDS IO signals
- 2 high-speed-links
- Power
- I2C





Deutsches Elektronen-Synchrotron
Ein Forschungszentrum der Helmholtz-Gemeinschaft

http://mtca.desy.de

Class D1.0, D1.1, D1.2, D1.3, D1.4

Zone 3 Connector Pin Assignment Recommendation for Digital Applications for AMC/µRTM Boards in the MTCA.4 standard

FEATURES

MTCA.4 management zone:
- Power, I²C, optional JTAG support

Digital signals in the user zone:
- Class D1.0: 48 LVDS I/O signals
- Class D1.1: 42 LVDS I/O signals, 2 high-speed links
- Class D1.2: 38 LVDS I/O signals, 4 high-speed links
- Class D1.3: 28 LVDS I/O signals, 8 high-speed links
- Class D1.4: 8 LVDS I/O signals, 16 high-speed links

Digital signals with a fixed direction:
- 2 LVDS low phase noise clocks
- 1 LVDS timing output signal
- 3 LVDS outputs for user applications

APPLICATIONS

- AMC / µRTM board design in MTCA.4 standard
- High-speed data processing
- Multi-channel data-converters, sensor readout and output
- Digital signal conditioning boards

GENERAL DESCRIPTION

This Class D1 pin assignment definition of the Zone 3 connector in the MTCA.4 standard is a recommendation mainly for AMC and µRTM boards transferring digital signals over the Zone 3 connector. This digital class is designed for two three row ADF Zone 3 connectors and AMC modules having an FPGA. The subclasses offers different numbers of digital input / outputs and high-speed communication links. The main goal is to classify the undefined Zone 3 pin assignment for applications to achieve a high

https://innovation.desy.de/sites/sites_custom/site_itt/content/e22/e161197/e176129/e176132/ZONE_3_Classification_Recomendation_Class_D1.0-4_RevA.3_ger.pdf

RTM types

- Rear panel interfaces
  - LEMO
  - SMA Clock output (with LNA)
  - LVDS
  - Optical
  - NIM?
- RF-Backplane interface
  - Clock distribution
- Functional
  - Programmable delay line
  - SFP Fanout module

Pictures from x2timer RTM modules

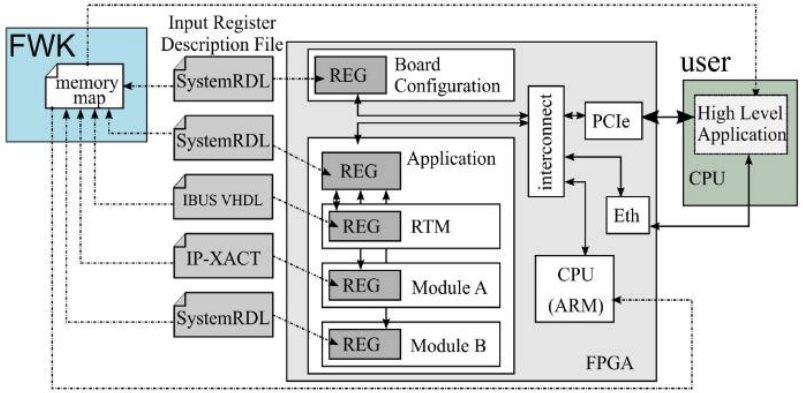
Firmware framework & software interface

FPGA firmware
Group ID: 45

REDMINE
MSK project management tool

MSK firmware framework

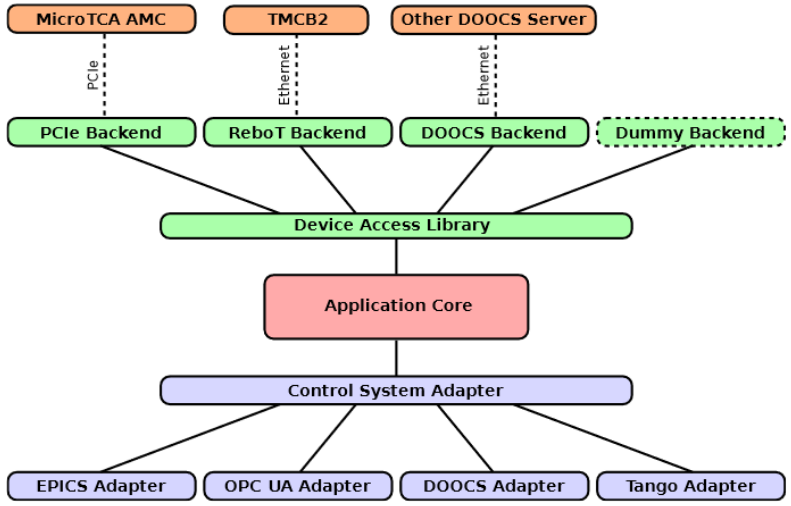
- Generic framework for various (Xilinx) FPGAs
- Maintained by MSK firmware group
- Register maps for software interface
- Supports also ARM core interface for SoC devices



MSK GitLab

Application Core / ChimeraTK software layer

- Middle layer to abstract hardware and control system
- Supports multiple controls systems
- Uses Xilinx xdma driver to access FPGA via PCIe
- Support to run on (Zynq) ARM cores in preparation
- Public available: https://github.com/ChimeraTK



ChimeraTK

Tutorial: from Martin Killenberg
From Tuesday!

Jenkins

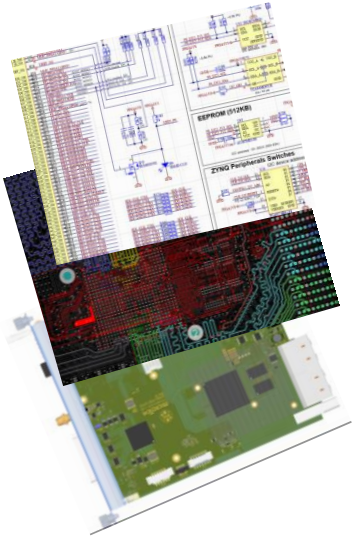
Summary & Roadmap

- For PETRA IV we will top our development on the x2timer design

- Improvements in the DAMC-X3TIMER
  - **Improvement of short term jitter** by using clock cleaner
  - **Better drift stability**
    - Usage of BiDi SFP transceivers
    - by thermal optimization of the boards
    - definition of Crate cooling requirements

- New features due the **Zynq SoC** architecture possible
  - **Realtime processing** on ARM CPU (e.g. PETRA filling pattern)
  - **Controls servers on Zynq SoC**
  - More flexibility for configuring peripherals with I2C or SPI

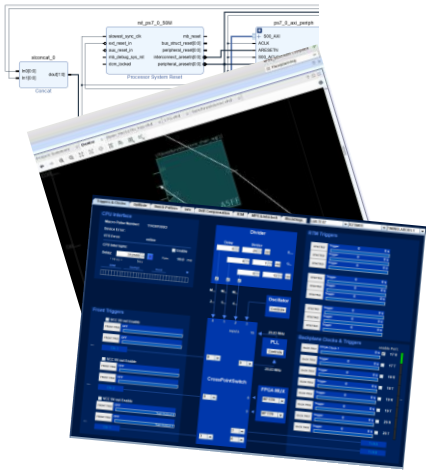
- More flexibility by using a **Software/Firmware framework**
  - Interface for **many control systems**
  - **Modular firmware** for easy portability



Roadmap 2023

- Schematics Design &
- Layout (Q2)
- Hardware production (Q3)
- Bringup & Test (Q4)

- Firmware development
- Software development
  - Servers
  - high level controls



Thank you for your attention!

Contact

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