Recent developments on the Multi-axis Motion Controller in MicroTCA.4

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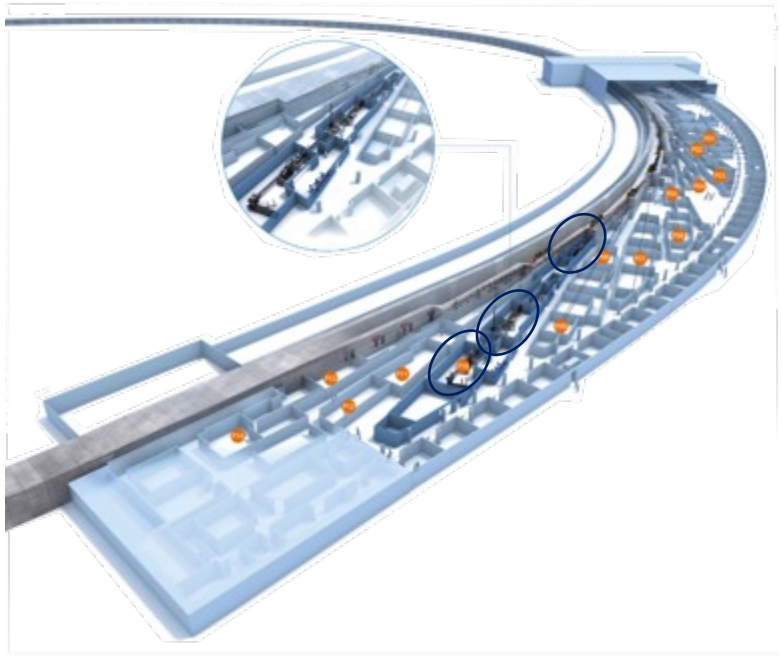
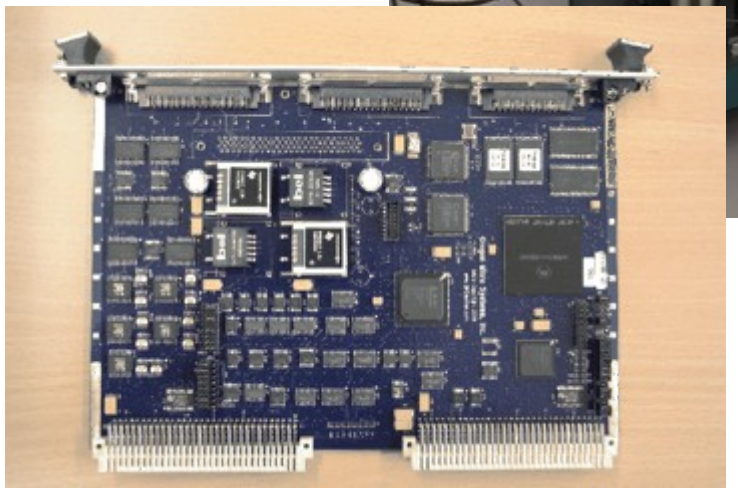
HELMHOLTZ SPITZENFORSCHUNG FÜR GROSSE HERAUSFORDERUNGEN

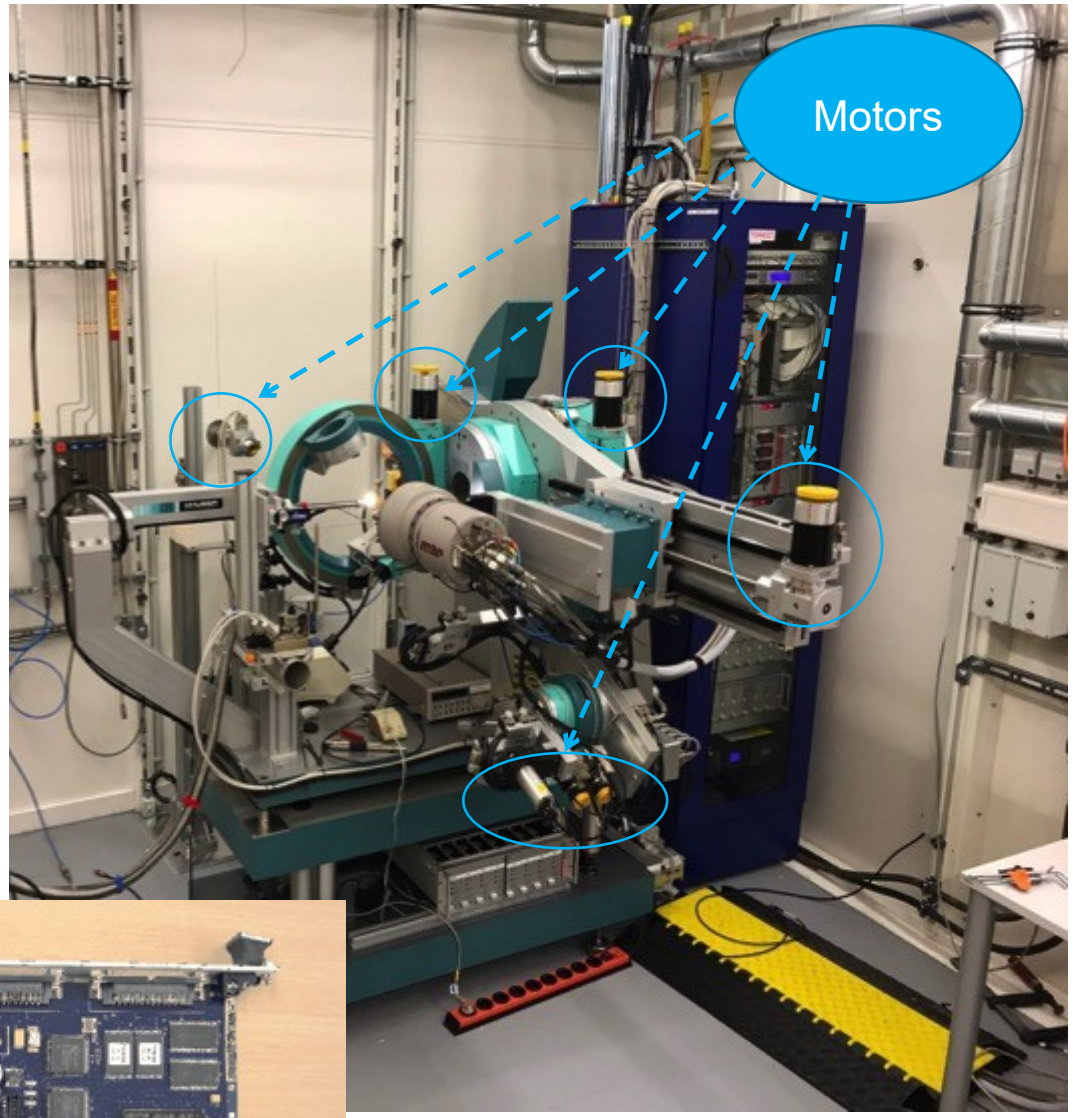
DESY.

Recapitulation: Existing solution

- DESY needs to move motors in experiments
- A replacement for VME systems is required (**OMS MAXv**)
- Limited to 8 motors per card, no card-to-card communication
- No suitable product on the market
  - Decision: Keep VME on Petra IV or do custom development
  - Funded by DESY Generator Program
- DAMC-MOTCTRL: Controls **48 motors**/axis per card
- MicroTCA Form factor: Scalable **interconnection** of several cards in **the crate and campus-wide**
- **Position-triggered data acquisition** with other MicroTCA cards
- Focus on competitive cost factor (licensing planned)







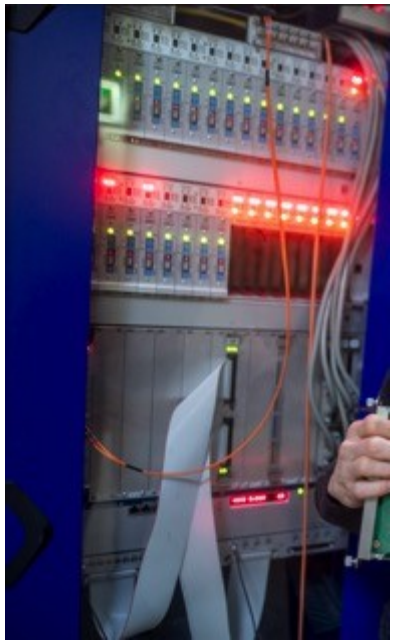
Diiffractometer at Beamline
(setup by Martin Tolkiehn;
Courtesy of Nikola Radaković)

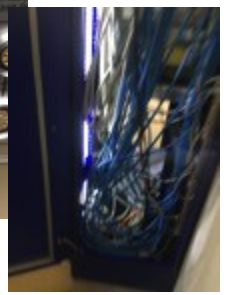
Large Investments on DESY Campus

- Beamlines have hundreds of existing motor drivers

- Commercial drivers built into proprietary ZMX+ frame
- Legacy hardware, but good enough to keep
- Incompatible interface
  - 12 SCSI connectors on MTCA front panel: no!
  - Users complain about long, stiff cables
  - Sensitive connectors (SCSI II)
  - 4 cables per motor driver frame
- Drop-in replacement needed

- DAMC-MOTCTRL
  - One MTCA card replaces six VME cards
  - one card drives 3 complete ZMX frames
  - 4 SCSI cables are replaced by one fiber link
  - Motor drivers and motors are kept



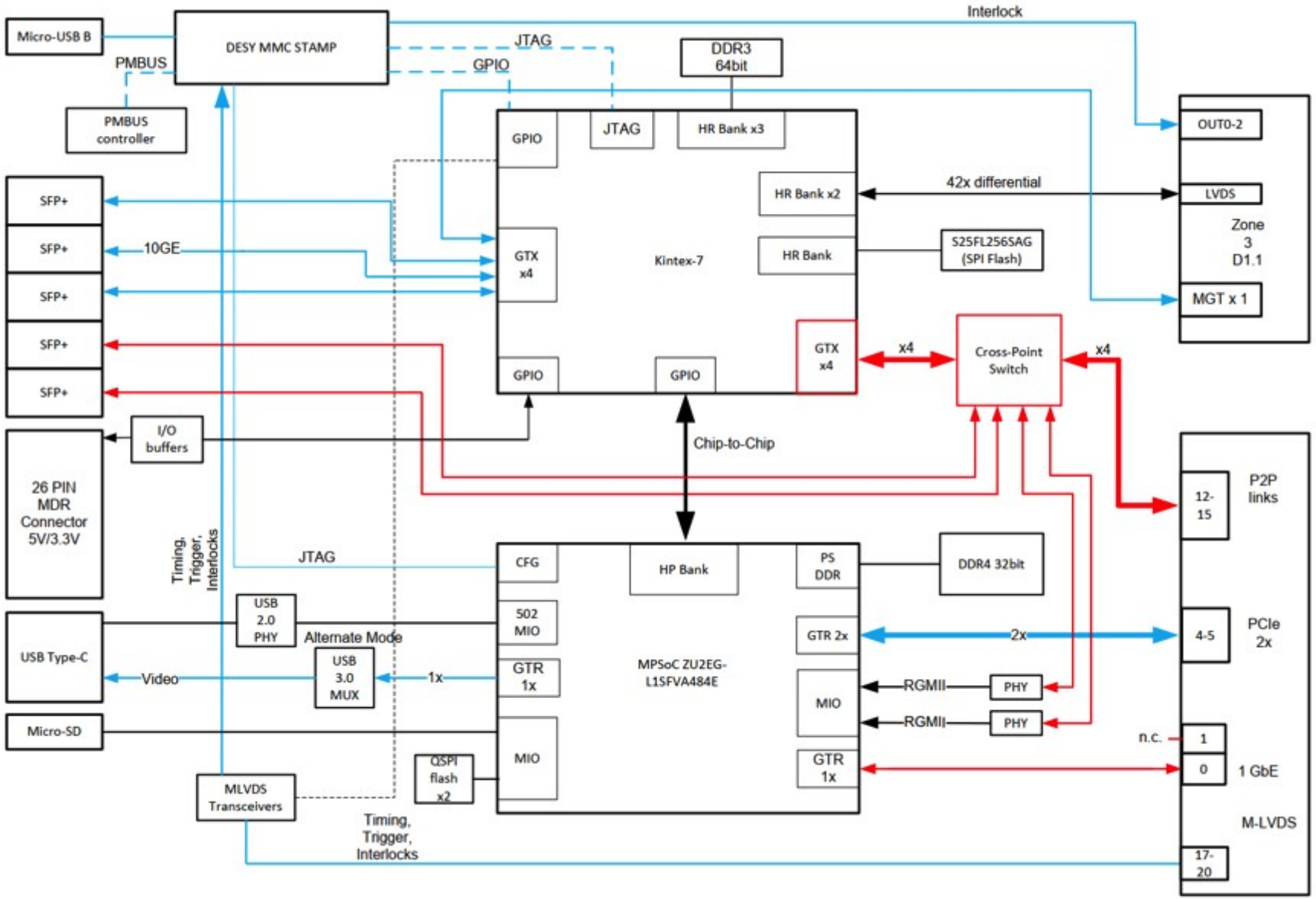


Block Diagram

- Heterogeneous Processing
  - “ARM CPU” and FPGA
- Kintex-7: real-time control
- MPSoC: control-system and communication to other cards
- 5 SFP+ Ports (1Gbps-10Gbps)
  - 3x Motor interfaces
  - 2x Ring topology
  - Support: EtherCAT, SERCOS

https://www.fs.com/de/products/66612.html

- Backplane Ethernet without PHY (design risk, 1000Base-SR/LR support new in recent PetaLinux, but we need 1000Base-X)
- 26-pin connector: 3.3V /5V IO
- Monitor/Keyboard interface via USB-C

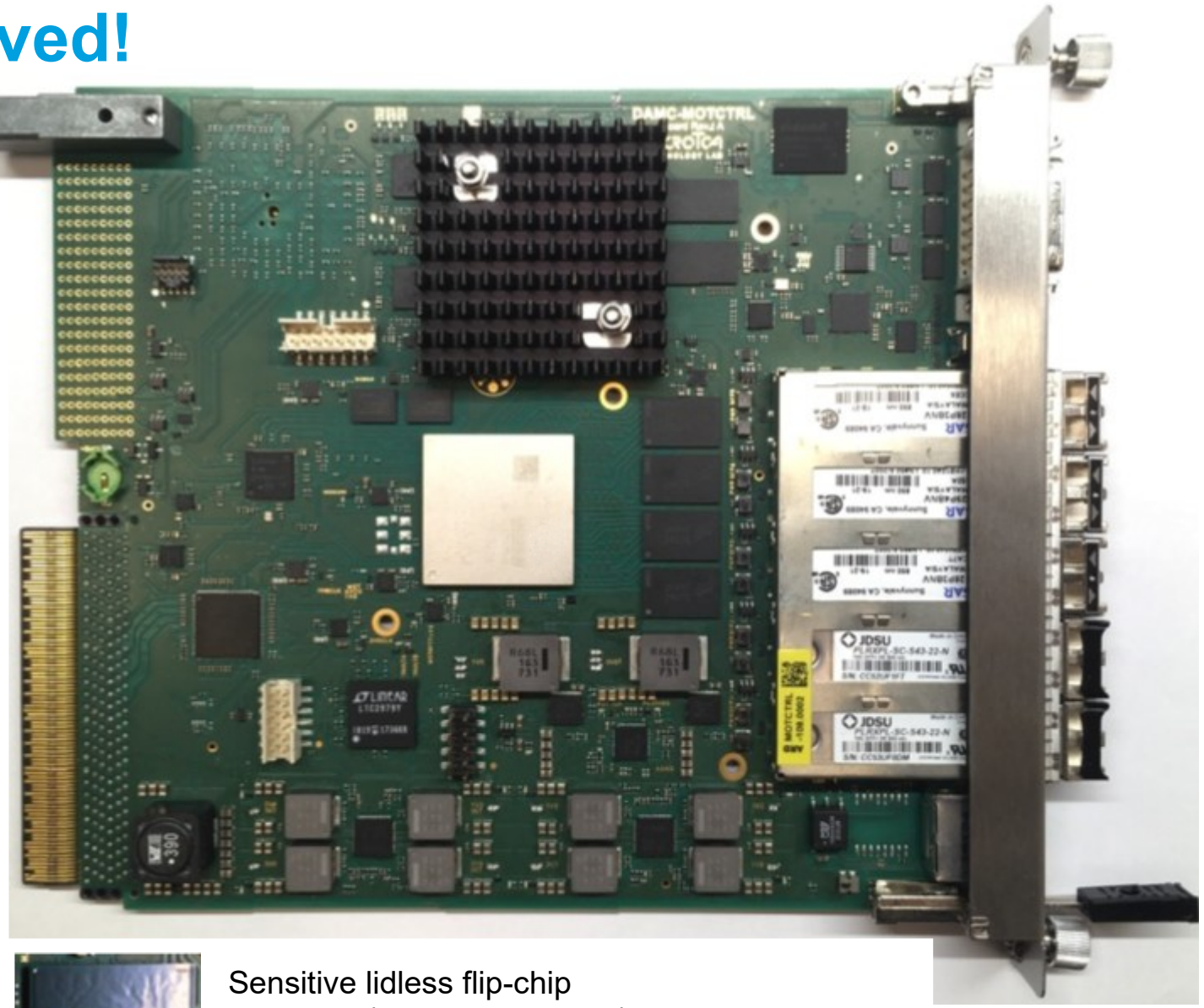


Update: The board has arrived!

(Highlight in these days...)

- Board follows platform concept
- Shares design templates and parts of DAMC-FMC2ZUP and DAMC-Z7IO
- We wanted to follow established concept: Designed around ICs available at the beginning of chip crisis
- Market almost empty: same chips, diff. packages
- Everything stocked (160k€ parts in stock)
- Example: Lidless (bare die) MPSoC FPGA

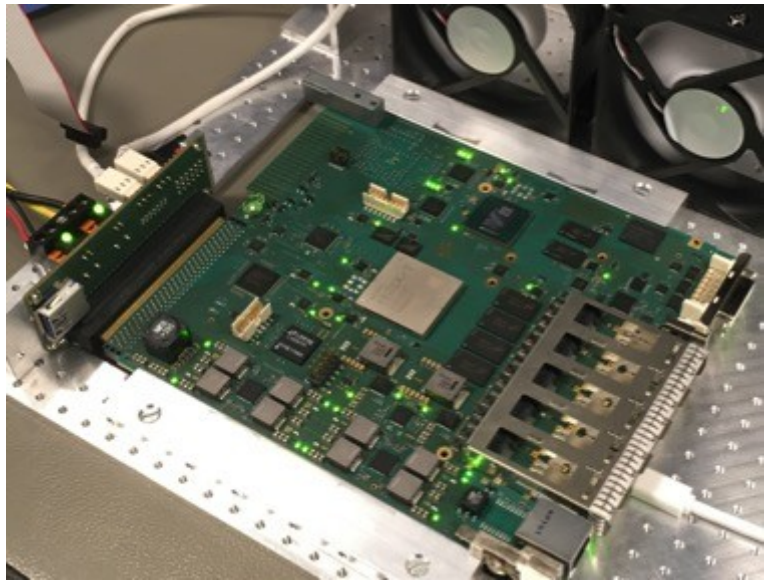
We needed to build up a nitrogen system for stocking our parts

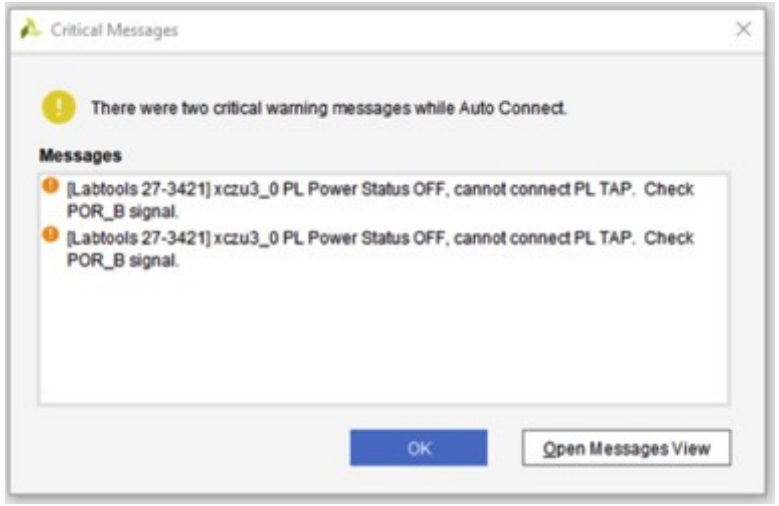


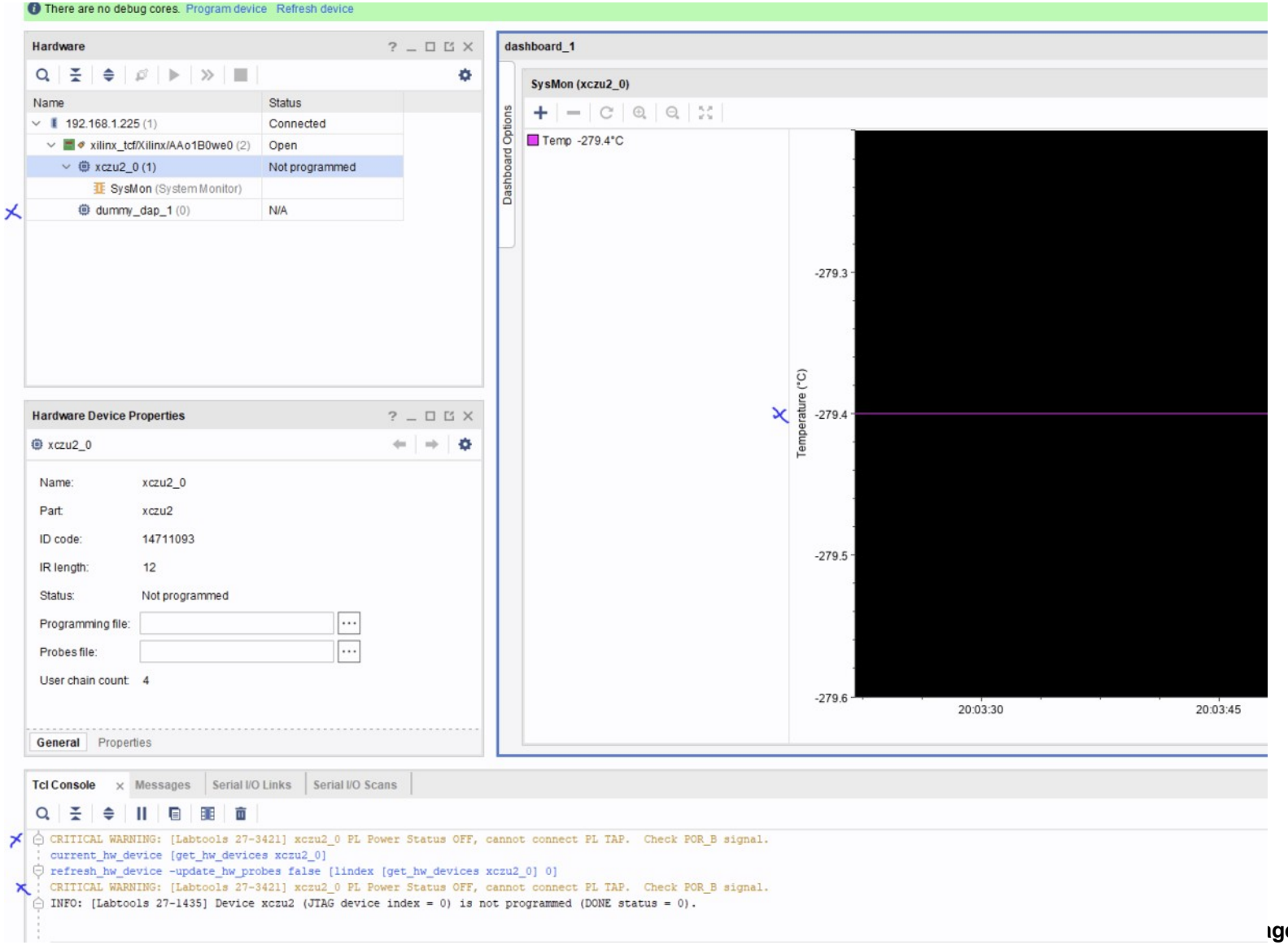
Sensitive lidless flip-chip package (exposed bare die)

Bring-up

Everything looked good (But the FPGA did not fully come up)





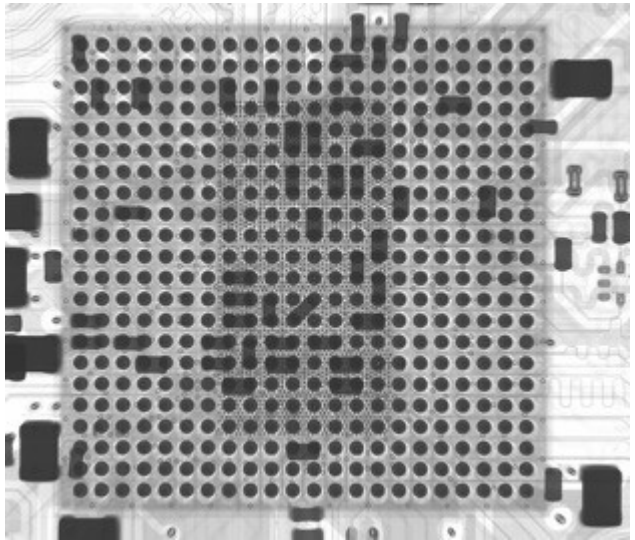


Bring-up

A little detail on the MPSoC ship

This die is broken into 4 pieces.
(Fully invisible here!)

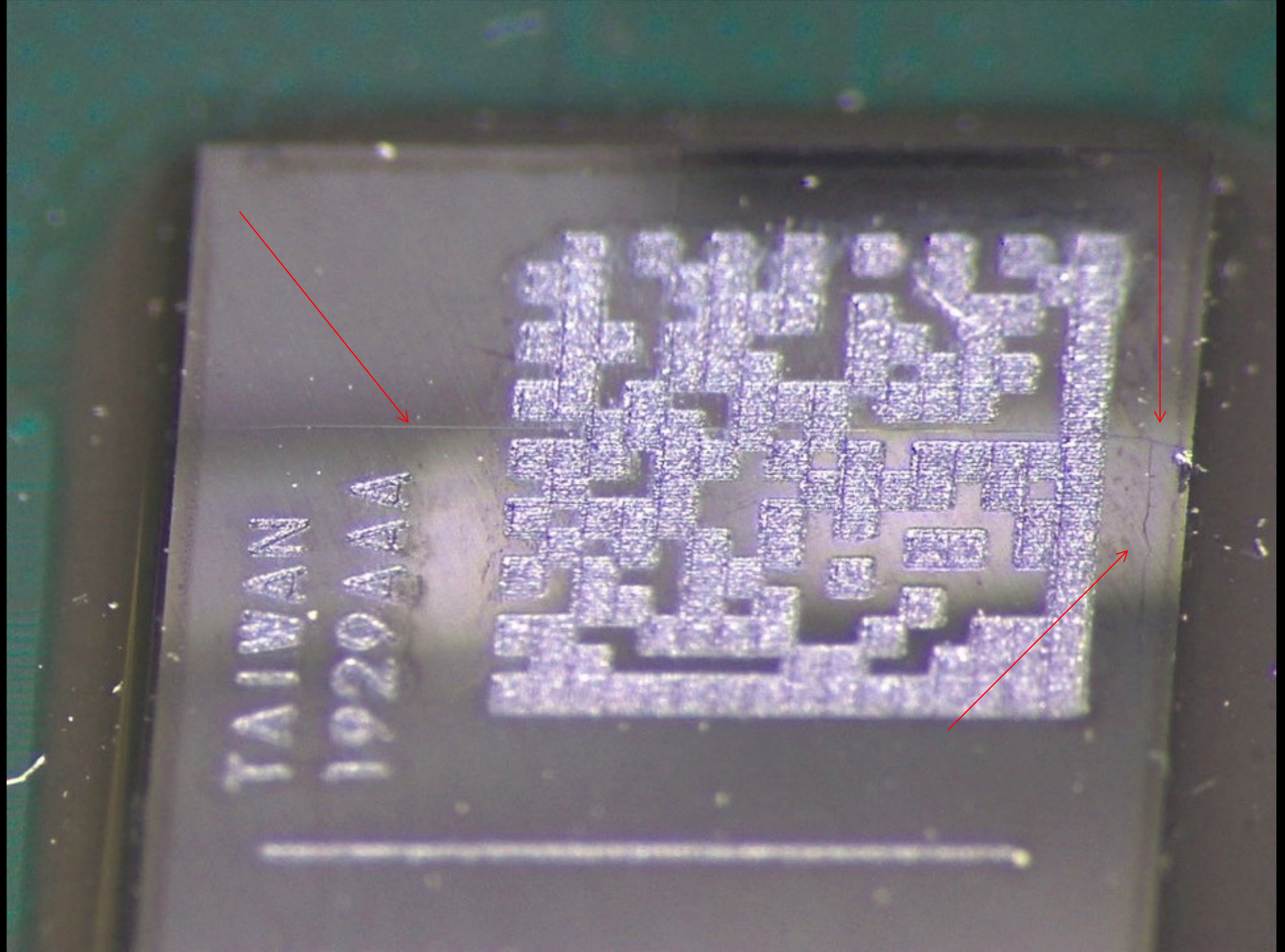
- High-end technology
  - 2 FPGAs → > 20 power rails
  - First time: discrete power supply (cost optimization): 25A, 0.85V +/-3%
  - 12 Layers PCB (no HDI)
- Many, many reasons for “issues”
- We noticed a little “edge on the FPGA” – not overlooked, but neglected for two weeks → lost to weeks



X-ray: all looks good!

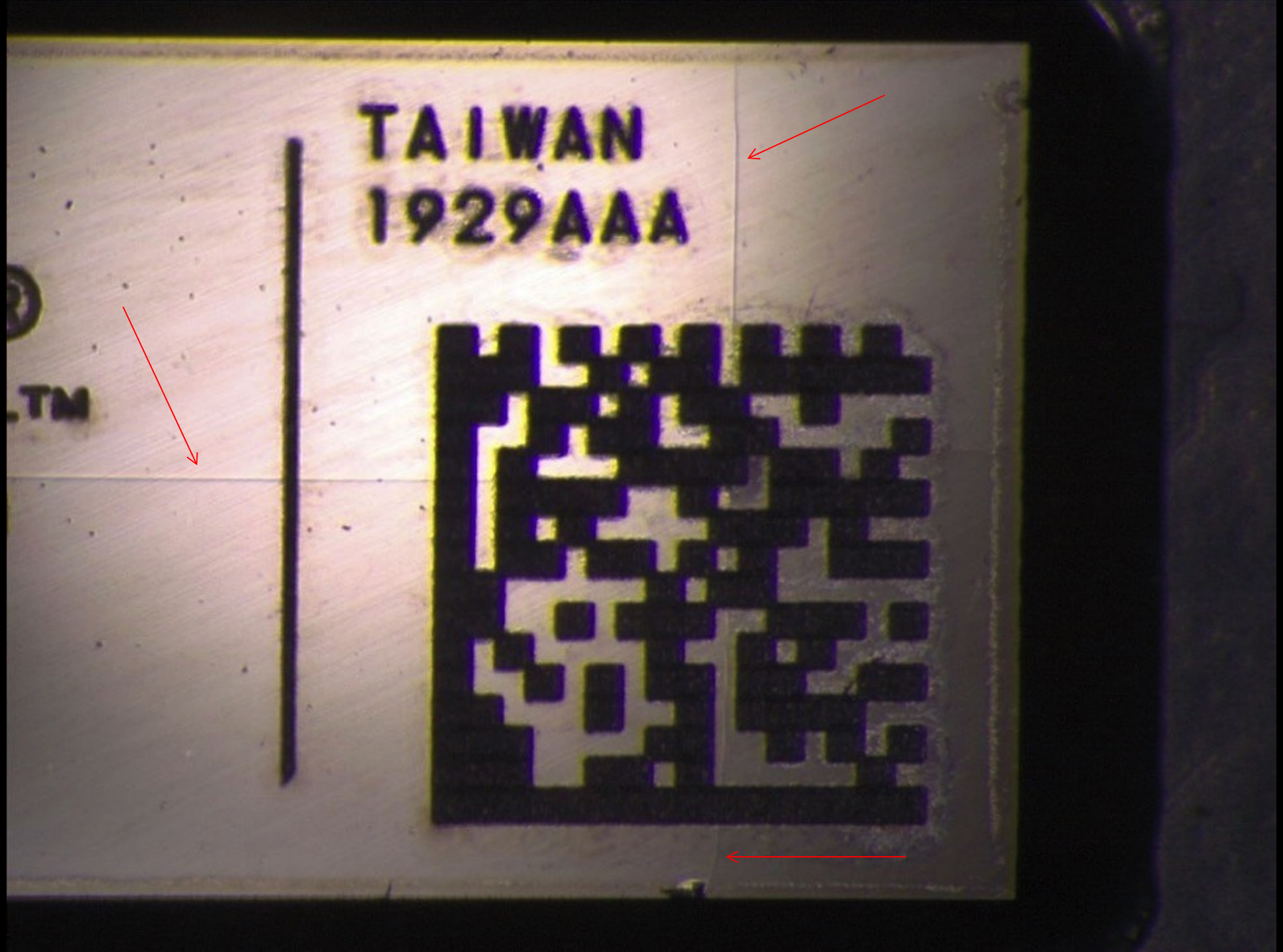
Bare-die package with broken off edge

FPGA had accidentaly fallen into assembly machine, but no damage was reported.



FPGA die is broken into 4 pieces.

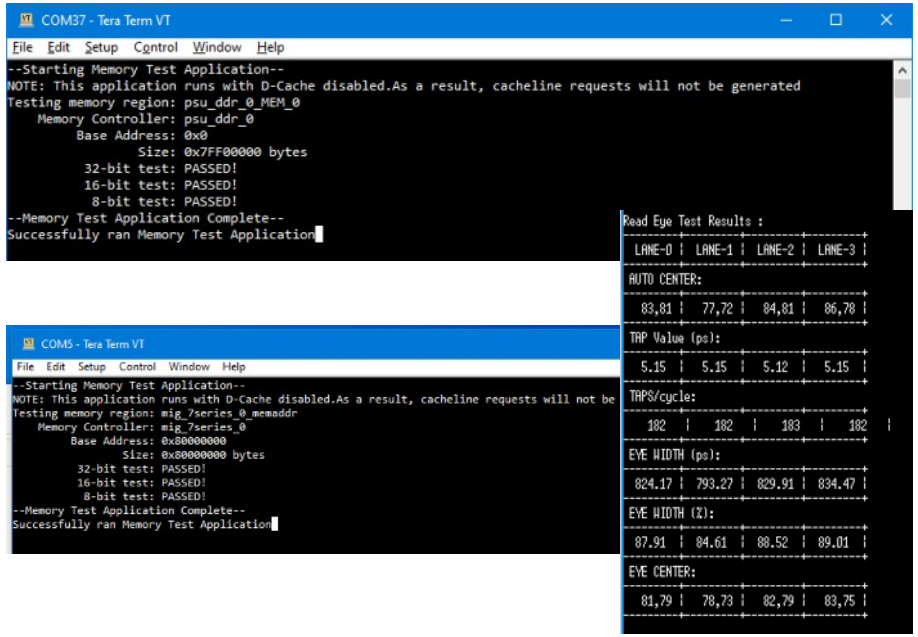
Special angle and light setting needed to see cracks.

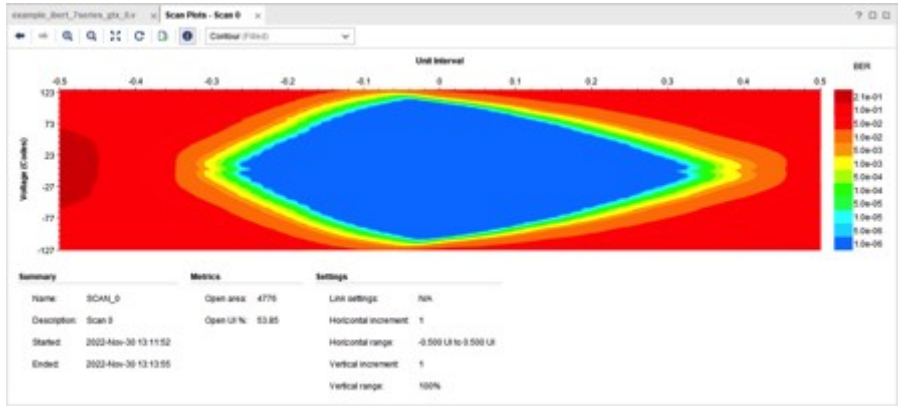


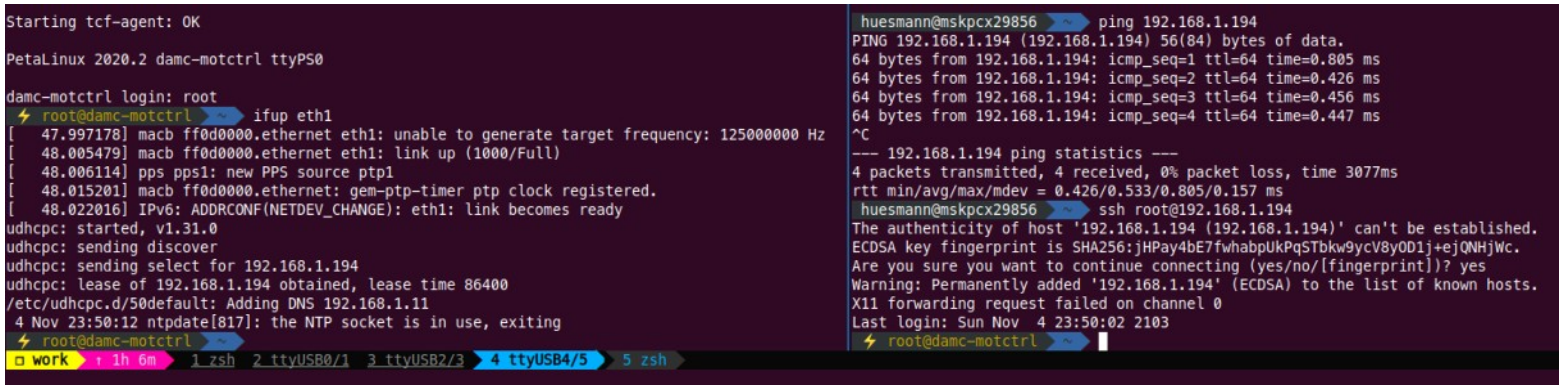
Hardware development state (AMC Card)

Finally everything is good (second board up within 2 hours)

- Not one single patch wire (Rev. A)
- Uses MMC Stamp (Rev. A)
- Already in crate!
- All memories good
- Wide-open DDR3/DDR4 eyes
- Very good SFP+ eyes
- Linux up and running
- Ethernet over backplane running
- We can SSH in to the board



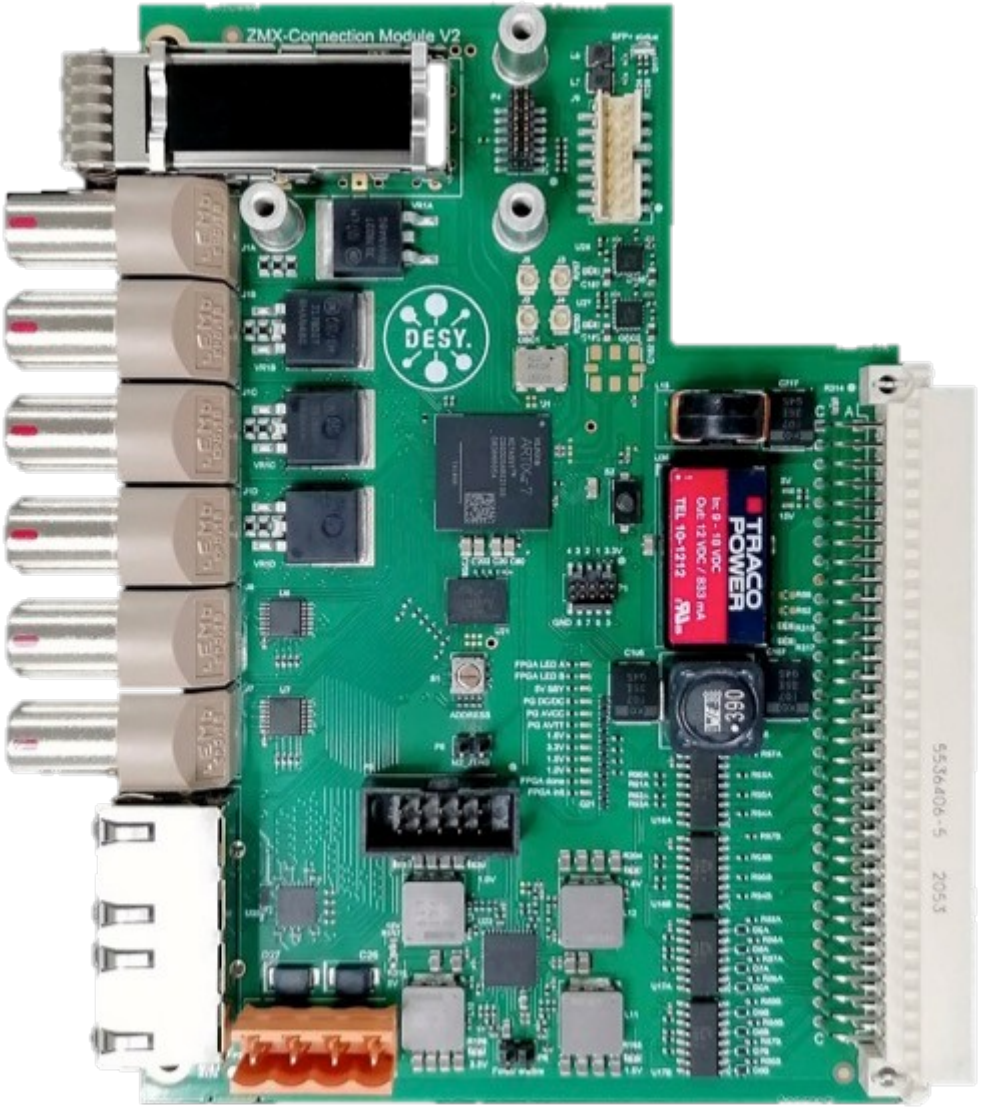


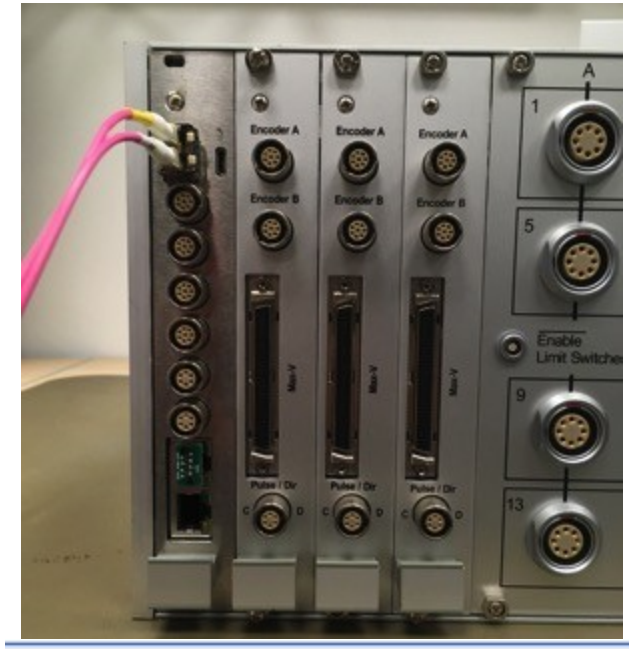


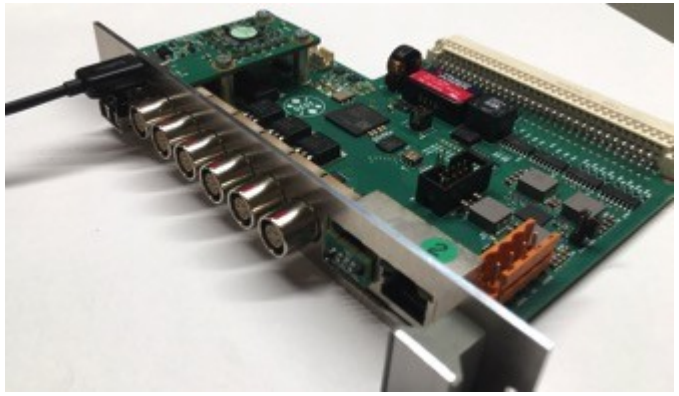
Hardware development state (ZMX Adapter Card)

Up and running (Rev. A)

- Based on Aritx-7
- 6.5 GBPSs Aurora link planned
- Full connectivity (Encoders for all motors, not only for two)
- Test: 27 Terabits without bit errors
- No single patch wire.

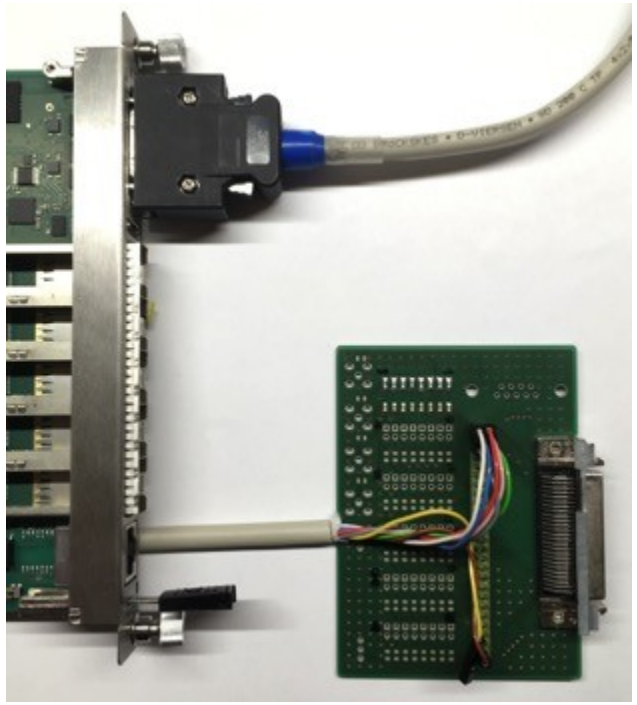


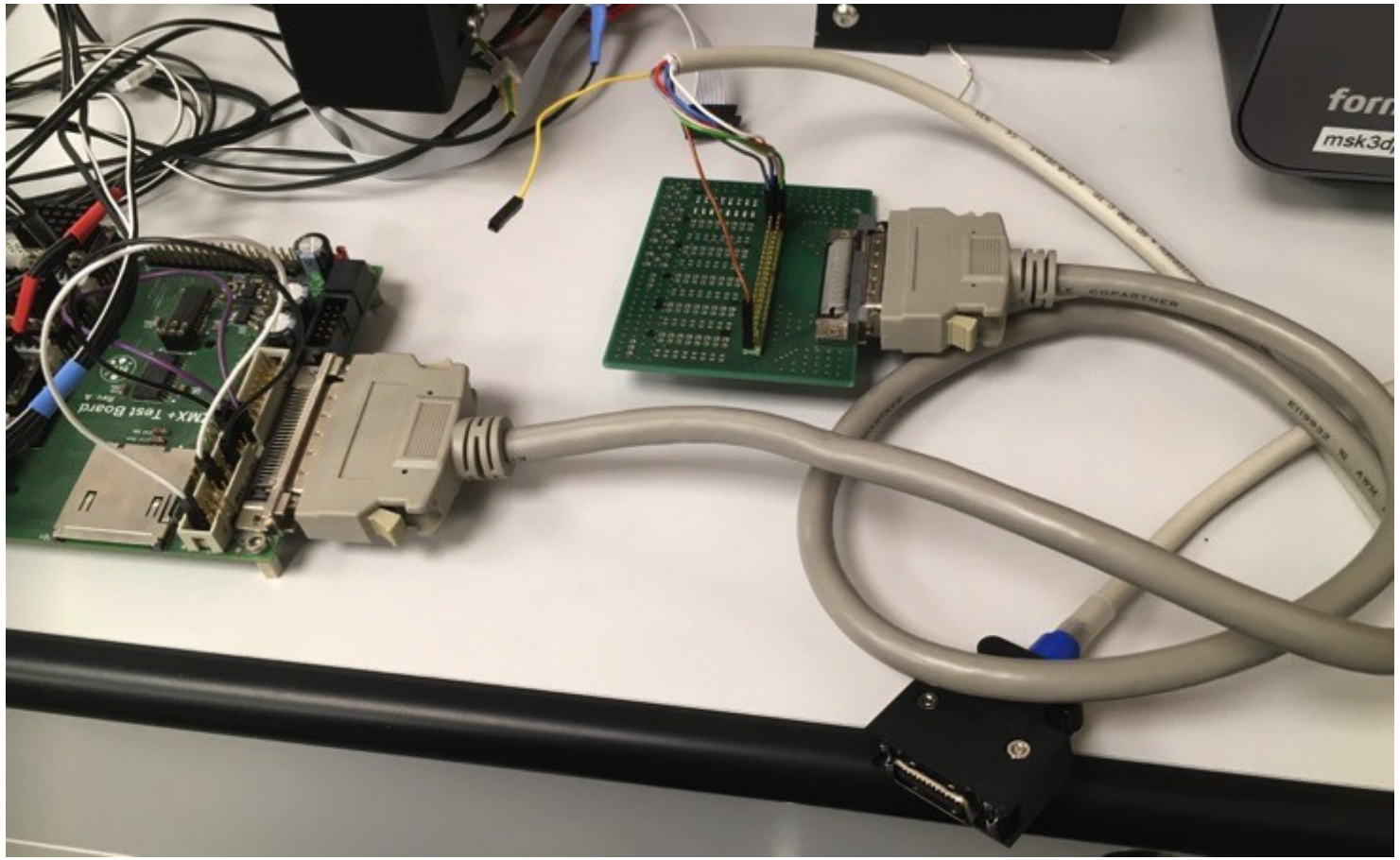




Video Demonstration

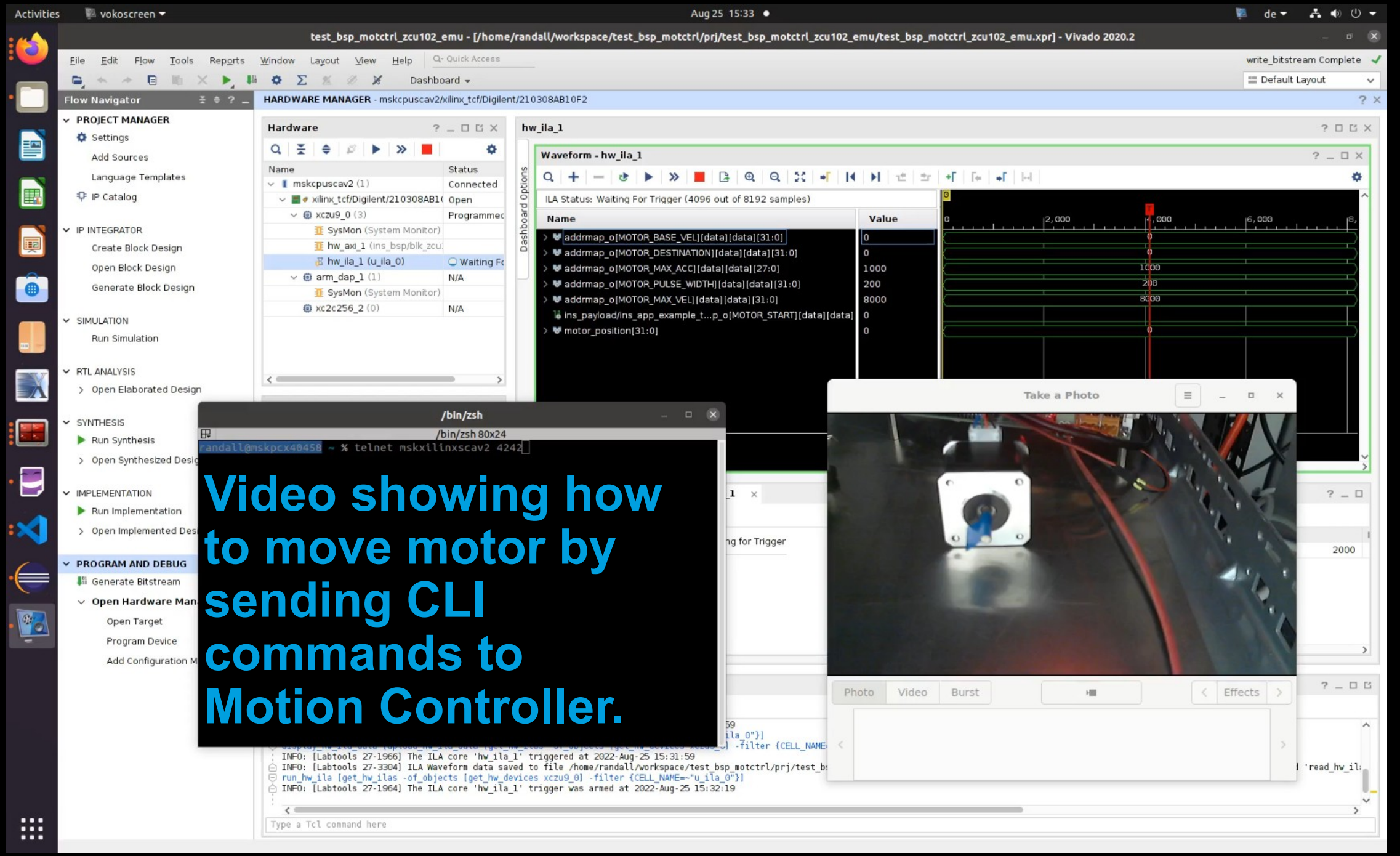
- Legacy IO connector allows simple setups
- ZMX+ Test Board contains motor drivers





Disclaimer:

- The command-line-interface you see is used for **demonstration only.**
- Board will get it's own API: "Certif SPEC" will support our API


Activities
vokoscreen
Aug 25 15:33
de
test_bsp_motctrl_zcu102_emu - [/home/randall/workspace/test_bsp_motctrl/prj/test_bsp_motctrl_zcu102_emu/test_bsp_motctrl_zcu102_emu.xpr] - Vivado 2020.2
File Edit Flow Tools Reports Window Layout View Help
write_bitstream Complete
Dashboard
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
IMPLEMENTATION
Run Implementation
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Man
Open Target
Program Device
Add Configuration M
HARDWARE MANAGER - mskcpuscav2/xilinx_tcf/Digilent/210308AB10F2
Hardware
Name
Status
mskcpuscav2 (1)
Connected
xilinx_tcf/Digilent/210308AB1
Open
xczu9_0 (3)
SysMon (System Monitor)
hw_axi_1 (ins_bsp/blk_zcu
hw_ila_1 (u_ila_0)
Waiting Fo
arm_dap_1 (1)
N/A
SysMon (System Monitor)
xc2c256_2 (0)
N/A
hw_ila_1
Dashboard Options
Waveform - hw_ila_1
ILA Status: Waiting For Trigger (4096 out of 8192 samples)
Name
Value
addrmap_o[MOTOR_BASE_VEL][data][data][31:0]
0
addrmap_o[MOTOR_DESTINATION][data][data][31:0]
0
addrmap_o[MOTOR_MAX_ACC][data][data][27:0]
1000
addrmap_o[MOTOR_PULSE_WIDTH][data][data][31:0]
200
addrmap_o[MOTOR_MAX_VEL][data][data][31:0]
8000
ins_payload/ins_app_example_t...p_o[MOTOR_START][data][data]
0
motor_position[31:0]
0
2,000
4,000
6,000
/bin/zsh
/bin/zsh 80x24
randall@mskpcx40458 ~ % telnet mskxilinxscav2 4242
Video showing how to move motor by sending CLI commands to Motion Controller.
Take a Photo
Photo
Video
Burst
Effects
INFO: [Labtools 27-1966] The ILA core 'hw_ila_1' triggered at 2022-Aug-25 15:31:59
INFO: [Labtools 27-3304] ILA Waveform data saved to file /home/randall/workspace/test_bsp_motctrl/prj/test_bs
run_hw_ila [get_hw_ilas -of_objects [get_hw_devices xczu9_0] -filter {CELL_NAME=~"u_ila_0"}]
INFO: [Labtools 27-1964] The ILA core 'hw_ila_1' trigger was armed at 2022-Aug-25 15:32:19
Type a Tcl command here

Thank you!

Acknowledgments: Nikola Radaković, Robert Wedel

Kontakt

DESY. Deutsches Elektronen-Synchrotron

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