Modular and Scalable Control System for Atomic Array Quantum Computers

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INTRODUCTION

Quantum Computer

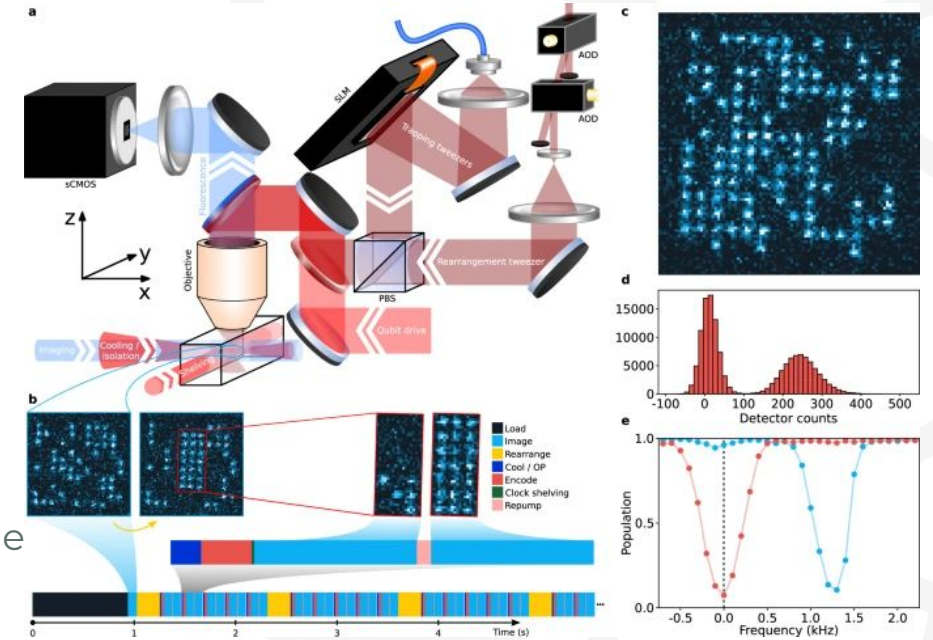
Using an Atomic Array of Neural Atoms

Basic processes involved in computation:

- Neutral atoms:
  evaporated, slowed down, trapped
- cooling, rearrangement
- 1 and 2 qubit operations
- quantum state readout

Requirements for the control system:

- Generate RF signals
  - Frequencies in the MHz to GHz range
- Adaptive optics, mirrors (piezos)
- Magnetic field for magneto-optic traps and creating hyperfine atomic states
- Camera capture & atom detection

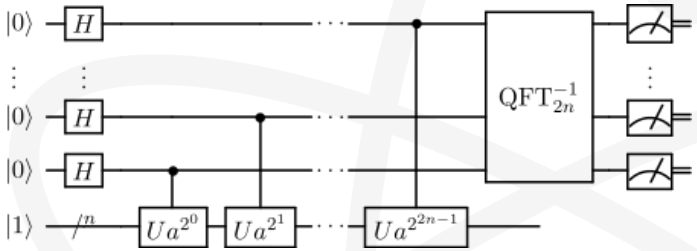


Barnes, K., Battaglino, P., Bloom, B.J. *et al.* Assembly and coherent control of a register of nuclear spin qubits. *Nat Commun* 13, 2779 (2022). https://doi.org/10.1038/s41467-022-29977-z

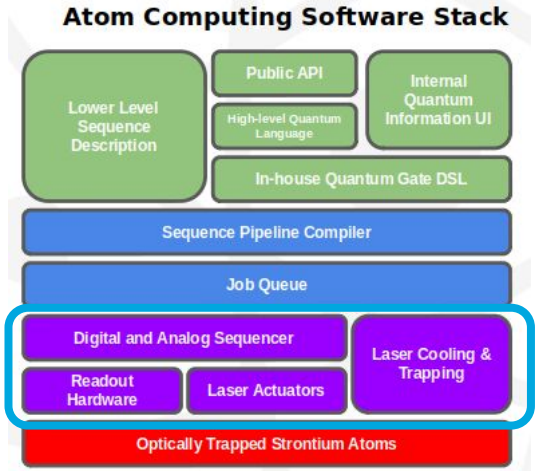
Technology stack

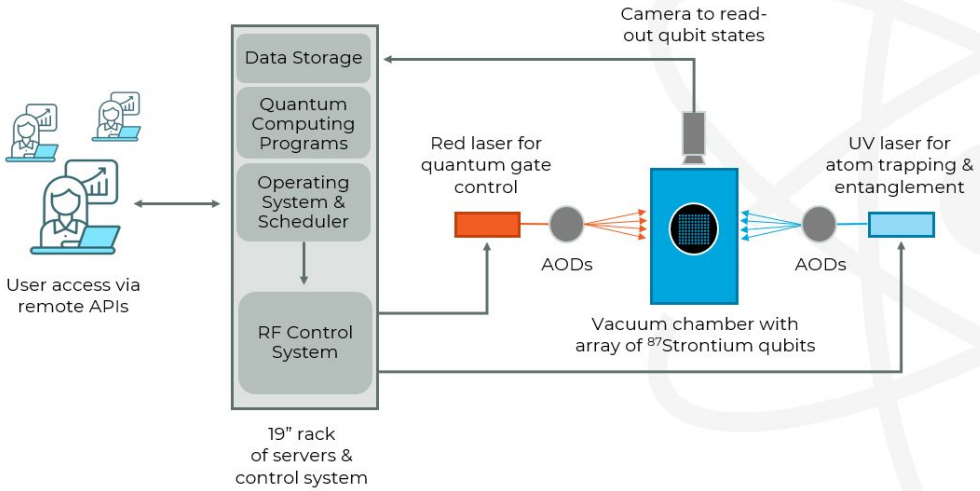
From High-Level Quantum Languages to hardware

- Quantum programs (circuits) are translated from a high-level quantum language to individual instructions for the control system



Quantum subroutine for order finding in Shor's algorithm, Bender2k14, CC BY-SA 4.0„ via Wikimedia Commons





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MICROTCA HARDWARE

MicroTCA crates

Serving two generations of QCs

- MicroTCA.4 crates
- Gigabit Ethernet used to communicate with the rest of the system
- 10 MHz distributed on the backplane
- MLVDS used for triggering the sequences
- COTS components where possible (crate, MCH, FMC carriers)
- **Phoenix (1st gen QC):** Tens of RF DAC and ADC channels, camera readout module
- **Next Gen QC:** Tens of RF DAC and ADC channels, camera readout modules, optics control, …

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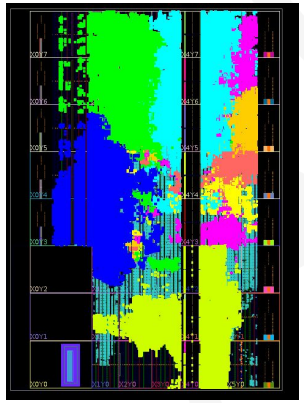
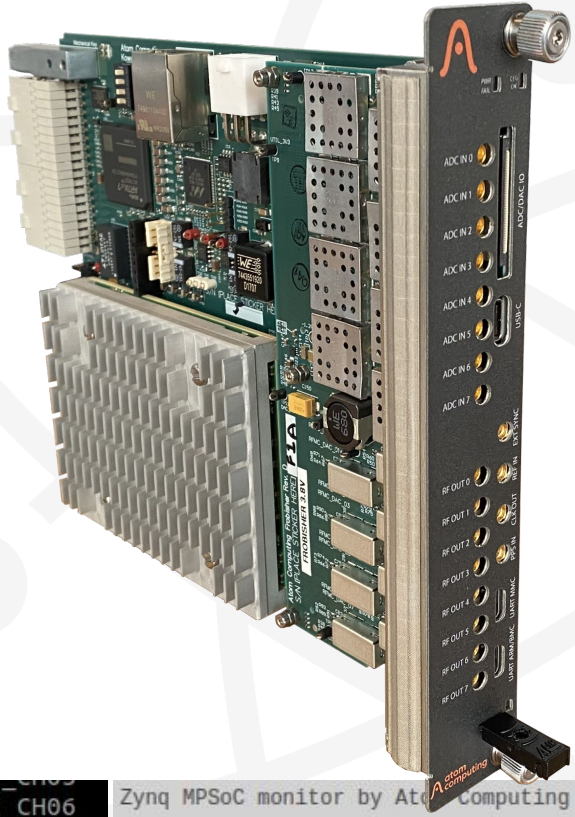
RFSoC-based SDR AMC

Generating waveforms in the GHz range

- Double width, full-size
- 3rd Gen Xilinx RFSoC
  - 8 ch 14-bit ADCs at 5 GSPS
  - 8 ch 14-bit DACs at ~10 GSPS
  - Large FPGA and a quad-core ARM
- RF on the front with AFE mezzanine (interchangeable with ZCU111)
- Backplane connectivity:
  - Gigabit Ethernet
  - TCLKA, MLVDS for triggering
  - point-to-point links
  - PCIe
- DESY MMC-Stamp (customized with SDK)
- Artix-7 for RTM (Class D1.1)
- Thermal OK(ish), power consumption OK






```
2.75 A      ok      I_CH06
0.00 A      ok      I_CH07
4.15 A      ok      I_CH08
0.00 A      ok      I_CH09
3.50 A      ok      I_CH10
3.45 A      ok      I_CH11
```

```
Zynq MPSoC monitor by Ato  Computing

Temperatures:
  ps_temp      = 59.95 degC
  remote_temp  = 61.04 degC
  pl_temp      = 65.22 degC
```

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Digital trigger Rear Transition Module

Providing triggers to other components

- Class D1.1: compatible with
  our RFSoC AMC and most of DESY cards
- Digital triggers outputs:
  control of external devices, camera triggers, …
- SFP links: control of magnet power supplies
  (UDP protocol over Gigabit Ethernet)
- LVDS lanes are driven by an Artix-7 on RFSoC AMC

```
mishipeshu> status
  status word = 0x0001000F
    link FSM state   = RUNNING (3)
    link ch0 aligned = 1
    link ch1 aligned = 1
    Zone 3 drive en  = 1
mishipeshu> uptime
  uptime: 58276 s
mishipeshu> lstats
  link statistics:
    words received      = 0x000003FE EA8CBC3E
    gt0 rx disp err     = 0
    gt0 rx not in table = 0
    gt1 rx disp err     = 0
    gt1 rx not in table = 0
```

Photo by Timothy Paule

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Precision DACs and ADCs FMC mezzanines

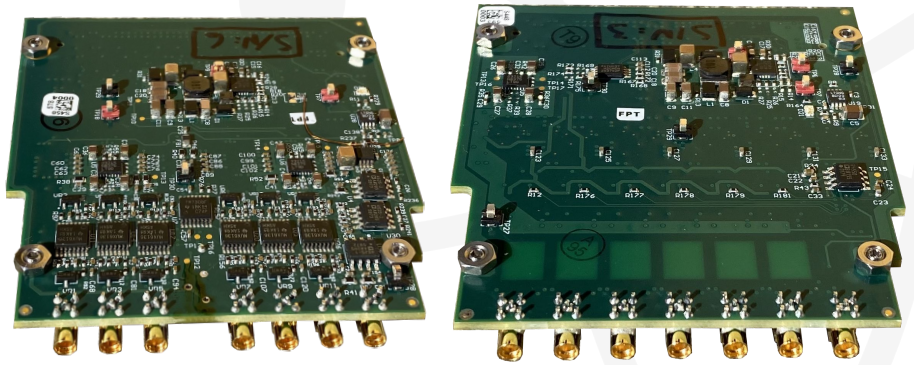
DAC

- VITA 57.1-compliant FMC mezzanine
- 6 DAC channels, 20 bit, 500 kSPS
- ±10V range
- Monitor output with analog mux
- User EEPROM for calib. parameters
- Temperature sensor on mgmt I2C (VITA 57.1 Subtype 1 record)

28	Full	Current	0xc1	0x63	0.352 A	ok	IMON_AVCCY
29	Full	Voltage	0xc1	0x63	0.7168 V	ok	Vcore
30	Full	Voltage	0xc1	0x63	1.8000 V	ok	VCC_Vadj
31	Full	Voltage	0xc1	0x63	1.2000 V	ok	VCC_1V2
32	Compact	0x14	0xc1	0x63	0x01		0x00 Opus DAC PG_M2C
33	Full	Temp	0xc1	0x63	31.0 C	ok	Opus DAC AT30TS7
34	Compact	0x14	0xc1	0x63	0x01		0x00 Opus DAC PG_M2C
35	Full	Temp	0xc1	0x63	30.5 C	ok	Opus DAC AT30TS7
36	Compact	0xf0	0xc1	0x63	0x10		HS 007 AMC3

ADC

- VITA 57.1-compliant FMC mezzanine
- 6 ADC channels, 18 bit, 2 MSPS
- ±10V range
- Monitor output with analog mux
- User EEPROM for calib. parameters



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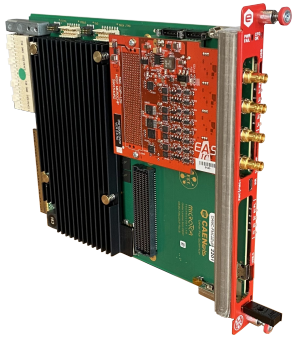
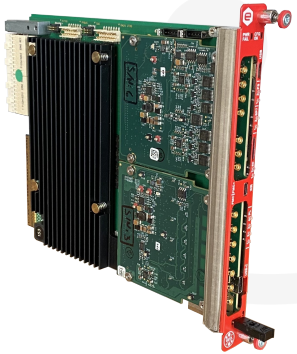
Combinations of FMC mezzanines

Addressing a wide range of applications

	Camera capture (quantum state readout)	Camera capture + IQ mixer calibration	Servoing piezos (adjustable optics)	Servoing more piezos (12 channels)
FMC1	CoaXPress	CoaXPress	DAC	DAC
FMC2		DAC	ADC	DAC





Init script auto-detects those variants and choses the corresponding FPGA bitstream

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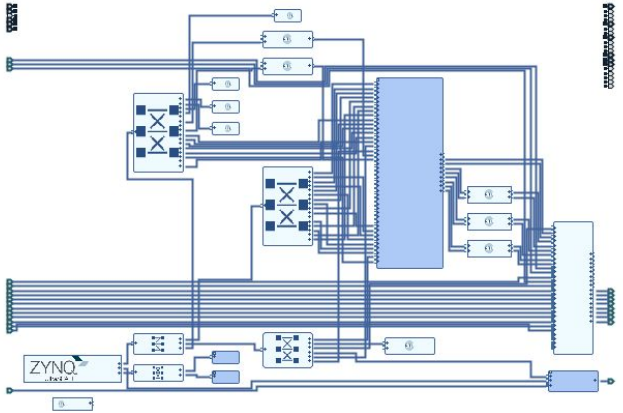
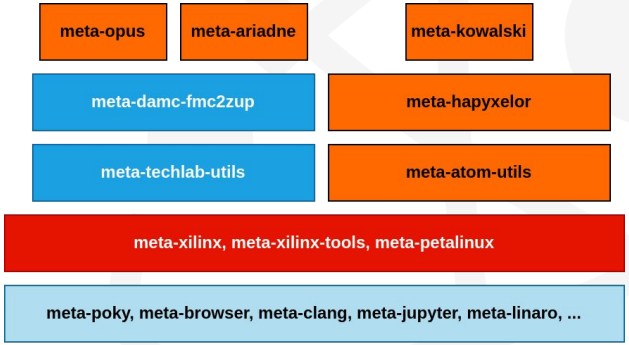
Gateware and software

Running on top of MicroTCA hardware

- Several Vivado projects:
  - RF generation and feedback
  - fiber noise cancelation
  - camera capture
  - piezo control
- IP library to simplify code reuse
- Yocto-based compilation flow, custom layers per AMC and project
- systemd as an init system
- All AMCs run GRPC servers on ARM, communicating with the middleware over backplane Ethernet






```
UNIT                                              LOAD      ACTIVE
atom.kowalski.fpga-load.service                   loaded    active
atom.kowalski.hapyxelor-server.service            loaded    active
atom.kowalski.lan0-marvell-phy-diff-swing.service loaded    inactive
atom.kowalski.rfsoc-clock.service                 loaded    inactive
```

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OUR EXPERIENCE WITH MICROTCA

Distributed company

Several locations throughout the US

Legend:

- Control System team
- Quantum Computers
- Yocto Package Server

Advantages of MicroTCA

Using MicroTCA for QC control system

- Remote management, configuration and monitoring, remote JTAG
- MicroTCA offers a well-defined form factor for custom developments
- COTS components where possible:
  - MCHs, crates, FMC carriers
  - MMC implementation from DESY
- Advanced features of DESY MMC-Stamp:
  - SDK for customization (working around HW issues in “software”, saved a board respin)
  - UART over IPMI, JTAG switch, very robust and featureful FRU parsing (FMC)
  - Currently working on integrating the newest features on our board (Sven’s presentation on Thu: “DESY MMC Solutions [...]”)
- Several boot sources on some boards (e.g. recovery boot on DAMC-FMC2ZUP)

Photo by Justin Ging

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Remote update

Updates without PICMG HPM.1

- Requires a technician on site
- 1 hour preparation +
  10 minute procedure per board
- Not a fail-proof procedure
  (no recovery image)
- Current FW version check non-trivial

Updates with PICMG HPM.1

- Can be done fully remotely
- ~minutes per board, easily automated
- (typically) recovery image present
- Possibility to check the running version

```
PICMG HPM.1 Upgrade Agent 1.0.9:

Validating firmware image integrity...OK
Performing preparation stage...OK

Performing upgrade stage:

--------------------------------------------------------------------------------
|ID  | Name        |                    Versions                        | %  |
|    |             |      Active     |      Backup     |      File       |    |
|----|-------------|-----------------|-----------------|-----------------|----|
|   0|FMC2ZUP-MMC  |   1.20 00000010 | ---.-- -------- |   2.00 00000000 |100%|
|    |Upload Time: 01:14             | Image Size:  186580 bytes         |    |
--------------------------------------------------------------------------------
(*) Component requires Payload Cold Reset

Firmware upgrade procedure successful
```

SUMMARY

Summary

MicroTCA at Atom Computing

- MicroTCA was crucial for rapid development of the control system for QCs
- Developing our own RFSoC AMC was a right decision
  (time to “market”, flexibility)
- Good support from MicroTCA Tech Lab at DESY, a lot of resources
- Some smaller interoperability issues, long lead times for some components
- Atom Computing made some (smaller) contributions to the community
  (e.g. backplane FRU parsing in frugy, I2C communication with MMC-Stamp)
- Modular and scalable platforms are also the future for QC control systems:
  Quantum Error Correction will require even tighter integration between components

“[…] **we estimate that several terabytes per second of bandwidth will be required between the quantum and classical plane.”** from Beverland et al, Assessing requirements to scale to practical quantum advantage

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Thank you!