Development of the MicroTCA Standard

Preparing the Next Generation

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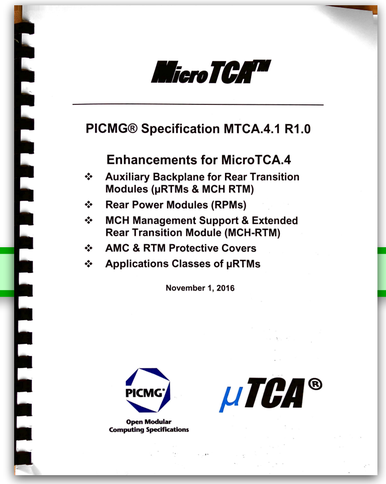
MicroTCA Specifications

MicroTCA.0

2006

MicroTCA.4

2011



MicroTCA.4.1

2016

Next Gen

2023

MicroTCA.0

2020

Rev. 3

> 740 Pages

MicroTCA.0

2022

Requirements for the Next Generation

- **Keep the standard alive for a long time**
  - Adapt state-of-the-art technology

- **Backward compatibility**
  - All existing AMC modules MUST be usable

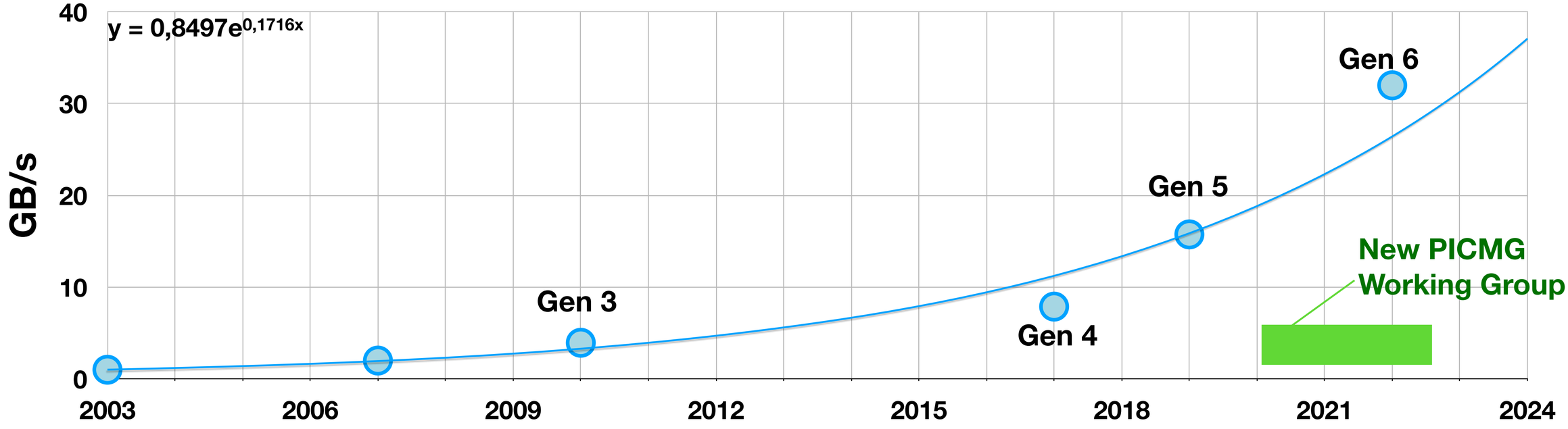
Motivation: Technology Trends

PCI Express version	Introduced	Line code	Transfer rate	Throughput (simplex)				
				×1	×2	×4	×8	×16
1.0	2003		2.5 GT/s	250 MB/s	0.50 GB/s	**1.0 GB/s**	2.0 GB/s	4.0 GB/s
2.0	2007	8b/10b	5.0 GT/s	500 MB/s	1.0 GB/s	**2.0 GB/s**	4.0 GB/s	8.0 GB/s
3.0	2010		**8.0 GT/s**	985 MB/s	1.97 GB/s	**3.9 GB/s**	7.88 GB/s	15.8 GB/s
4.0	2017	128b/130b	16.0 GT/s	1969 MB/s	3.94 GB/s	**7.9 GB/s**	15.75 GB/s	31.5 GB/s
5.0	*2019*	128b/130b	**32.0 GT/s**	3938 MB/s	7.88 GB/s	**15.8 GB/s**	31.51 GB/	63.0 GB/s

Now

Goal

Transfer Rate 4 Lanes / Specs ready (Test specs + 1 year)



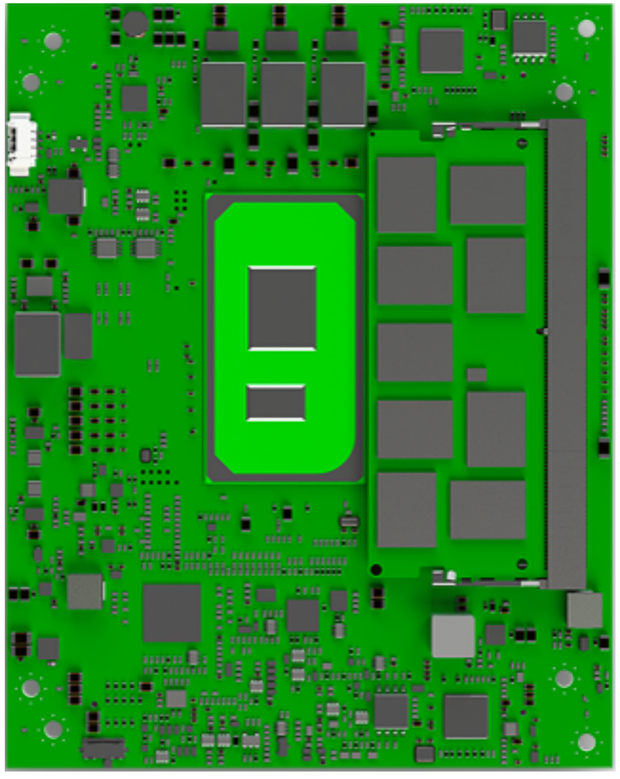
Technology Trends: CPU & FPGA

COM-HPC defines the direction of technology

- Client type modules up to **200 Watt**
- Up to 49 **PCIe gen 5** lanes
- PICMG published 2021

Actual design:

- Intel 12th Gen: PCIe gen 5



© SECO

FPGA & PCI board

- PCIe gen 4
- **≤ 225 W**

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PICMG MicroTCA Next Generation Working Group

Initial Executive Members … 14.11.2019	**ESS** **DESY** **Lodz University of Technology** **N.A.T.** **nVent**
+ Members of working group	**Amphenol** **Atom Computing** **BAE Systems** **Comtel** **Concurrent Technologies** **Embeck** **IOxOS** **MicroLab** **ORNL** **Pixus Technologies** **Positronic** **powerBridge** **Samtec** **VadaTech** **Yamaichi**

Chair	**Kay Rehlich, DESY**
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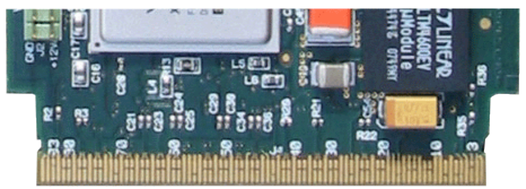
Secretary	**Thomas Holzapfel, powerBridge**

Challenges: Speed

- **PCIe gen 5**
  - AMC card-edge & backplane connector allows 32 GT/s
  - Simulation of a full channel was done w/ newest PCI-SIG test specs
  - Routing is not simple, high speed PCB material is required
  - Simulation shows that 32 GT/s will work
- **100 G Ethernet**
  - Simulation shows that 25 GT/s will work

- Main challenge is the crosstalk
- MicroTCA Next Gen: Provide PCIe x8 or x16 with **two connectors**
  —> up to factor 8 or 16 more throughput & lower latency than today!

AMC Connector Options



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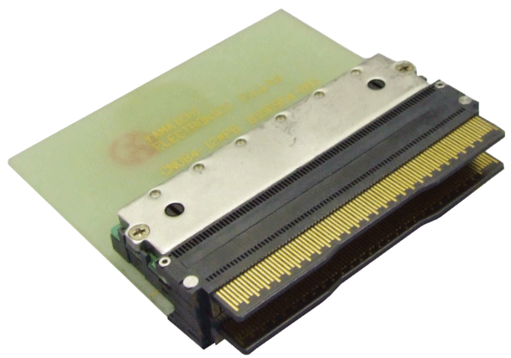

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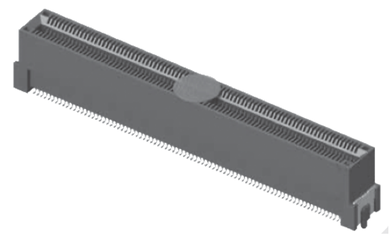


Backplane connector:

No change required

Improved PCB layout

Harting connector does not allow > PCIe gen 3 (remains backward compatible)

Options for the AMC are:

1. PCB Card Edge contacts
2. Yamaichi connector

PCB thickness = 1.6 mm !

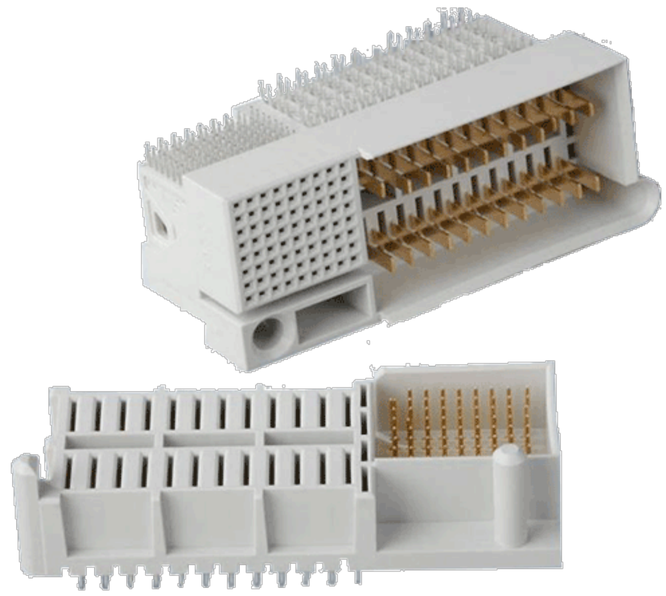
Challenges: Power

More speed ==> more power

MCH requires more than 80 W!

Challenges: Power

- **> 80 W for MCH and Fan**
  - Limitation of AMC connector: 8 pins @ 10.8 V = 98 W
  - Limitation of Power Module connector: 110 W
- **Solution:**
  - Use 9 power pins on MCH



- **Crate cooling**
  - More airflow ==>

    Fans need more power

Strategy

- First Step
  - **Update MTCA.0**
    - Specs for PCIe gen 5 and Ethernet 25 G / lane
    - 110 W for MCH and cooling

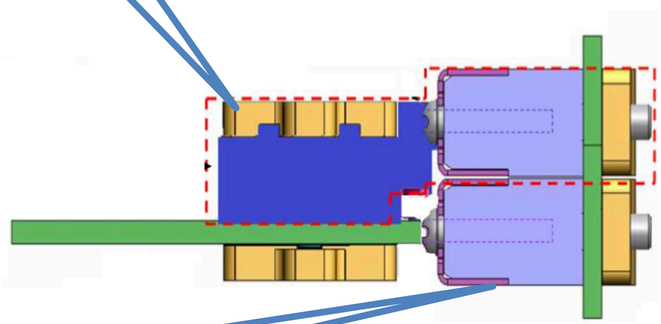
Almost ready

- Second Step
  - **MicroTCA Next Generation**
    - Improved MCH with more Fat Pipe channels
    - Optional 2nd connector for AMCs: more PCIe lanes
    - Up to 220 W per power channel

AMC Connector for 220 W and More Connectivity

New Yamaichi Connector

More Fat Pipe lanes e.g. PCIe x8, x16

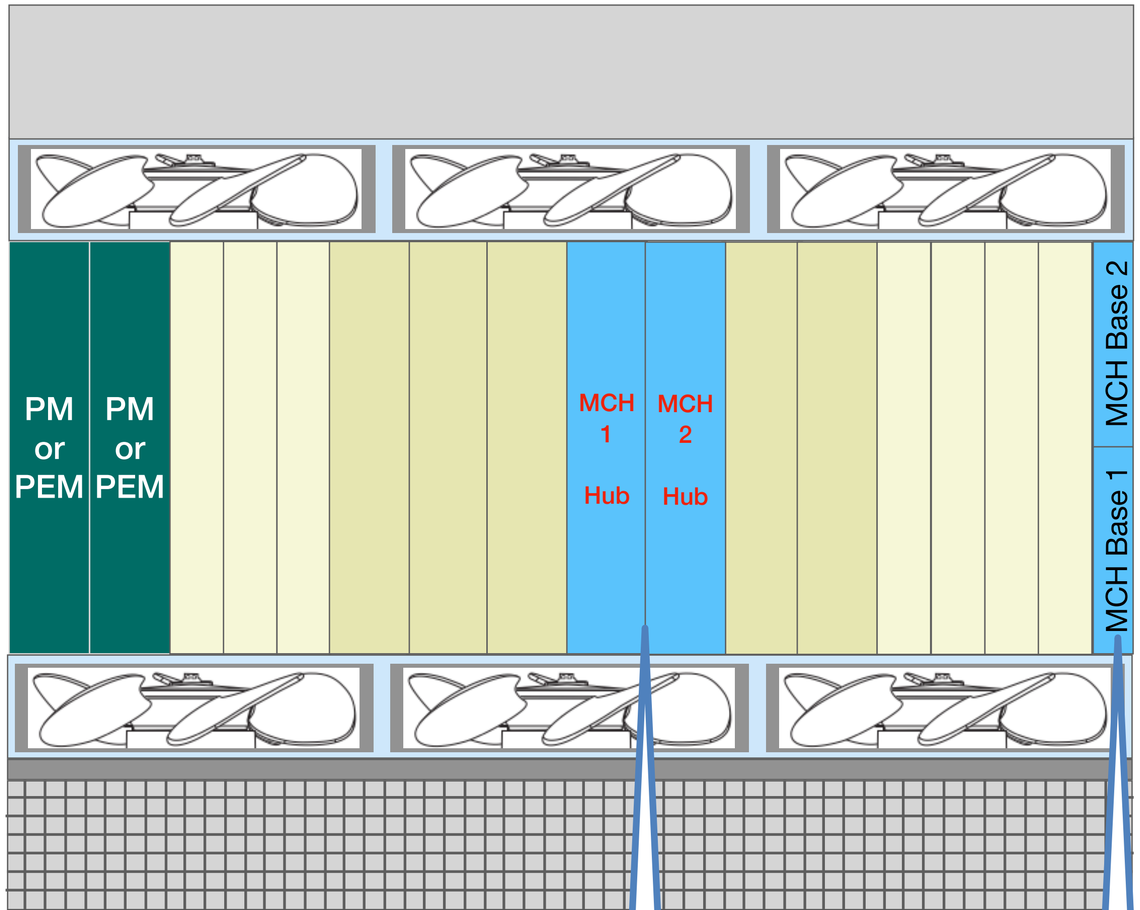


220 W: 2 * 9 power Pins

Card-edge Connector

Split MCH: Base and Hub

Preliminary



A separate Hub has advantages:

- More fat pipes (e.g. PCIe lanes) possible
- Self-contained hot-swap
- Same power channel w/ Base
- Application specific designs possible
- Independent upgrade
- Better cooling for next gen switches

Hub in the middle of the crate to ease high speed links routing and damping

MCH Base: crate management
Ethernet hub (ports 0, 1)
Clock module

Conclusions

Tough goals:

- 2 kW per crate
- 220 W max. per AMC slot
- 32 GT/s PCIe gen 5

1. Step —> MTCA.0 Rev. 3

- To PICMG “procedure” this year
- Defines 32 GT/s
- Defines 110 W for MCH and cooling

Still lots of work to be done:

- Find best cooling solution
- Definition of connectivity
- Definition of management
- Further items:
  - Ports 2, 3 protocols
  - FMC management
- …
- Building prototypes
- Writing specs