MicroTCA.4 Standard

Communication Links, Clocks & Triggers

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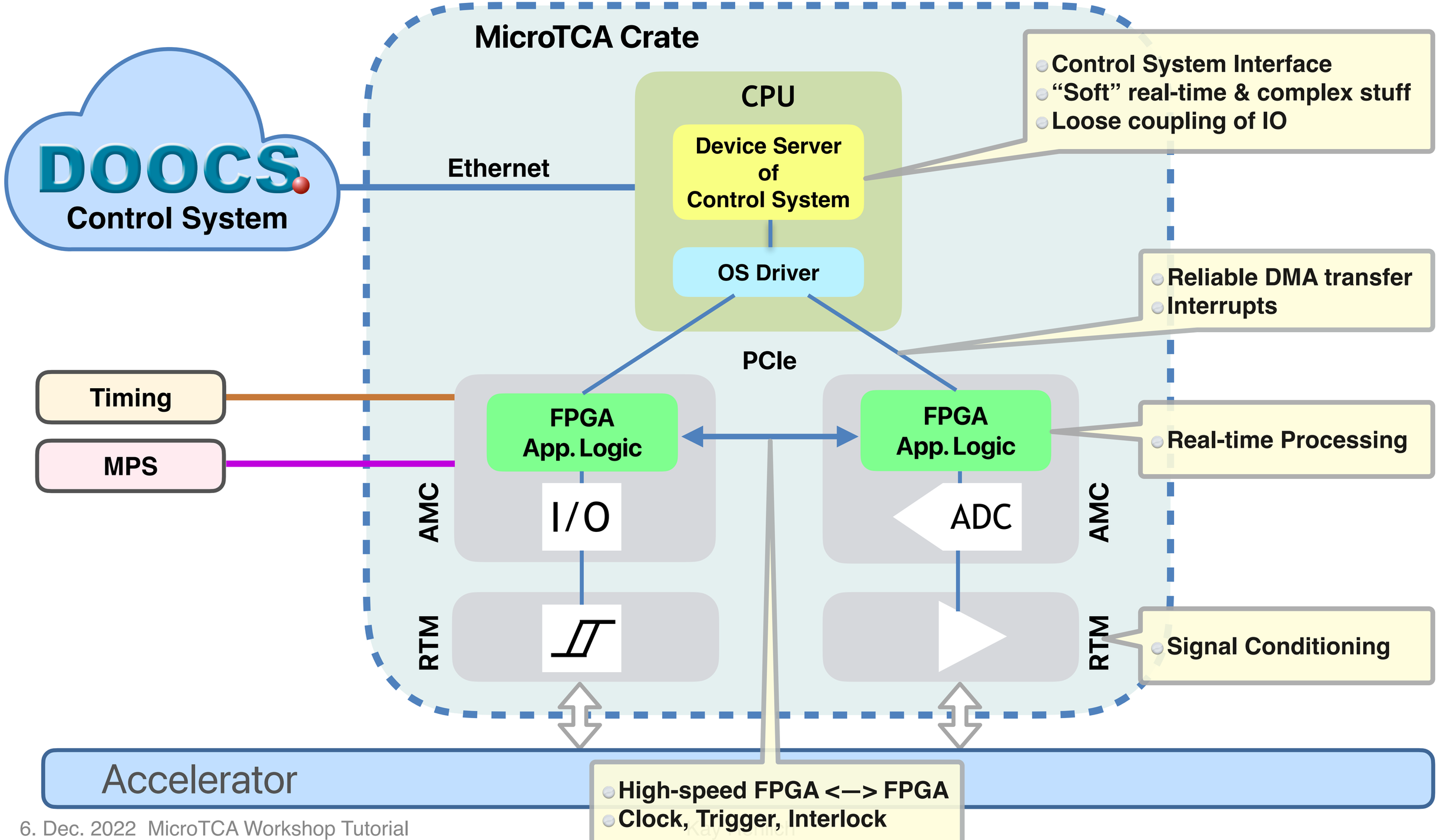
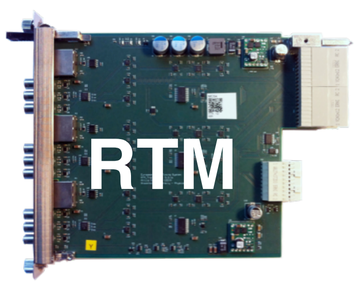
DESY

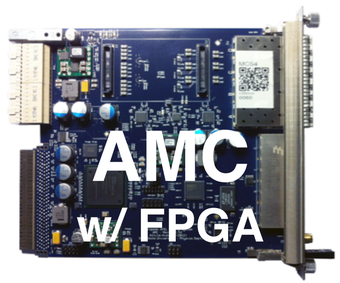
Example: European XFEL Software Architecture

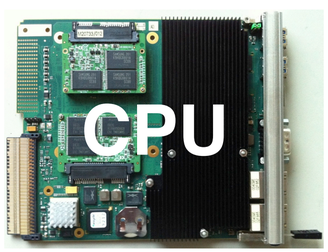


Motivation

Why did we select MicroTCA for XFEL

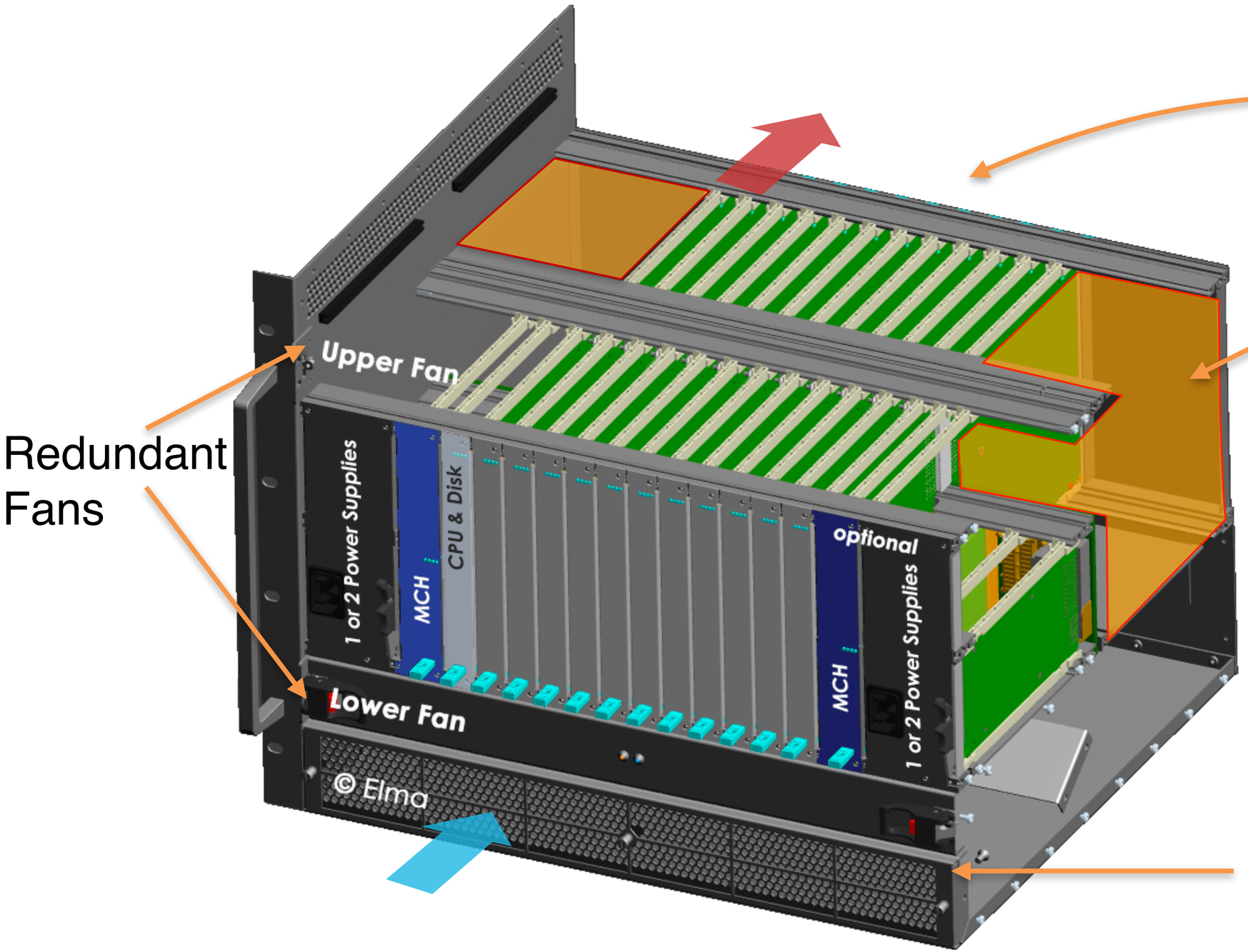






- **Modularity** !!!
- Standard hardware & software **interfaces**
- **Loose coupling** of components
  - Implement functions on the right component (architecture):
  - Do complex stuff on a standard **CPU**: faster development
  - Do real-time on **FPGA**: Allow CPU software to crash without disturbing accelerator operation
- Simplified **maintenance** and good **diagnostics** of all components
- **Remote management** is a MUST for large facilities
- **Redundancy** of key components
- Integrated and standardised **clock, trigger, interlock** distribution
- Modern **communication links** (high-speed and low noise)

MicroTCA.4: A Modular Crate System



Most cables from rear

Space for ….

MTCA.4.1

Redundant Fans

1 … 4 Power Supplies

Filter

MicroTCA Crate Backplane Communication

Common modules

Application modules

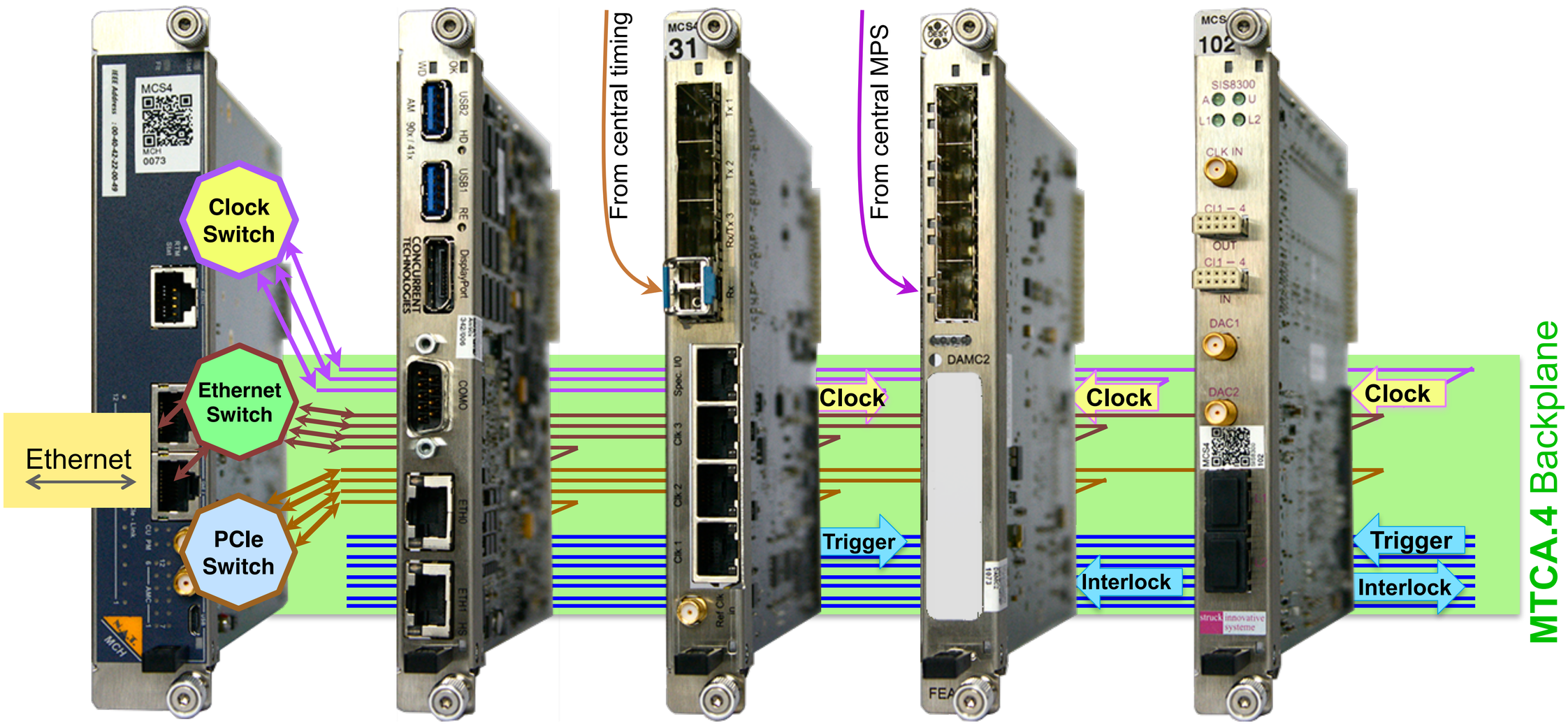
MCH

CPU

Timing

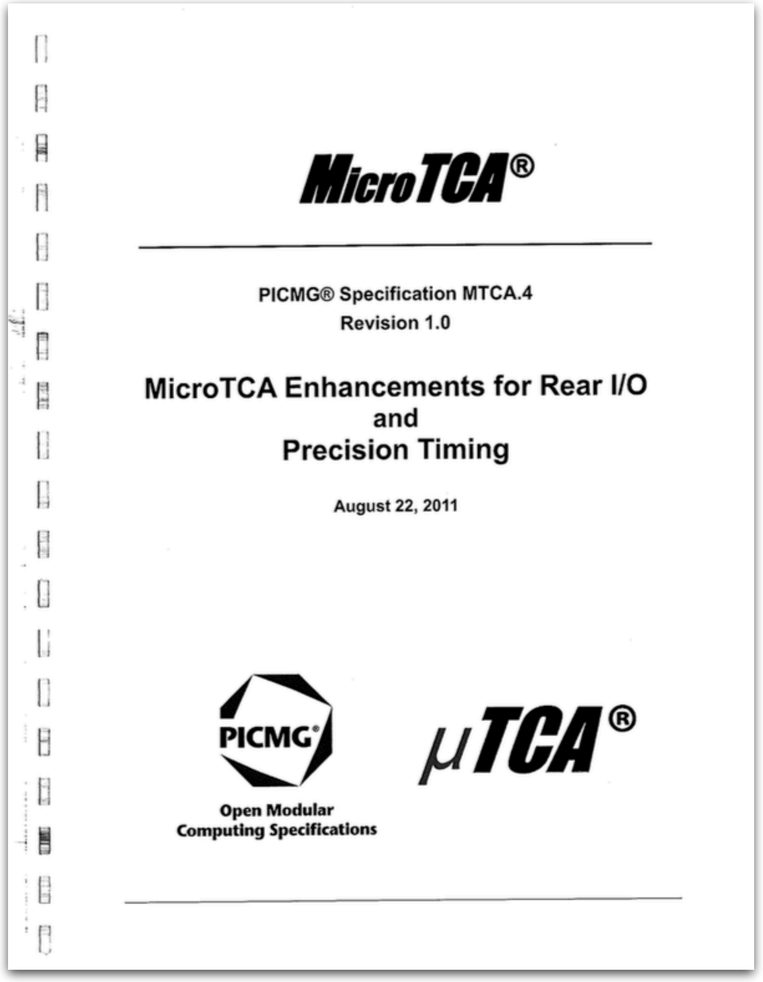
Machine Protection System

ADC
Digi. IO
Controller
….

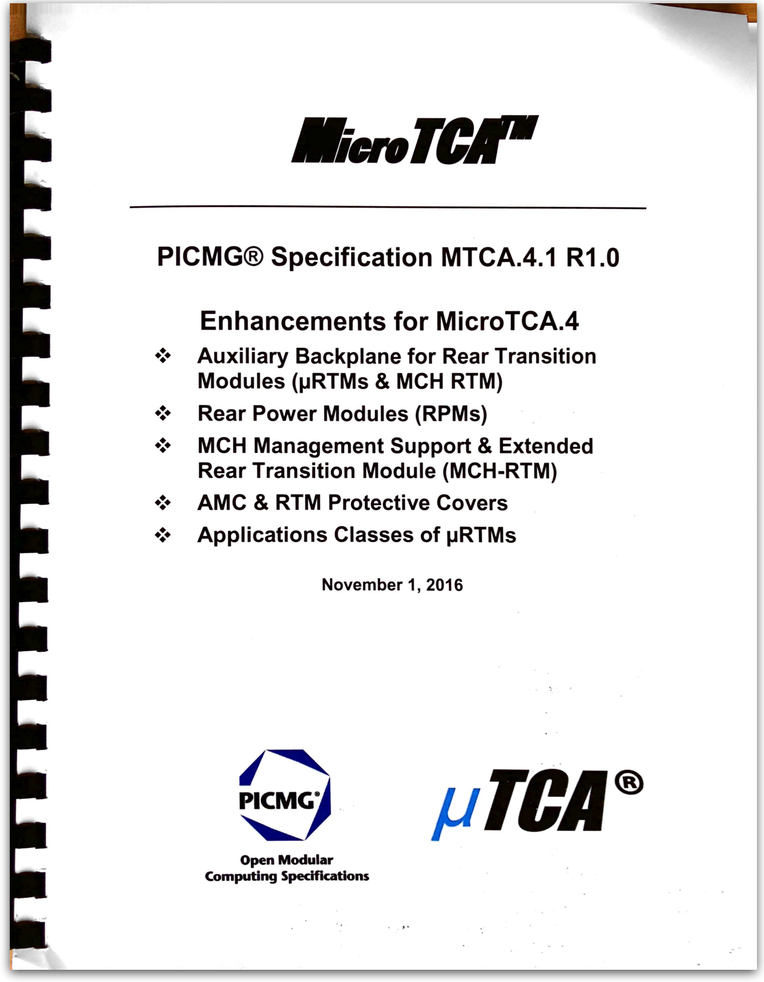


MTCA Specifications

MicroTCA.0



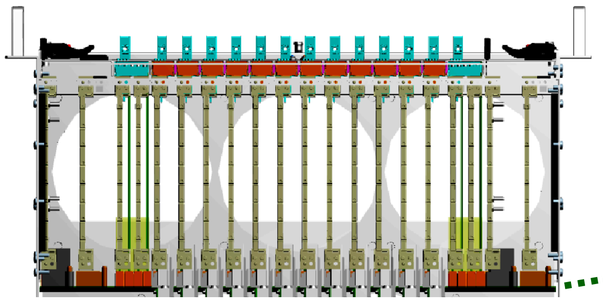
MicroTCA.4

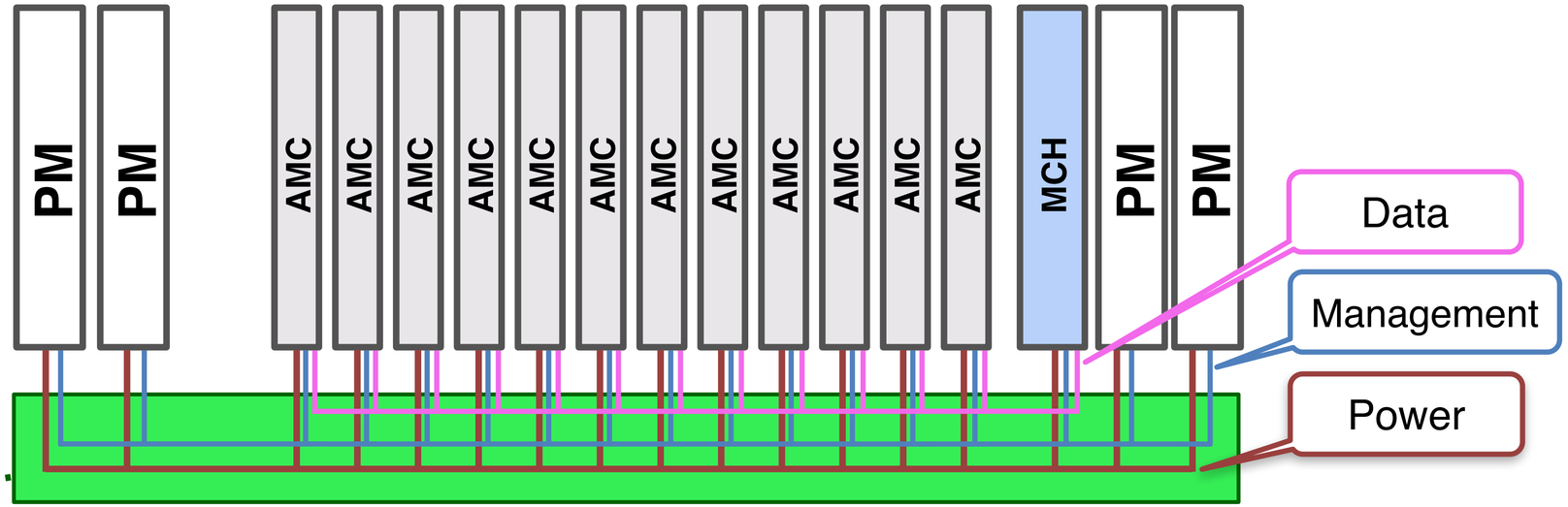


MicroTCA.4.1

MicroTCA Generations: **MTCA.0** MTCA.4 MTCA.4.1

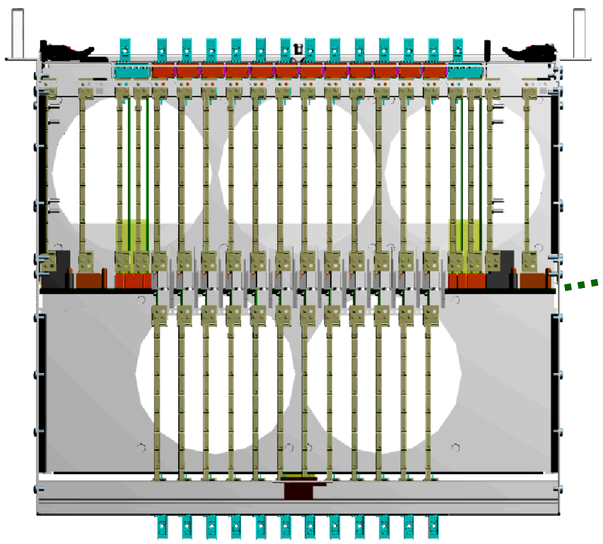
Front Side



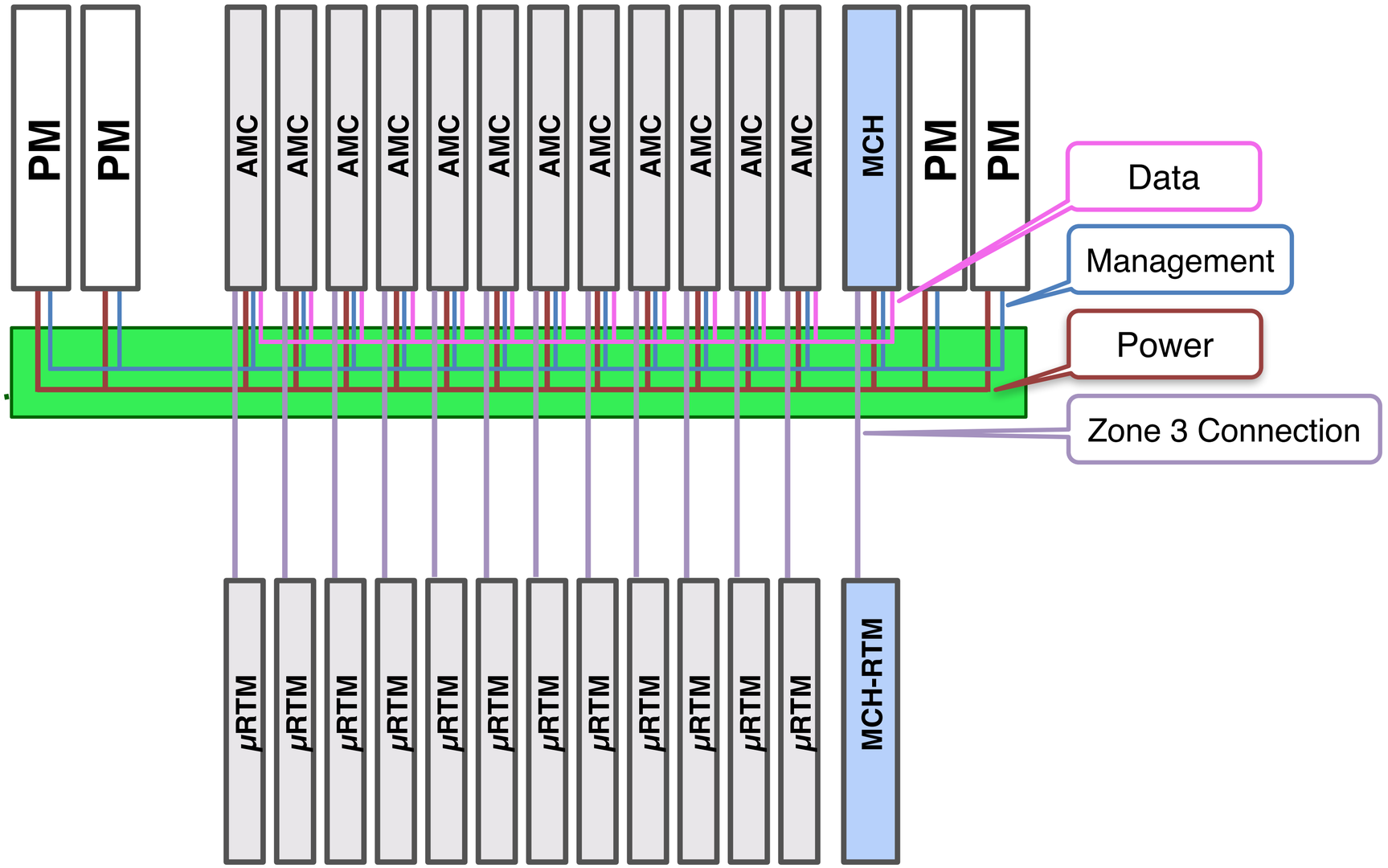


MicroTCA Generations: MTCA.0 **MTCA.4** MTCA.4.1

Front Side

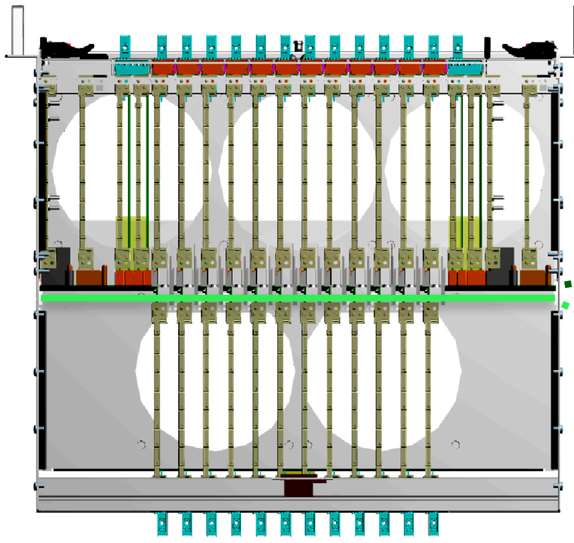


Rear Side

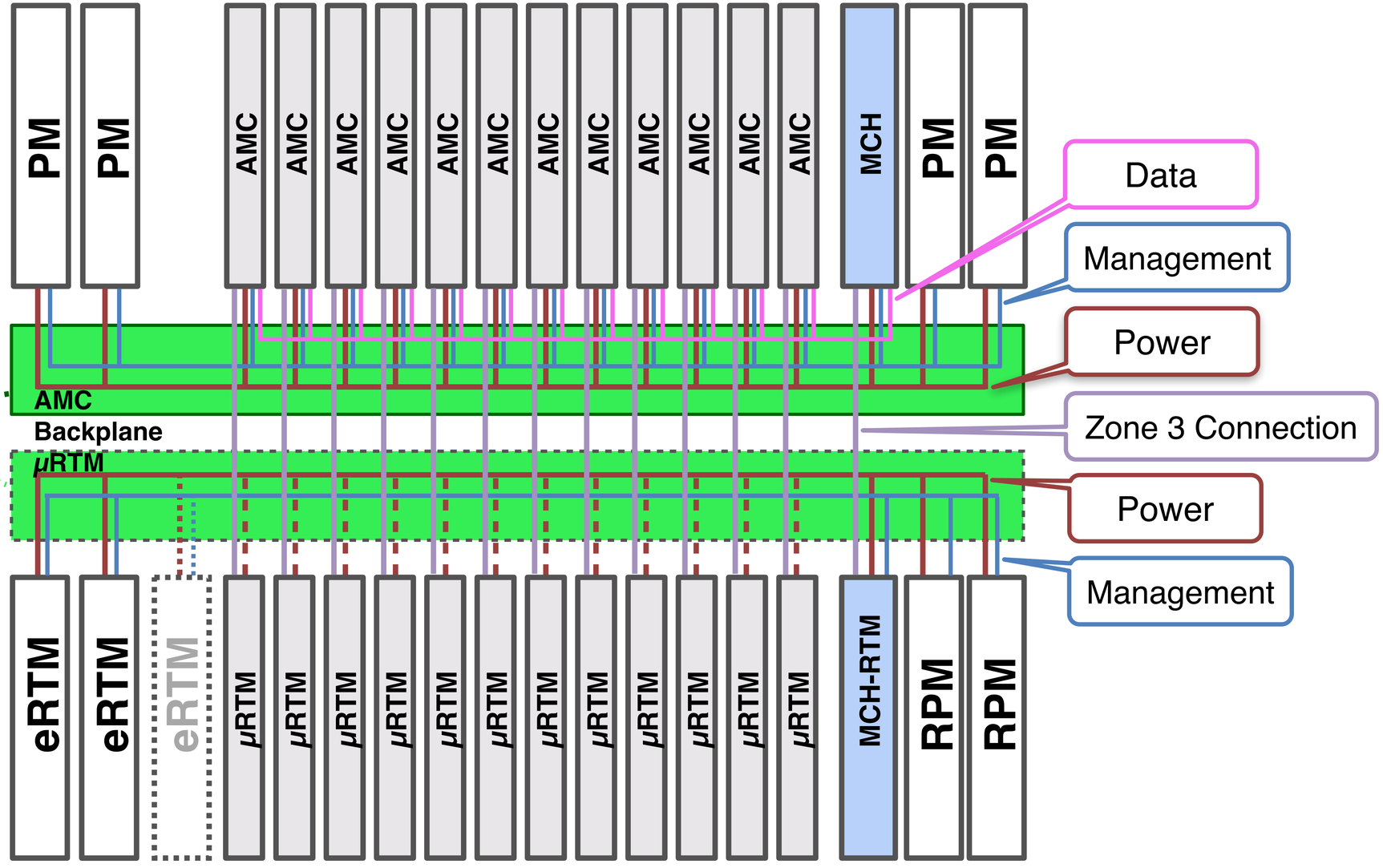


MicroTCA Generations: MTCA.0 MTCA.4 **MTCA.4.1**

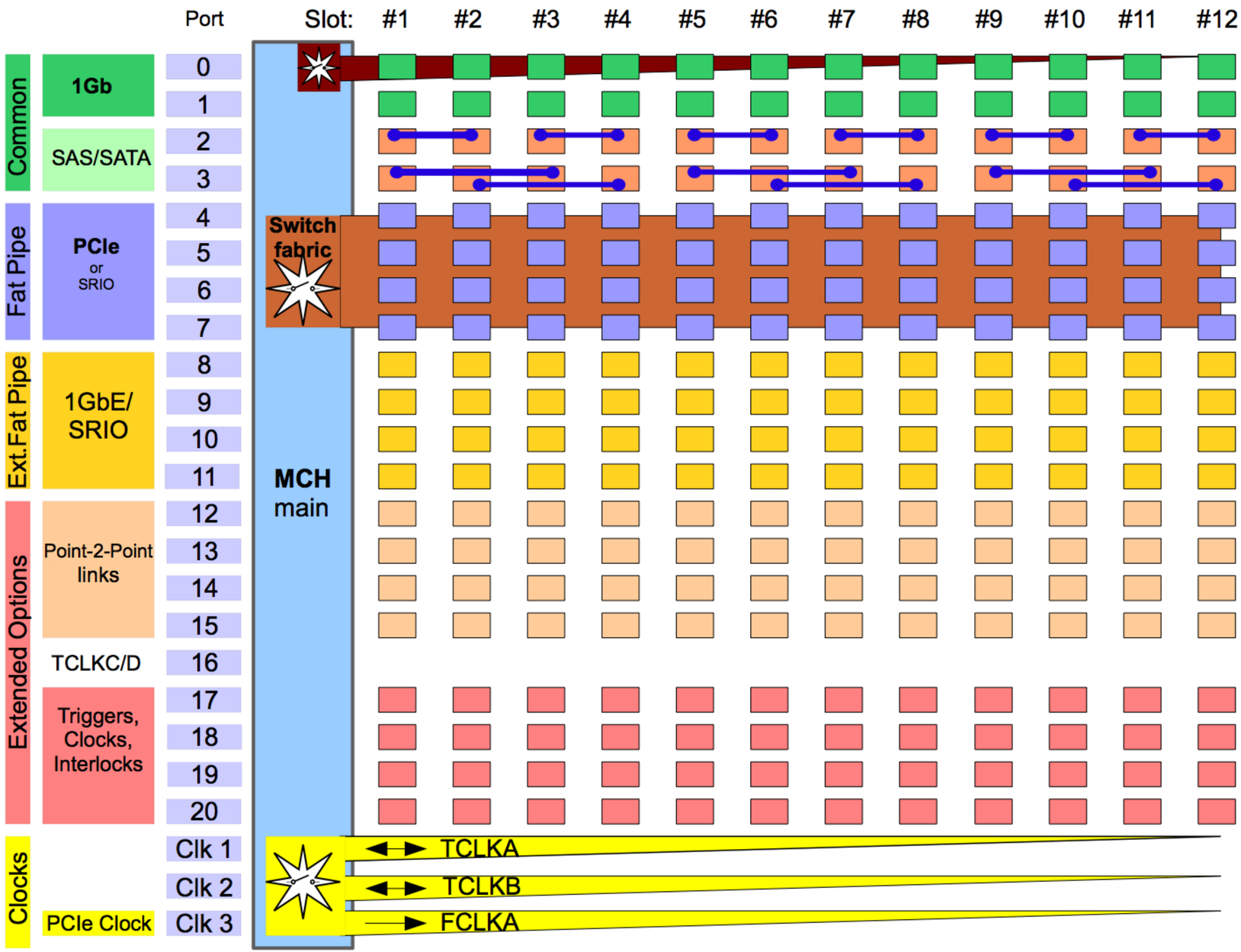
Front Side



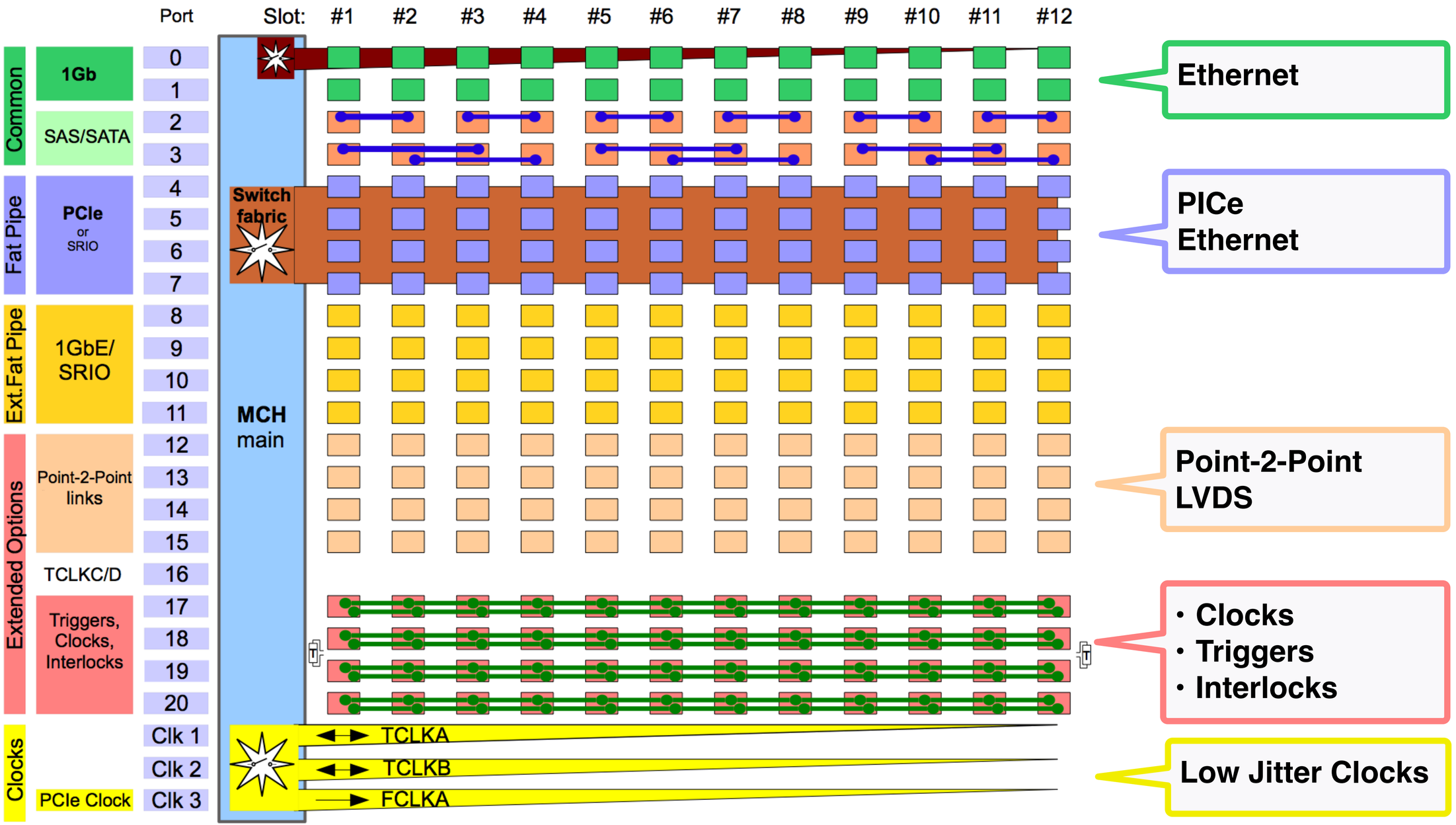
Rear Side



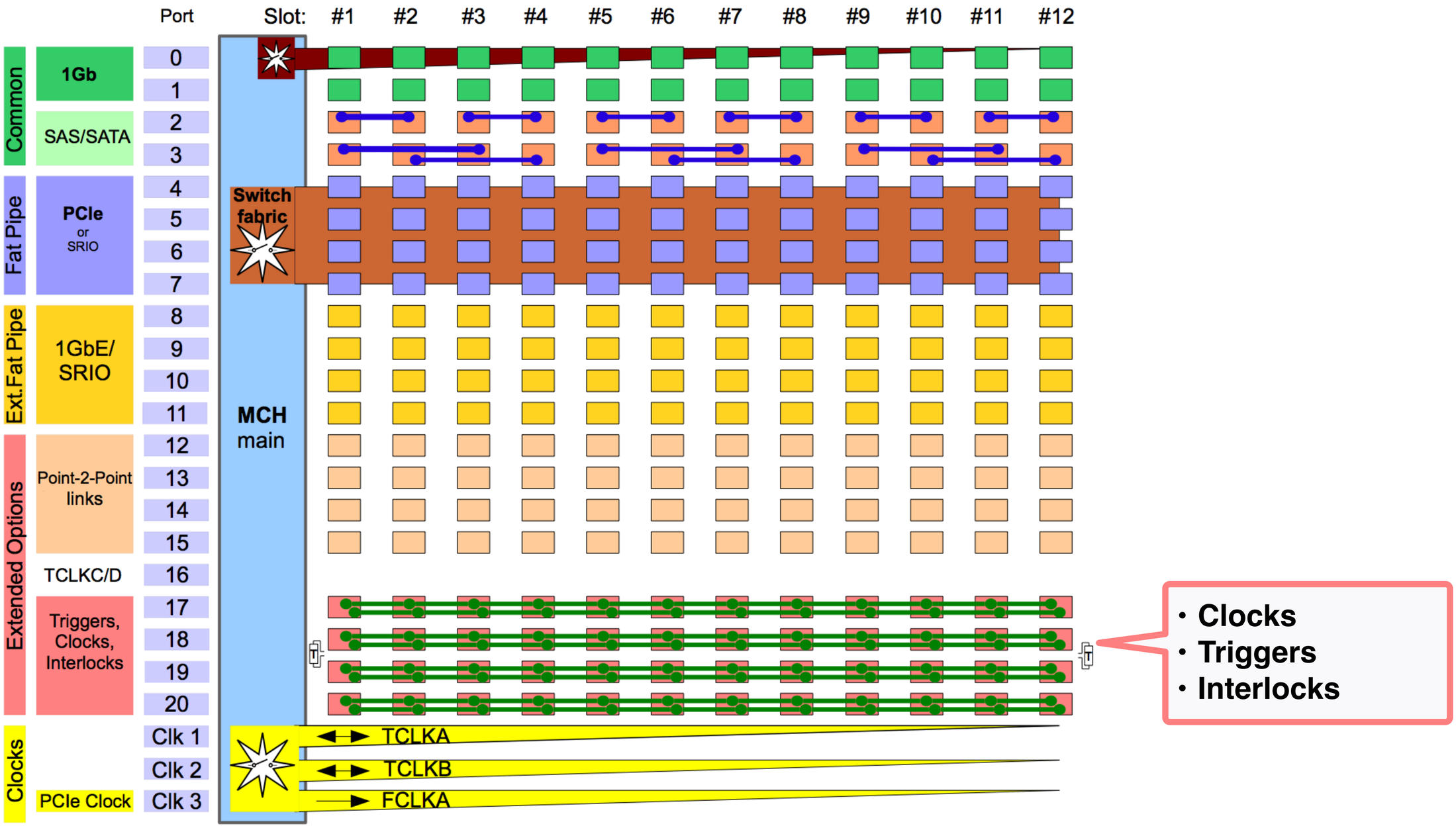
Basic MTCA.0


Port
Slot:
#1
#2
#3
#4
#5
#6
#7
#8
#9
#10
#11
#12
Common
1Gb
SAS/SATA
Fat Pipe
PCIe
or
SRIO
Ext.Fat Pipe
1GbE/
SRIO
Extended Options
Point-2-Point
links
TCLKC/D
Triggers,
Clocks,
Interlocks
Clocks
PCIe Clock
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
Clk 1
Clk 2
Clk 3
Switch
fabric
MCH
main
TCLKA
TCLKB
FCLKA

MTCA.4: Communication Links



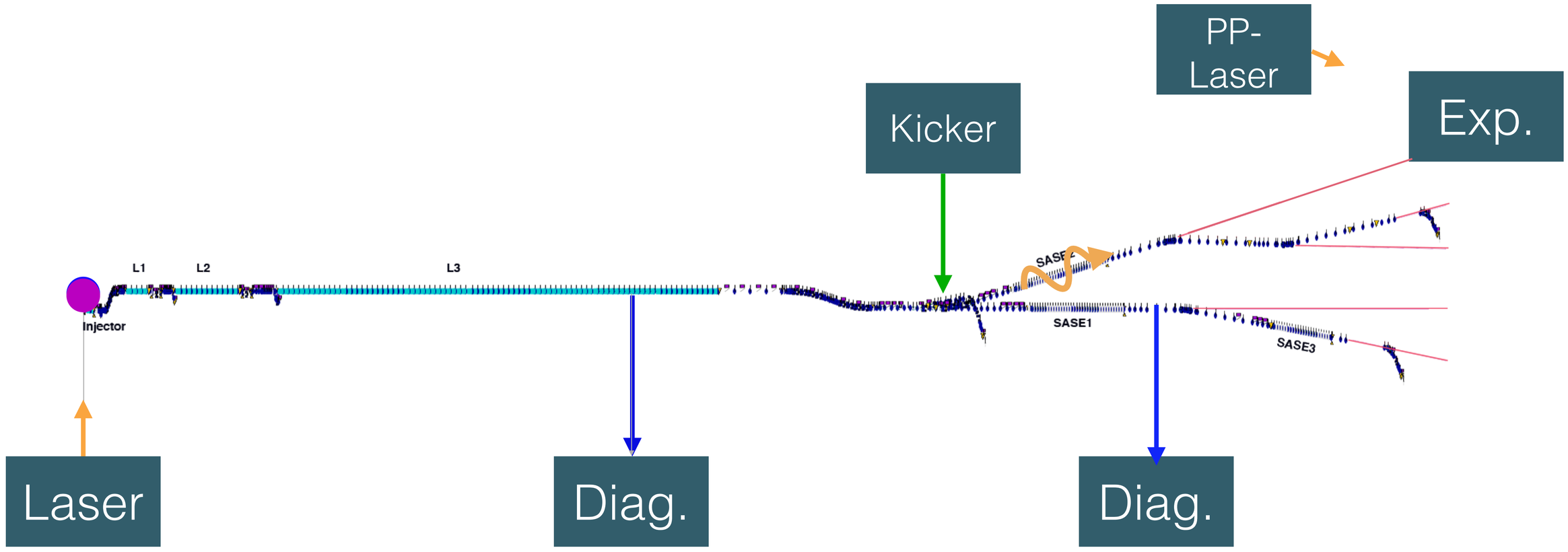
Versatile MLVDS Links



Usage of the MLVDS Bus Lines

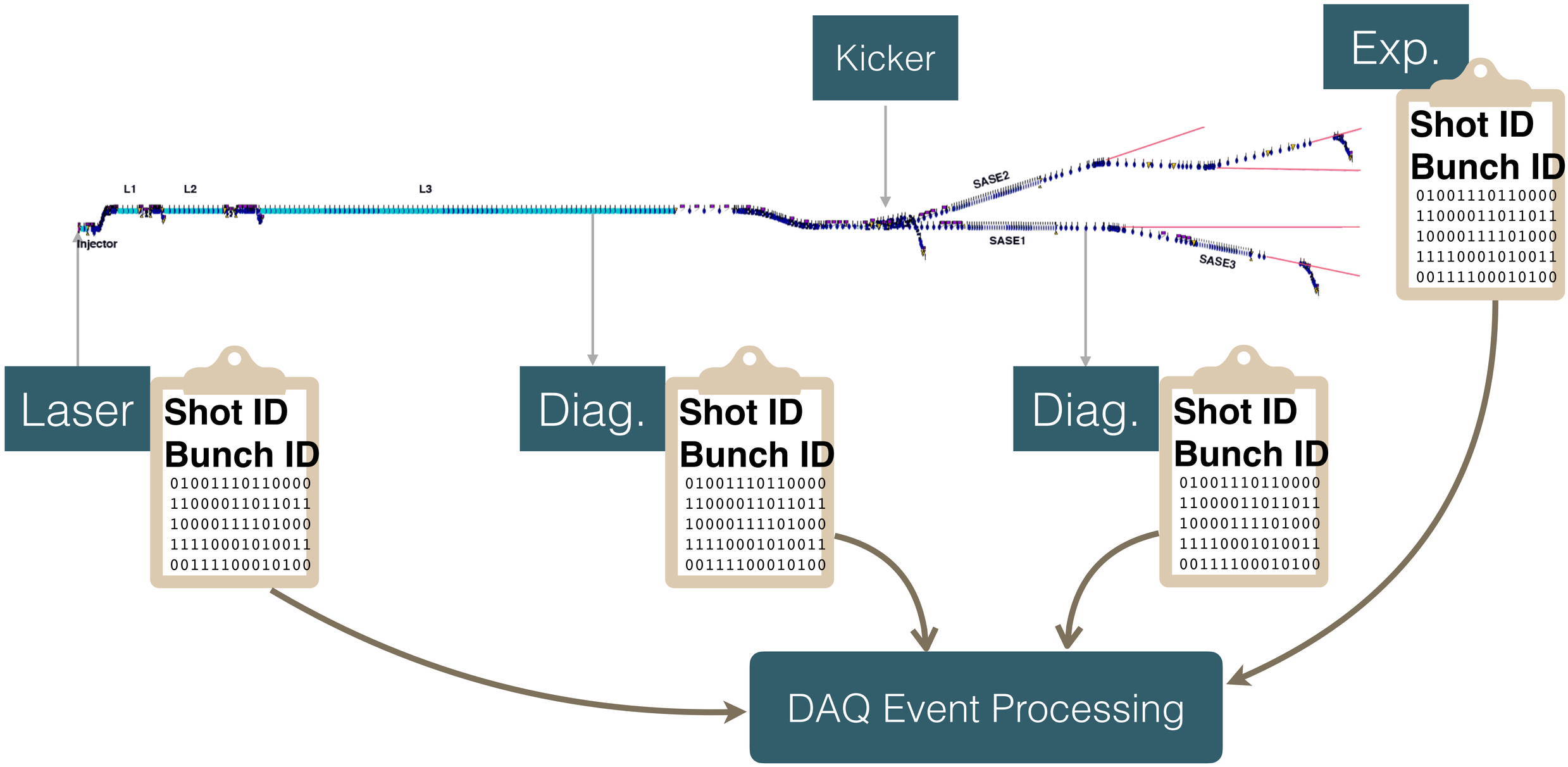
- **Trigger or Gate** 1 —> N
- **Clock** 1 —> N
- **Gated Clock** 1 —> N
- **Interlock** M —> N
- **Data transfer FPGA <—> FPGA** 1 —> N
  - e.g. **Timing** AMC —> **ADC** AMC

Introduction - Clocks & Triggers

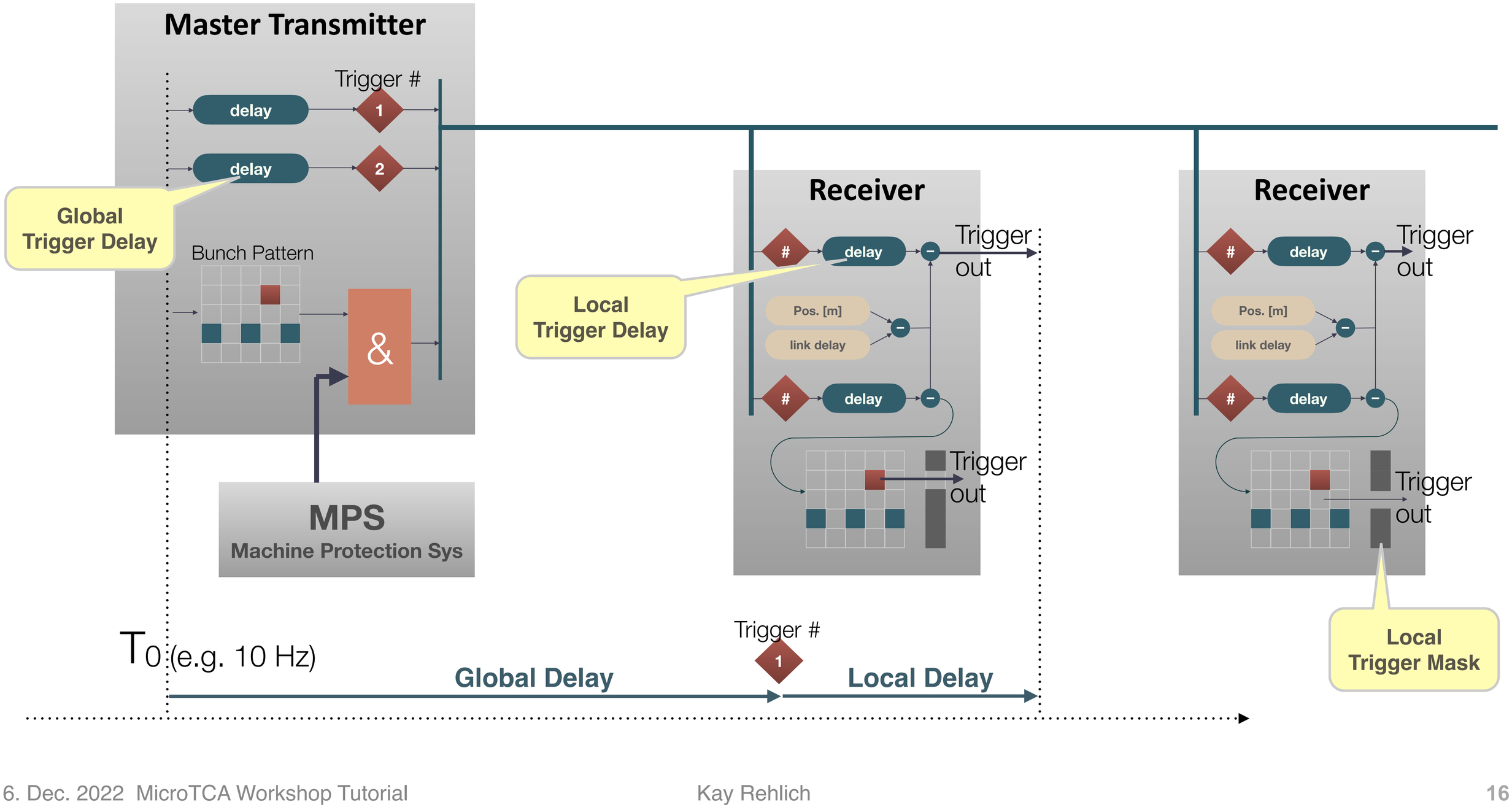


- Define the source and destination of bunches (XFEL: 27000 / sec.)
- Trigger and clocks for diagnostics and actuators depending on location

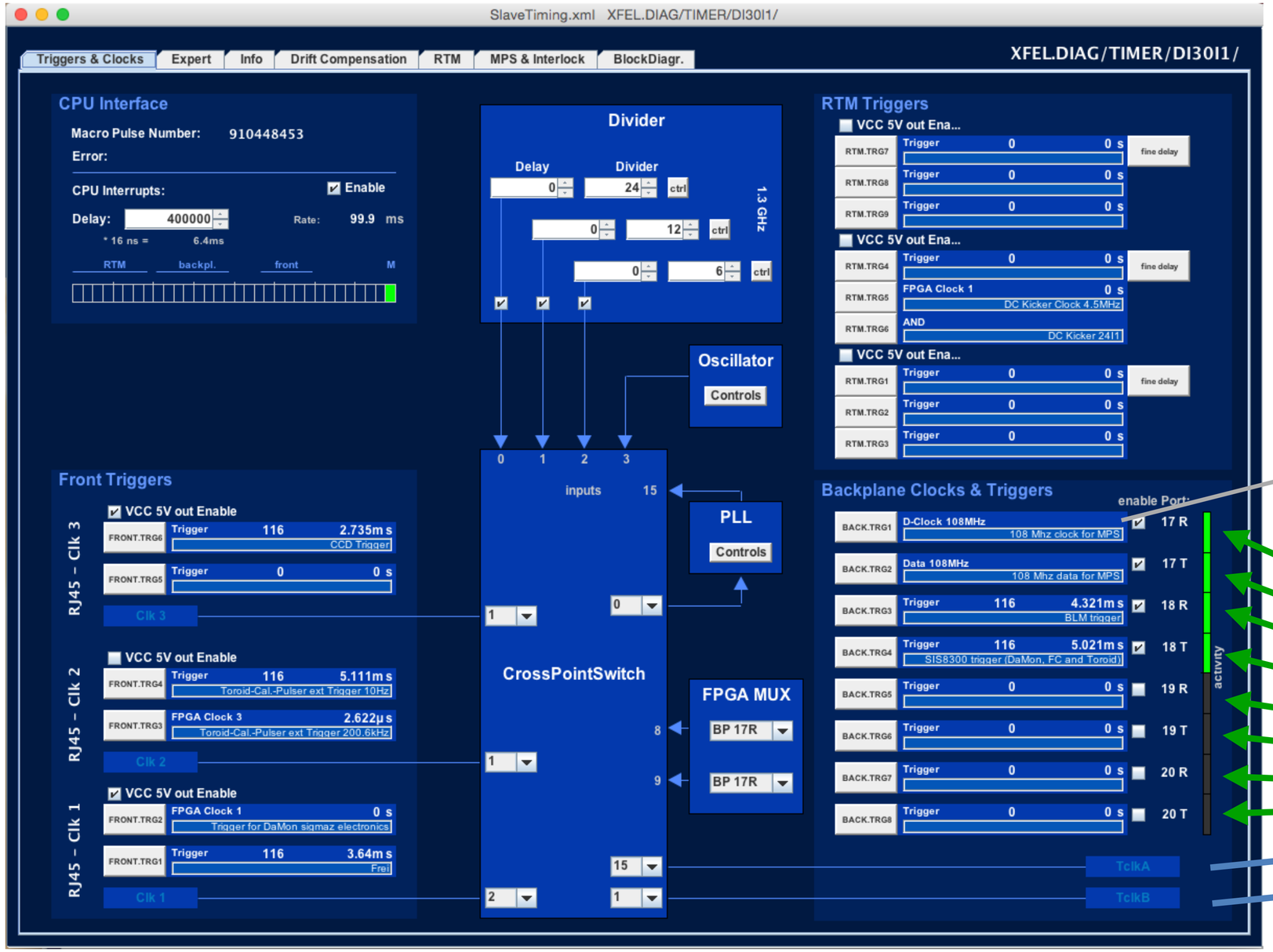
Introduction - Data Tags for Software



Trigger and Bunch Pattern Distribution



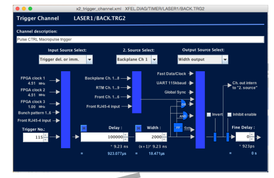
Usage of the MLVDS Lines: Timing Example



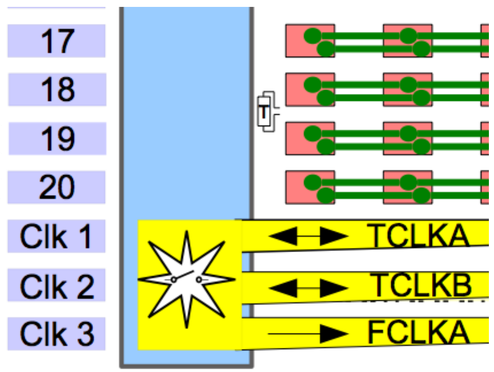
RTM Outputs

Front Outputs

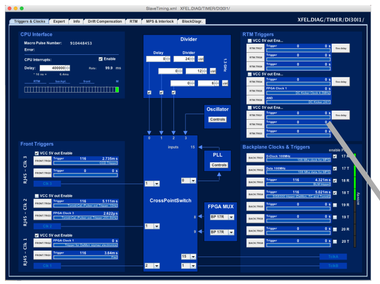
Channel configuration

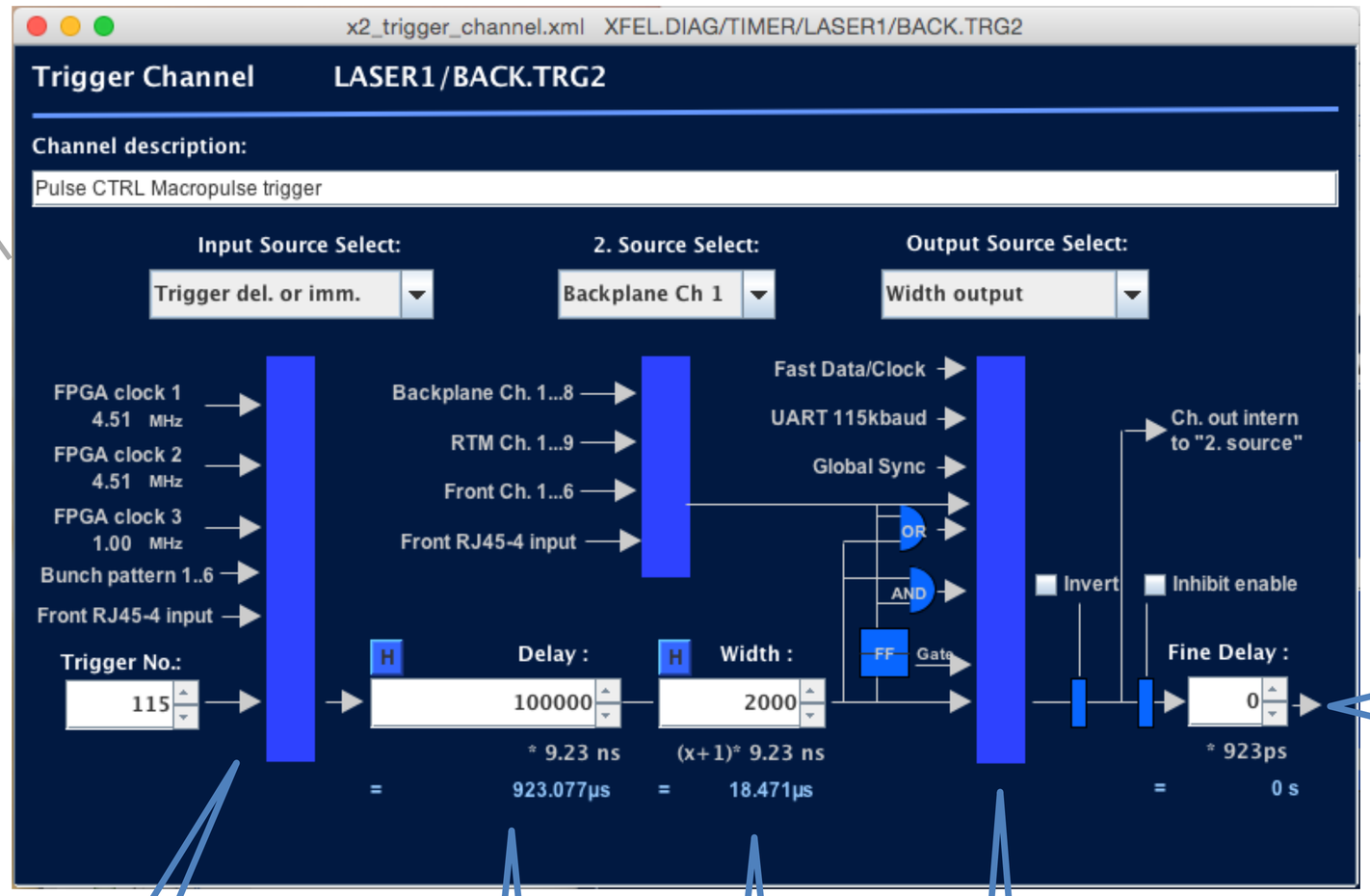


Backplane Outputs



One Trigger/Clock/Data Channel Configuration out of 23





Selection of:
- **Trigger # (0 … 255)**
- **Bunch Pattern**
- **Clock from FPGA**
- **Front Input**

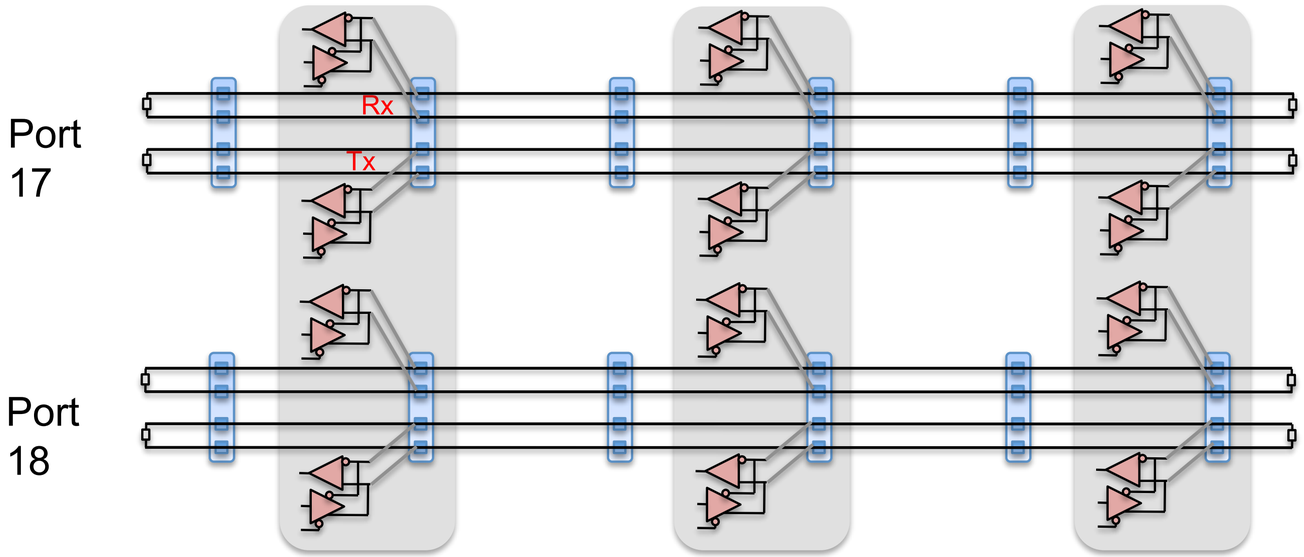
Delay and Width:
- **up to 150ms**
- **in 9.23ns steps**

Combination w/ second channel:
- **Gates (start**
- **Bursts of clocks**
- **Combine with 2nd channel**

Select source:
- **Single delayed & width**
- **Combination w/ 2nd Ch.: AND, OR, FlipFlop**
- **Serial data**

Output can be:
- **Inverted**
- **Inhibited**
- **Fine Delay: .92 ns steps**

Port 17 … 20 Used as Wired-OR for Interlocks



M-LVDS Type-2 receivers (SN65MLVD082) are failsafe by using an offset threshold. In addition, the driver rise and fall times are between 1 and 2.0 ns to provide operation at 250 Mbps while also accommodating stubs on the bus.
Outputs are slew rate controlled to reduce EMI and crosstalk effects associated with large current surges.

M-LVDS Type 2
Can be used for interlocks

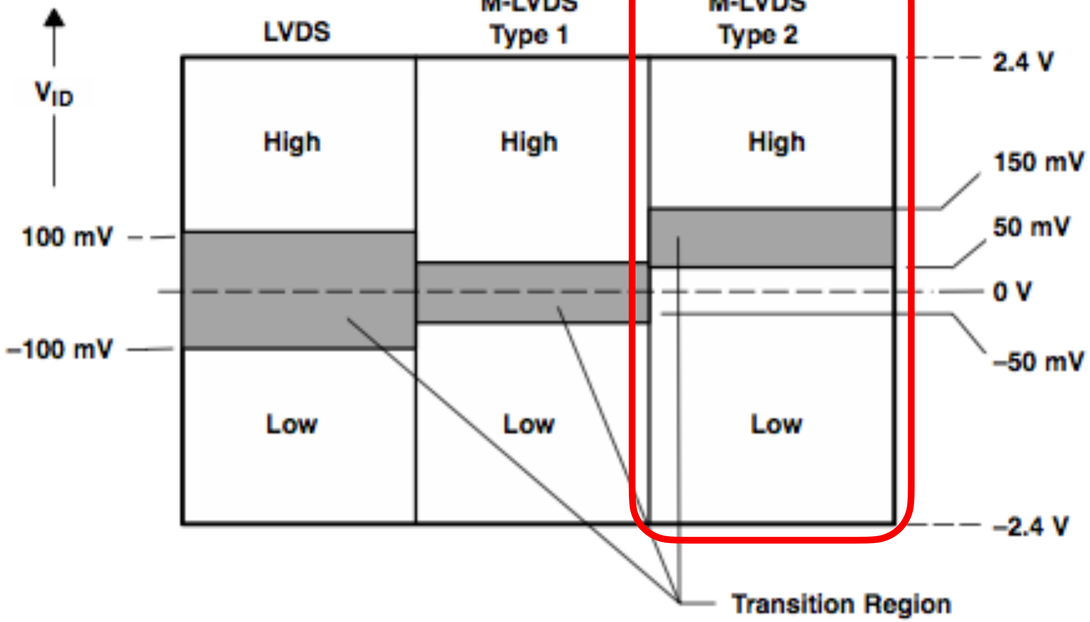
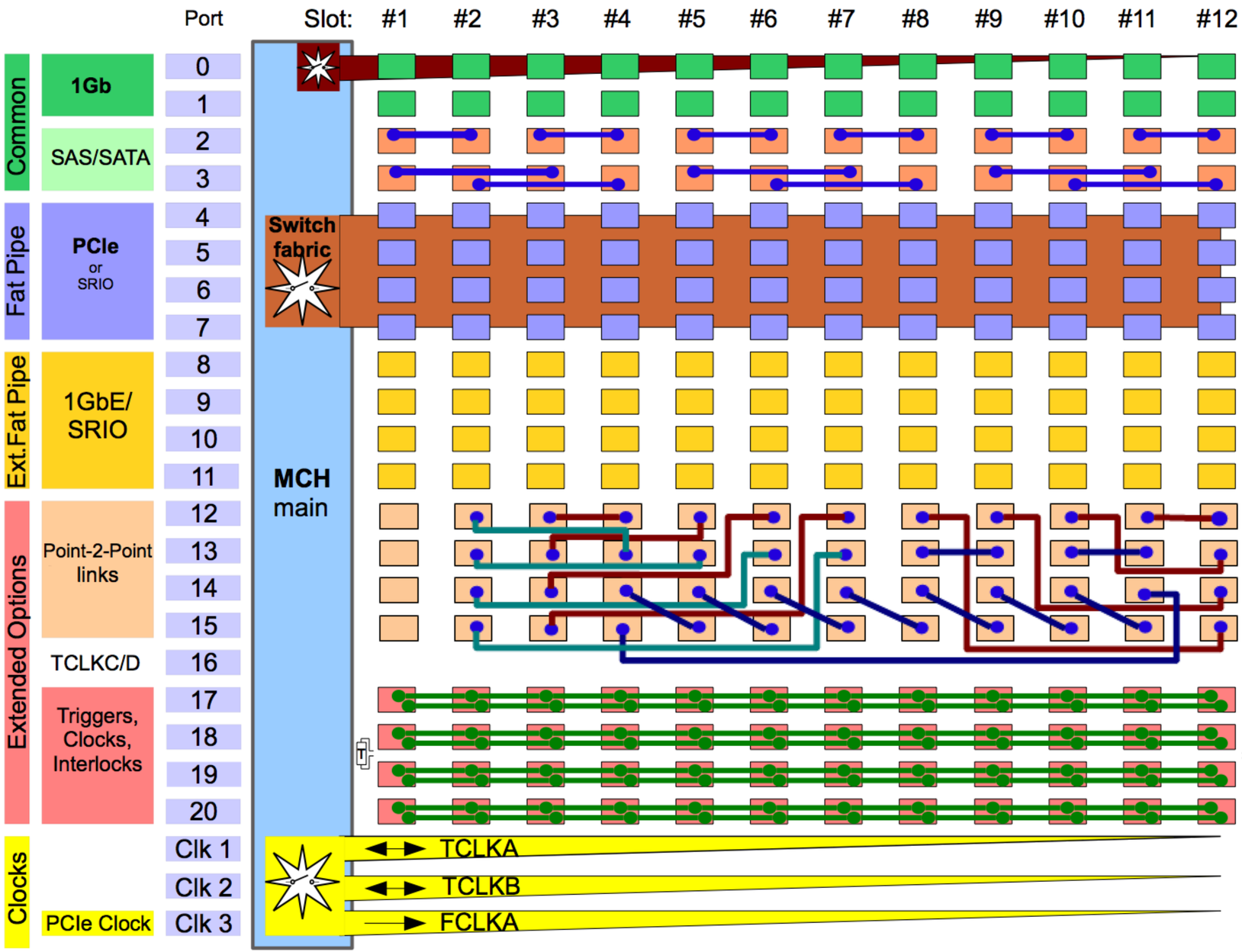
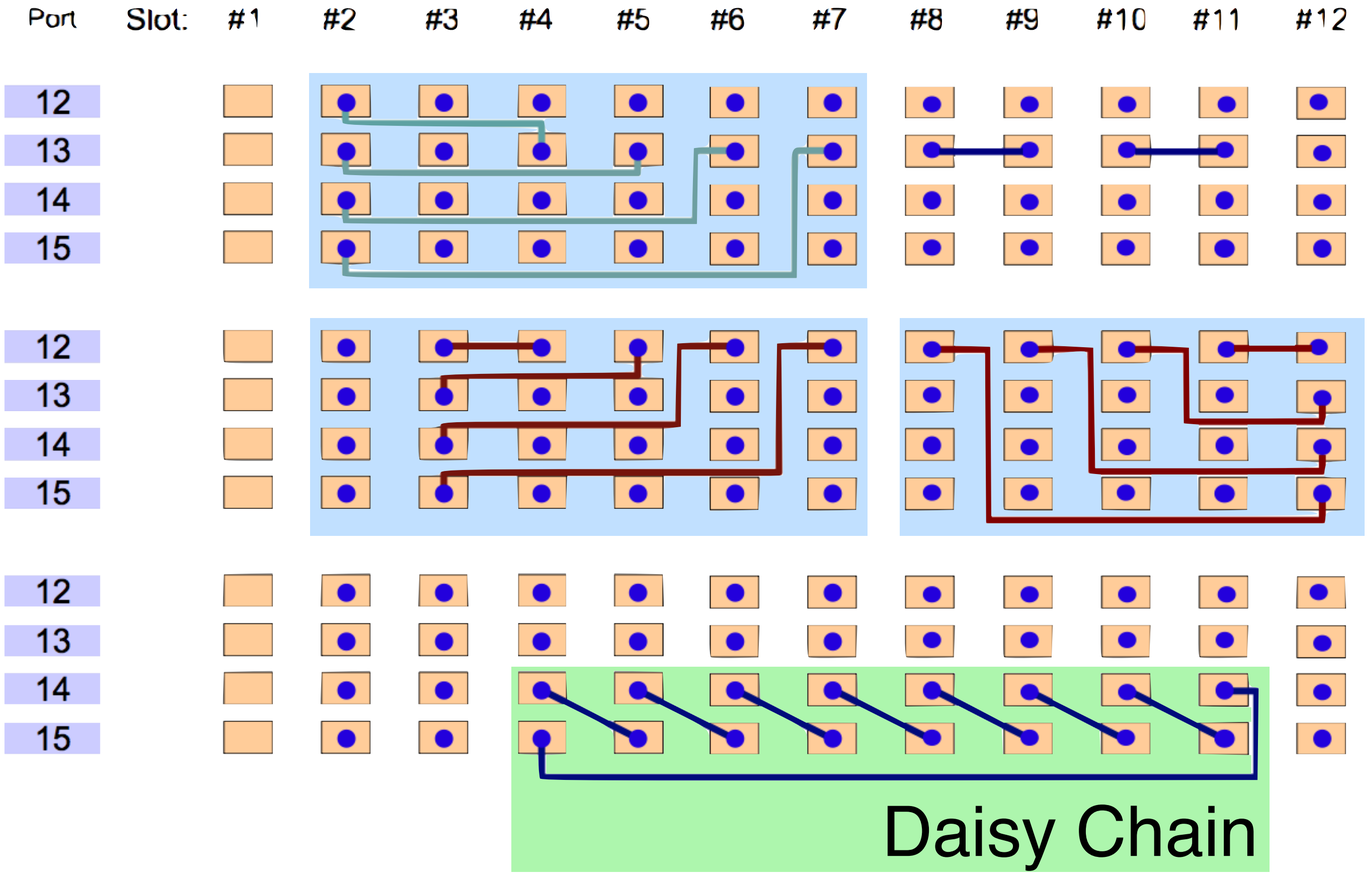


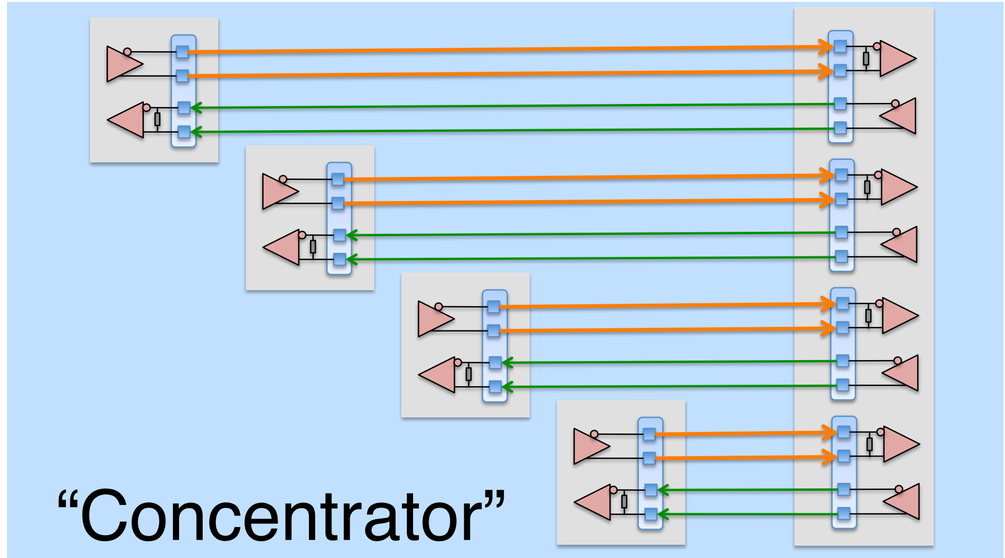
Figure 2–3. LVDS and M-LVDS Differential Input Voltage Thresholds

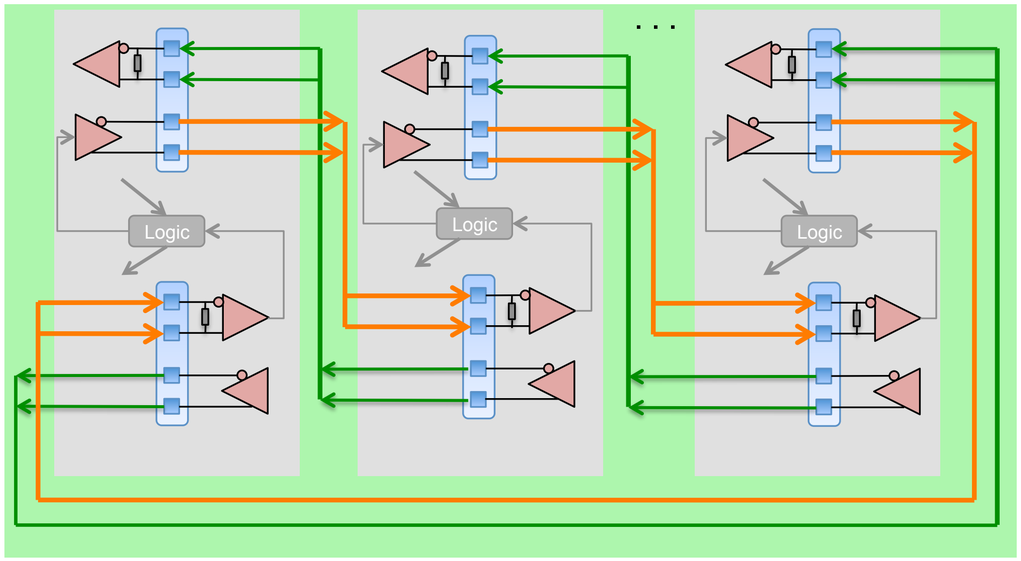
Point-to-Point Bi-directional LVDS Links



3 Overlaid Point-2-Point Topologies

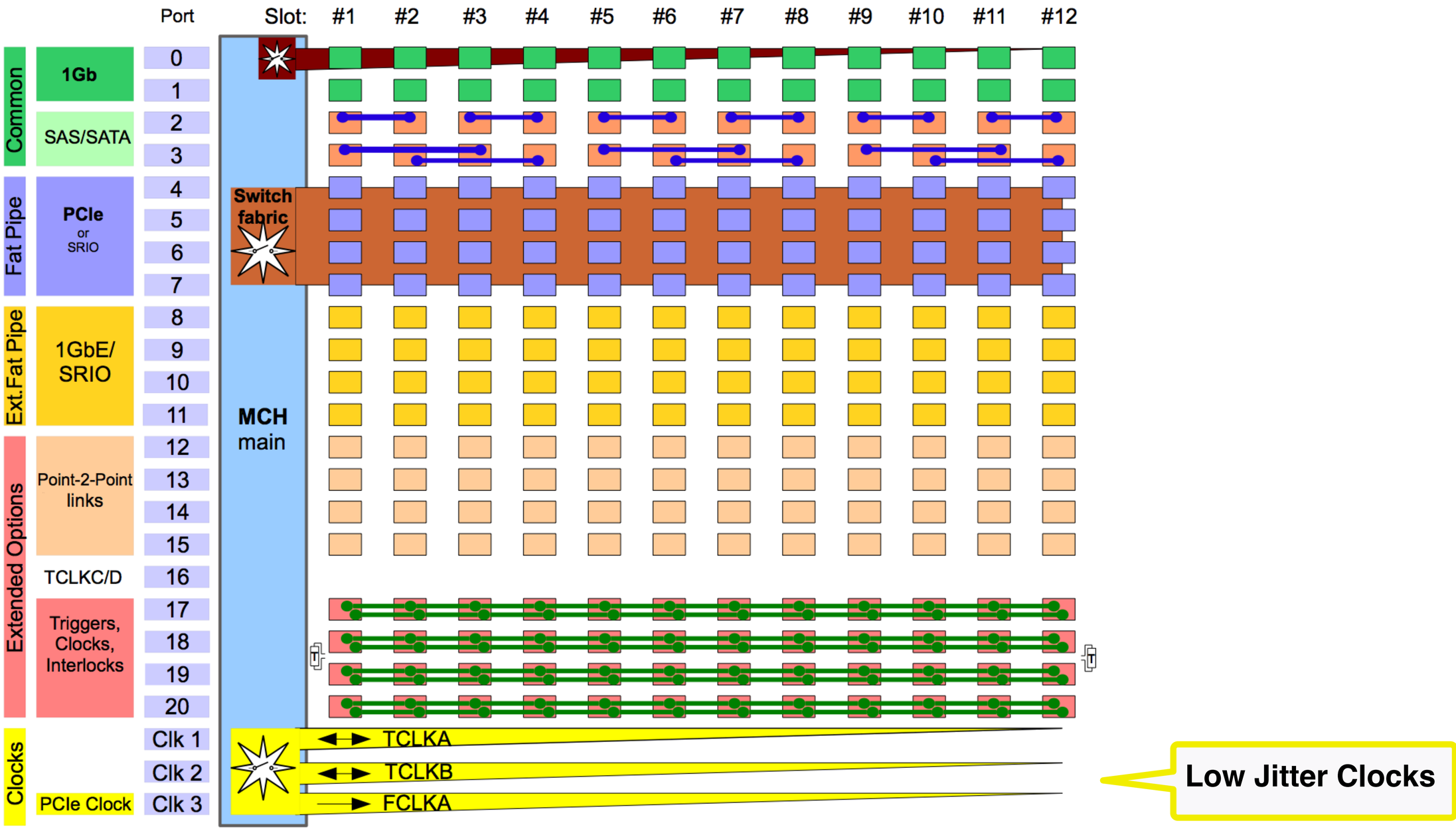




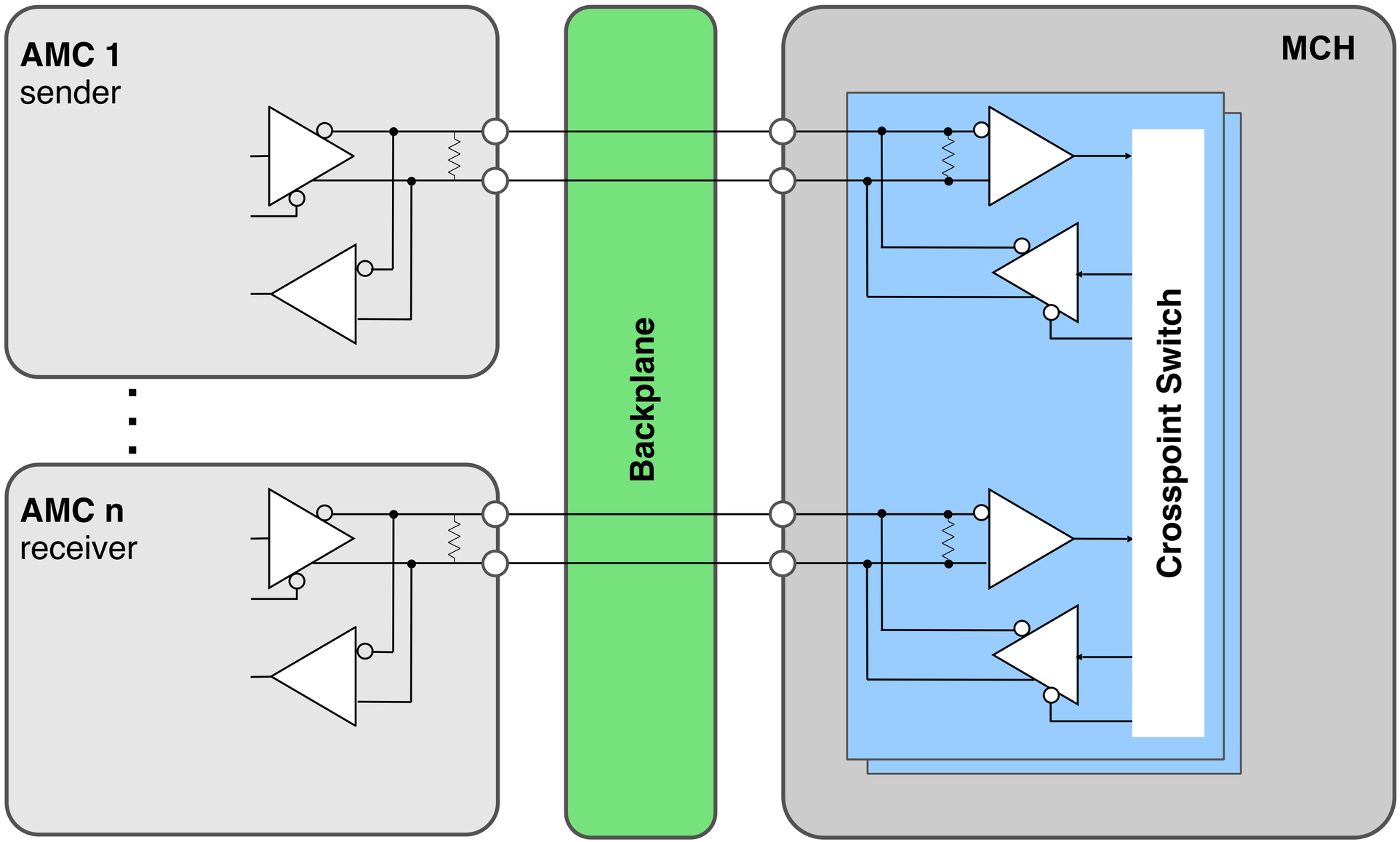


Other topologies are possible by modifying the backplane

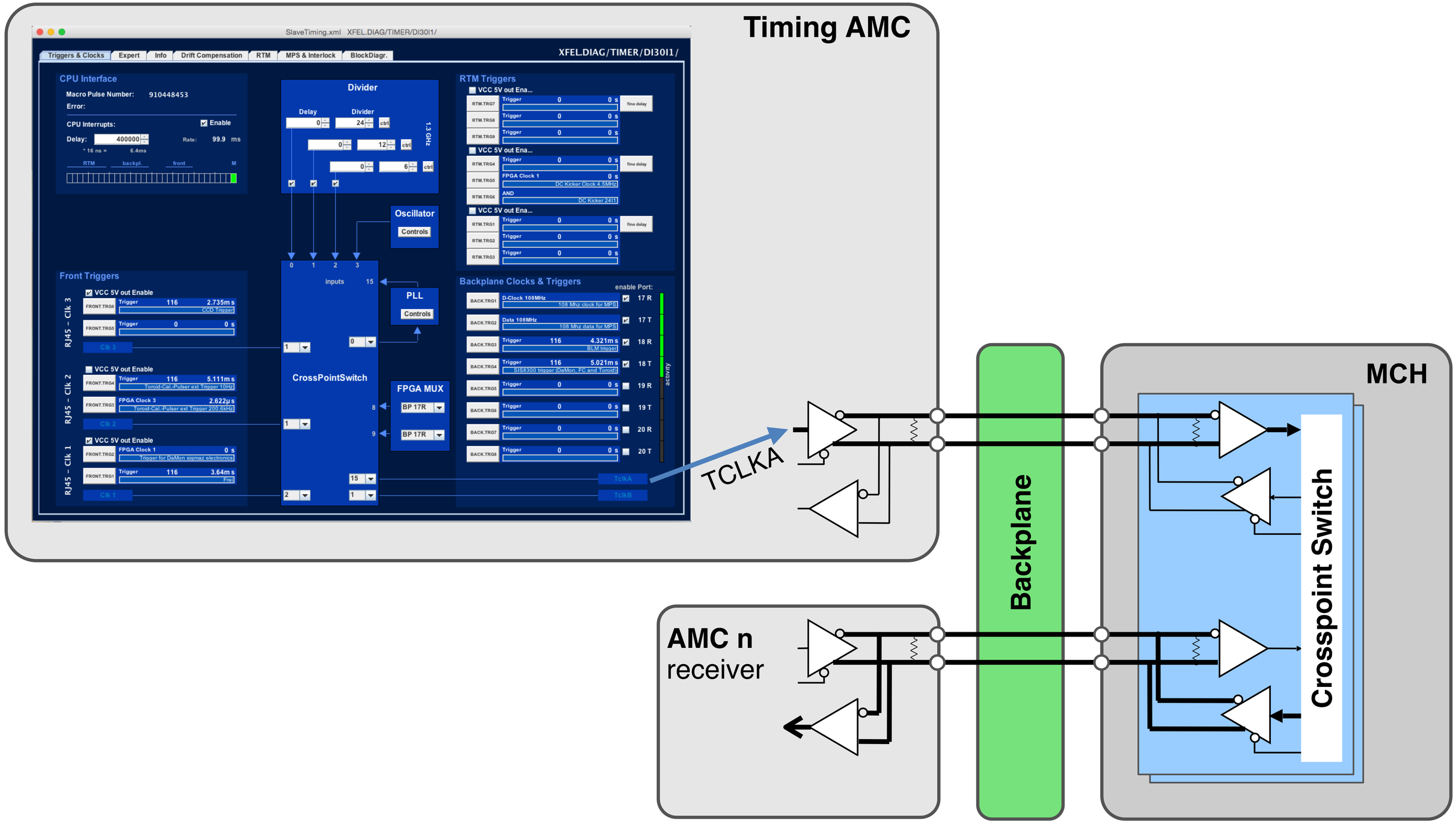
Low Jitter Clocks



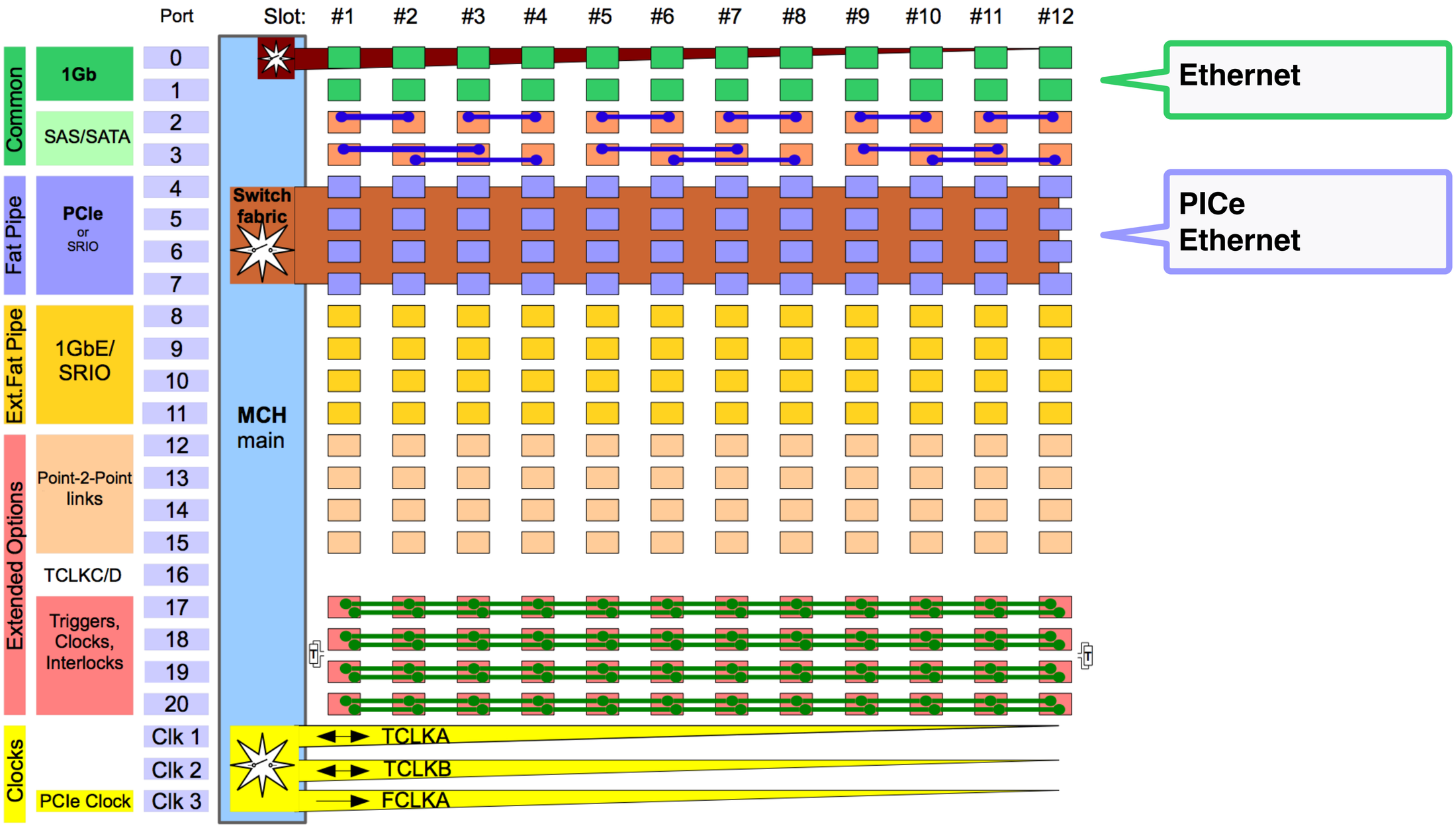
Low Jitter Clock Distribution: Bi-directional LVDS



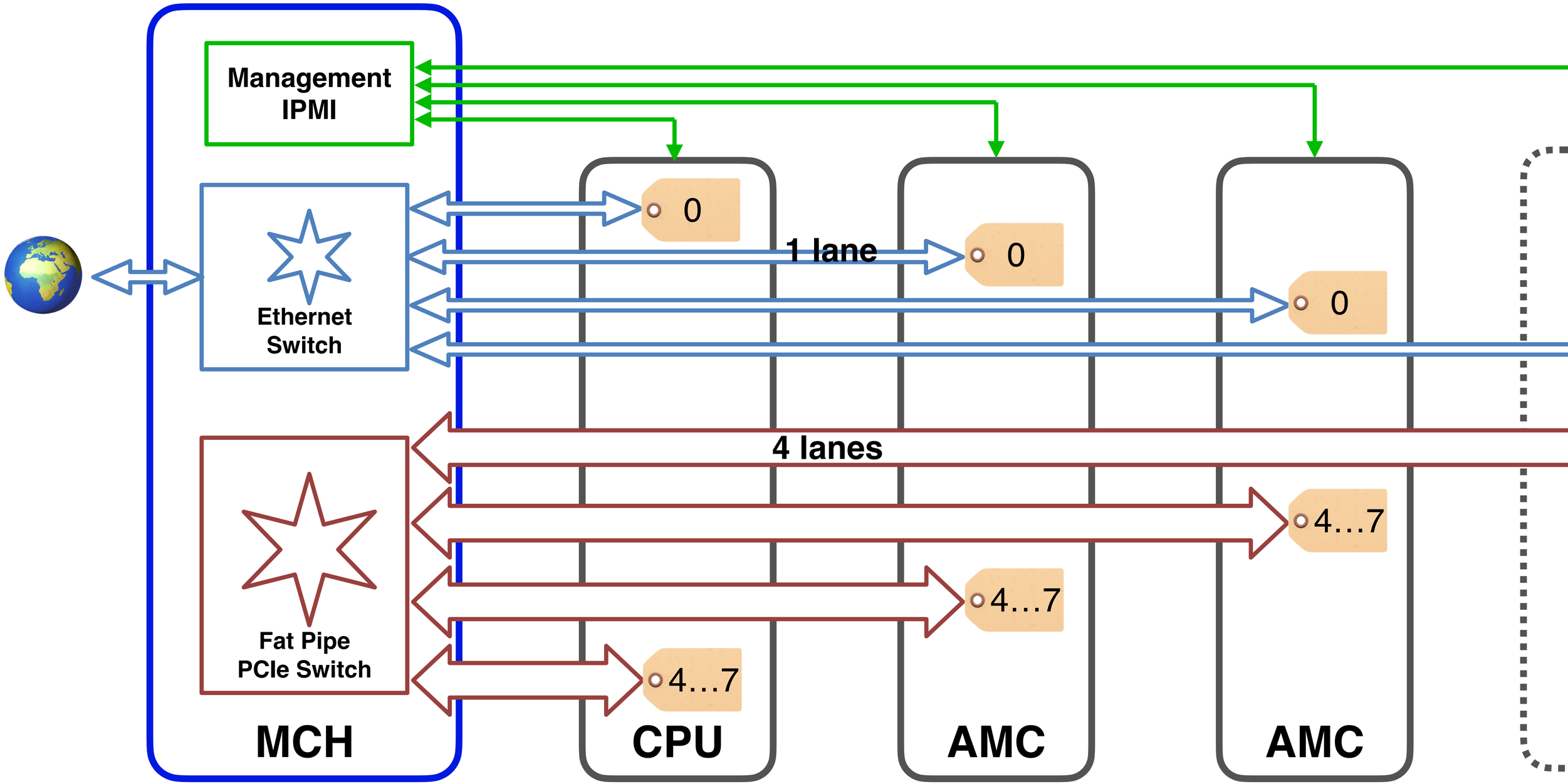
Low Jitter Clock Distribution: Bi-directional LVDS



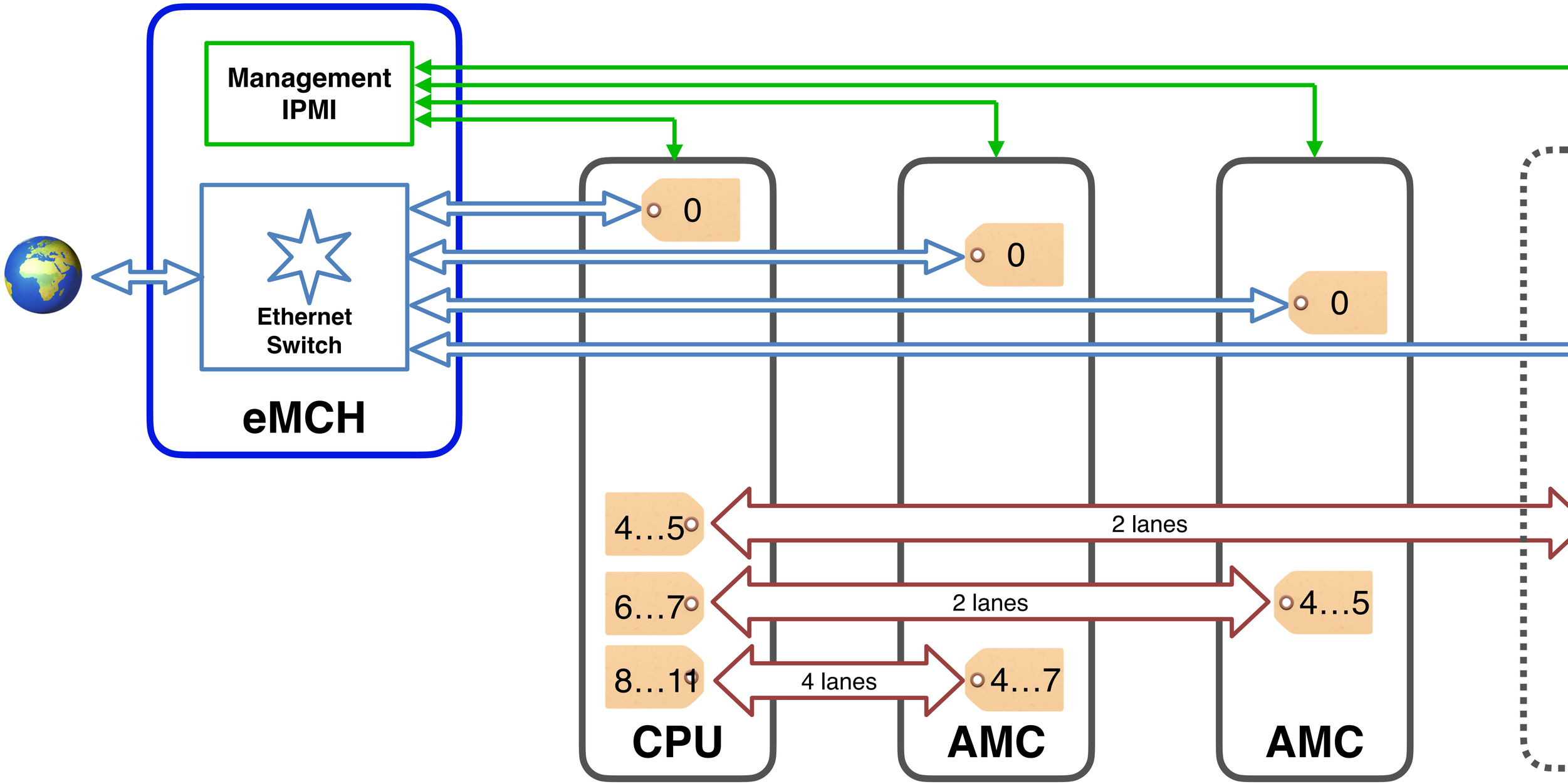
PCIe and Ethernet



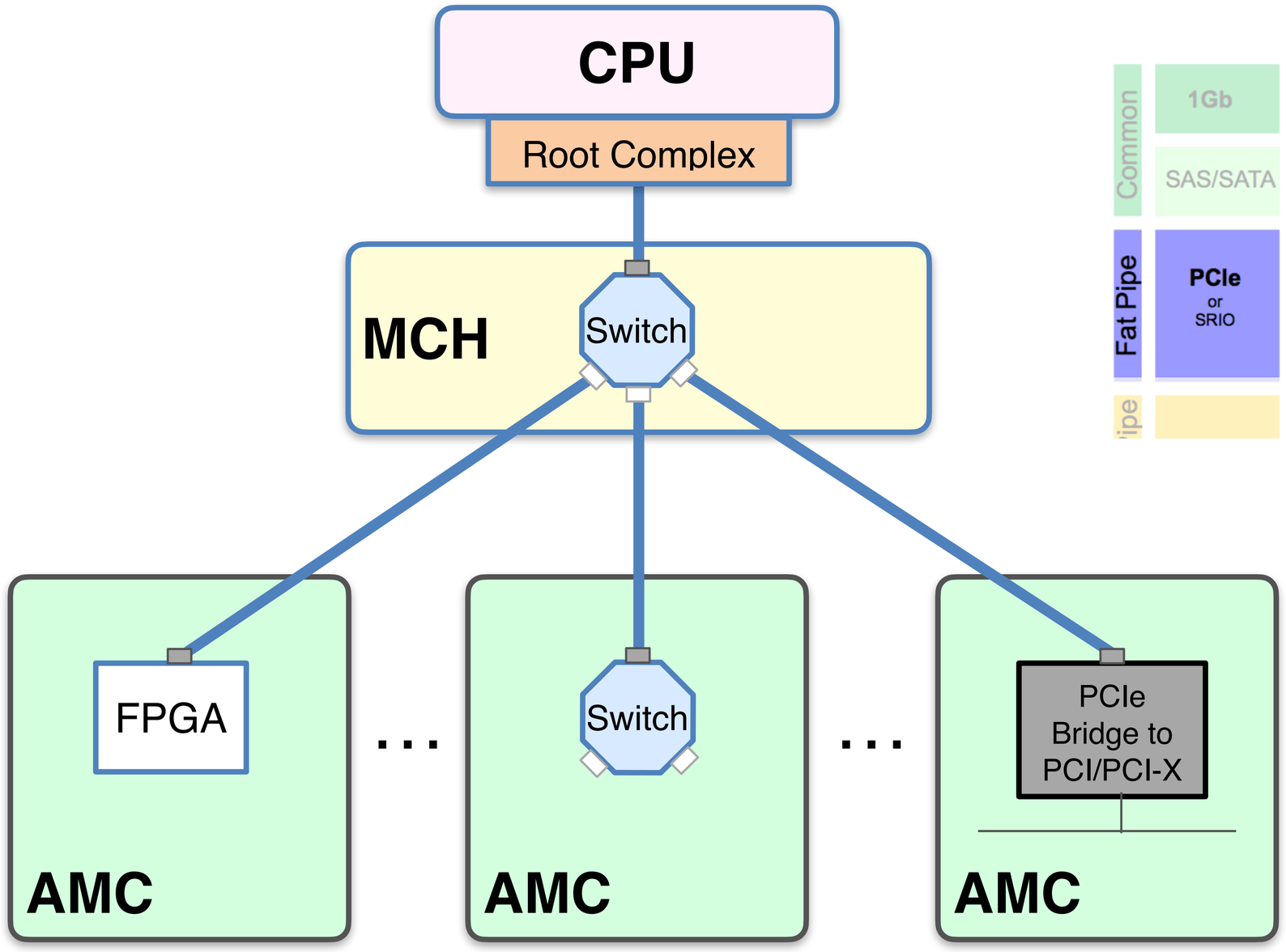
Switched Data Communication: <= 12 Slot System

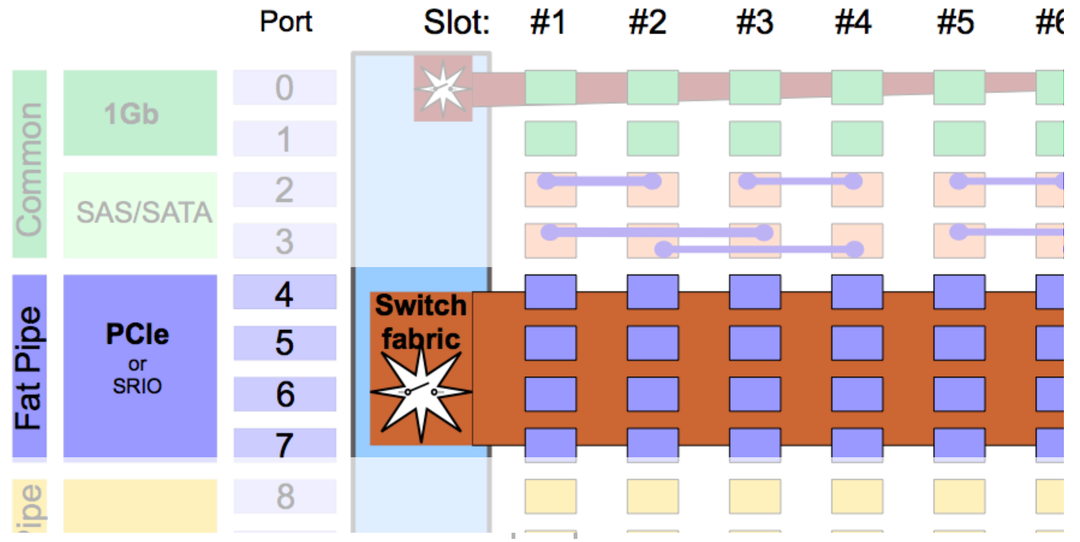


Switched Data Communication: Simple 4 Slot System

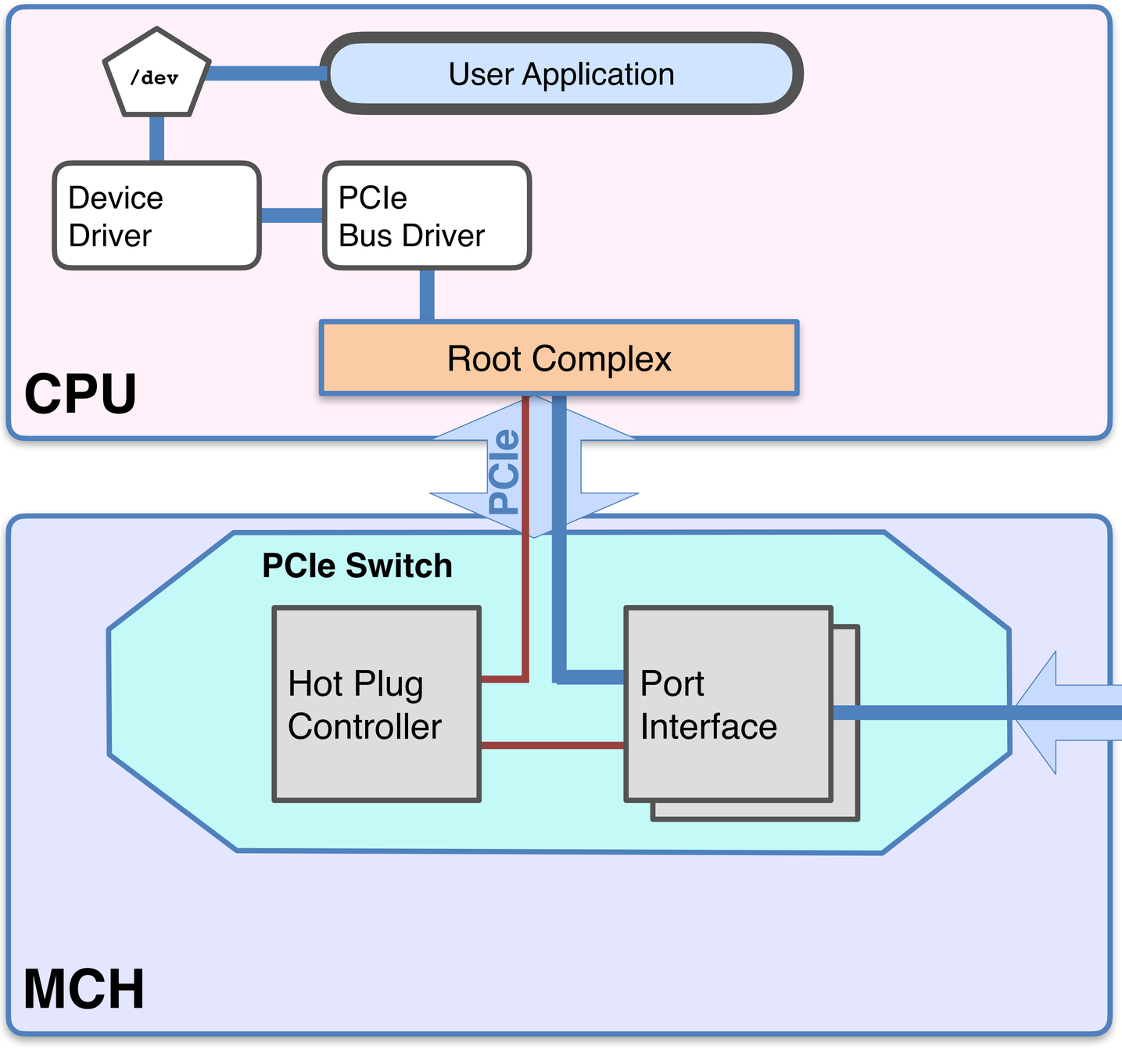


PCIe Topology





Architecture : PCIe with Hot-Swap

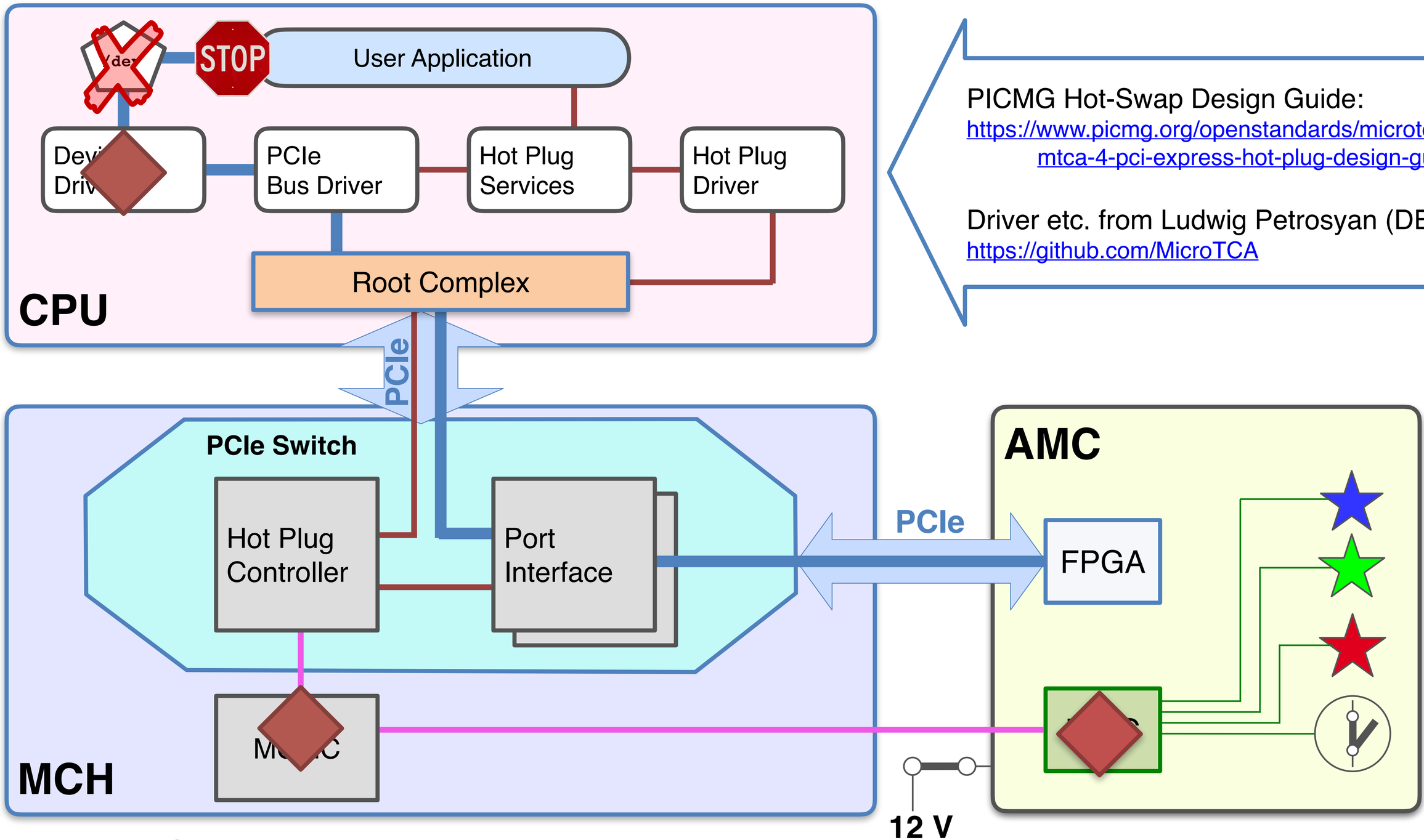


Application is running

next

Pull handle
or stop via management

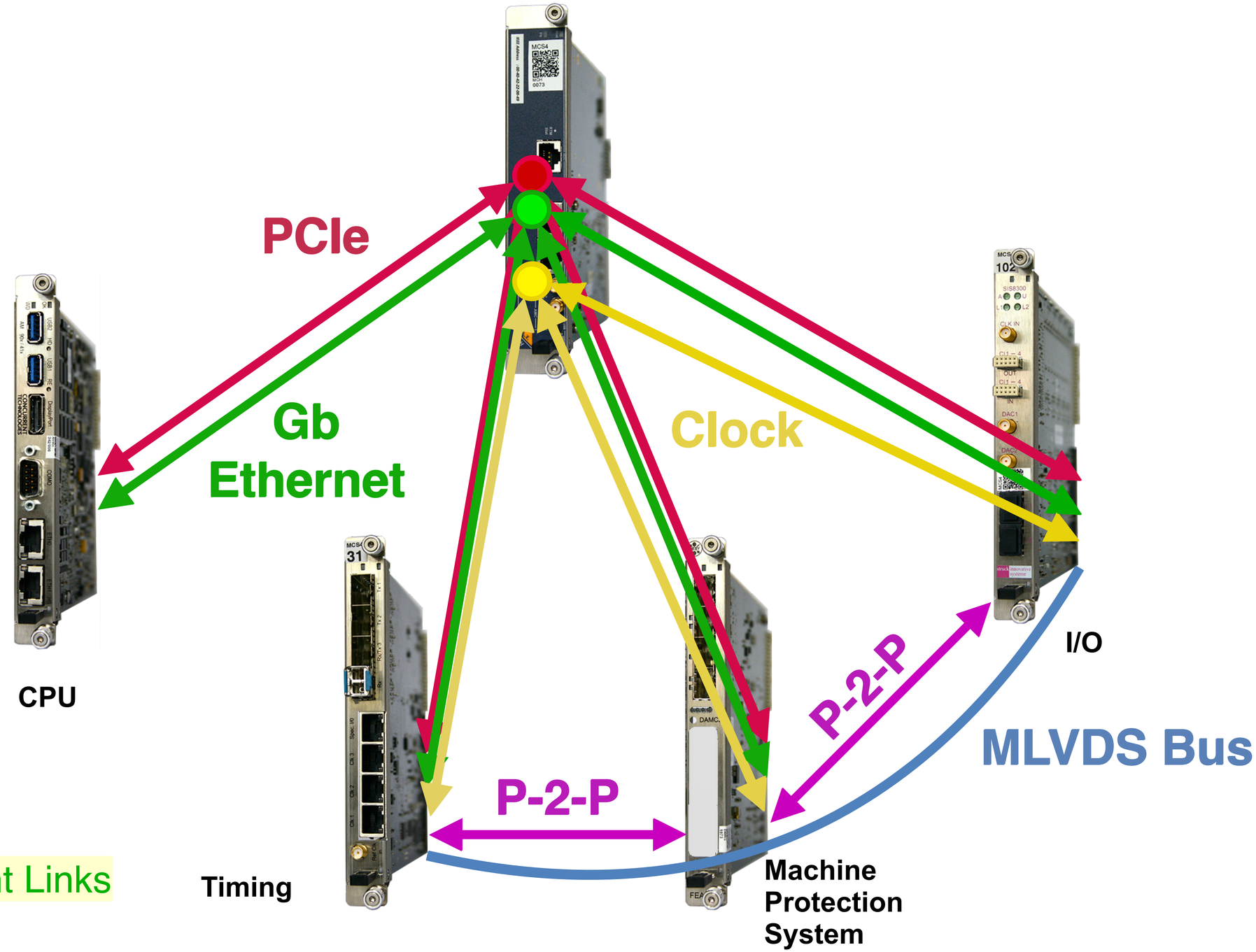
Architecture : PCIe with Hot-Swap



PICMG Hot-Swap Design Guide:
https://www.picmg.org/openstandards/microtca/mtca-4-pci-express-hot-plug-design-guide/

Driver etc. from Ludwig Petrosyan (DESY):
https://github.com/MicroTCA

MicroTCA.4 Communication Links



+ IPMI Management Links