MTCA WORKSHOP 2022 - TUTORIAL

Application Concepts and Troubleshooting in MicroTCA

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Hamburg, 6th December, 2022

MicroTCA TECHNOLOGY LAB

DESY.

MicroTCA Workshop 2022 - Tutorial

Application Concepts and Troubleshooting in MicroTCA

Introduction

MicroTCA Application Concepts

- System Configuration Options
- Example 1: European XFEL
- Example 2: LISA EGSE
- Trends and Concept Changes

MicroTCA Troubleshooting

- Potential Sources of Failure
- Error chain and systematic debugging

Recommendations

Introduction

MicroTCA Technology Lab at DESY

Introduction

About the Lab

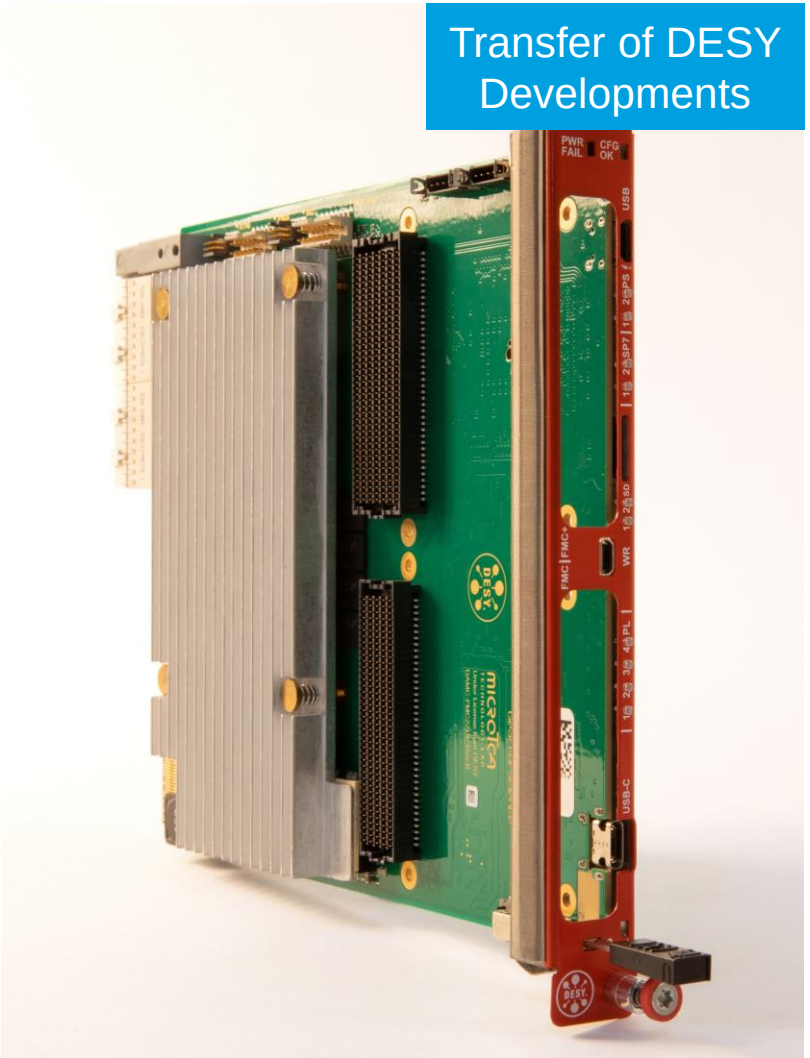
> Founded in 2016 as Helmholtz Innovation Lab
> More than 10 years of experience in Tech-Transfer
> Strong expertise in MicroTCA system architecture
> Close relationship to DESY MicroTCA users
> Close partnership with industry

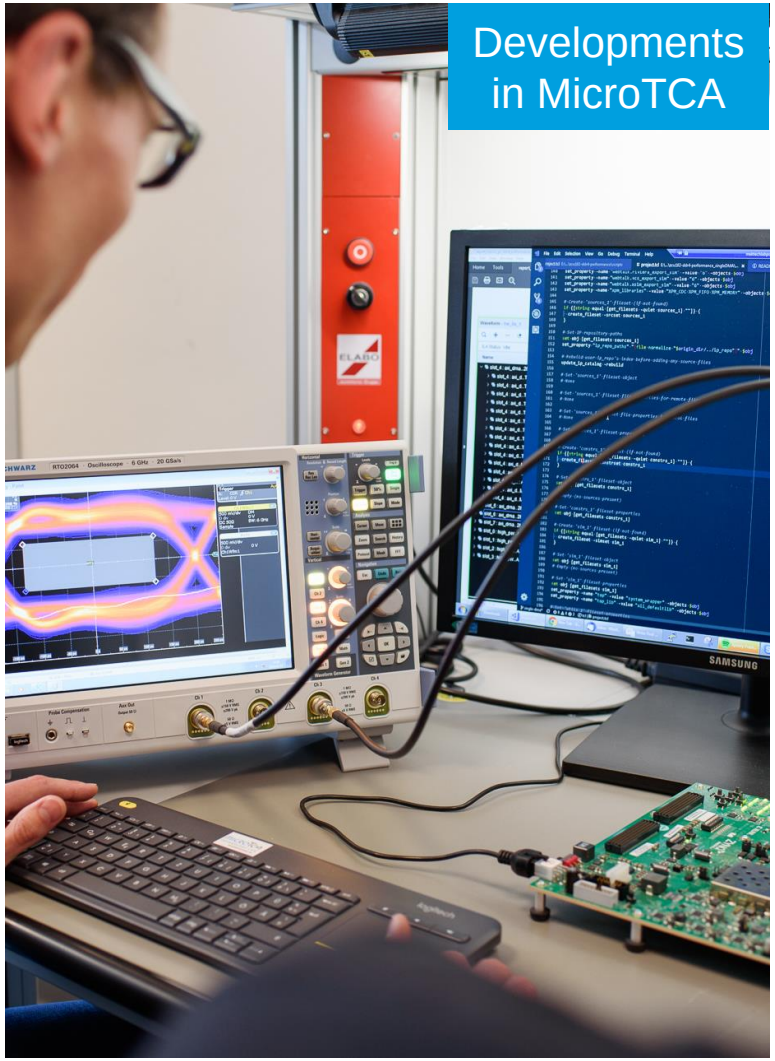
Organization as of today

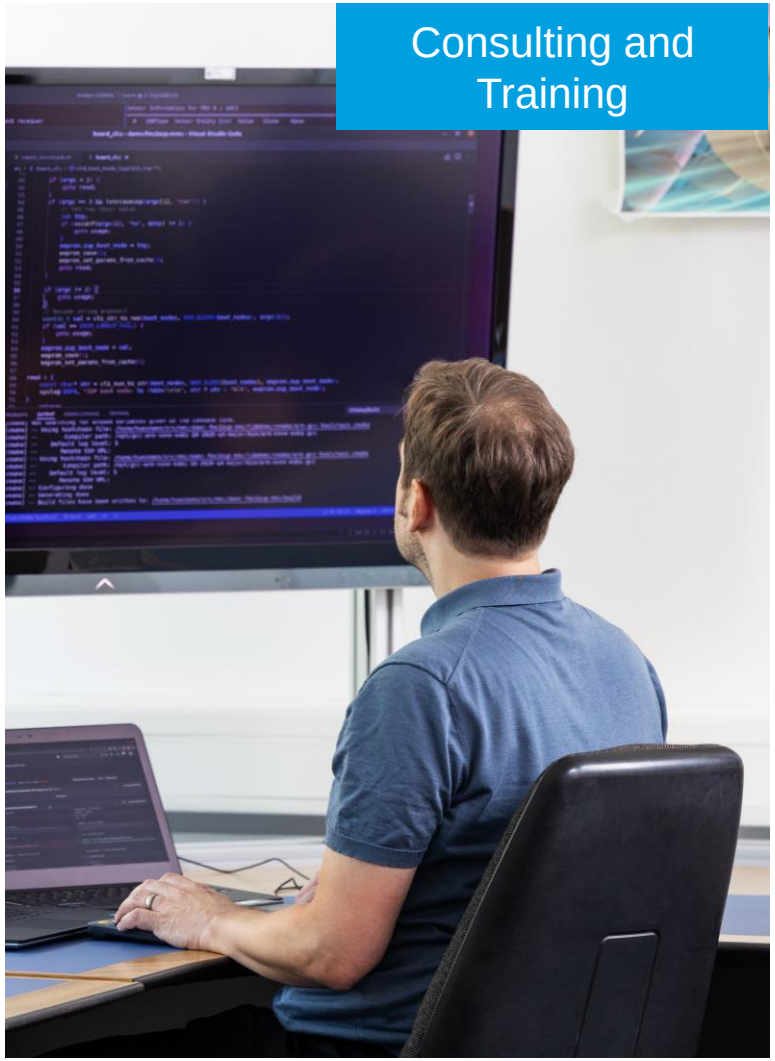
> Sub division of Innovation and Technology Transfer
  - Synergies in terms of administration
  - Focus on development and consulting

MicroTCA Technology Lab at DESY

Products and Services







MicroTCA Application Concepts

MicroTCA Configuration Options

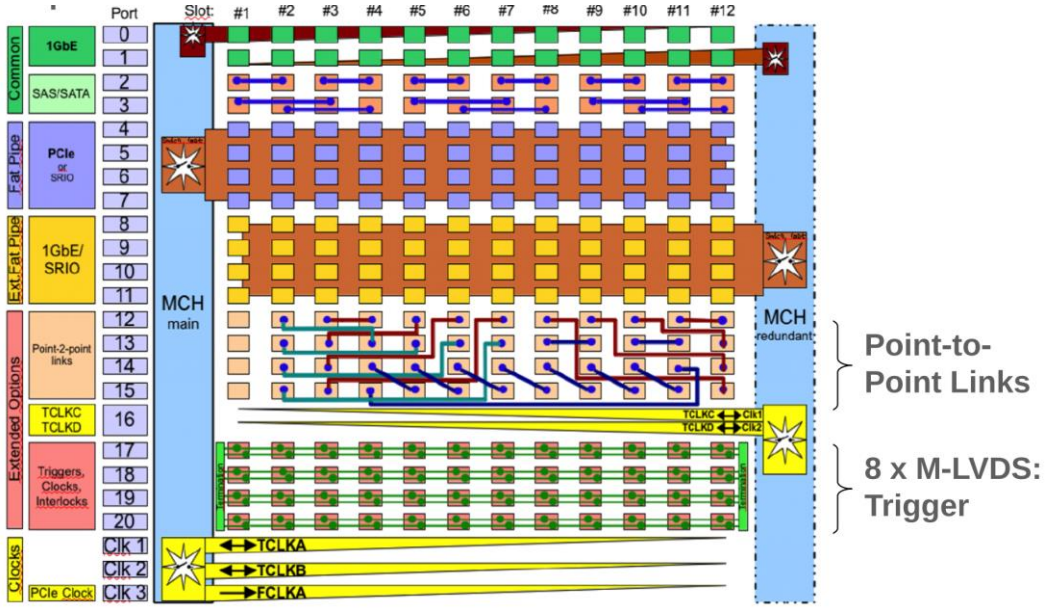
Formfactors and Chassis

- Several formfactors with different characteristics
- Trade off between:
  - Capacity / size
  - Cooling / Airflow
  - Performance
  - Cost
  - Redundancy
  - Functionality (e.g. JSM)
  - Backplane topology

MicroTCA Configuration Options

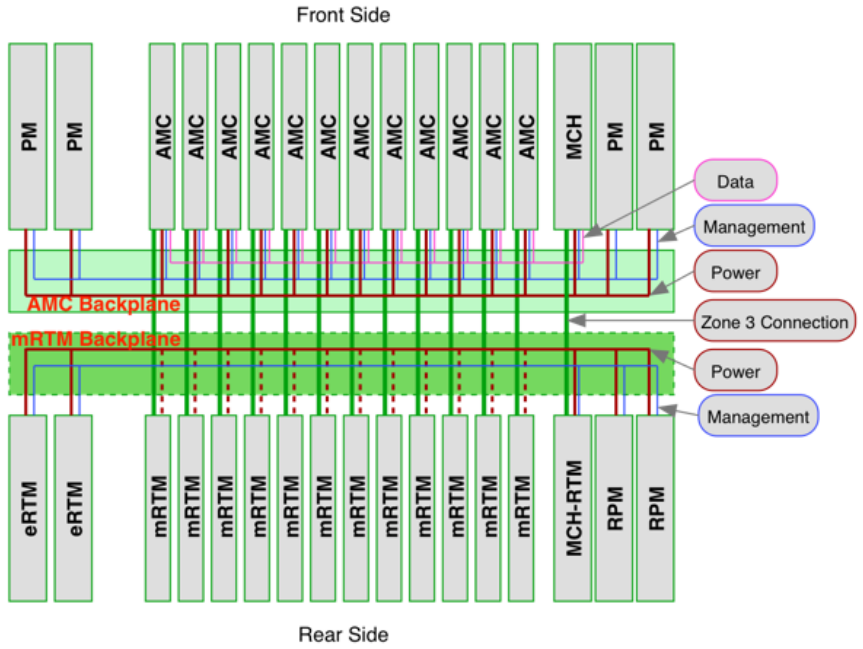
Frontside View

- AMC backplane protocols
  - IPMI
  - Gigabit Ethernet
  - SATA
  - Fat Pipe (PCIe, SRIO, 10/40 Gb Ethernet)
  - Point-to-point links (Multi-Gigabit Transceiver)
  - MLVDS lanes
  - Clocks
  - JTAG
- RTM backplane for extended functionality in MicroTCA.4.1



MicroTCA Configuration Options

Backside View and RTM Backplane



MicroTCA Configuration Options

MCH and Power Supply

MicroTCA Carrier Hub (MCH):

> Switching characteristic
  - Fat Pipes
  - Ethernet
  - Clocks
> RTM backplane management needed
> User interfacing
> Formfactor

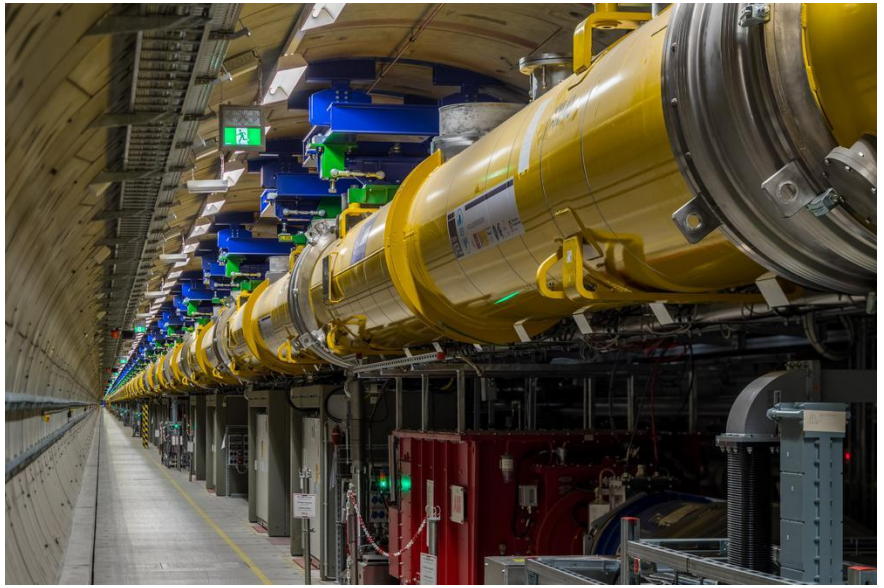
Power Supply

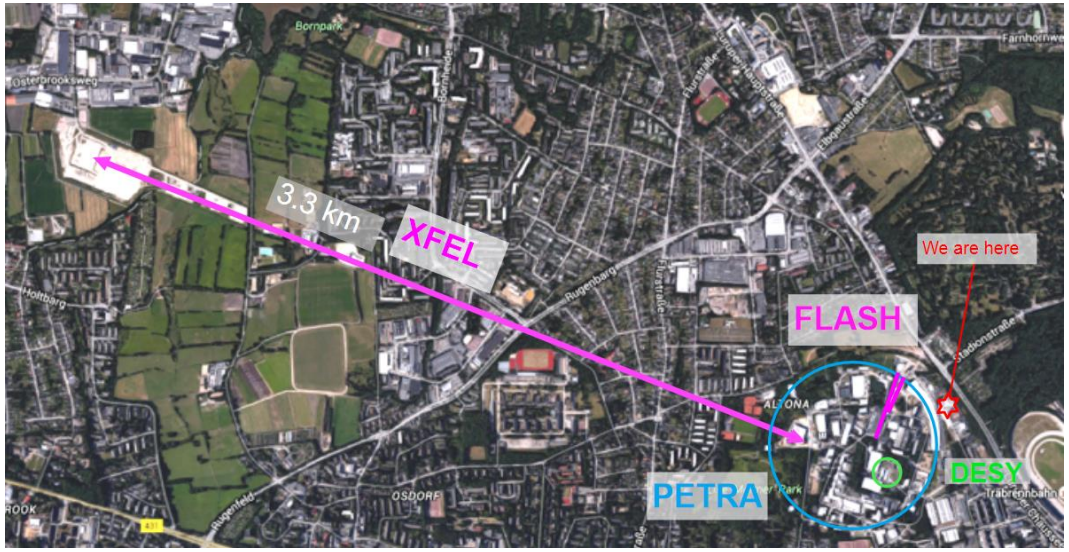
> 1000W/600W
> Formfactor

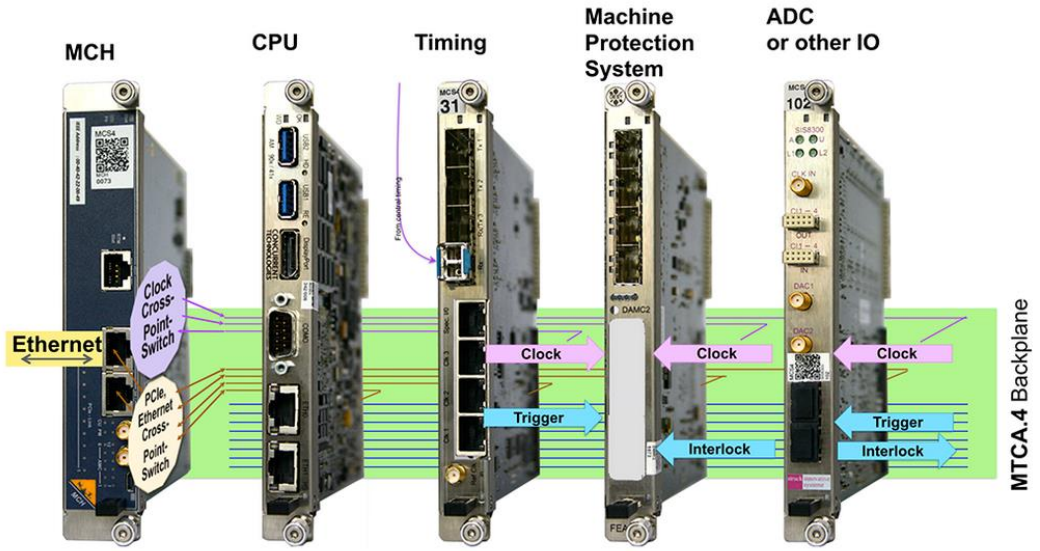
Example 1: European XFEL

Large Scale Installation

- More than 200 MicroTCA crates in different subsystems: LLRF, Interlocks, Diagnostics, Special Diagnostics, Vacuum, Magnets, Experiments
- Synchronization of all subsystems
- Remote Management



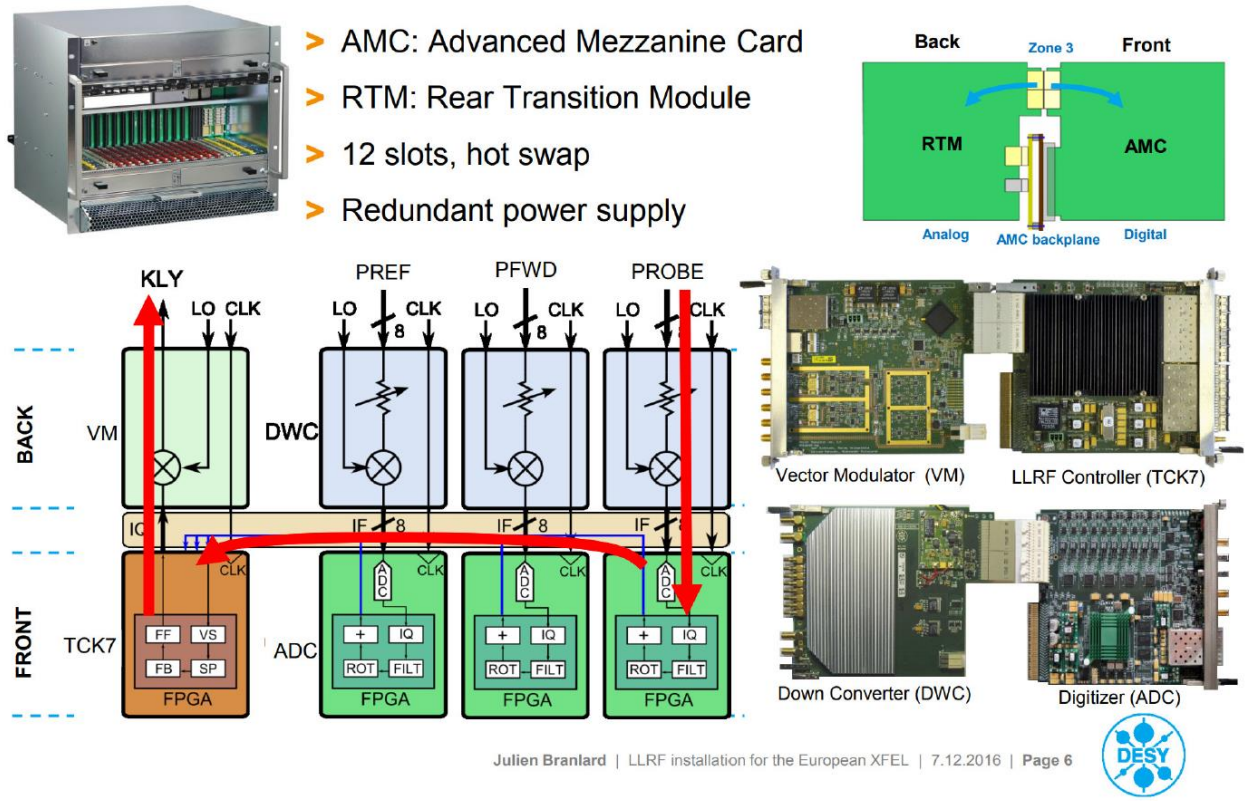


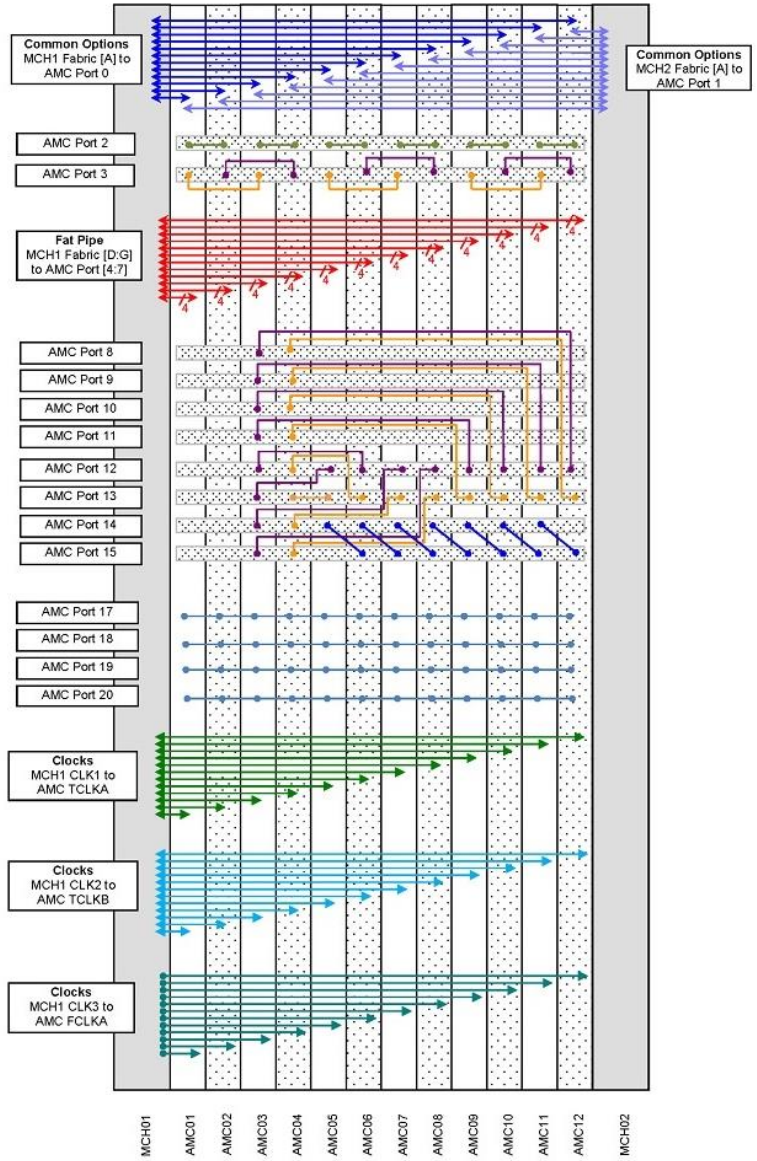


Example 1: European XFEL

LLRF Control System

- Data Aggregation Backplane
- Point-to-Point links





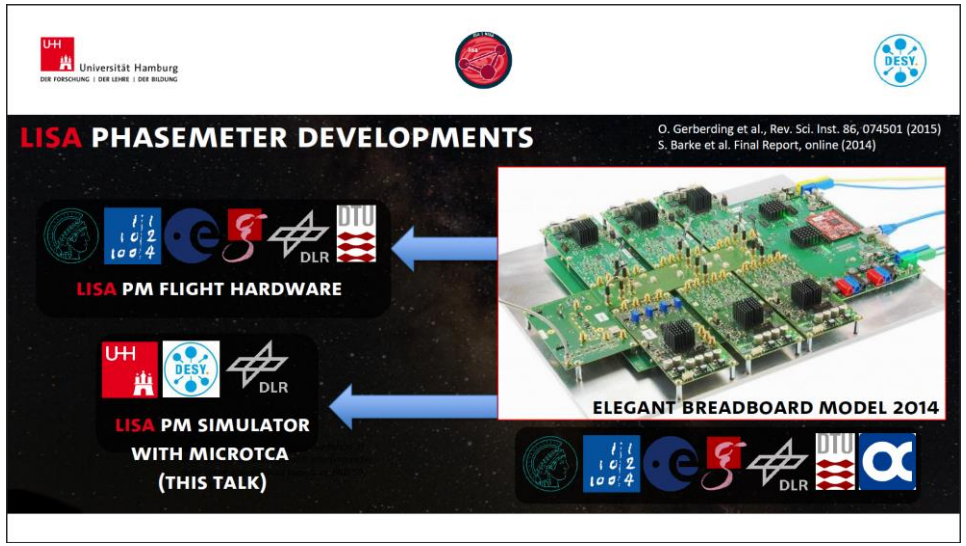
Data aggregation backplane topology

Example 2: LISA

MicroTCA based EGSE

see talk by Christian Darsow-Fromm on Wednesday, 10:00 am

- Electronic Ground Support Equipment for the LISA gravitational wave detector
- 48 ADC channels, 2 DAC channels
- Clock and tone generation and distribution



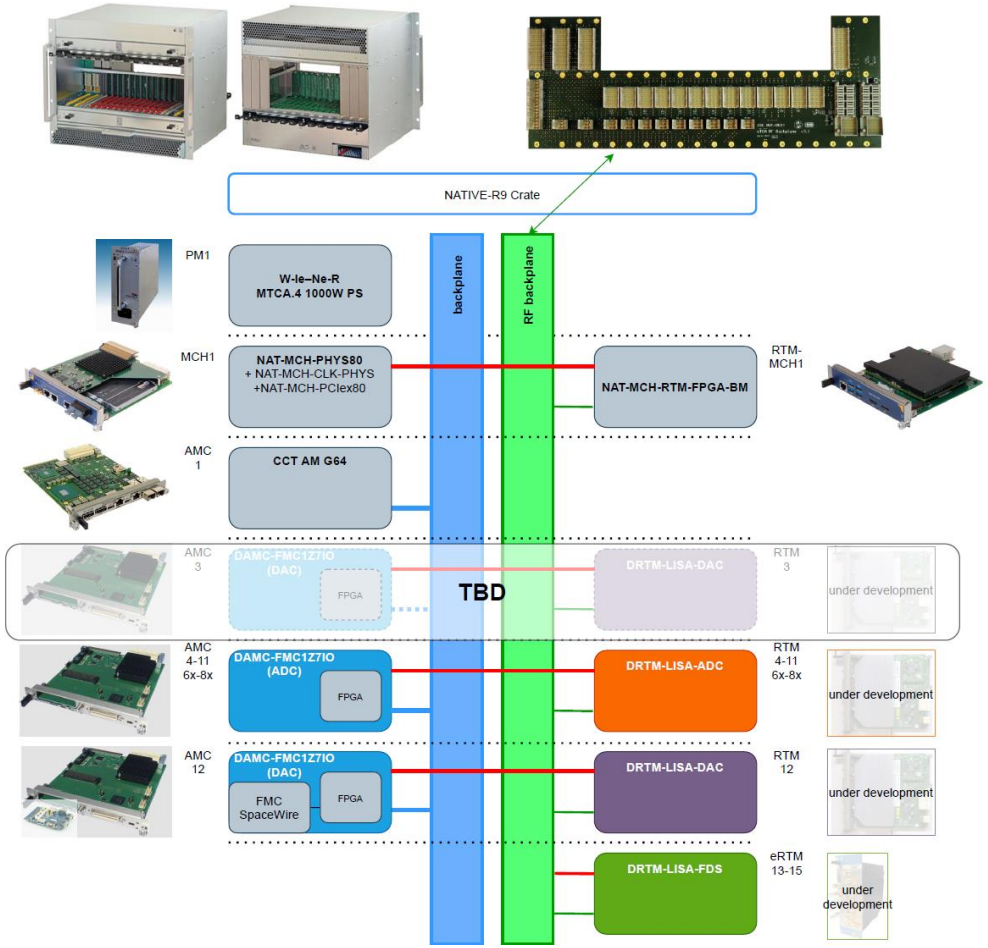


Figure: O. Gerberding et al., LISA Symposium 2022, LISA Phasemeter based on MicroTCA as ground support equipment: Development status

Example 2: LISA EGSE

Timing and Trigger Signals

- RTM backplane (MicroTCA.4.1)
- eRTM for clock and tone generation, distribution via RTM backplane
- Trigger from application software, distribution via backplane
- Digital Zone3 signals, class D1.0

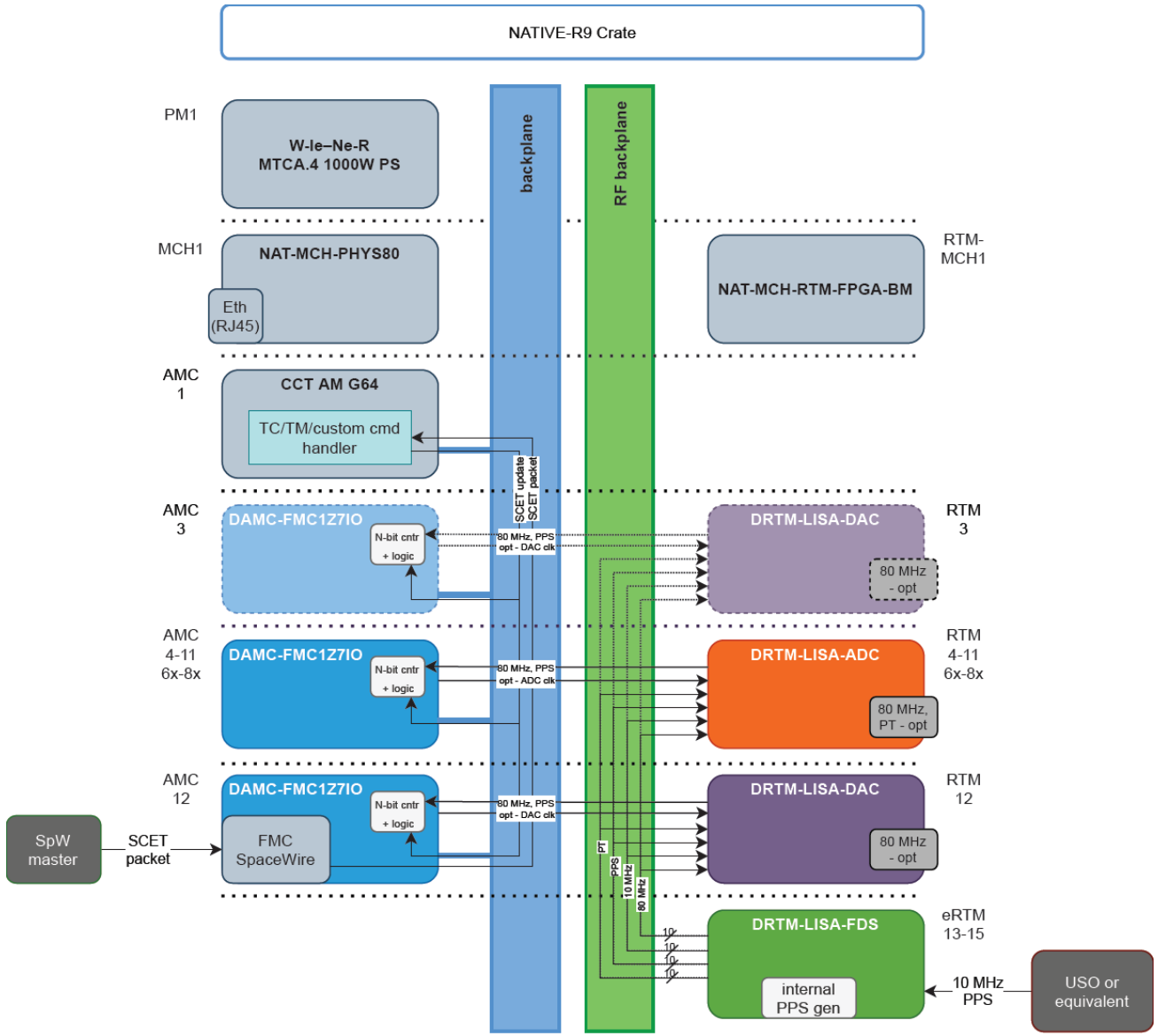
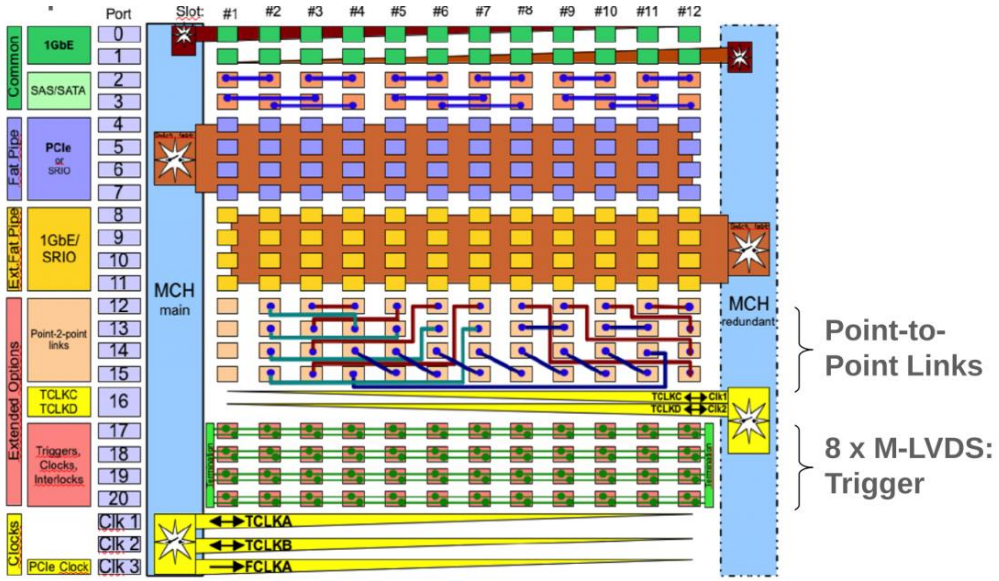


Figure: O. Gerberding et al., LISA Symposium 2022, LISA Phasemeter based on MicroTCA as ground support equipment: Development status

Example 2: LISA EGSE

Data Flow

- Application software data access via PCIe
- Point-to-point links for processed data transfer from ADC to DAC:
  - AMC 4-7 to AMC 3
  - AMC 8-11 to AMC 12
  - Aurora link, up to 7.68 Gbps



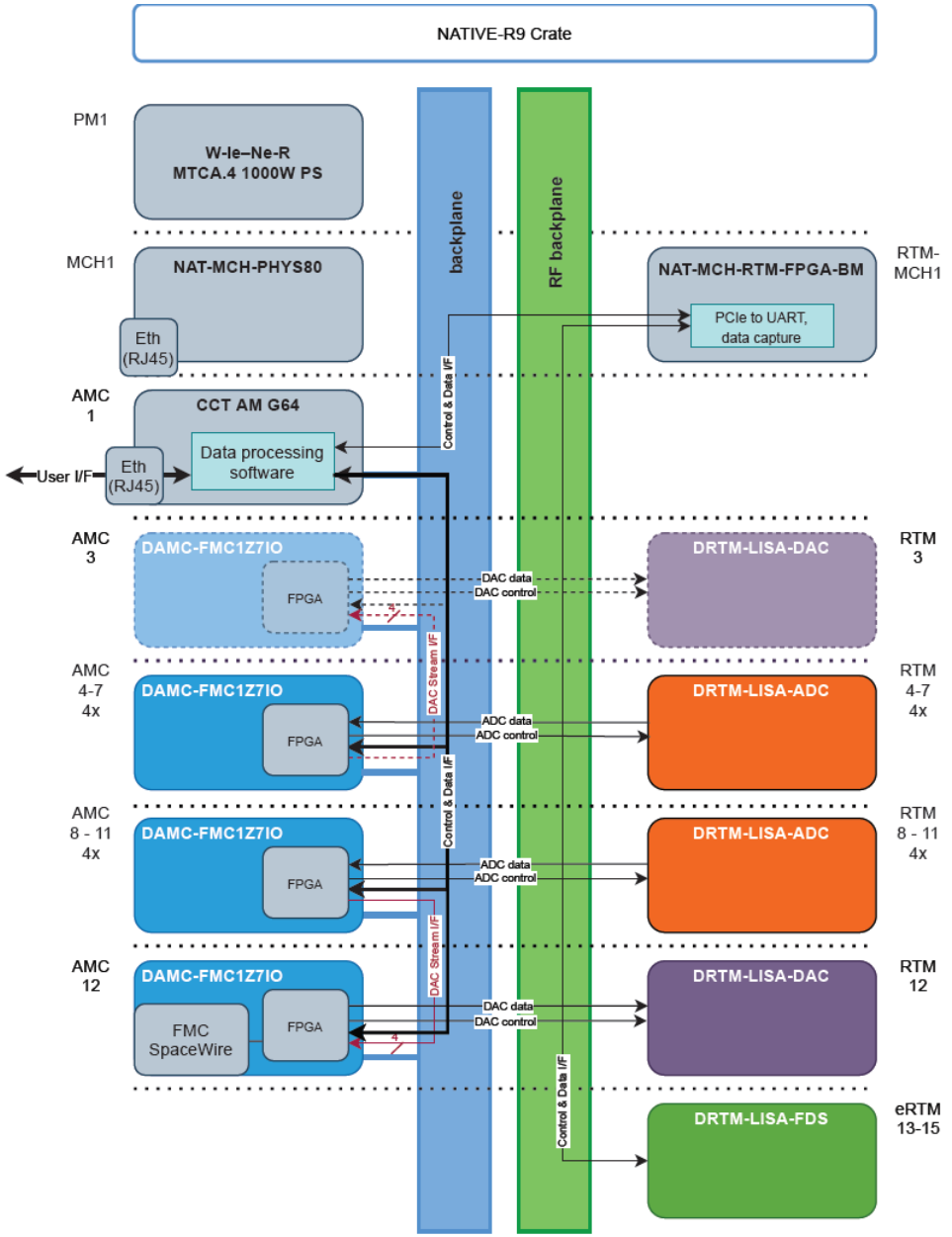


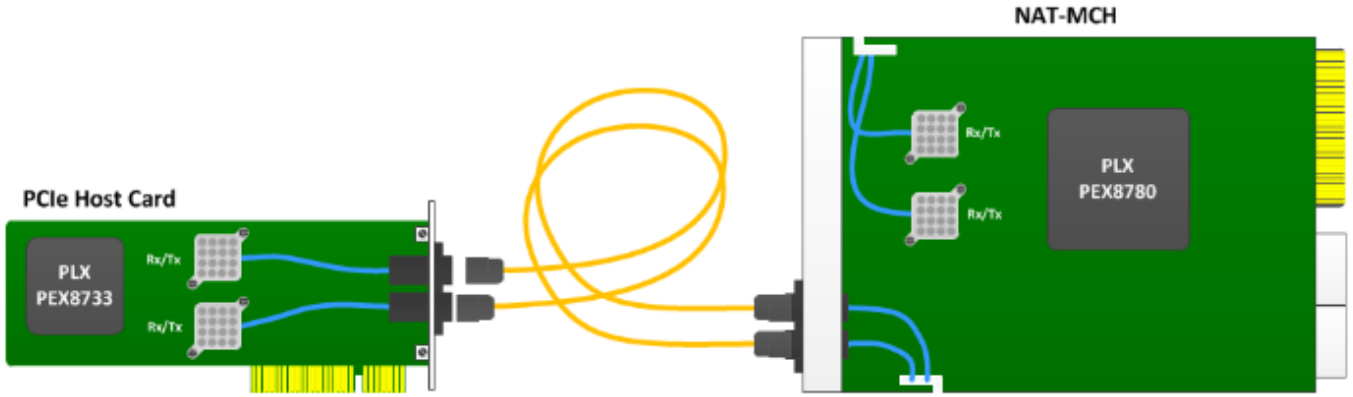
Figure: O. Gerberding et al., LISA Symposium 2022, LISA Phasemeter based on MicroTCA as ground support equipment: Development status

Trends and Concept Changes

External Computing Power via PCIe up-link

> PCIe connection between a “normal” PC and a MicroTCA crate
  - Optical, long cables possible
  - Up to Gen.3 x16
  - Saves one AMC slot
  - More computing power

MCH with optical uplink



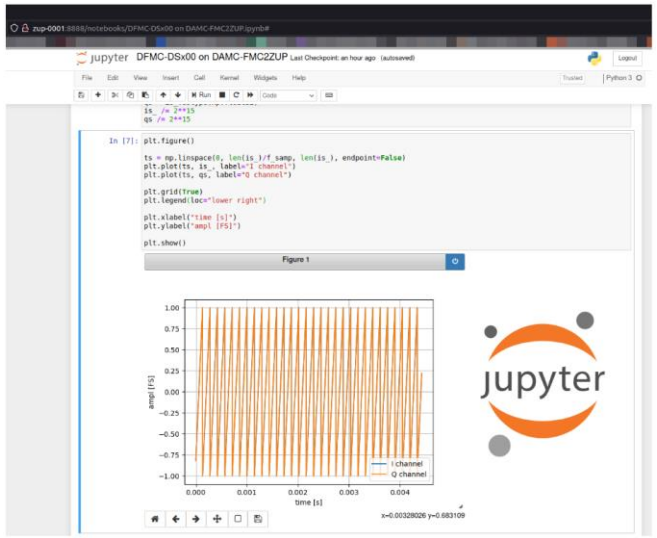
from P. Nonn et al: MicroTCA based LLRF Control Systems for TARLA and NICA

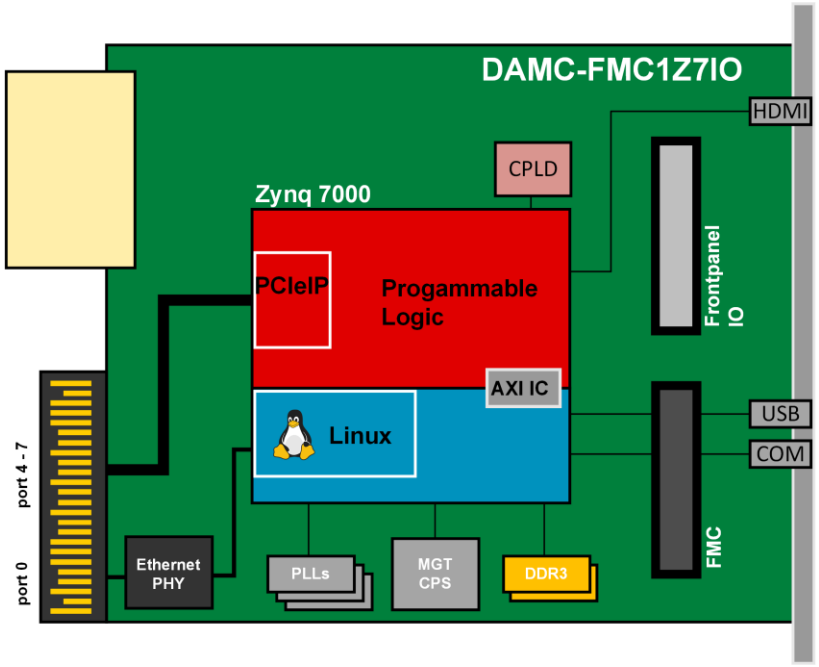
Trends and Concept Changes

SoCs instead of FPGAs

- Programmable logic (FPGA) and Processing System (CPU) integrated on a single AMC
- Embedded Linux makes the board acting like a „normal“ computer capable to run application software
- „Island Solutions“ possible


```
sven@sven-VirtualBox ~ ssh root@192.168.1.86
Last login: Fri Dec  2 17:39:57 2022 from 192.168.1.91
root@damc-fmc1z7io ~ axi_dma_demo_cpp --mode uio --debug
[2022-12-02 17:40:23.013642] [0xb6f45230] [debug]   UioIf: uio name = /dev/uio4
[2022-12-02 17:40:23.013898] [0xb6f45230] [debug]   DDR4 init = true
[2022-12-02 17:40:23.015813] [0xb6f45230] [debug]   UioIf: uio name = /dev/uio2
[2022-12-02 17:40:23.017254] [0xb6f45230] [debug]   UioIf: uio name = /dev/uio1
[2022-12-02 17:40:23.018657] [0xb6f45230] [debug]   UioIf: uio name = /dev/uio3
[2022-12-02 17:40:23.019105] [0xb6f45230] [debug]   UDmaBuf: size      = 16777216
[2022-12-02 17:40:23.019194] [0xb6f45230] [debug]   UDmaBuf: phys addr = 38100000
[2022-12-02 17:40:23.019927] [0xb6f45230] [debug]   UioAxiDmaIf: start, start_desc = 44120000
[2022-12-02 17:40:23.020598] [0xb5a59450] [debug]   DataHandlerPrint: process data, size = 8192
[2022-12-02 17:40:23.020763] [0xb5a59450] [debug]   DataHandlerPrint: Received all packets
Counters: OK = 4096, total = 4096
root@damc-fmc1z7io ~ ifconfig
eth0      Link encap:Ethernet  HWaddr 80:1f:12:dc:7a:6a
          inet addr:192.168.1.86  Bcast:192.168.1.255  Mask:255.255.255.0
          inet6 addr: fe80::821f:12ff:fedc:7a6a/64 Scope:Link
          UP BROADCAST RUNNING MULTICAST  MTU:1500  Metric:1
          RX packets:13647 errors:0 dropped:0 overruns:0 frame:0
          TX packets:381 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:1000
          RX bytes:684922 (668.8 KiB)  TX bytes:76774 (74.9 KiB)
          Interrupt:27 Base address:0xb000

lo        Link encap:Local Loopback
          inet addr:127.0.0.1  Mask:255.0.0.0
          inet6 addr: ::1/128 Scope:Host
          UP LOOPBACK RUNNING  MTU:65536  Metric:1
          RX packets:0 errors:0 dropped:0 overruns:0 frame:0
          TX packets:0 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:1000
          RX bytes:0 (0.0 B)  TX bytes:0 (0.0 B)

root@damc-fmc1z7io ~
```





MicroTCA Troubleshooting

Troubleshooting in MicroTCA

General Suggestions

- MicroTCA systems are very dynamic and provide a lot of options for customization
  - configurable hardware
  - configurable firmware/software
  - {…}
- Debug systematically
- Try to isolate the root cause – use “bisection”
- Consult vendor manuals
- Consult vendor support
  - describe the issue as detailed as possible
  - provide system information (e.g. “collect system information now” on N.A.T. MCH)

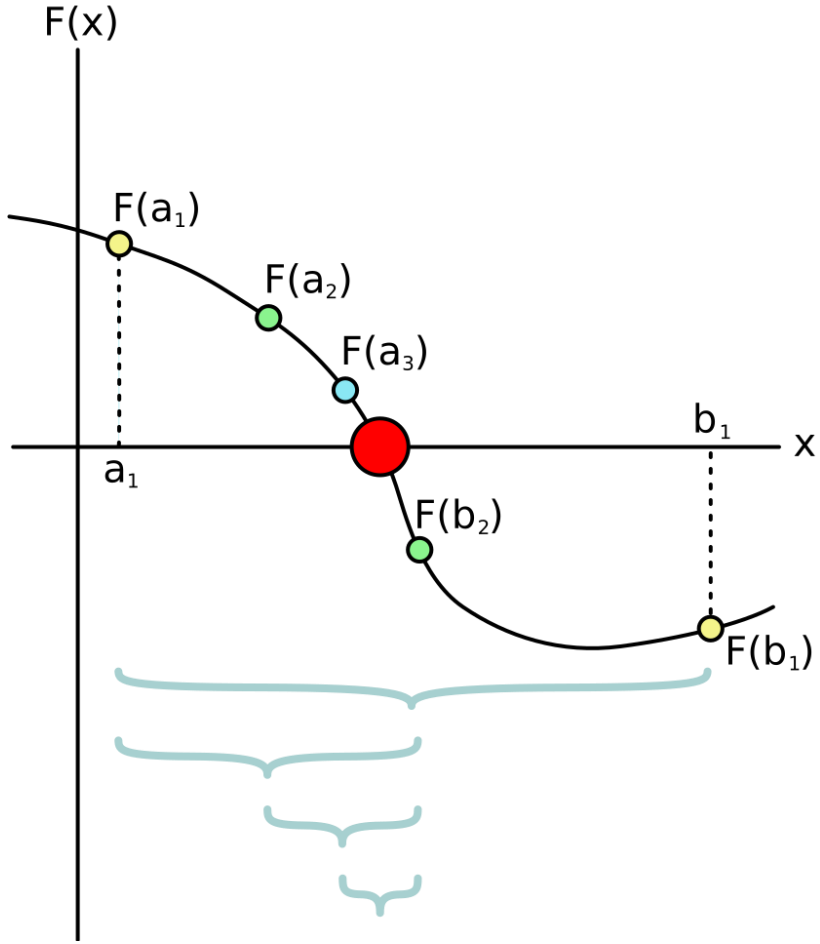
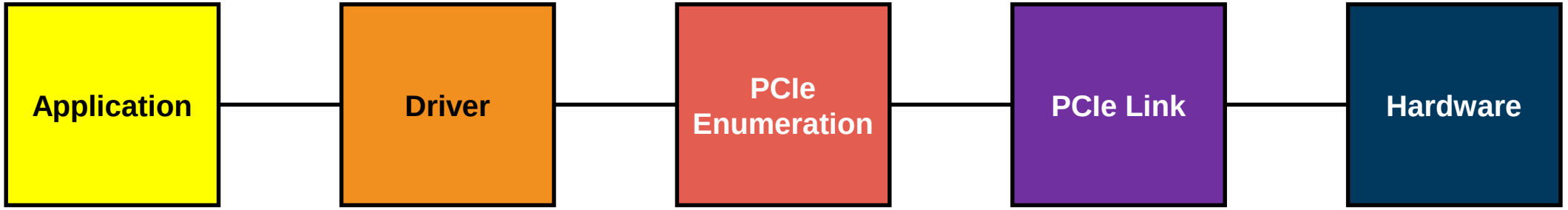


Figure: Bisection method.svg: Tokuchan - Bisection method.svg, CC BY-SA 3.0, *https://commons.wikimedia.org/w/index.php?curid=9382140*

Troubleshooting in MicroTCA

Potential Sources of Failure

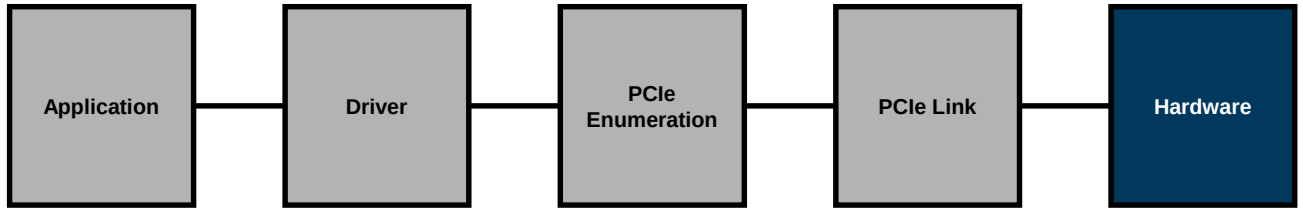


Application	Driver	PCIe Enumeration	PCIe Link	Hardware
> (app dependent)	> dmesg	> lspci	> show_ekey	> show_fru
> pcimem	> lspci	> dmesg	> show_link_state	> show_sensorinfo

Troubleshooting in MicroTCA

Step 1: Hardware

- > Check LEDs (on MCH and on AMCs)
- > Check M-states of FRUs (AMCs, power modules, fan trays, …)
- > Check voltages and temperatures on AMCs
- > Check if payload (FPGA/SoC) is programmed



- (app dependent)
- pcimem

- dmesg
- lspci

- lspci
- dmesg

- show_ekey
- show_link_state

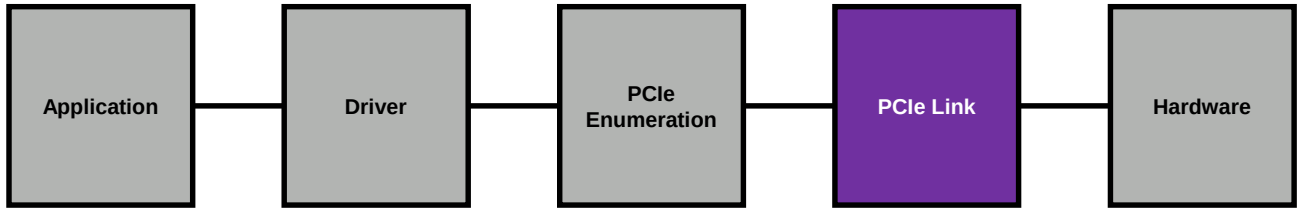
- show_fru
- show_sensorinfo

```
nat> show_sensorinfo 7
Sensor Information for FRU 7 / AMC3
=================================================================
  #   SDRType  Sensor Entity Inst  Value   State    Name
-----------------------------------------------------------------
  -   MDevLoc          0xc1  0x63                  DAMC-FMC2ZUP
  0   Full     0xf2    0xc1  0x63  0x01            AMC Hot Swap
  1   Compact  0x0b    0xc1  0x63  0x00            0x00  801F12F0DFD6
  2   Full     Temp    0xc1  0x63  32.0 C     ok    STAMP Temp
  3   Full     Voltage 0xc1  0x63  3.384 V    ok    AMC MP 3V3
  4   Full     Voltage 0xc1  0x63  12.56 V    ok    AMC PP 12V
  5   Full     Current 0xc1  0x63  0.000 A    ok    I_RTM MP 3V3
  6   Full     Current 0xc1  0x63  0.00 A     ok    I_RTM PP 12V
  7   Compact  0x14    0xc1  0x63  0x01            0x00  CPLD Done
  8   Compact  0x14    0xc1  0x63  0x00            0x00  RTM MP 3V3 PG
  9   Compact  0x14    0xc1  0x63  0x00            0x00  RTM PP 12V PG
 10   Compact  0x14    0xc1  0x63  0x00            0x00  RTM Fault
 11   Compact  0x14    0xc1  0x63  0x01            0x00  PGood_A
 12   Compact  0x14    0xc1  0x63  0x01            0x00  PGood_B
 13   Compact  0x14    0xc1  0x63  0x01            0x00  FPGA1 Init
 14   Compact  0x14    0xc1  0x63  0x01            0x00  FPGA1 Done
 15   Compact  0x14    0xc1  0x63  0x01            0x00  FPGA2 Init
 16   Compact  0x14    0xc1  0x63  0x01            0x00  FPGA2 Done
 17   Full     Temp    0xc1  0x63  36.5 C     ok    Inlet Temp
 18   Full     Temp    0xc1  0x63  40.0 C     ok    Outlet Temp
 19   Full     Temp    0xc1  0x63  38.0 C     ok    LTM4630 Temp
 20   Full     Temp    0xc1  0x63  40.5 C     ok    LTM4650 Temp
 21   Full     Temp    0xc1  0x63  46.5 C     ok    LTM4633_F Temp
 22   Full     Temp    0xc1  0x63  44.0 C     ok    LTM4633_R Temp
 23   Full     Temp    0xc1  0x63  44.5 C     ok    ZUP IC Temp
 24   Full     Temp    0xc1  0x63  47.0 C     ok    S7 IC Temp
 25   Full     Current 0xc1  0x63  0.46 A     ok    IMON_AVTT
 26   Full     Current 0xc1  0x63  0.64 A     ok    IMON_AVTTY
 27   Full     Current 0xc1  0x63  0.256 A    ok    IMON_AVCC
 28   Full     Current 0xc1  0x63  0.560 A    ok    IMON_AVCCY
 29   Full     Voltage 0xc1  0x63  0.7168 V   ok    Vcore
 30   Full     Voltage 0xc1  0x63  1.8000 V   ok    VCC_Vadj
 31   Full     Voltage 0xc1  0x63  1.2000 V   ok    VCC_1V2
 32   Compact  0xf0    0xc1  0x63  0x10            HS 007 AMC3
-----------------------------------------------------------------
```

Troubleshooting in MicroTCA

Step 2: PCI Express Link

- Check link state (LEDs, MCH console, *show_link_state*)
- Check e-keying process (*show_ekey*)
- Check AMC FRU information (*show_fruinfo*)
- Check MCH configuration and error counters

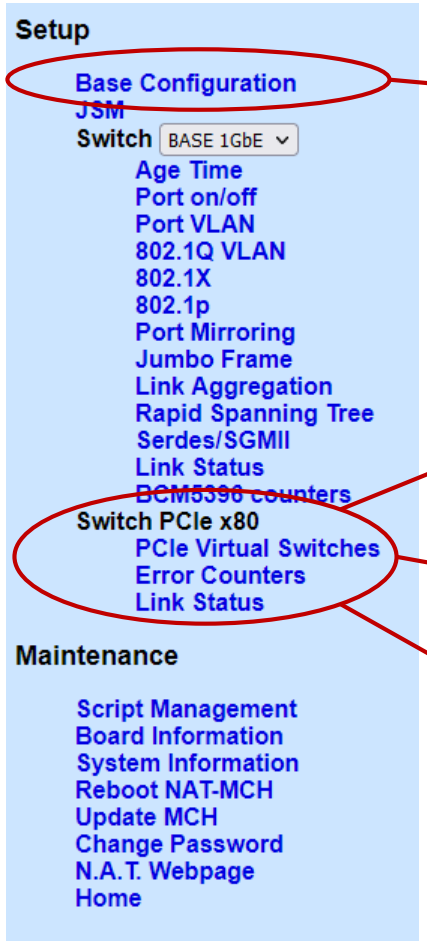


Application	Driver	PCIe Enumeration	PCIe Link	Hardware
• (app dependent) • pcimem	• dmesg • lspci	• lspci • dmesg	• show_ekey • show_link_state	• show_fru • show_sensorinfo

```
nat>show_fruinfo 7
----------------------------------------
FRU Info for device 7:
----------------------------------------
Common Header    : 0x01 0x00 0x00 0x01 0x0c 0x18 0x00 0xda
----------------------------------------
Internal Use Area : -
----------------------------------------
Chassis Info Area : -
----------------------------------------
Board Info Area          : at offs=8, len=88
Manufacturer(13)         : DESY/CAEN ELS
Board Name(17)           : DAMC-FMC2ZUP-11EG
Serial Number(10)        : 21Y17W0554
Part Number(12)          : DAMCFMC2ZUP1
FRU file ID(20)          : fru_damc-fmc2zup.bin
----------------------------------------
Product Info Area        : at offs=96, len=96
Manufacturer(13)         : DESY/CAEN ELS
Product Name(17)         : DAMC-FMC2ZUP-11EG
Product Number(12)       : DAMCFMC2ZUP1
Part Version(04)         : revB
Product Serial Number(10): 21Y17W0554
Asset Tag(04)            : none
FRU file ID(20)          : fru_damc-fmc2zup.bin
----------------------------------------
Multi Record Area  : at offs=192

Record(0): Type ID=0xc0, PICMG Record ID=0x16, offset=0x000, len=11
Module Current Requirements Record:
    Current Draw: 6.5 A

Record(1): Type ID=0xc0, PICMG Record ID=0x19, offset=0x00b, len=124
AMC Point-to-Point record:
AMC Slot  3, OEM GUID Count = 1
    Record Type = AMC, len=124
    Channel Descriptor count = 10
    Channel(0): Port[4 5 6 7]
    Channel(1): Port[8 9 10 11]
    Channel(2): Port[0 - - -]
    Channel(3): Port[1 - - -]
    Channel(4): Port[2 - - -]
    Channel(5): Port[3 - - -]
    Channel(6): Port[12 - - -]
    Channel(7): Port[13 - - -]
    Channel(8): Port[14 - - -]
    Channel(9): Port[15 - - -]
    Link Descriptors: size=65
    Link 0 of Channel 0: lanes[0..3]=[1111], PCIe,  Gen 3, no SSC, Grp=0x1, Match=0x1
    Link 1 of Channel 1: lanes[0..3]=[1111], PCIe,  Gen 3, no SSC, Grp=0x1, Match=0x1
    Link 2 of Channel 0: lanes[0..3]=[1111], PCIe,  Gen 3, no SSC, Grp=0x0, Match=0x1
    Link 3 of Channel 0: lanes[0..3]=[1100], PCIe,  Gen 3, no SSC, Grp=0x0, Match=0x1
    Link 4 of Channel 0: lanes[0..3]=[1000], PCIe,  Gen 3, no SSC, Grp=0x0, Match=0x1
    Link 5 of Channel 2: lanes[0..3]=[1000], Eth ,  1000Base-BX, Grp=0x0, Match=0x0
    Link 6 of Channel 3: lanes[0..3]=[1000], Eth ,  1000Base-BX, Grp=0x0, Match=0x0
    Link 7 of Channel 4: lanes[0..3]=[1000], SATA,  LinkTExt=[1000], Grp=0x0, Match=0x2
    Link 8 of Channel 5: lanes[0..3]=[1000], SATA,  LinkTExt=[1000], Grp=0x0, Match=0x2
    Link 9 of Channel 6: lanes[0..3]=[1000], 0xf0,  LinkTExt=[0000], Grp=0x0, Match=0x0
    Link 10 of Channel 7: lanes[0..3]=[1000], 0xf0,  LinkTExt=[0000], Grp=0x0, Match=0x0
    Link 11 of Channel 8: lanes[0..3]=[1000], 0xf0,  LinkTExt=[0000], Grp=0x0, Match=0x0
    Link 12 of Channel 9: lanes[0..3]=[1000], 0xf0,  LinkTExt=[0000], Grp=0x0, Match=0x0

Record(2): Type ID=0xc0, PICMG Record ID=0x30, offset=0x087, len=15
Zone 3 Interface Compatibility record:
unknown Type of Interface - 0x5
----------------------------------------
```

Troubleshooting in MicroTCA

Step 2: PCI Express Link



MCH web-interface for configuration and status information

PCIe Virtual Switch configuration

Select Host AMCs (Upstream) for each virtual
Select Host AMCs (Non-Transparent Upstrear
Select which AMCs shall be connected to eac

Link Width		
Virtual Switch	Upstream AMC	NT-Upstrea AMC
none		
0	AMC1/4..7	- none -
1	- none -	
2	- none -	
3	- none -	
Max. Link Speed		

Apply
Note: You need to click apply before you c

RCV_CNT	
Bad TLP	
Bad DLLP	

Reset Refresh

Configuration Option	default	Description
Upstream slot power up delay	5 sec	Delay applied to the slot where the upstream CPU (root complex) resides in. The delay is applied before payload power is turned on. (*)
PCIe hot plug delay for AMCs	0 sec	Delay applied to the slots where downstream AMCs reside in. The delay is applied after payload power is turned on. (*)
100 MHz spread spectrum clock (**)	Disabled	If enabled, the FCLKA clock will be of spread spectrum type with 100 MHz means. If disabled the FCLKA is a 100MHz fixed clock.
hot plug support	Disabled	Enables PCIe Hot Plug Support. Refer to Appendix F "PCIe Hot Plug Support (optional)" for details on how the **NAT-MCH** firmware is handling the hot plug signals.
PCIe early Ekey	Disabled	Executes the E-Keying before payload power is applied
'no ekey' for PCIe	Disabled	The PCIe ports are only enabled during E-Keying from **NAT-MCH** Firmware version V2.15 upwards when the E-Keying information match. To get a downwards compatible behavior, this can be deactivated by setting the parameter 'no ekey' for PCIe to option enabled. In this case, the PCIe ports are always enabled regardless of the E-Keying information.

PCIe Link Status Menu

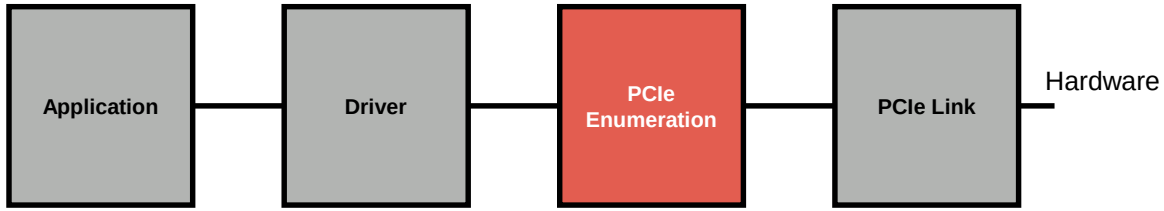
	AMC1	AMC2	AMC3	AMC4	AMC5	AMC6	AMC7	OPT1	RTM
	4..7	4..7	4..7	4..7	4..7	4..7	4..7		
	x4	-	x4	-	x2	-	-	-	-
Link Speed	8 GT/s	-	8 GT/s	-	5 GT/s	-	-	-	-

PCIe LED link status LEDs

Troubleshooting in MicroTCA

Step 3: PCI Express Enumeration

- Check *lspci* for PCI slots
- Rescan bus (*sudo lspci -H1*)
- Check if virtual memory is allocated (*sudo lspci –s <dev> –vv)*
- Reboot CPU
- Go back and check MCH link status



• (app dependent)	• dmesg	• lspci	• show_ekey
• pcimem	• lspci	• dmesg	• show_link_state

```
$ lspci
00:00.0 Host bridge: Intel Corporation Xeon E3-1200 v6/7th Gen Core Processor Host Bridge/DRAM Registers (rev 05)
00:01.0 PCI bridge: Intel Corporation Xeon E3-1200 v5/E3-1500 v5/6th Gen Core Processor PCIe Controller (x16) (rev 05)
00:01.1 PCI bridge: Intel Corporation Xeon E3-1200 v5/E3-1500 v5/6th Gen Core Processor PCIe Controller (x8) (rev 05)
00:02.0 VGA compatible controller: Intel Corporation HD Graphics P630 (rev 04)
00:08.0 System peripheral: Intel Corporation Xeon E3-1200 v5/v6 / E3-1500 v5 / 6th/7th/8th Gen Core Processor Gaussian Mixture Model
00:14.0 USB controller: Intel Corporation 100 Series/C230 Series Chipset Family USB 3.0 xHCI Controller (rev 31)
00:14.2 Signal processing controller: Intel Corporation 100 Series/C230 Series Chipset Family Thermal Subsystem (rev 31)
00:15.0 Signal processing controller: Intel Corporation 100 Series/C230 Series Chipset Family Serial IO I2C Controller #0 (rev 31)
00:15.1 Signal processing controller: Intel Corporation 100 Series/C230 Series Chipset Family Serial IO I2C Controller #1 (rev 31)
00:16.0 Communication controller: Intel Corporation 100 Series/C230 Series Chipset Family MEI Controller #1 (rev 31)
00:17.0 SATA controller: Intel Corporation Q170/Q150/B150/H170/H110/Z170/CM236 Chipset SATA Controller [AHCI Mode] (rev 31)
00:1c.0 PCI bridge: Intel Corporation 100 Series/C230 Series Chipset Family PCI Express Root Port #1 (rev f1)
00:1c.1 PCI bridge: Intel Corporation 100 Series/C230 Series Chipset Family PCI Express Root Port #2 (rev f1)
00:1c.2 PCI bridge: Intel Corporation 100 Series/C230 Series Chipset Family PCI Express Root Port #3 (rev f1)
00:1c.3 PCI bridge: Intel Corporation 100 Series/C230 Series Chipset Family PCI Express Root Port #4 (rev f1)
00:1d.0 PCI bridge: Intel Corporation 100 Series/C230 Series Chipset Family PCI Express Root Port #9 (rev f1)
00:1f.0 ISA bridge: Intel Corporation CM238 Chipset LPC/eSPI Controller (rev 31)
00:1f.2 Memory controller: Intel Corporation 100 Series/C230 Series Chipset Family Power Management Controller (rev 31)
00:1f.3 Audio device: Intel Corporation CM238 HD Audio Controller (rev 31)
00:1f.4 SMBus: Intel Corporation 100 Series/C230 Series Chipset Family SMBus (rev 31)
01:00.0 PCI bridge: PLX Technology, Inc. Device 8725 (rev ca)
01:00.1 System peripheral: PLX Technology, Inc. Device 87d0 (rev ca)
01:00.2 System peripheral: PLX Technology, Inc. Device 87d0 (rev ca)
01:00.3 System peripheral: PLX Technology, Inc. Device 87d0 (rev ca)
01:00.4 System peripheral: PLX Technology, Inc. Device 87d0 (rev ca)
02:01.0 PCI bridge: PLX Technology, Inc. Device 8725 (rev ca)
02:02.0 PCI bridge: PLX Technology, Inc. Device 8725 (rev ca)
02:08.0 PCI bridge: PLX Technology, Inc. Device 8725 (rev ca)
02:09.0 PCI bridge: PLX Technology, Inc. Device 8725 (rev ca)
02:0a.0 PCI bridge: PLX Technology, Inc. Device 8725 (rev ca)
03:00.0 PCI bridge: PLX Technology, Inc. Device 8780 (rev ab)
04:01.0 PCI bridge: PLX Technology, Inc. Device 8780 (rev ab)
04:03.0 PCI bridge: PLX Technology, Inc. Device 8780 (rev ab)
04:05.0 PCI bridge: PLX Technology, Inc. Device 8780 (rev ab)
04:07.0 PCI bridge: PLX Technology, Inc. Device 8780 (rev ab)
04:09.0 PCI bridge: PLX Technology, Inc. Device 8780 (rev ab)
04:0b.0 PCI bridge: PLX Technology, Inc. Device 8780 (rev ab)
04:0c.0 PCI bridge: PLX Technology, Inc. Device 8780 (rev ab)
05:00.0 Serial controller: Xilinx Corporation Device 7022
09:00.0 Processing accelerators: Xilinx Corporation Device 9034
0e:00.0 Ethernet controller: Intel Corporation Ethernet Controller X710 for 10GbE SFP+ (rev 02)
0e:00.1 Ethernet controller: Intel Corporation Ethernet Controller X710 for 10GbE SFP+ (rev 02)
11:00.0 Ethernet controller: Intel Corporation I210 Gigabit Network Connection (rev 03)
12:00.0 Ethernet controller: Intel Corporation I210 Gigabit Backplane Connection (rev 03)
13:00.0 Ethernet controller: Intel Corporation I210 Gigabit Backplane Connection (rev 03)
14:00.0 Ethernet controller: Intel Corporation I210 Gigabit Network Connection (rev 03)
15:00.0 Non-Volatile memory controller: Samsung Electronics Co Ltd NVMe SSD Controller SM981/PM981/PM983
```

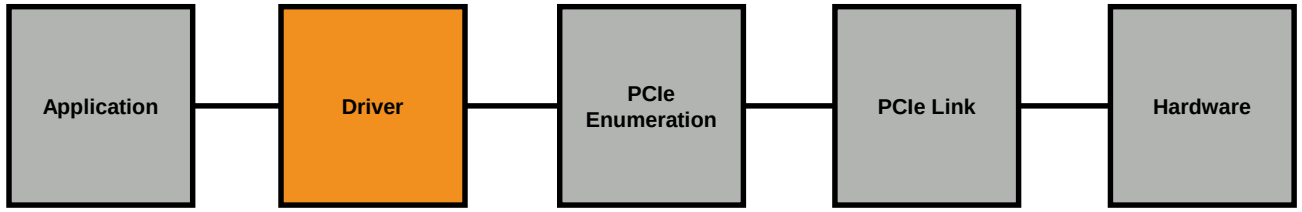
```
$ sudo lspci -s 06:00 –vv
06:00.0 Serial controller: Xilinx Corporation Device 7024 (prog-if 01 [16450]
        ...
        Region 0: Memory at 92800000 (32-bit, non-prefetchable) [size=8M]
        Region 1: Memory at 93000000 (32-bit, non-prefetchable) [size=64K]
        …
                LnkSta: Speed 5GT/s, Width x4, TrErr- Train- SlotClk+ ...
```

Troubleshooting in MicroTCA

Step 4: Driver

- Check if driver is loaded (*lsmod*)
- Use *insmod* to manually load the driver
- Check if the driver is used (*lspci -s <device> -v*)
- Check output of *dmesg* command

```
[...]
[ 4567.125524] xdma:xdma_mod_init: Xilinx XDMA Reference Driver xdma v2020.1.8
[ 4567.125527] xdma:xdma_mod_init: desc_blen_max: 0xfffffff/268435455, timeout: h2c 10 c2h 10 sec.
[ 4567.125575] xdma:xdma_device_open: xdma device 0000:05:00.0, 0x000000006414bdad.
[ 4567.125802] xdma:map_single_bar: BAR0 at 0x93000000 mapped at 0x000000009debbcb1, length=16777216(/16777216)
[ 4567.125815] xdma:map_single_bar: BAR1 at 0x94000000 mapped at 0x0000000019b447b4, length=65536(/65536)
[ 4567.125820] xdma:map_bars: config bar 1, pos 1.
[ 4567.125821] xdma:identify_bars: 2 BARs: config 1, user 0, bypass -1.
[ 4567.125895] xdma:probe_one: 0000:05:00.0 xdma0, pdev 0x000000006414bdad, xdev 0x00000002bf83b8a, 0x00000000a804c23d, usr 16, ch 1,1.
[ 4567.126401] xdma:cdev_xvc_init: xcdev 0x00000002f8f22c6, bar 0, offset 0x40000.
[ 4567.126449] xdma:xdma_device_open: xdma device 0000:09:00.0, 0x00000000da1910f9.
[ 4567.126600] xdma:map_single_bar: BAR0 at 0x95000000 mapped at 0x0000000084611659, length=16777216(/16777216)
[ 4567.126612] xdma:map_single_bar: BAR1 at 0x94800000 mapped at 0x00000000cd3ec099, length=65536(/65536)
[ 4567.126617] xdma:map_bars: config bar 1, pos 1.
[ 4567.126618] xdma:identify_bars: 2 BARs: config 1, user 0, bypass -1.
[ 4567.126734] xdma:pci_keep_intx_enabled: 0000:09:00.0: clear INTX_DISABLE, 0x406 -> 0x6.
[ 4567.126752] xdma:probe_one: 0000:09:00.0 xdma1, pdev 0x00000000da1910f9, xdev 0x00000000eaa036b5, 0x0000000069f8f59f, usr 16, ch 1,1.
[ 4567.127315] xdma:cdev_xvc_init: xcdev 0x0000000068f58705, bar 0, offset 0x40000.
[...]
```



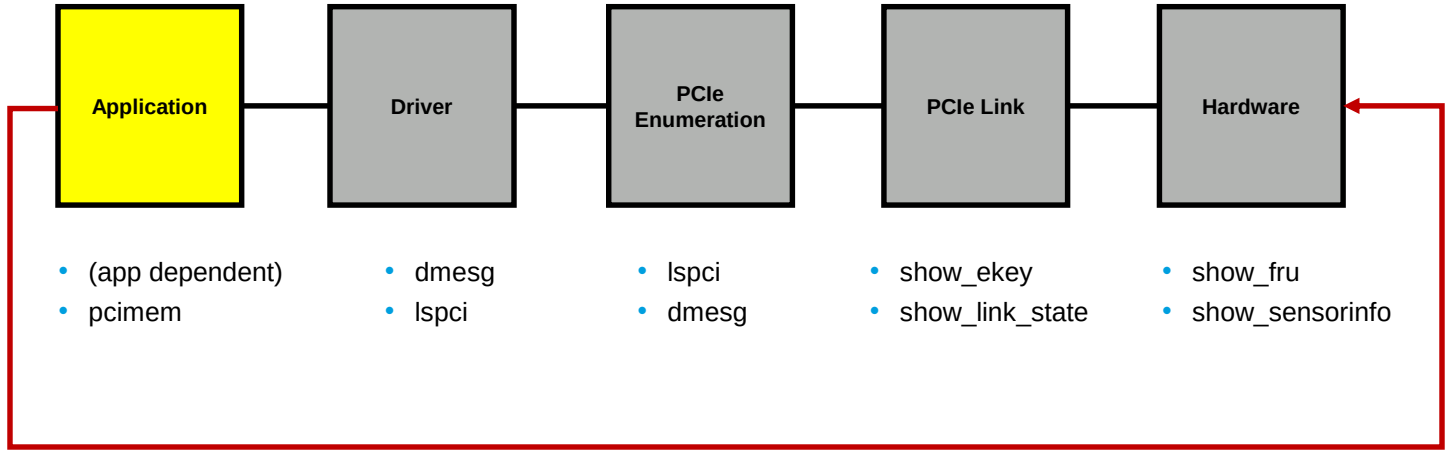
Application	Driver	PCIe Enumeration	PCIe Link	Hardware
• (app dependent) • pcimem	• dmesg • lspci	• lspci • dmesg	• show_ekey • show_link_state	• show_fru • show_sensorinfo

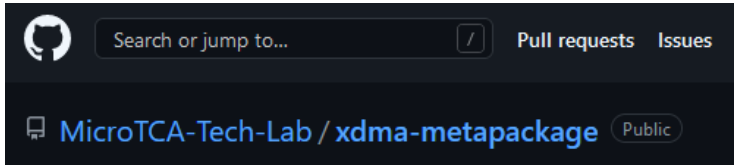
Troubleshooting in MicroTCA

Step 5: Application

- Read/write registers
  - *pcimem*
  - Xilinx XDMA tools: *reg_rw*
- Debug application software
- Go back to FPGA/SoC configuration

```
$ cd xdma-metapackage/dma_ip_drivers/XDMA/linux-kernel/tools
$ ./reg_rw /dev/xdma/slot3/user 0x0
argc = 3
device: /dev/xdma/slot3/user
address: 0x00000000
access type: read
access width: word (32-bits)
character device /dev/xdma/slot3/user opened.
Memory mapped at address 0x7f3755061000.
Read 32-bit value at address 0x00000000 (0x7f3755061000): 0xdf3c2702
$ ./reg_rw /dev/xdma/slot5/user 0x0
argc = 3
device: /dev/xdma/slot5/user
address: 0x00000000
access type: read
access width: word (32-bits)
character device /dev/xdma/slot5/user opened.
Memory mapped at address 0x7f6e41f2b000.
Read 32-bit value at address 0x00000000 (0x7f6e41f2b000): 0xdf3c1710
```





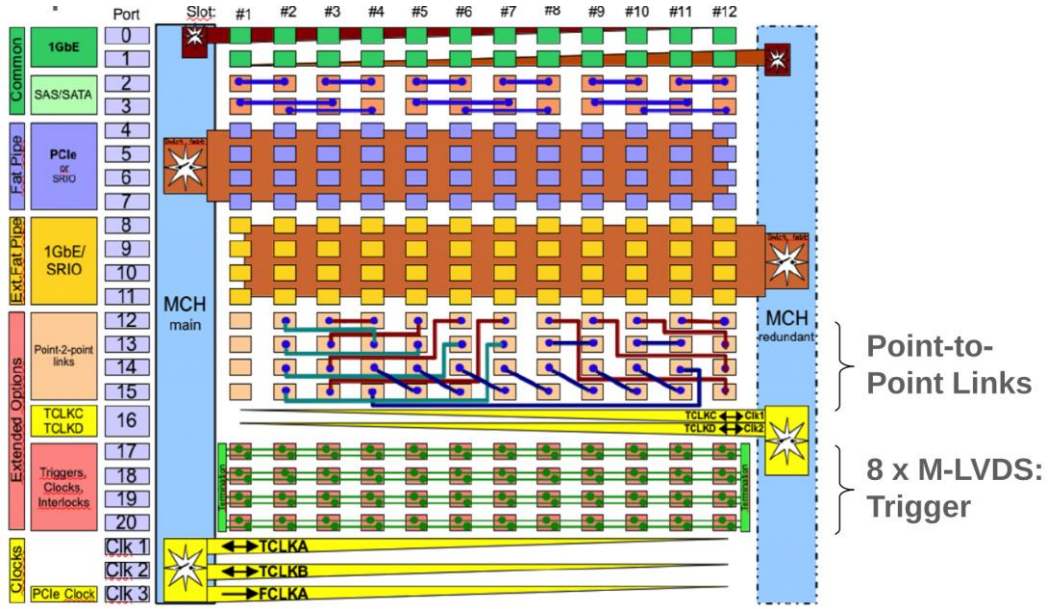
https://github.com/MicroTCA-Tech-Lab/xdma-metapackage

Recommendations

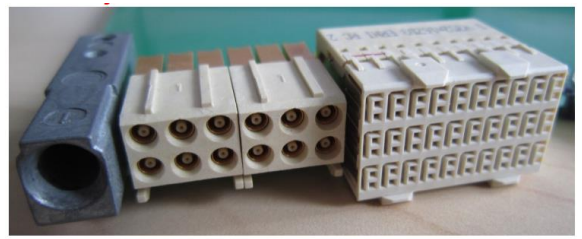
Recommendations

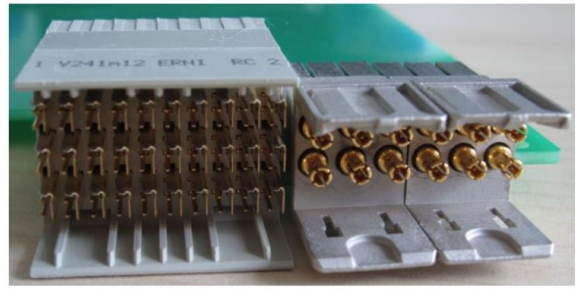
Questions you should answer before start ordering

- Chassis:
  - Redundancy?
  - Number of AMCs/RTMs?
  - RTM backplane needed?
  - AMC backplane topology?
- MCH Configuration:
  - Fat Pipe Switch?
  - Clock Module?
  - External CPU via PCIe?
- AMC/RTM/FMC compatibility:
  - Zone3 compatibility
  - Reference implementations
  - In doubt: contact AMC vendor
- Timing (app. specific)?



Class D1.3 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
Digital clocks fixed I/O		3	LVDS - O	LVDS - O	LVDS - I	LVDS - I	LVDS - O	LVDS - O
		4	LVDS - O	LVDS - O	LVDS - O	LVDS - O	LVDS - O	LVDS - O
User -configuration		5	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		6	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		7	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		8	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		9	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		10	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
User Configuaration	J31	1	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		2	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
Standard Gbit-Links		3	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	CML - I	CML - I	CML - O	CML - O
		4	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	CML - I	CML - I	CML - O	CML - O
		5	LVDS - I	LVDS - I	CML - I	CML - I	CML - O	CML - O
		6	LVDS - O	LVDS - O	CML - I	CML - I	CML - O	CML - O
		7	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	CML - I	CML - I	CML - O	CML - O
		8	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	CML - I	CML - I	CML - O	CML - O
		9	LVDS - I	LVDS - I	CML - I	CML - I	CML - O	CML - O
		10	LVDS - O	LVDS - O	CML - I	CML - I	CML - O	CML - O



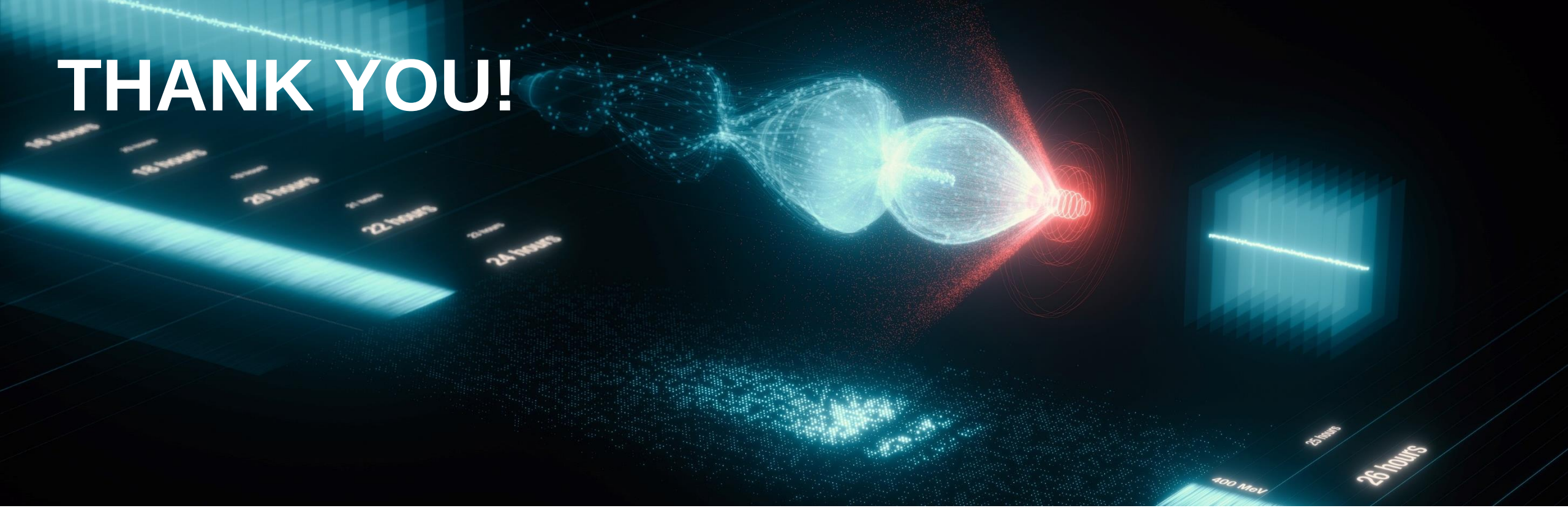


Recommendations

Things you should think about or you should do before start developing

- Solution already available?
  - COTS
  - Open Source
- Consult the specification documents
  - PICMG: MicroTCA, AMC, etc.
  - ANSI/VITA 57 FMC
  - PCI Express
  - Ethernet (IEEE 802.3)
- Become clear about the required performance
- Join the community

THANK YOU!



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Carsten Dülsen, Patrick Huesmann

DESY.

Backup Slides

Backup Slides

Block diagram Concurrent AM G6x