

# CNN Update Dresden

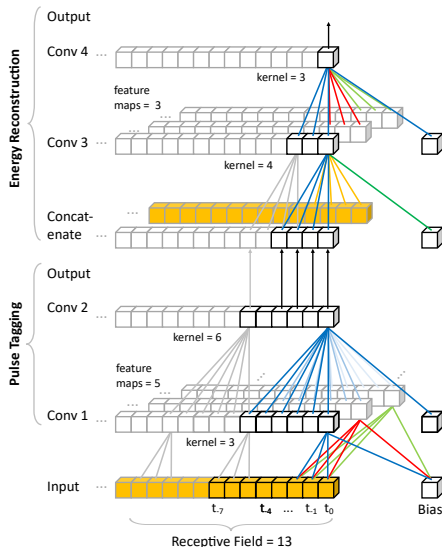
TA5-WP2: Working meeting - neural networks on FPGAs

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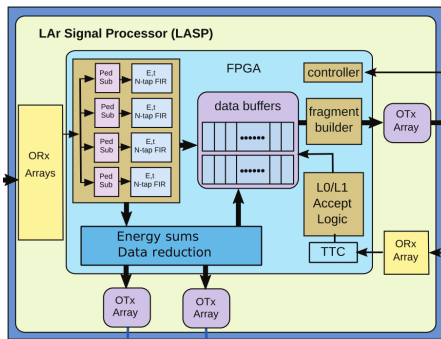
# Reminder: CNNs in Dresden

- Convolutional Neural Network with configurable architecture
- Study for Phase-II upgrade of ATLAS LAr calorimeter
- Implemented directly in VHDL
- VHDL code uses framework of firmware for Liquid Argon Signal Processor
- Goal: Real time energy reconstruction from ADC sequence on detector cell level



# Integration into detector firmware

- CNNs being integrated with rest of LASP firmware (MR pending minor adjustments)
- Provides same interface as FIR (baseline filter for energy reconstruction)
- New compilation and simulation targets



# Performance improvements

Netzwerk	$f_{\max}$	ALMs	DSPs	Latency
4Conv	487 MHz	16698	42	72 clock cycles = 6 BC = 150ns
3Conv	423 MHz	21256	46	60 clock cycles = 5 BC = 125ns

- Results for  $12\times$  multiplexing
- Maximum clock frequency improved, but still not at targeted 480 MHz for both networks
- Performance after integration similar, but frequencies inconsistent

# Next steps

- Prepare full compilation target with 32 parallel CNN instances ( $12 \times$  multiplexing each)
- Use hardware demonstrator setup to validate simulation results:

