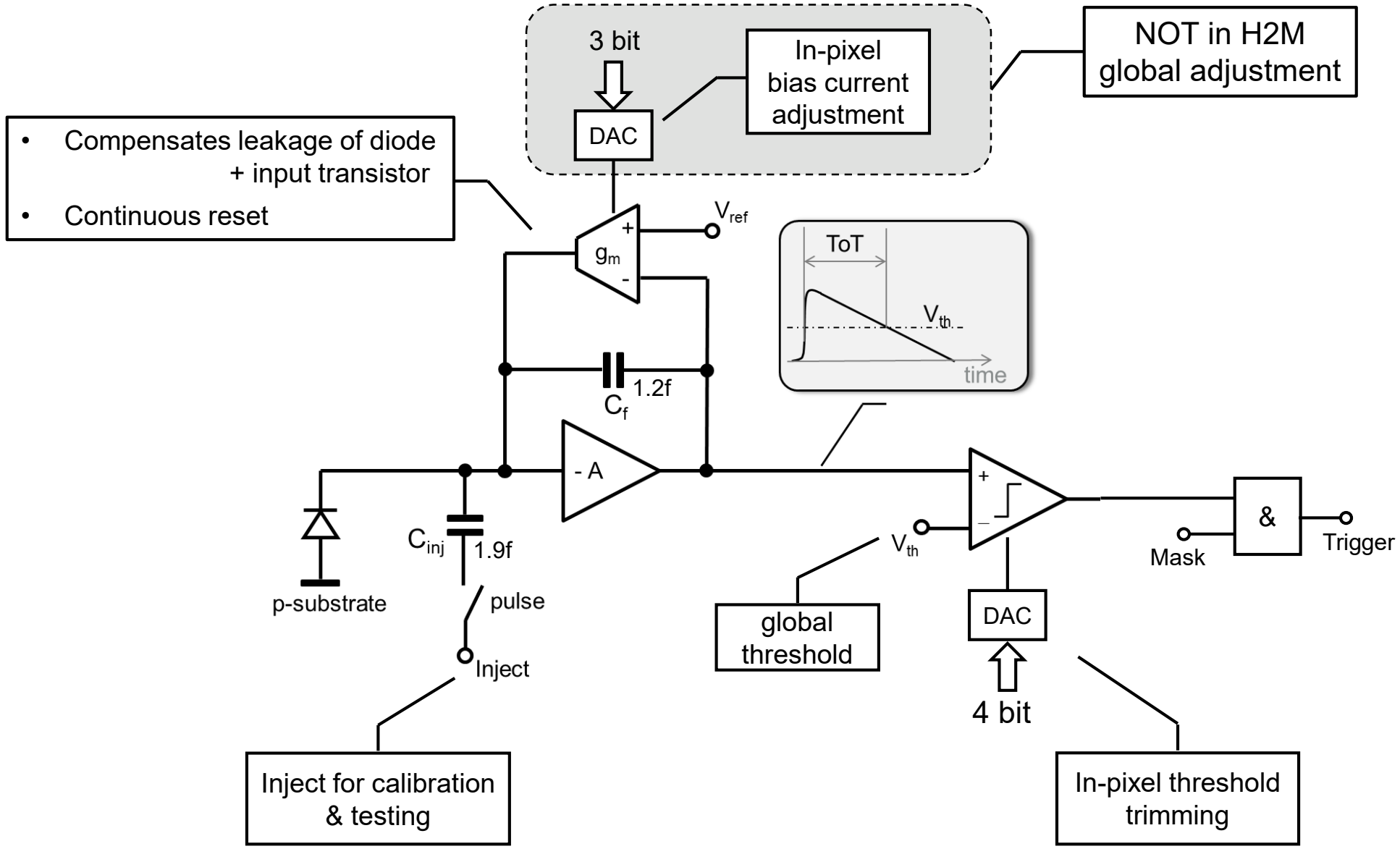
MAPS Front-End DESY D1 & D2

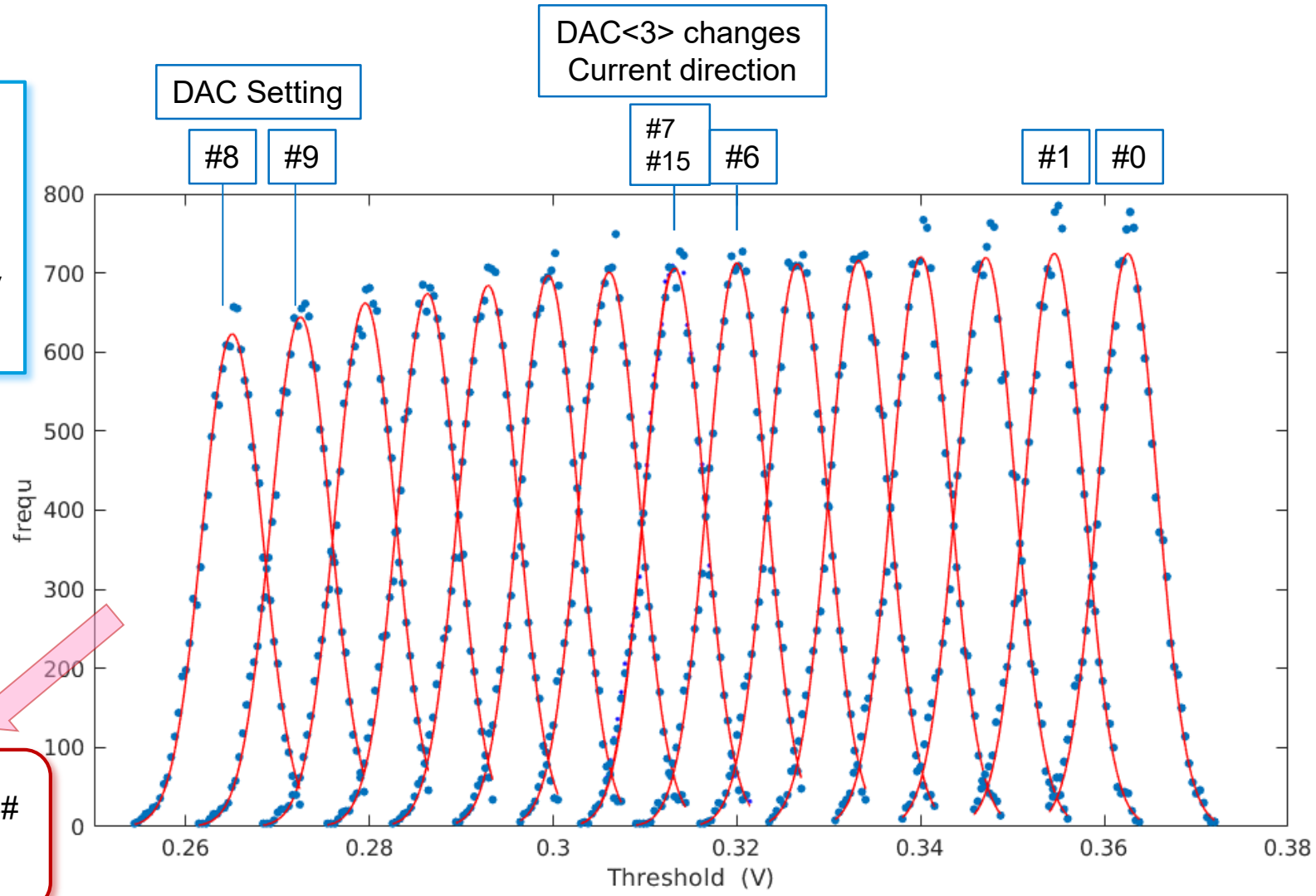


Threshold Scan

Counting on rising & falling edge

- Perform tran-analysis for 60µs time period
- No input
  1. For all DAC settings #0..#15
  2. Sweep Comp thres V_{th}, step size 400µV
  3. Count rising & falling edges @ Trigger

Post-Layout Simulation
Settings:
$I_{DAC\ Bias}$: 60nA
V_{refKr}: 325 mV
$V_{refComp}$: 325 mV
Bias CSA: 1.2uA
Bias Comp: 1.0uA



Gain ≈ 7 mV/DAC#

σ ≈ 3.2 mV_{rms}