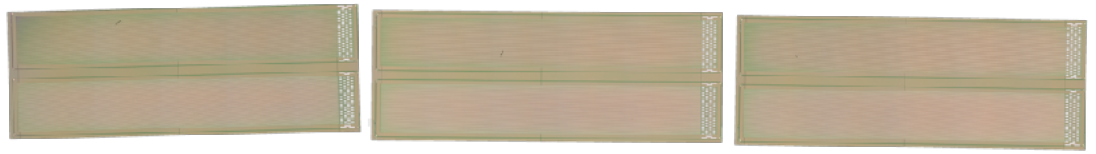
Passive CMOS Strip Sensors



Naomi Davis
November 8th

HELMHOLTZ

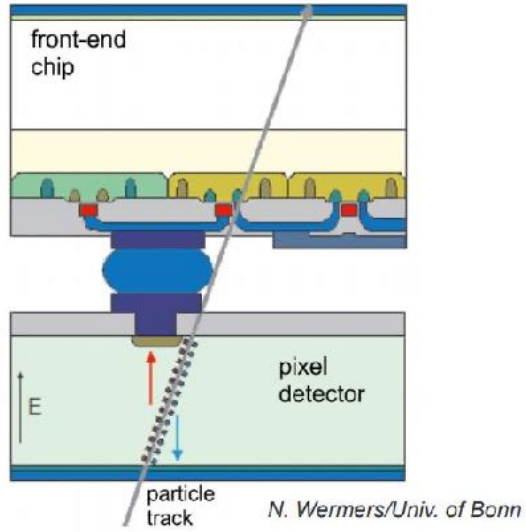
DESY.

Motivation

The need for alternative silicon sensor designs

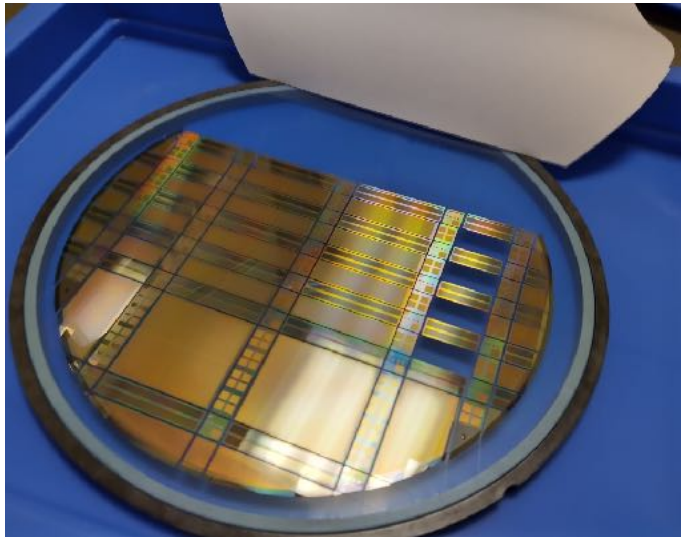
The current status:

- Silicon sensors as the main tracking device in HEP
- Demand to cover ever-larger area (sensors as the main cost-driver)
- Current technology only available from few foundries



Passive CMOS technology:

- Simplified CMOS process without active elements
  - Fast, large-scale production
  - Possible cost reduction
  - Wafer-scale industrial production (wafer size ≥ 200mm)
  - Many technology nodes to choose from
  - Designs are easy to port if e.g. company stops producing



Source: https://arxiv.org/pdf/2204.00501.pdf

Sensor Design

Stitched passive strip sensors on an 8” wafer

Specs

- LFoundry: 150nm process
- High resistivity wafer: 3-5 kΩcm
- Strip pitch: 75.5 um
- Designs: Regular and Low dose 30um/55um

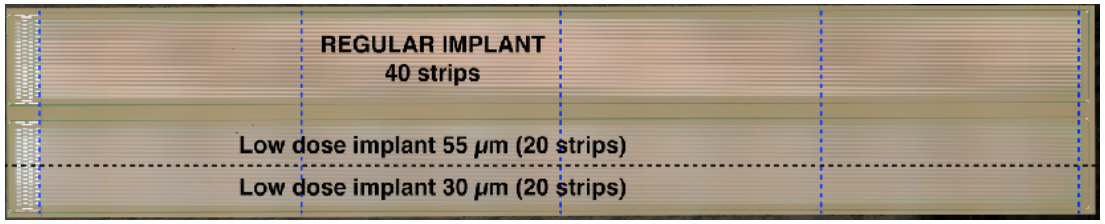
Stitching

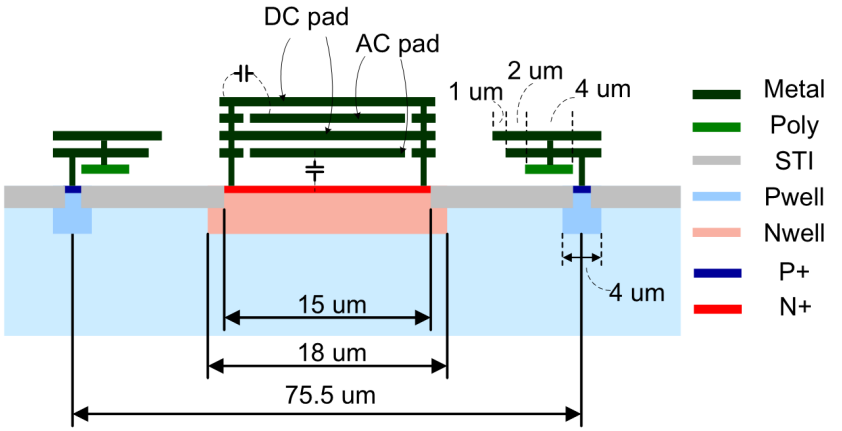
- Connect neighbouring reticles to obtain larger sensor
- Masks up to 1cm^2: Long strips (4.1 cm) & Short strips (2.1 cm)

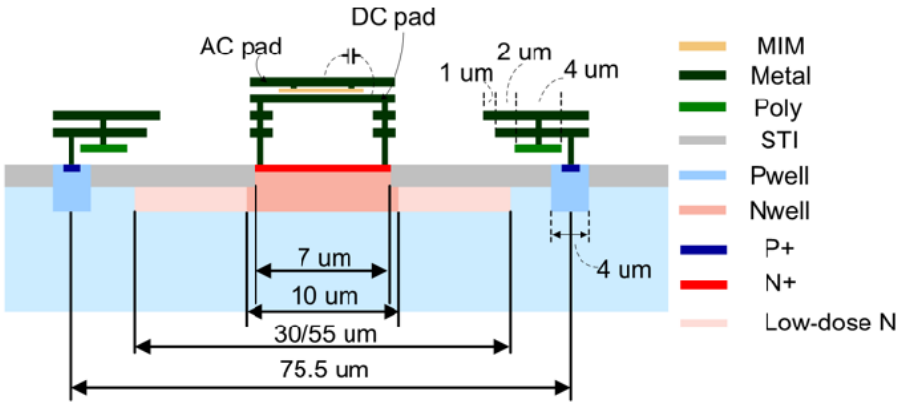
Sensor Studies

- Irradiation of sensors, TB measurements
- Edge TCT
- Lab tests with Sr-90 source
  - Charge collection at stitched areas (stitching successful!)

Next Up: Submission of new sensor design







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Thank you.