DESY.

https://www.desy.de/

Thin, Precise, Fast

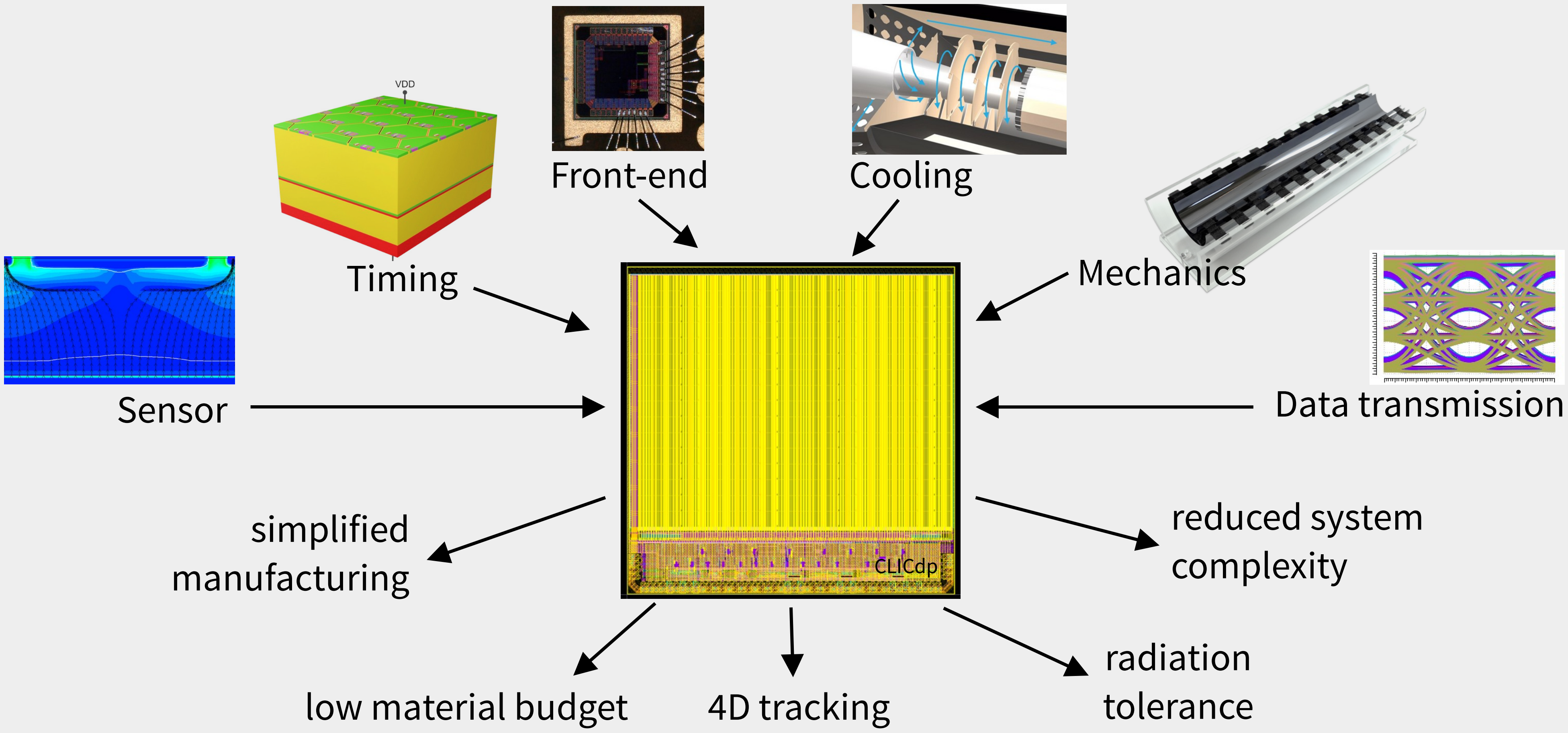
Ways Towards the Ultimate Silicon Sensor

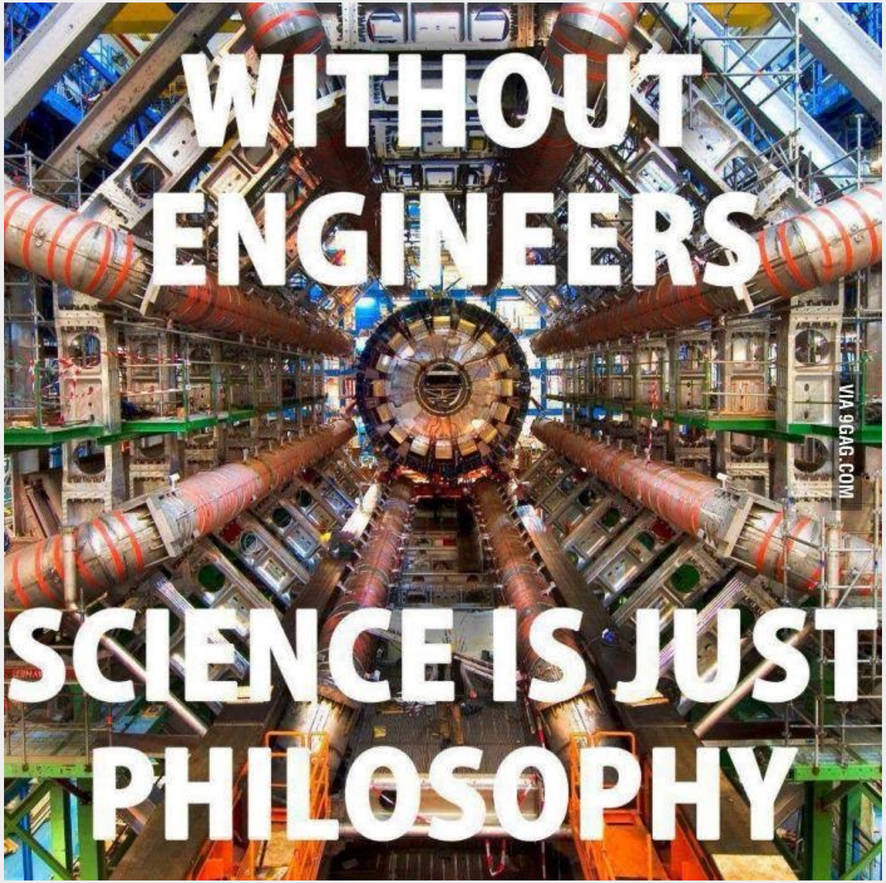
Faster, Harder, Scooter

Scooter, 2009

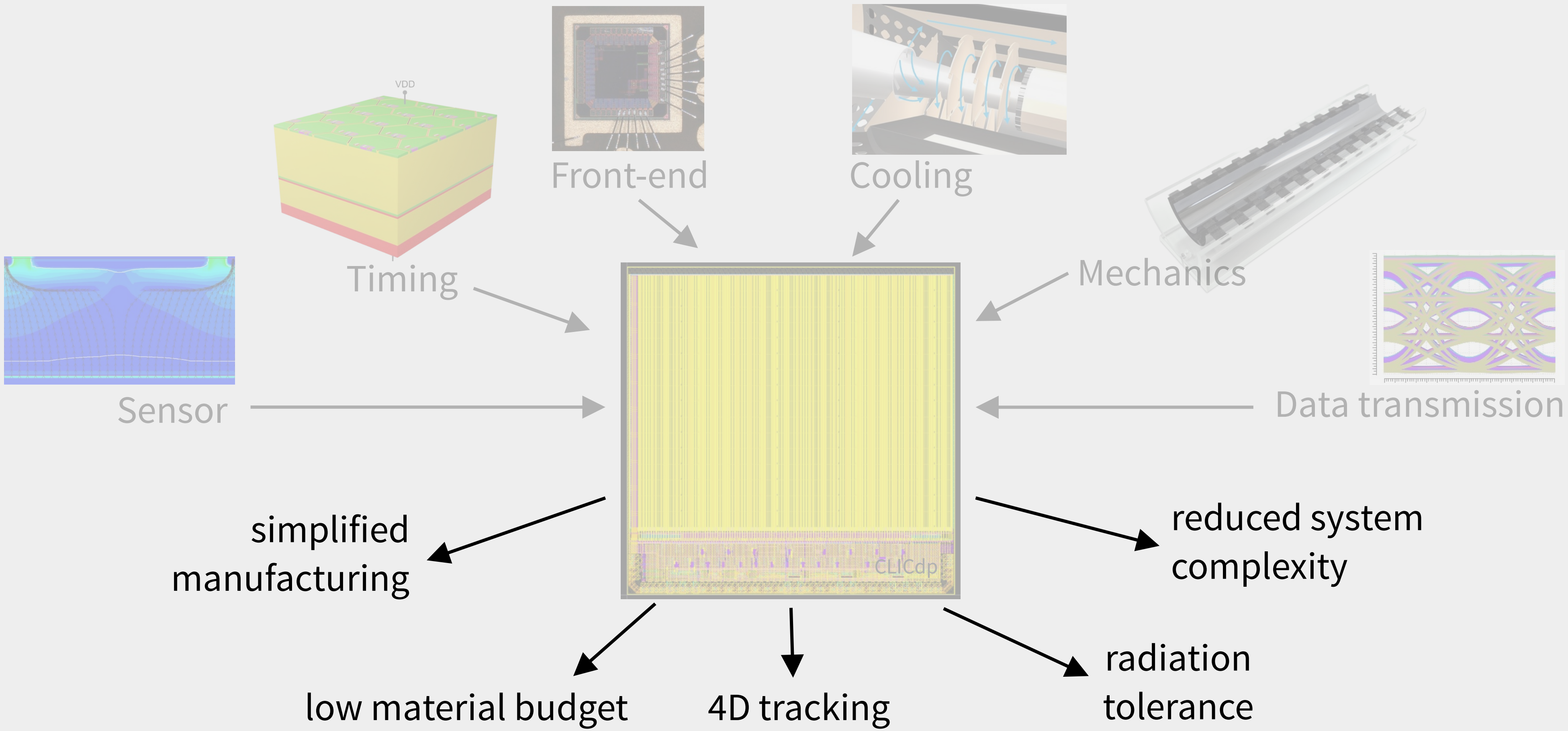
Ways Towards the Ultimate Silicon ~~Sensor~~ Detector

The Ultimate Silicon Sensor: A Detector-On-Chip System




WITHOUT ENGINEERS
SCIENCE IS JUST PHILOSOPHY
VIA 9GAG.COM

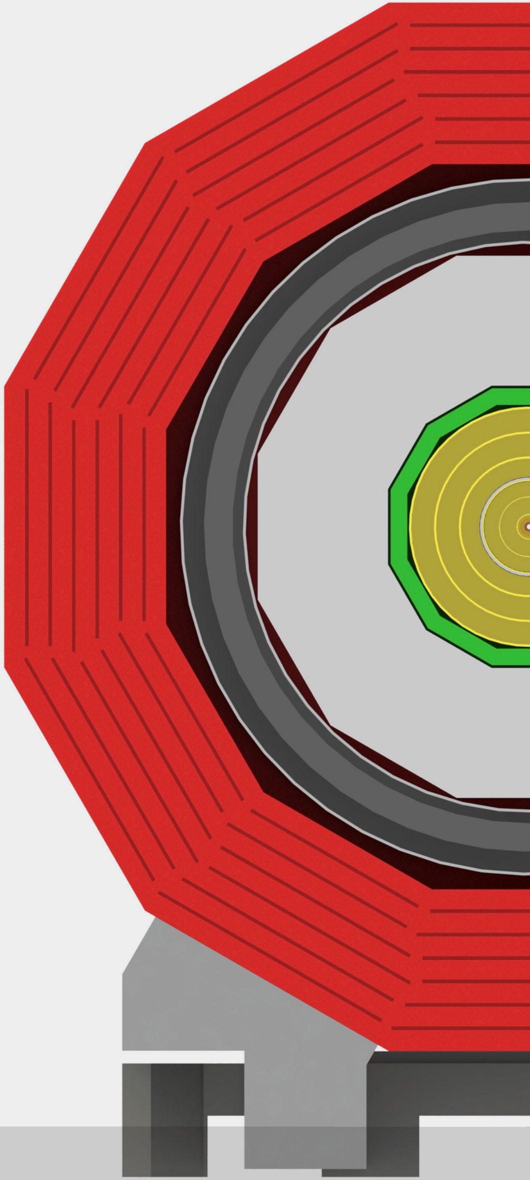
The Ultimate Silicon Sensor: A Detector-On-Chip System



The Question Is What Is The Question

Scooter, 2009

Requirements Differ…



The Landscape of Future Colliders & Upgrades

European Strategy Update

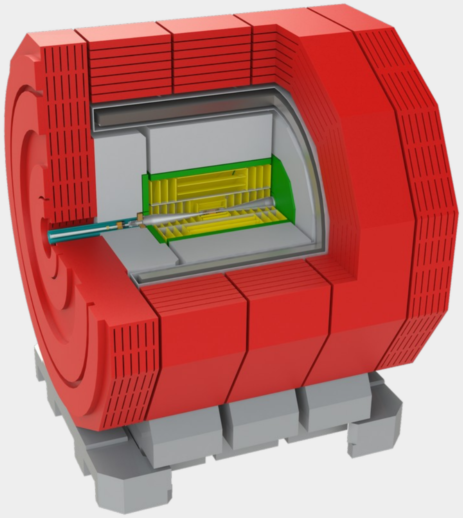
- European Strategy Update evaluated possible directions for particle physics
- ECFA published Detector R&D Roadmap to structure development of detectors & technology
  ECFA, 2021
- Higgs boson plays unique role in extending knowledge
  - Address questions within SM, provide sensitivity to new physics
  - Precision measurements required

Next collider: Lepton machine!
"Ultimate ultimate sensor":
Everything plus rad. hardness
for Hadron machine (far future)

< 2030	2030-2035	2035-2040	2040-2045	> 2045
SPS fixed target, Other fixed target, Belle II, ALICE LS3, PIP-II/LBNF/DUNE	ALICE 3, LHCb (≥ LS4), EIC, LHeC	ILC	FCC-ee, CLIC	FCC-hh, FCC-eh, Muon Collider

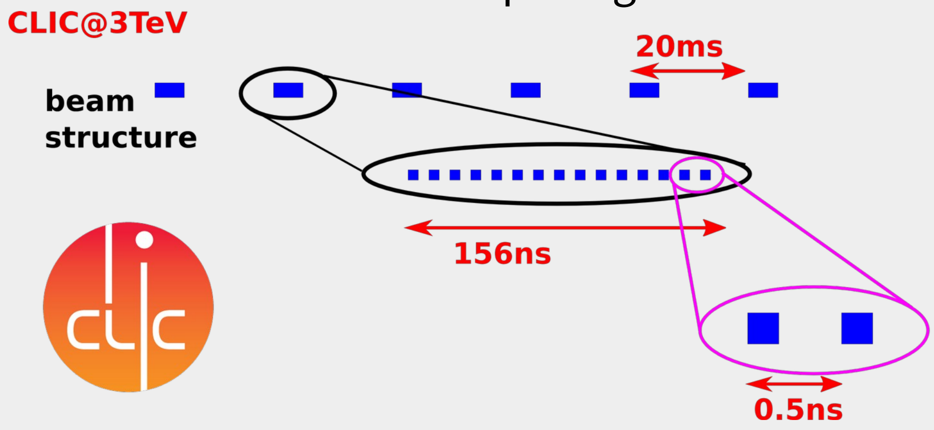
ECFA Detector R&D Roadmap

Challenges at Linear Colliders

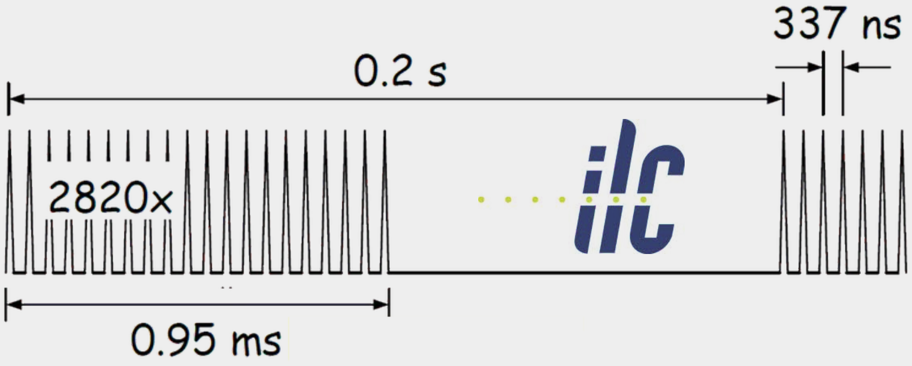


- High precision, low material, radiation hardness less of an issue
- Adjustable cms energies – emphasis on different components
- LC operate in bunch trains with low duty cycle:
  trigger-less, frame-based readout architecture possible

CLIC: 312 bunches **(156 ns)**, 50 Hz rep. rate
0.5 ns bunch spacing



ILC: 2820 bunches **(~1 ms)**, 5 Hz repetition rate
337 ns bunch spacing

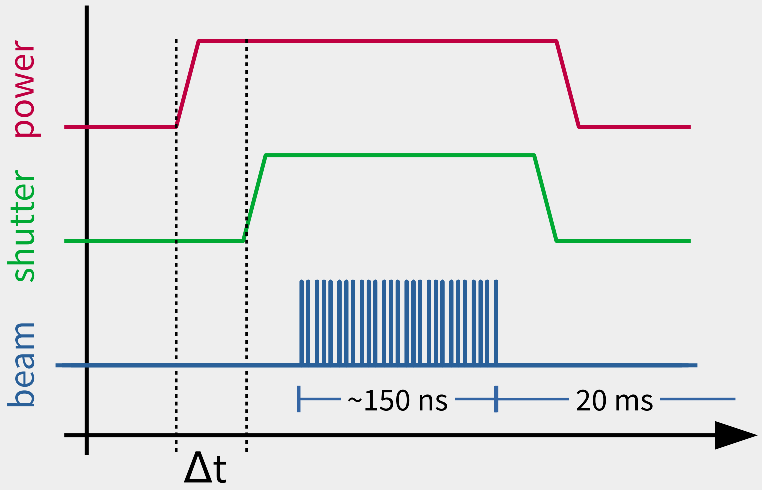


Linear Colliders: Power Pulsing

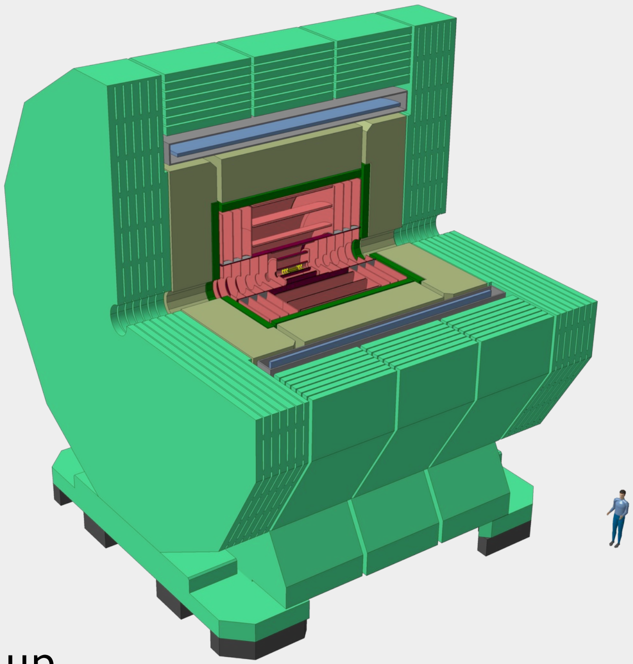
- LC have very low duty cycle, for CLIC < 0.01 ‰

- Save power by switching to lower-power idle state between bunch trains
  - **Analog power pulsing**: Multiplex DACs of amplifiers, discriminators between ON and OFF state
  - **Digital power pulsing**: e.g. by gating clock to pixel matrix

- Allows to significantly reduce overall heat dissipation, reduce requirements on cooling capacity, material, …



Challenges at Circular Lepton Colliders



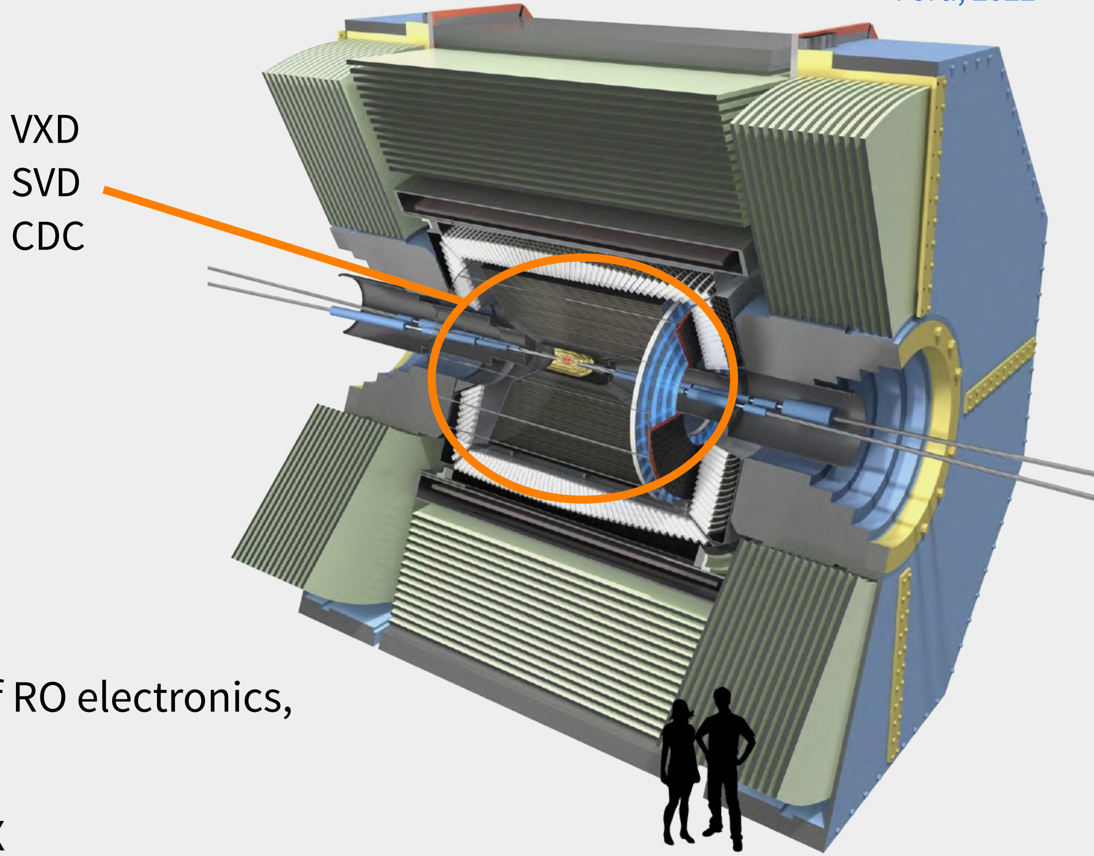
Precision requirements similar to linear colliders, however…

- Continuous beams (no bunch trains); bunch spacing down to 20 ns
- Power management and cooling (no power pulsing)
- Physics events at up to 100 kHz
  - Fast detector response ($\lesssim 1\ \mu s$) to minimize dead-time and pile-up
  - Strong requirements on front-end electronics and DAQ systems
- At the same time: low material budget! Minimize electronics, cables, cooling, …

Belle II Upgrades

- Currently luminosity limited by
  - beam-beam effects,
  - Beam lifetime,
  - injection backgrounds
- Upgrade detectors for
  - better resilience against backgrounds,
  - improved performance
- Many Upgrade ideas currently discussed:
  - ”adiabatic improvements”, replacement of RO electronics, entirely new sub-detectors, …
  - Upgrade proposals with MAPS, e.g. OBELIX

Forti, 2022



Silicon Detector Requirements at Lepton Colliders

- Precision measurements especially demanding on vertex & tracking detectors
  - Momentum resolution – large lever arm, minimum scattering
  - Impact parameter resolution – high resolution, min. scattering, small radii
  - Time resolution – fast sensor response, large S/N

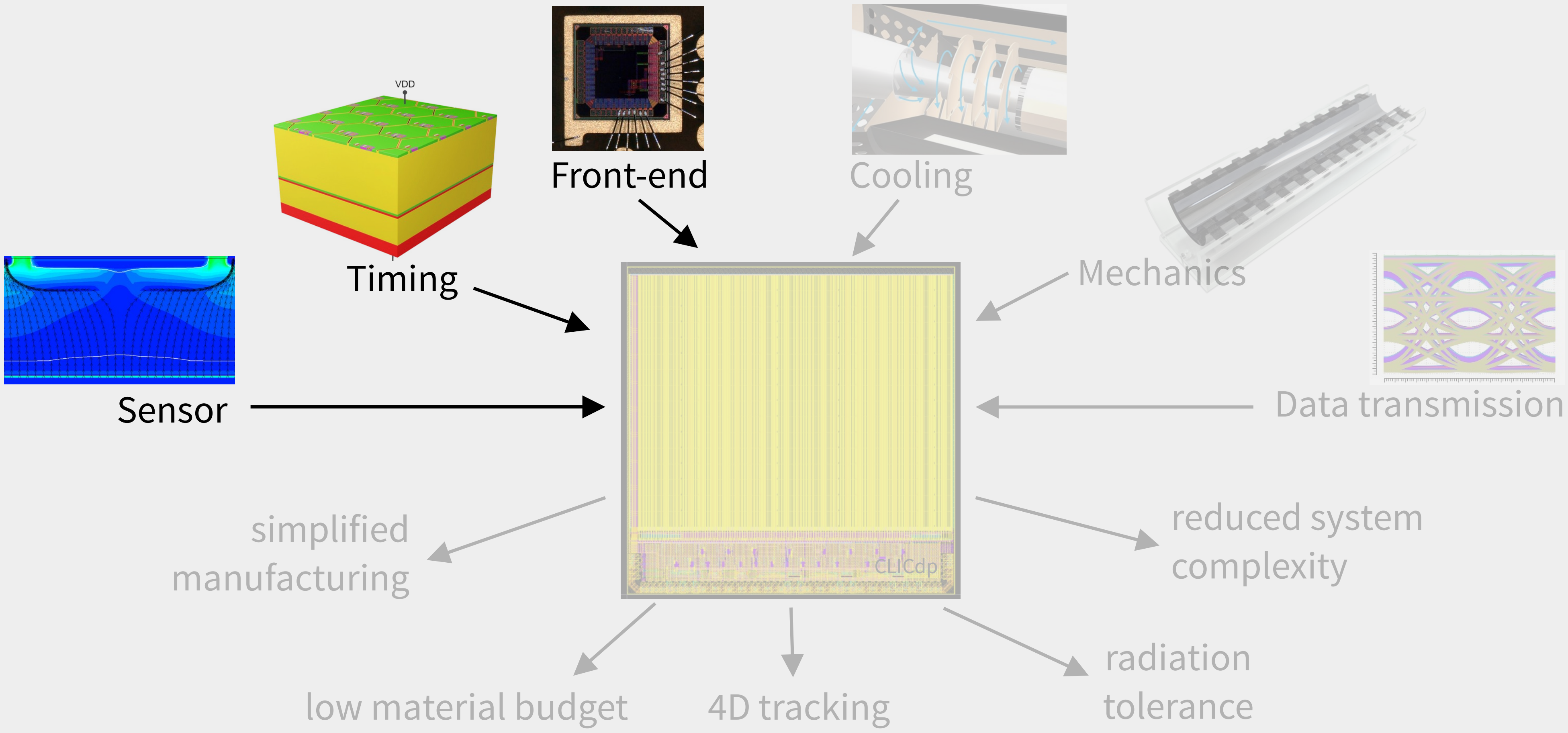
	Lepton Colliders		(HL-) LHC (ATLAS/CMS)
Material budget	$< 1\% X_0$		$10\% X_0$
Single-point resolution	≤ 3 µm		~ 15µm
Time resolution	~ ps – ns		25ns
Granularity	≤ 25 µm x 25 µm		50µm x 50µm
Radiation tolerance	$< 10^{11}\ n_{eq} / cm^2$		**$O(10^{16}\ n_{eq} / cm^2)$**
Duty cycle	< 0.01 ‰ @ ~ms (linear)	100 % @ ~ns (circular)	100 % @ 25ns

Opportunities in Small-Scale Experiments

- Many non-accelerator (or small accelerator) based experiments planned
- Several will require silicon detectors (e.g. LUXE)
- Requirements differ significantly, no funding for dedicated R&D

ECFA Detector R&D Roadmap

The Ultimate Silicon Sensor: A Detector-On-Chip System



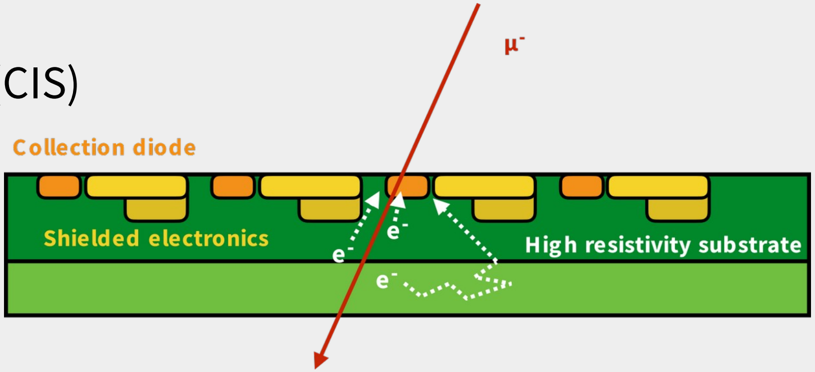
And No Matches

Scooter, 2013

New Technologies for the “Ultimate” Sensor

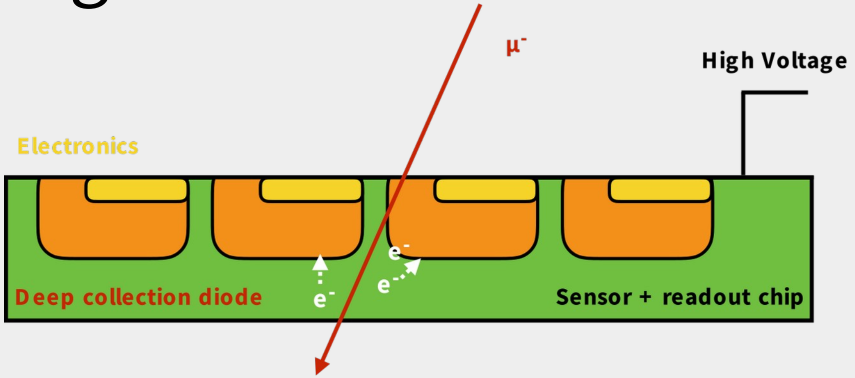
Monolithic Active Pixel Sensors

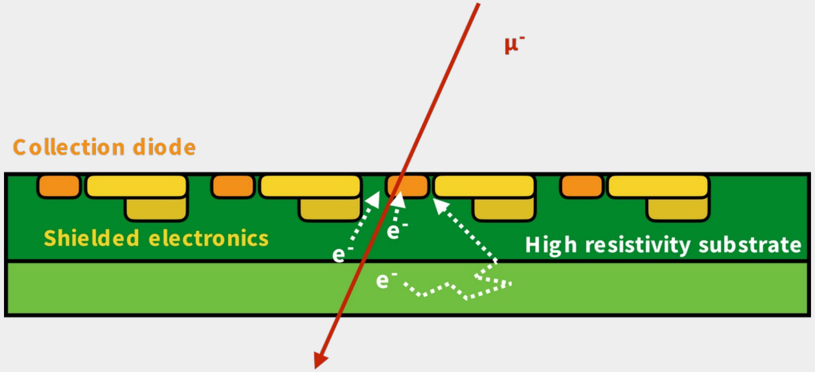
- Electronics & sensor in the same wafer
  - Produced in commercial CMOS imaging processes (CIS)
  - Fully integrated:
    amplification, discrimination & readout
  - Shield electronics via additional implants



- Large-scale manufacturing simplified compared to hybrids
  - No bump bonding required
  - No limitation on minimum pitch size
- Design can be very intricate
  - Sensor: electric field complex
  - ASIC design, process limitations, …
- Different approaches
  - Deep collection diode surrounding electronics
  - Separate shielding & collection diode

Large & Small Electrode Designs





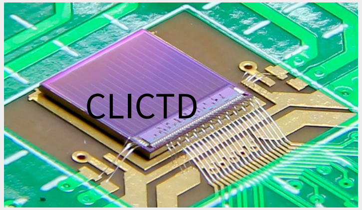
- Shield electronics via deep collection diode around electronics
  - Allows high bias voltage to be applied
  - Fast & large signal, large depletion volume
- Challenge: large collection diode leads to
  - large input capacitance
  - increased power consumption

- Electronics outside charge-collection well
  - Requires high-resistivity material (e.g. epitaxial layer) to allow depletion
  - Small collection diode leads to small capacitance
- Challenge: effect of p-well potential on electric field / charge collection

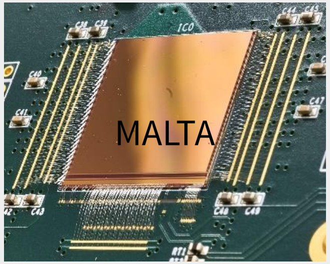
Many Technologies, Many Chips

- Started with 350nm process, now at 180nm – 130nm technologies
- Many successful chips designed & produced over last few years
  - First large-area detectors built in HEP
  - Many spin-offs for applications outside HEP (medical, space)
- So far: no single prototype satisfies *all* requirements!

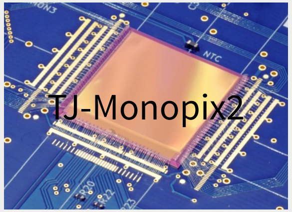
Kremastiotis et al., 2020



Pernegger et al., 2021



Bespin, 2023

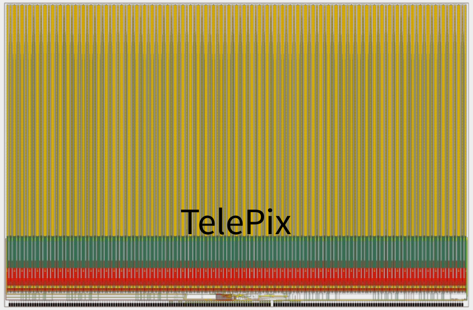


IPHC, 2021

List by no means exhaustive, chips not to scale…

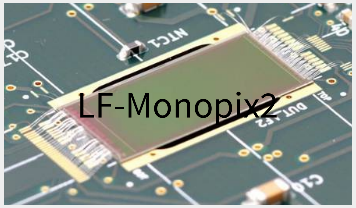
Augustin et al, 2020

Augustin et al., 2022

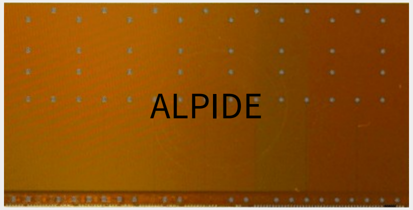


Schimassek, 2021

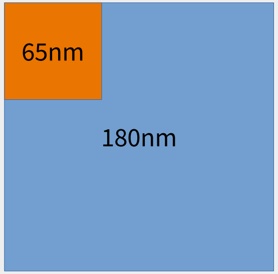
Dingfelder et al., 2022



Mager et al., 2016

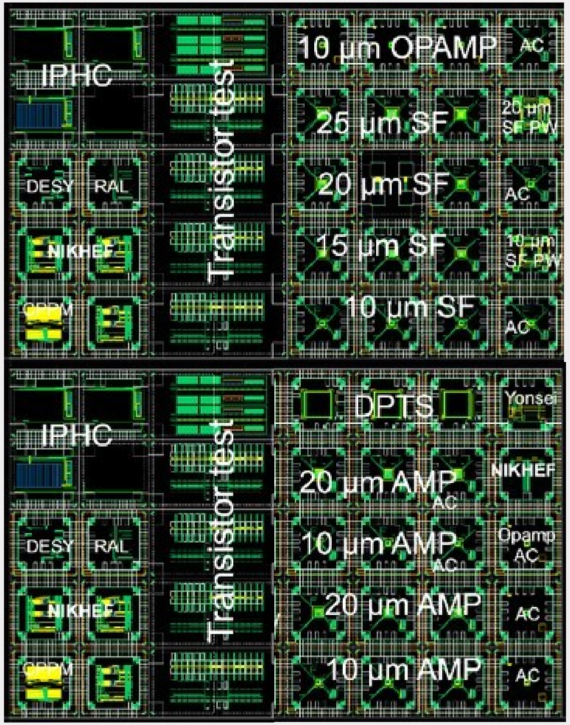


65nm CMOS Imaging Technology Node



- MAPS design in 65 nm CMOS imaging process – first application in HEP
  - Higher logic density → reduced pixel pitch
  - Lower analog/digital power consumption
  - Large 300 mm wafers

MLR1 reticle

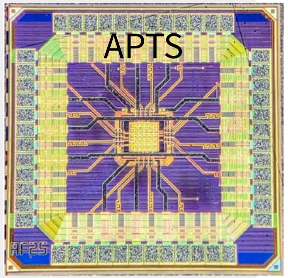


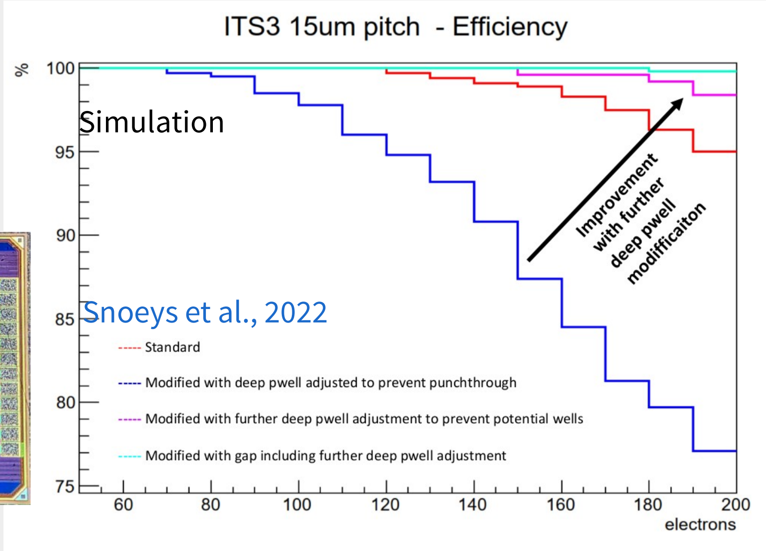
- International collaboration for common submissions to foundry, organized through CERN EP R&D programme

- Goal: explore new technology in terms of
  - Scalability - wafer-scale sensors through stitching
  - Timing resolution - through sensor layout optimization
  - Position resolution - through increased granularity

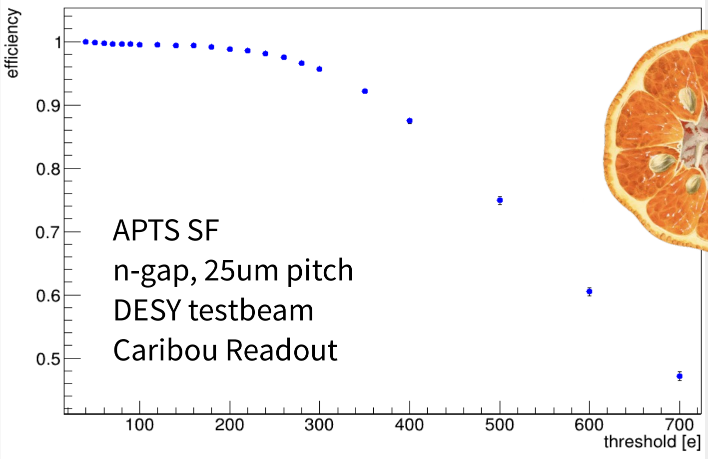
(Some) Results from First Submission

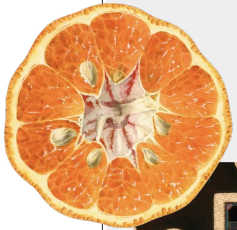
- Many test chips for pixel characterization & front-ends: APTS, DPTS, CE65, DMLR1
  - Enormous effort from many groups to characterize different pitches, front-ends
  - Validation of process modifications in 65nm

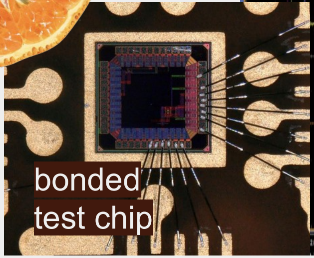


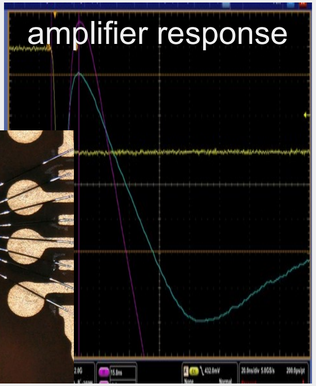


- "Tangerine" – Helmholtz Innovation Pool project for next-generation silicon detectors
  - Focus: fast pixel front-end (ns timing, with ToT and ToA)
  - Sensor charact. with APTS chip
  - Sensor simulations with TCAD & Allpix² MC





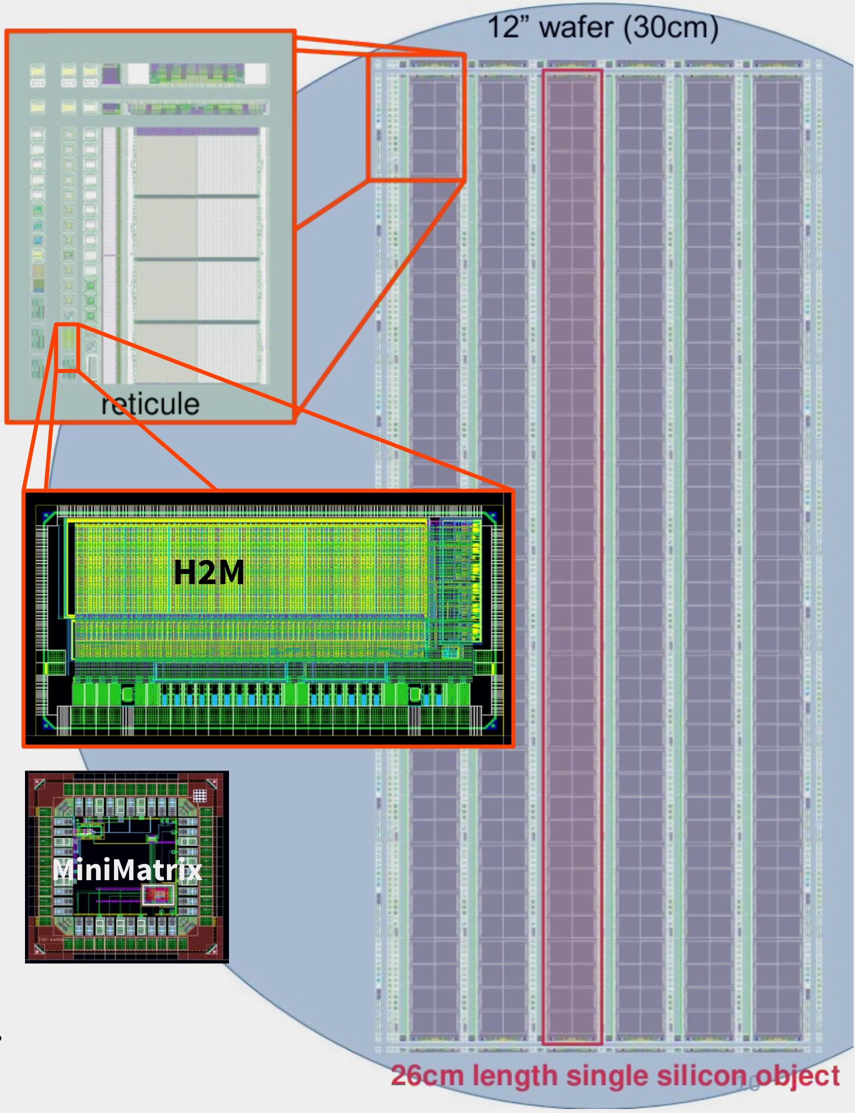




Second Submission Taped Out

- ALICE ITS3: wafer-scale stitched sensor MOSS
  - Learn stitching, yield, defects masking
  - Study power schemes, leakage, spread, noise, speed
- H2M – Hybrid to Monolithic (DESY, CERN, IFAE)
  - Full-matrix chip following digital-on-top design
  - Port full hybrid feature set to monolithic chip
  - Timepix-like architecture, different modes (ToT, ToA, …)

- Expected back from foundry end of April 2023
- This isn't the end – have not yet found the holy grail:
  Analog circuitry doesn't scale, very thin active region, …



Break It Up

Scooter, 2009

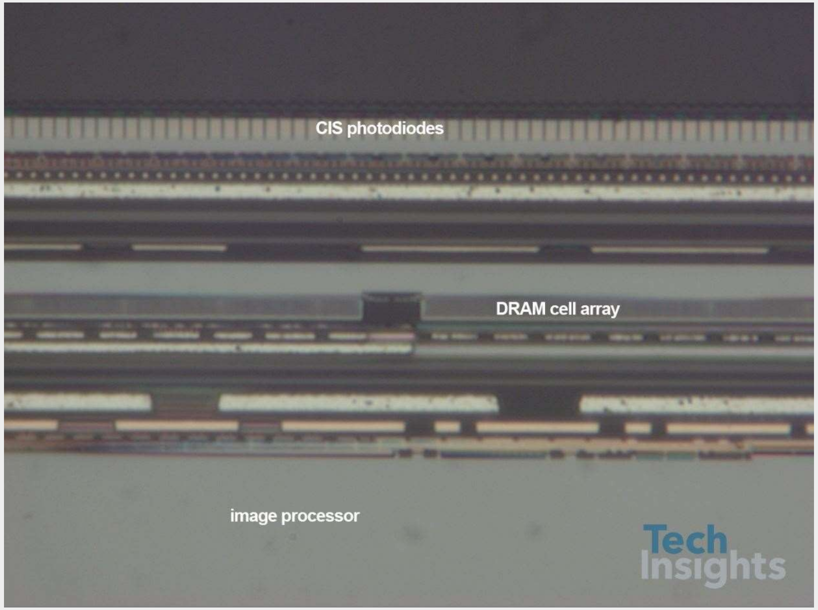
- 3D Integration / Wafer-Wafer Bonding
- Hybrid approach to separate functionality:
  - CIS process: sensor & amplifier
  - CMOS process: digital logic, readout
- Bonding & thinning at wafer level can be expensive for prototyping
- Popular in industry, e.g.
  - Sony IMX400 for Cell Phones
    20 Million 1.22-μm Pixel @ max. 1 kfps
- More flexibility on digital circuitry, but might come with higher power dissipation

Sony, 2017

90-nm 1Al5Cu
BI-CIS (2.6 μm)

30-nm 1W3Al
DRAM (2.6 μm)

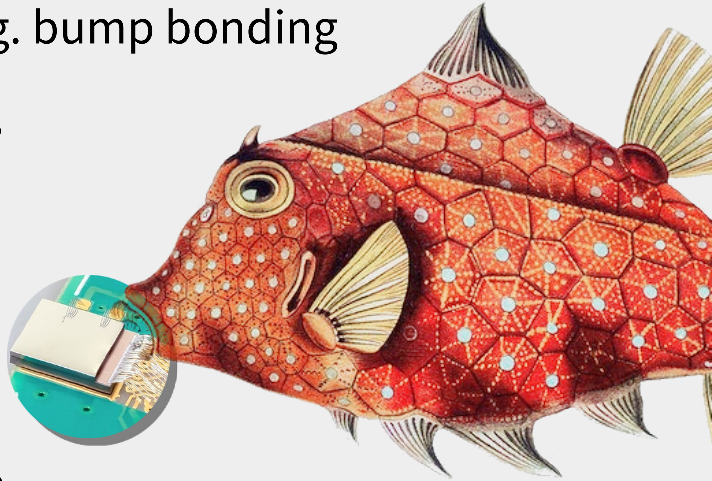
40-nm 1Al6Cu
Logic



How Much Is The ~~Fish~~ Submission?

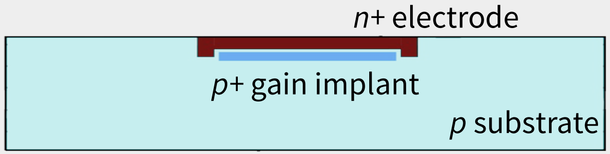
Scooter, 2013

- “CMOS sensors are cheap and production is scalable” – yes and no
  - Initial cost of small technology nodes very expensive (mask production, …)
  - Multi-project wafer runs (MPWs) not always available, prototypes require engineering runs
  - Scaling for final production indeed scales better than e.g. bump bonding
- Same issues of course also apply to CMOS readout ASICs

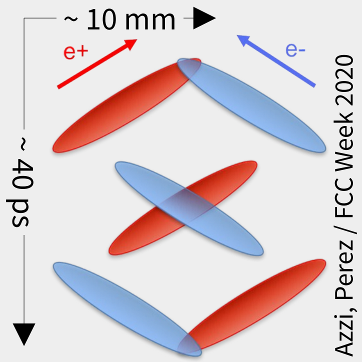


- General issue: single-vendor problem
  - Processes & designs specific to individual vendors
  - Also true for specialty foundries (LGADs, current sensors)

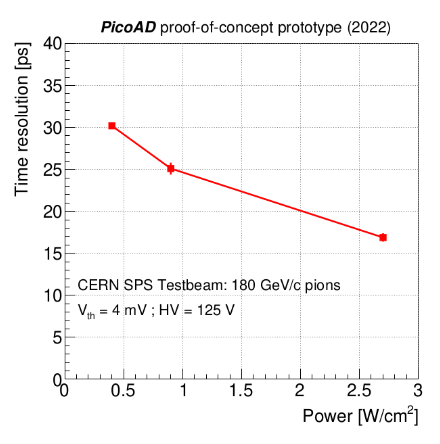
Picosecond Timing

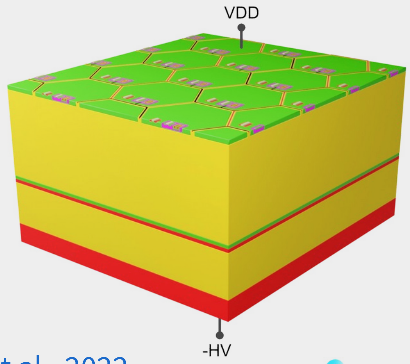


- Timing information for pile-up mitigation $\sigma_t \sim O(30\ ps)$
- PID for heavy flavor physics, CP violation, B physics $\sigma_t \sim O(30\ ps)$
- Chromatization: √s depends on longitudinal bunch pos. $\sigma_t \sim O(6\ ps)$



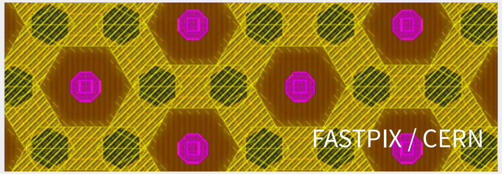
- Dedicated timing detectors with **LGAD sensors / UFSD**
  - Low gain (x10–30) → fast-rising pulse enables timing
  - Dedicated timing layers: additional material
  - Integration into MAPS detectors: 4D measurements





Kugathasan et al., 2020

ATTRACT FASTPIX



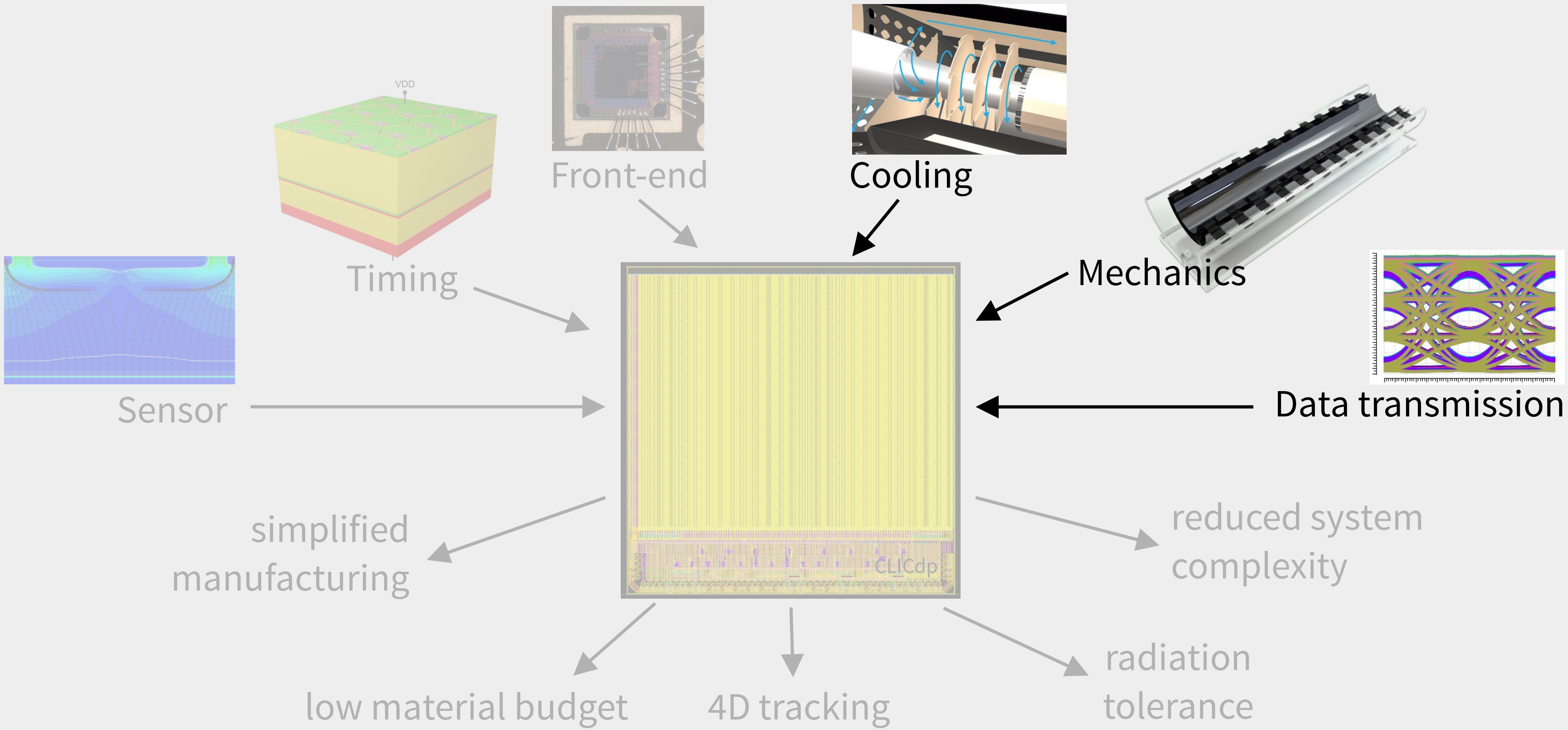
← 180nm commercial CMOS process

130nm BiCMOS, dedicated processing →

Iacobucci et al., 2022

MONOLITH

The Ultimate Silicon Sensor: A Detector-On-Chip System



Liquid Is Liquid

Scooter, 2019

Considerations for Cooling, Mechanics & Data Transmission

I Want You To Stream – Data Transmission

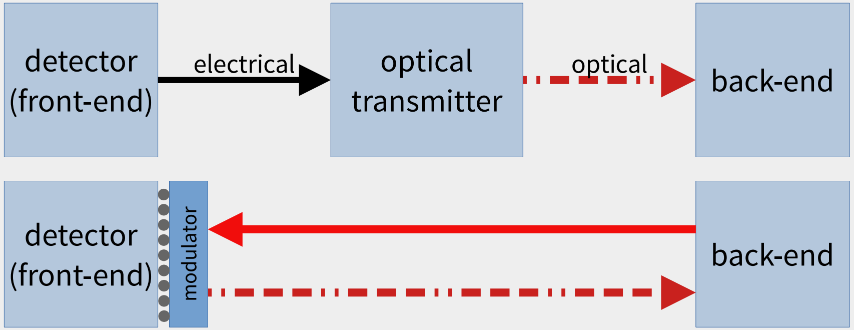
Scooter, 2020

- Bandwidth & power consumption of data transmission critical for future experiments:

$$\frac{1\,cm^2\,\text{chip area}}{(15\,\mu m)^2\,\text{pixel pitch}} \geq 450\,kPix \rightarrow 450\,kPix \cdot 20\,\text{bit} \cdot 10^{-5}\,\text{occupancy} \simeq 90\,b \rightarrow \frac{90\,\text{bit}}{20\,ns} \geqslant 4.5\,Gb\,s^{-1}\,cm^{-2}$$

- Currently: **Electrical transmission** off-chip, conversion by optical transmitters
  - Limited bandwidth *~ Gb/s*
  - Driving signals is power consuming *~ pJ/bit*
  - Additional material, electromagnetic interference, …

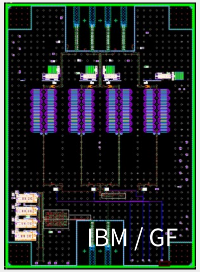
- **Silicon Photonics:** external laser, modulation on ASIC
  - Increased bandwidth *>> 10 Gb/s*
  - Energy efficient, only modulation *<< pJ/bit*
  - **3D integration with MAPS**



GLOBALFOUNDRIES

90 nm SOI CMOS

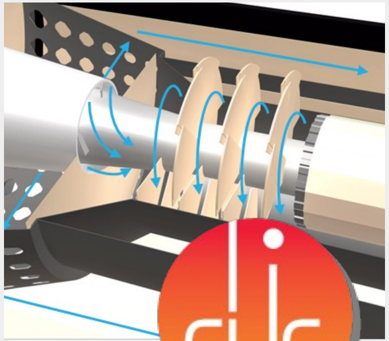
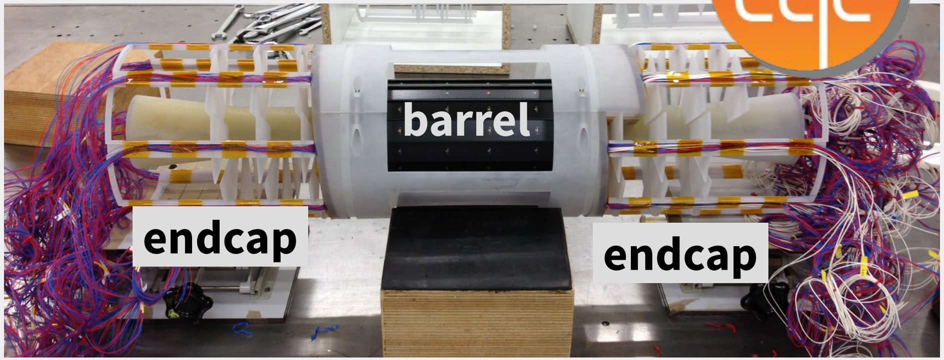
100 Gbps Transceiver (COTS)

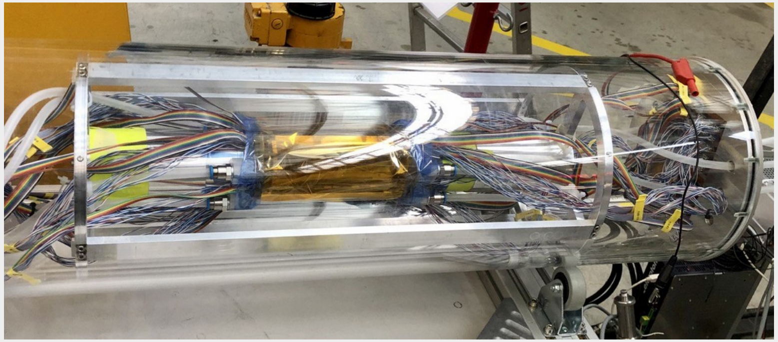


Forced Gas Flow Cooling

- To drastically reduce material budget, we need to avoid “active cooling”
  - Cooling with forced gas flow through tracking volume
  - Remove material for piping, coolant, thermal connectors, …
  - Demands reduction of heat dissipation

- Example: CLIC Vertex Detector
  - Cooled with forced air flow
  - Spiral vertex disks direct air
- Example: mu3e Detector
  - Cooled with helium flow



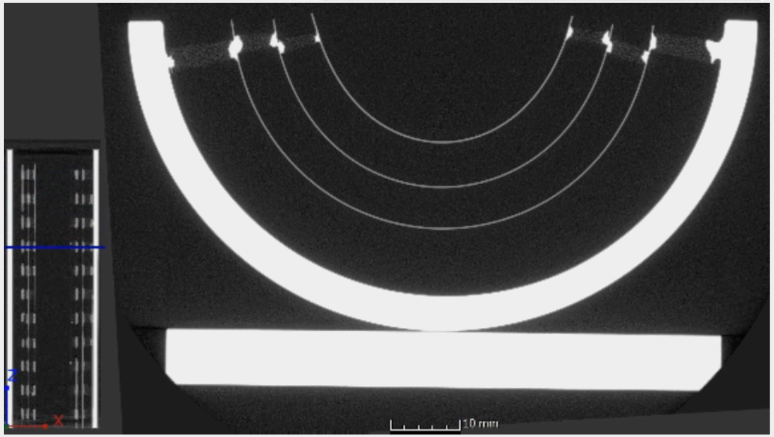
Mind The Gap – Fully-Active Detectors

Scooter, 2013

- "Remove everything that doesn't look like a sensor"
  - Below 50 µm thickness silicon becomes flexible
  - Bending wafers into cylinders adds stability
  - Building half-shells from full-wafer sensors

- ALICE started R&D effort for **ITS3 upgrade**
  - Monolithic CMOS pixel detectors
  - Wafers thinned & bent
  - Held in place by low-density carbon foam spacers

Šuljić, 2020



Neverending Story

Scooter, 2017

Summary

The Only One – The Ultimate Silicon Detector

Scooter, 2011

- The ultimate silicon sensor will be a **detector-on-chip system**.
- Requirements for **future lepton collider experiments** similar:
  - Very low material budget
  - High position & time resolution
- **Monolithic Active Pixel Sensors** matured in past years
  - Many new prototypes & full detectors
  - Move to smaller technology nodes on the way
  - Considerations for future developments: cost, 3D integration, timing
- Sensor is always **part of a system**
  - Data transmission – power reduction, bandwidth increase with silicon photonics
  - Cooling with forced gas flow to minimize material – power dissipation critical
- Far future: Radiation hardness – industry is developing processes for wide-bandgap semiconductors

Missing Powering Aspects?
Wait for the next talk… :-)

DESY.

Solid state	**DRDT 3.1**	Achieve full integration of sensing and microelectronics in monolithic CMOS pixel sensors
	DRDT 3.2	Develop solid state sensors with 4D-capabilities for tracking and calorimetry
	DRDT 3.3	Extend capabilities of solid state sensors to operate at extreme fluences
	DRDT 3.4	Develop full 3D-interconnection technologies for solid state devices in particle physics
Electronics	**DRDT 7.1**	Advance technologies to deal with greatly increased data density
	DRDT 7.2	Develop technologies for increased intelligence on the detector
	DRDT 7.3	Develop technologies in support of 4D- and 5D-techniques
	DRDT 7.4	Develop novel technologies to cope with extreme environments and required longevity
	DRDT 7.5	Evaluate and adapt to emerging electronics and data processing technologies
Integration	**DRDT 8.1**	Develop novel magnet systems
	DRDT 8.2	Develop improved technologies and systems for cooling
	DRDT 8.3	Adapt novel materials to achieve ultralight, stable and high precision mechanical structures. Develop Machine Detector Interfaces.
	DRDT 8.4	Adapt and advance state-of-the-art systems in monitoring including environmental, radiation and beam aspects