ATLAS Phase-2 Trigger Upgrade

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on behalf of the ATLAS TDAQ community

15th Terascale Detector Workshop

1-3 March 2023

ATLAS EXPERIMENT

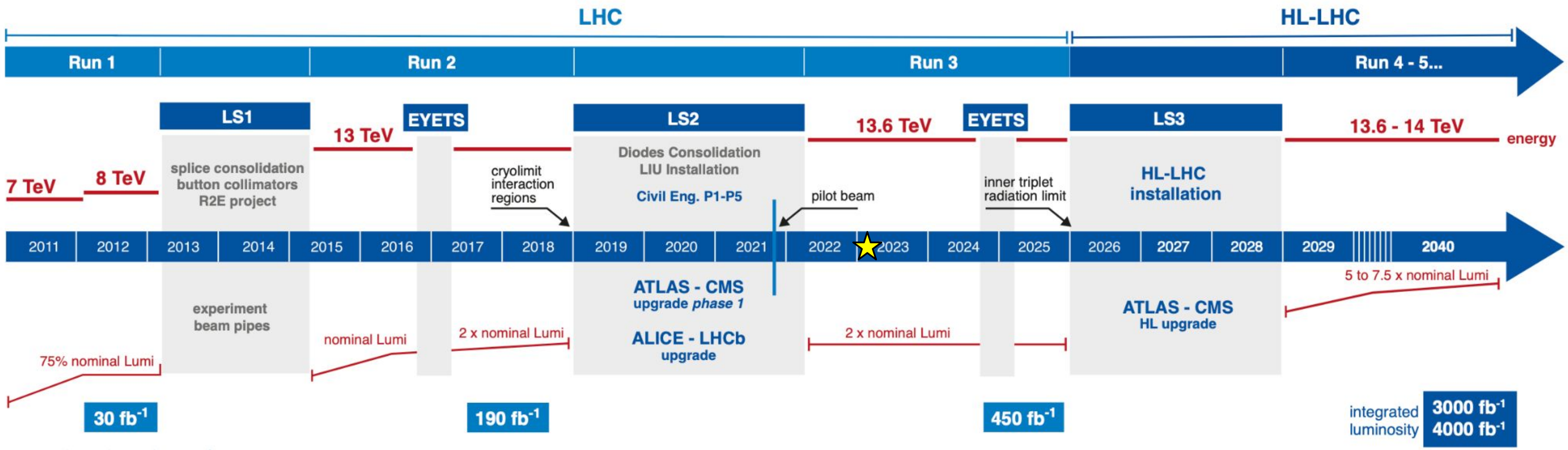
IFIC INSTITUT DE FÍSICA CORPUSCULAR

CSIC CONSEJO SUPERIOR DE INVESTIGACIONES CIENTÍFICAS

VNIVERSITAT DE VALÈNCIA

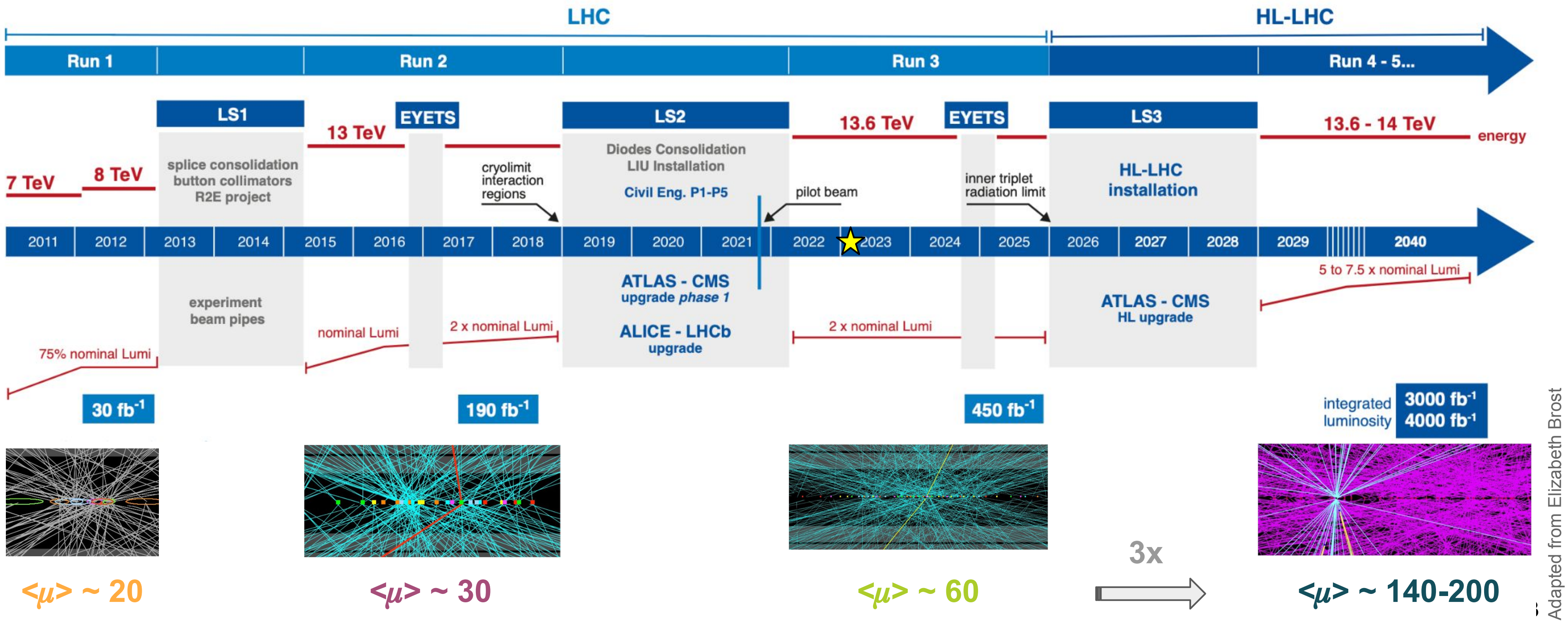
Present and Future of the LHC

- Exploring the ***energy frontier,*** only ~6% of the data acquired (180 out of 3000 fb^{-1})



Present and Future of the LHC

➢ Exploring the ***energy frontier,*** only ~6% of the data acquired (180 out of 3000 fb^{-1})



Run 3 (2022-2025)

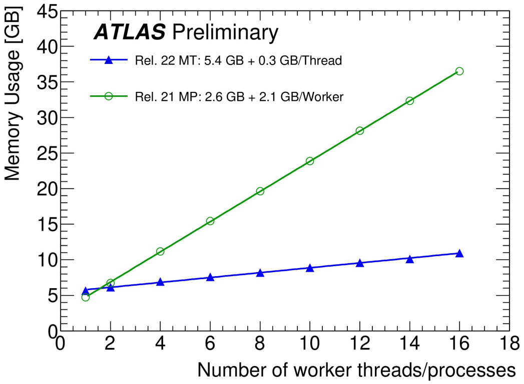
- Increase of the center-of-mass energy **13 TeV → 13.6 TeV**
- **The success of Run 3 and culmination of the Phase-I upgrades is fundamental** to pave the path for the HL-LHC

New hardware

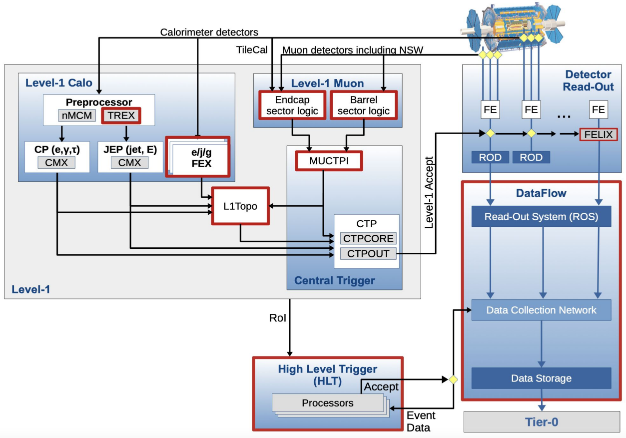
First major ATLAS renovation (*Phase-I upgrade*)

New software

Migration to a multithreaded software in preparation for HL-LHC



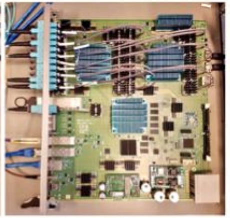
Completion of NSW-A on 28 May 2021



eFEX

jFEX

gFEX



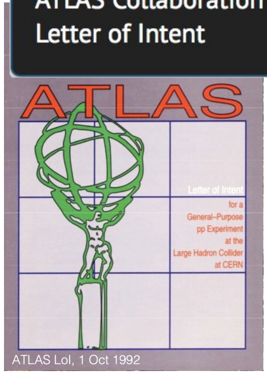
MUCTPI

L1Topo

The ATLAS Experiment reached 30 years

1992

1 OCTOBER 1992
ATLAS Collaboration publishes Letter of Intent



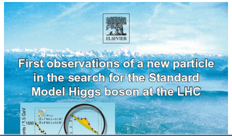
ATLAS LoI, 1 Oct 1992

15 DECEMBER 1994
Submission of Technical Proposal

4 JUNE 2003
ATLAS cavern inaugurated

20 NOVEMBER 2006
World's largest superconducting magnet switches on

30 MARCH 2010
First LHC collisions at 7 TeV



4 JULY 2012
ATLAS and CMS observe a particle consistent with the Higgs boson

years of discovery – 1992-2022
ATLAS EXPERIMENT

1 OCTOBER 2022

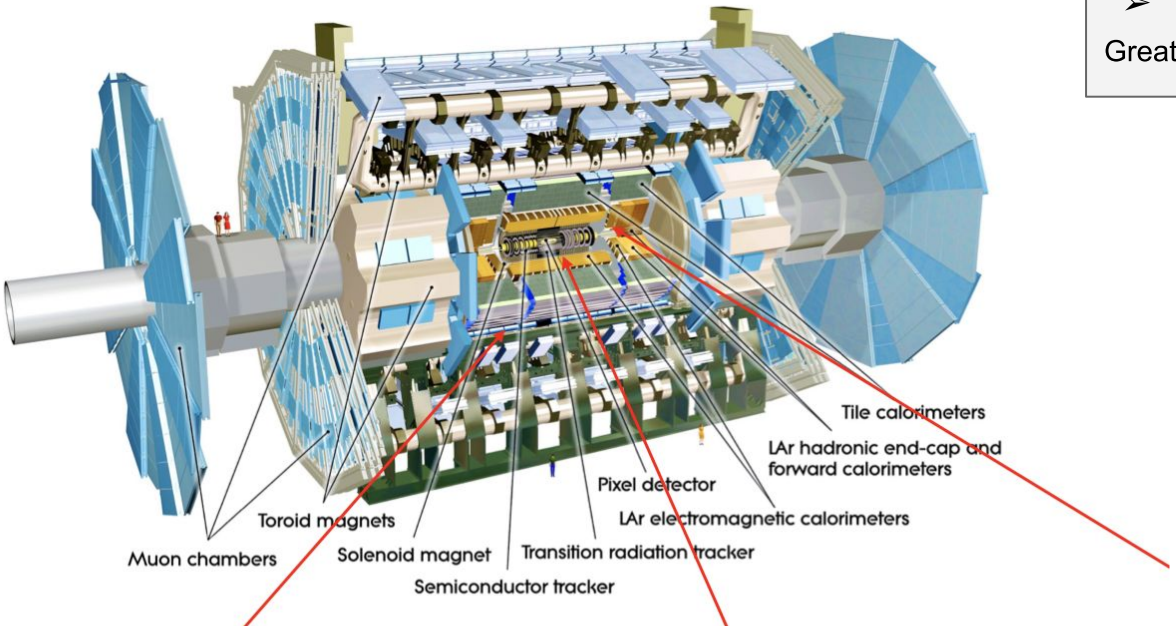
Data-taking to continue until 2035

ATLAS Phase-II Upgrade for the HL-LHC

ATLAS was designed 30 years ago and needs a major upgrade to face the HL-LHC conditions

Ambitious upgrade program ("new detector"):
- ➢ Unprecedented luminosity $7.5 \times 10^{34}\ cm^{-2}s^{-1}$
- ➢ harsh environment ~200 collisions (*pileup*)

Great challenge, cutting edge technology



Upgraded Trigger and Data Acquisition (TDAQ) System

Level-0 rate ~ 1 MHz (100 kHz in Run 3)

Event Filter rate ~ 10 kHz (1 kHz in Run 3)

Upgraded electronics

Liquid Argon calorimeter
Tile calorimeter
Muon spectrometer

High Granularity Timing Detector (HGTD)

Forward region ($2.4 < |\eta| < 4.0$)

New muon chambers

New Inner Tracker (ITk)
(all silicon, $|\eta| < 2.5 \rightarrow |\eta| < 4.0$)

ATLAS Review Process

https://twiki.cern.ch/twiki/bin/view/AtlasPublic/AtlasTechnicalDesignReports

2013 TDR TDAQ Phase-I upgrade (ATLAS-TDR-023, CERN-LHCC-2013-018)

2017 TDR TDAQ Phase-II upgrade (ATLAS-TDR-029, CERN-LHCC-2017-020)

2022 TDR TDAQ Phase-II upgrade - Event Filter Tracking Amendment (ATLAS-TDR-029-ADD-1, CERN-LHCC-2022-004)

Mandatory milestones:

- SPR: Reviews the specifications of (a) deliverable(s) so as to ensure that all requirements will be considered in the design phase.
- PDR: Reviews the design of the deliverable(s) during the prototyping phase.
- FDR: Reviews the final design of the deliverable(s) after a successful prototyping and testing stage and prior to the pre-production phase.
- PRR: Reviews the production readiness of the deliverable(s), as demonstrated through the pre-production phase.
- IRR: Reviews the readiness of the deliverables to be installed.

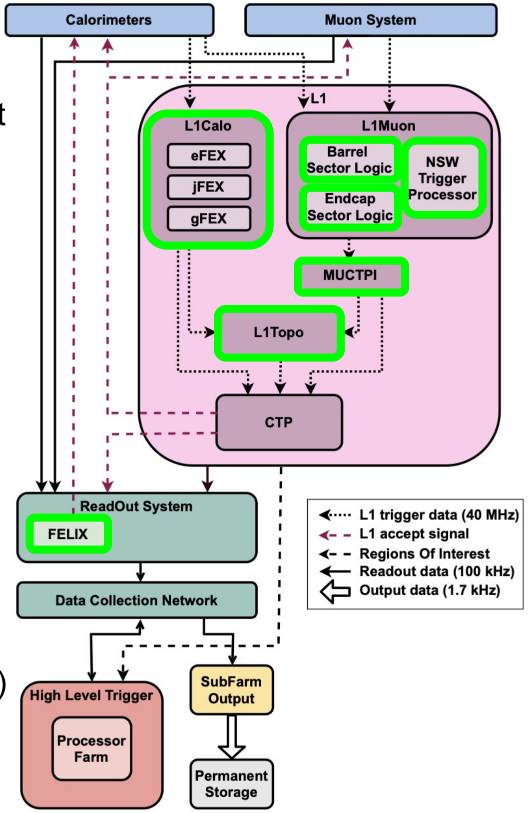
ATLAS TDAQ Upgrade in a nutshell

Run 3 (2022-2025)

Technical Design Report
ATLAS TDAQ system
Phase-I upgrades
ATLAS-TDR-023
CERN-LHCC-2013-018

L1 trigger
40 MHz → 100 kHz

High Level Trigger (HLT)
100 kHz → 1.7 kHz



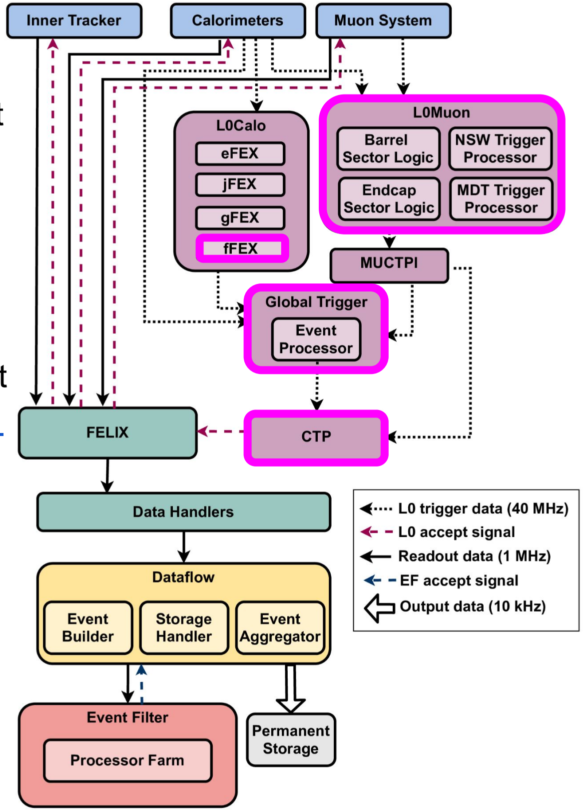
HL-LHC (2029-2040)

Technical Design Report
ATLAS TDAQ system
Phase-II upgrades
ATLAS-TDR-029
CERN-LHCC-2017-020

EF Tracking Amendment
ATLAS-TDR-029-ADD-1
CERN-LHCC-2022-004

L0 trigger
40 MHz → 1 MHz

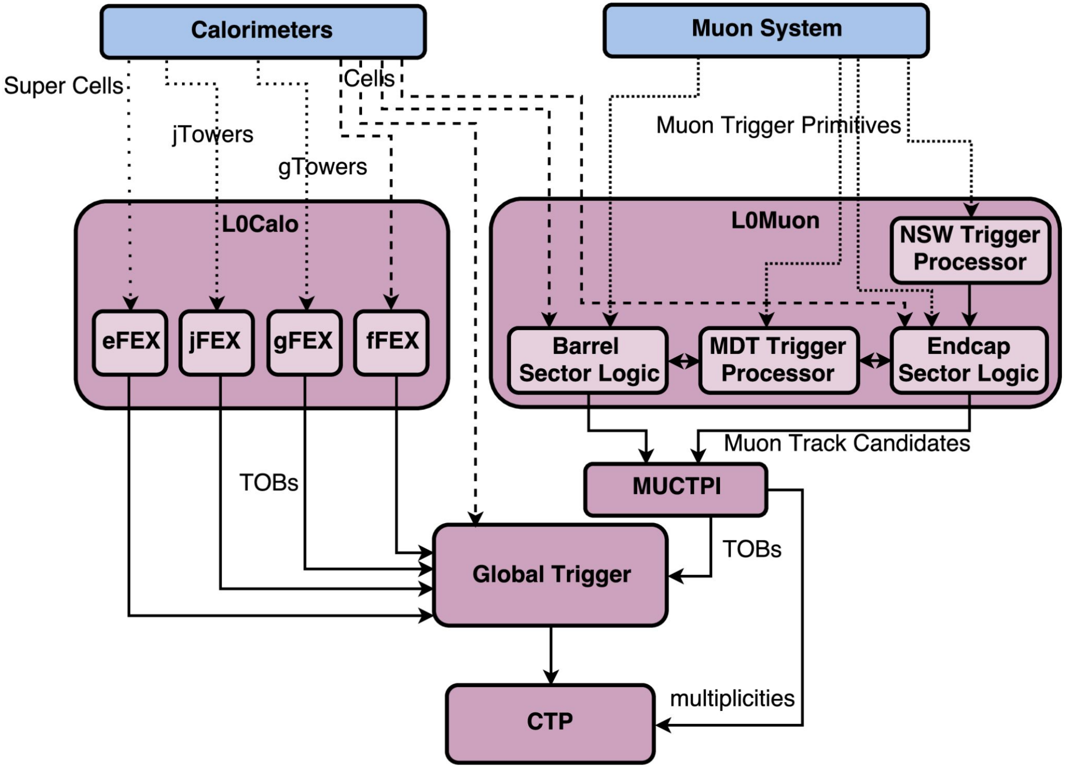
Event Filter (EF)
1 MHz → 10 kHz



ATLAS Level-0 Trigger System

Level-0 Trigger subsystems:

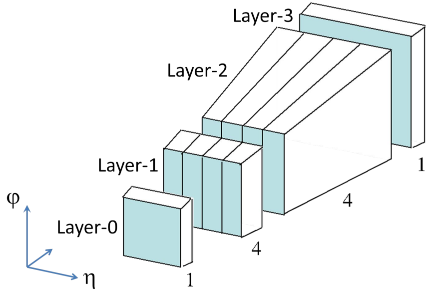
- **L0Calo**:
  LAr and Tile calorimeter data with coarse granularity sent to FPGA based Feature Extractors (FEXs) to build Trigger Objects (TOBS): electron, photon, tau, jets, $E_{T,miss}$
- **L0Muon**:
  muon candidates are formed in the barrel and endcap, with new processors for the NSW and MDT
- **Global Trigger**:
  runs full granularity offline-like reconstruction
- **Central Trigger**:
  MUCTPI combines muon candidates from barrel and endcap
  CTP makes final L0 decision

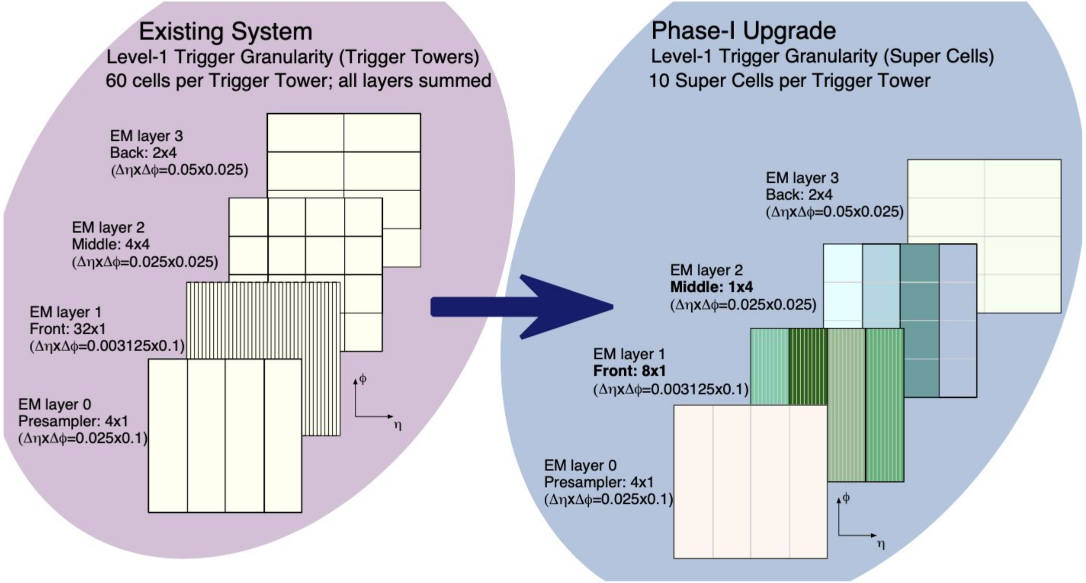


ATLAS Level-1 Calorimeter Trigger

Phase-I LAr upgrade (CERN-LHCC-2013-017):

- Finer granularity LAr digital signal to L1Calo:
  - Run 2: 0.1 x 0.1 trigger tower (60 cells)
  - Run 3: 10 E_T values from "1-4-4-1" samples (SuperCells) per trigger tower
- Better resolution and background rejection



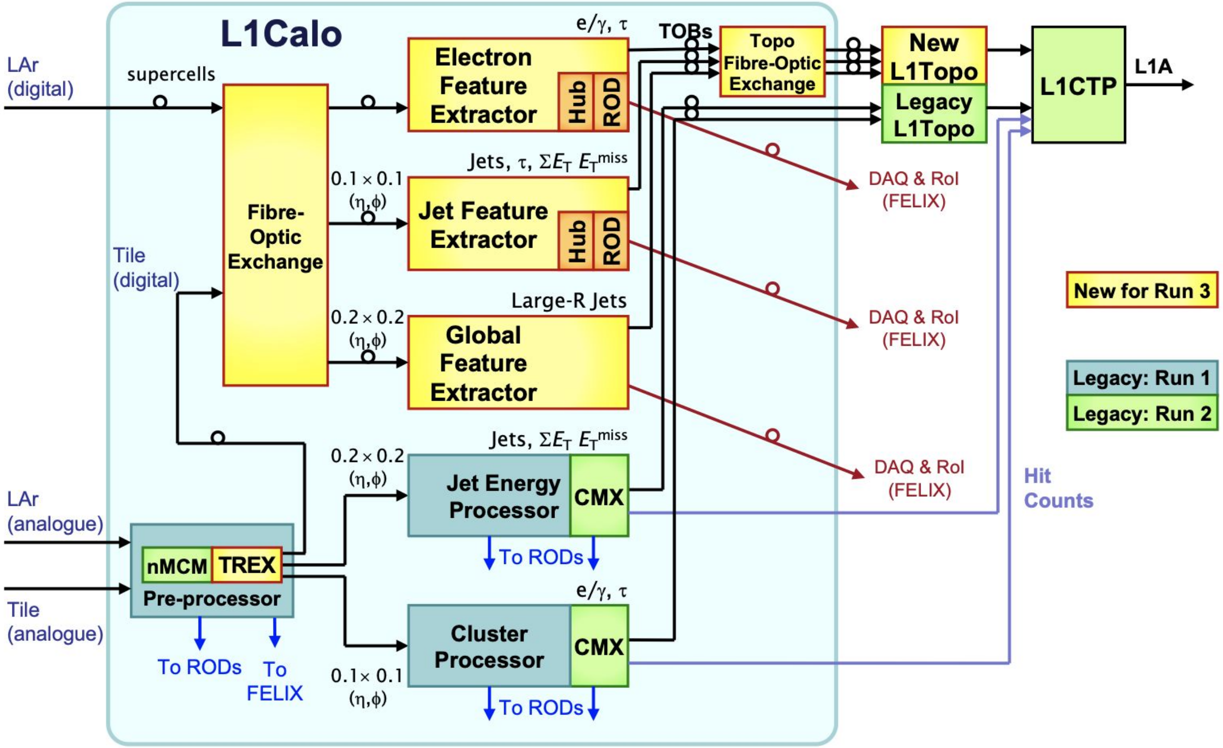


ATLAS Level-1 Calorimeter Trigger

Phase-I L1Calo upgrade:

- **FOX (Fibre Optic Exchange)**
  optical exchange networks to rearrange the data in suitable order for the FEX processors
- **TREX (Tile Rear Extension)**
  digitizes analogue signals from Tile for the FEX processors
- **e/j/gFEX (electron/jet/global Feature EXtractors)**
  new custom electronic boards with FPGA technology
- **New L1Topo**
  Multiplicity and topological selections (increases number of L1Calo triggers thresholds)

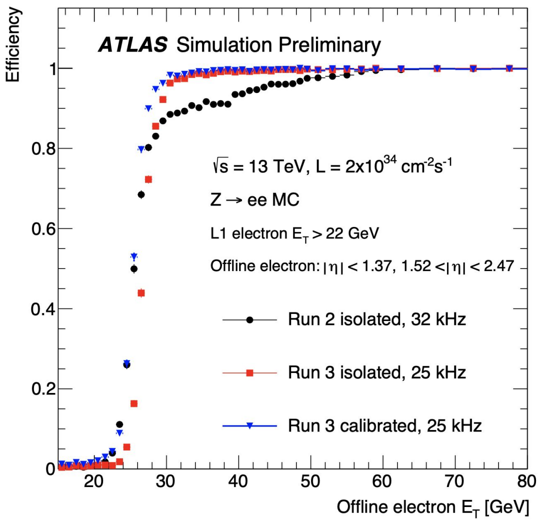
Legacy system running in parallel during the Run 3 commissioning

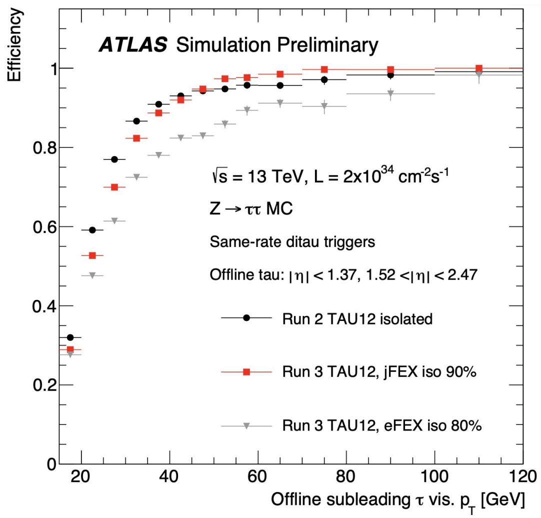


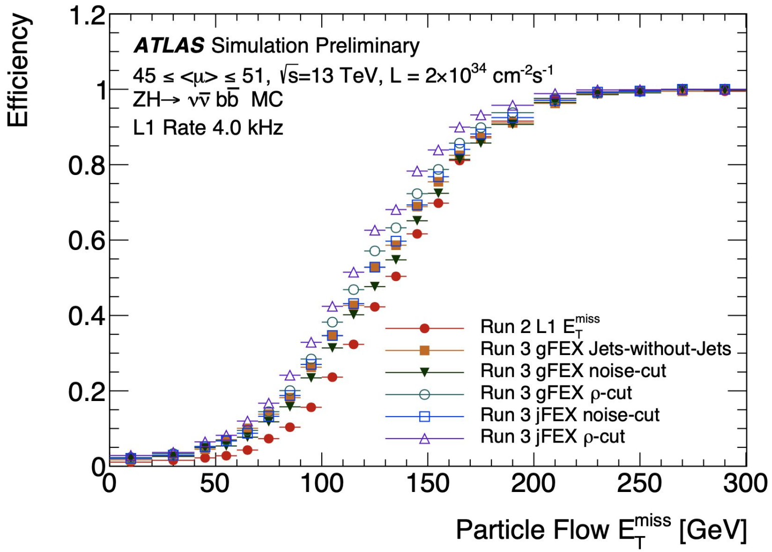
ATLAS Level-1 Calorimeter Trigger

Phase-I L1Calo performance improvements for Run 3:

- **L1 EM trigger (eFEX):** sharper turn-on curve and 20% rate reduction with respect to the legacy Run 2 trigger by applying more sophisticated jet discriminant cuts (R_η, R_{had}, w_{stot}) using the higher LAr calorimeter granularity
- **L1 TAU trigger (eFEX, jFEX):** isolation requirement on jFEX matches Run 2 ditau trigger performance
- **L1 MET trigger (jFEX, gFEX):** various algorithms proposed, outperforming the legacy Run 2 trigger for same rate



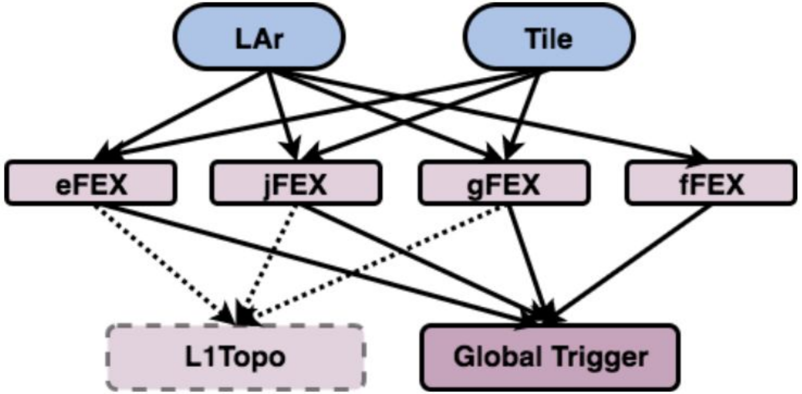




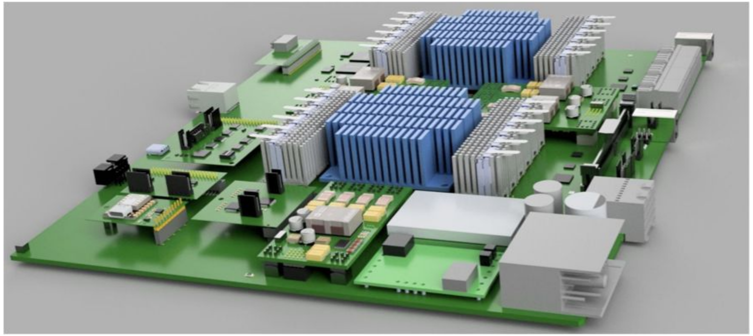
ATLAS Level-0 Calorimeter Trigger

Phase-II L0Calo upgrade:

- Based on the Phase-I L1Calo Trigger installed during LS2
- Various hardware, firmware and software modifications needed for Run 4
- Performance will be enhanced by an additional processing system, **forward FEX (fFEX)**, to reconstruct forward electrons and jets



Forward FEX

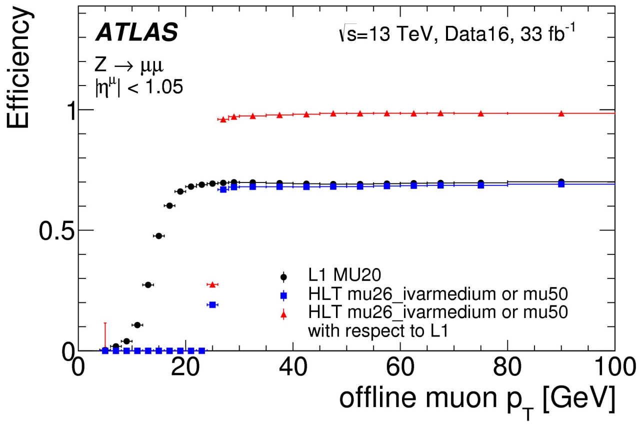


ATLAS Muon Trigger Upgrade

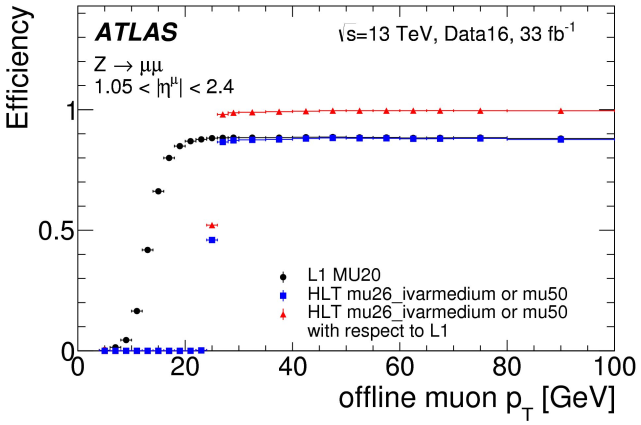
Main goals:

- Upgrade electronics to cope with the latencies and rates of the trigger for the HL-LHC (original system with maximum latency of 6.4 μs in barrel and 3.2 μs in endcap, maximum rate of 100 kHz)
- Improve acceptance x efficiency and momentum resolution
- Suppress fake triggers with more coincidences especially in the endcaps

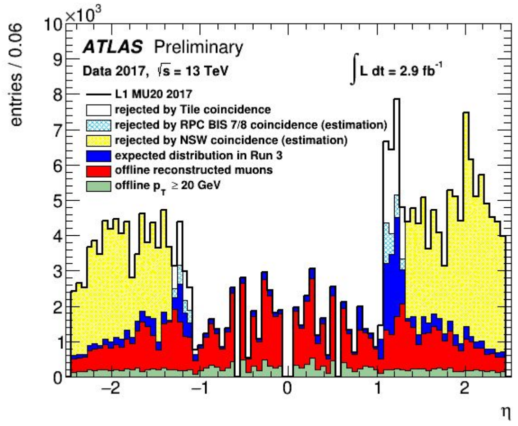
70% in the barrel



90% in the endcap



Endcap dominated by fakes



ATLAS Muon Trigger Upgrade

ATLAS Original & Phase-0
Run 1 & 2

Level-1 Muon Trigger System

Triggering:

- **Resistive Plate Chambers (RPC)**
  (barrel, $|\eta| < 1.05$)
- **Thin Gap Chambers (TGC)**
  (endcap, $1.05 < |\eta| < 2.4$)

Readout:

- **Monitored Drift Tube (MDT)**
  (barrel+endcap, $|\eta| < 2.7$)
- **Cathode Strip Chambers (CSC)**
  (endcap, $2.0 < |\eta| < 2.7$)

ATLAS Phase-I
Run 3

Level-1 Muon Trigger System

Upgrades:

- **New Small Wheel (NSW)**
  (endcap, $1.3 < |\eta| < 2.7$)
  Maximum latency: 60 μs
  Maximum rate: 1 MHz
  Micromegas and small-strip TGCs replaces Small Wheel (CSC, MDT)
- **RPC BIS78**
  (endcap, $1.0 < |\eta| < 1.3$)
  RPC for triggering & small-diameter MDT (sMDT) for readout

ATLAS Phase-II
HL-LHC

Level-0 Muon Trigger System

Upgrades:

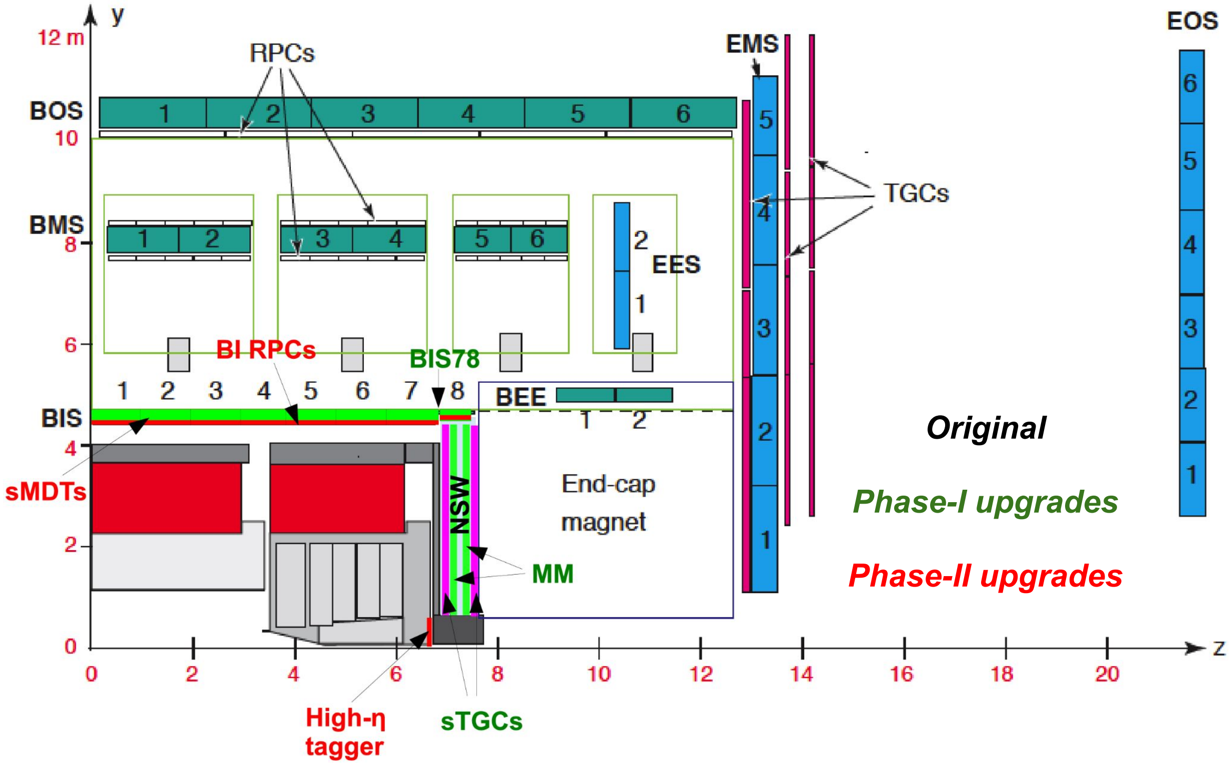
- **Improved RPC coverage**
- **RPC and TGC electronics upgrade**
  Maximum latency: 60 μs
  Maximum rate: 1 MHz
- **New MDT Trigger Processor**

ATLAS Muon Trigger Upgrade

Phase-II ATLAS muon spectrometer layout (CERN-LHCC-2017-017):

- RPC ($|\eta| < 1.05$)
- TGC ($1.05 < |\eta| < 2.4$)
- NSW ($1.3 < |\eta| < 2.7$)
- MDT ($|\eta| < 2.7$)

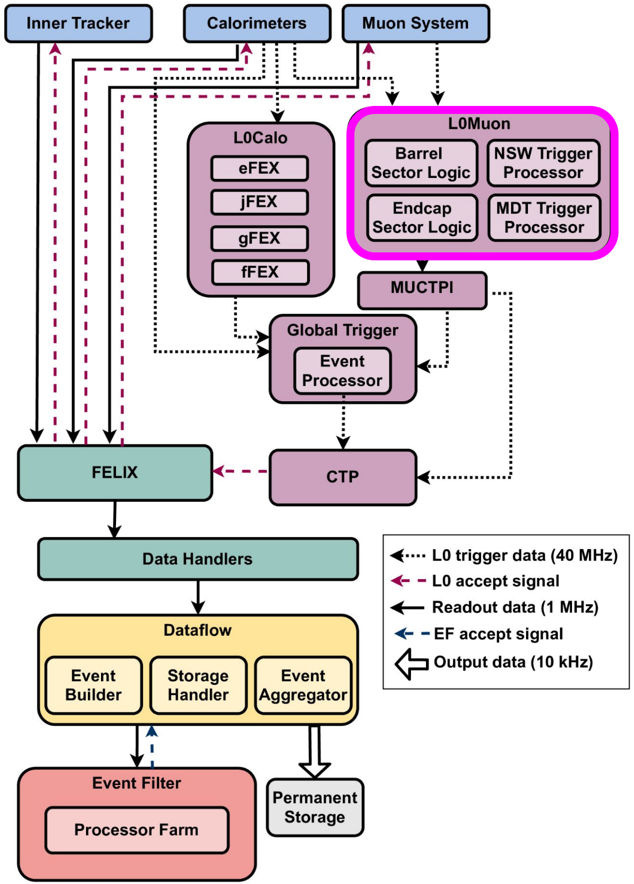
Addition of RPCs in the Barrel Inner (BI) station
Barrel efficiency > 90%



ATLAS Level-0 Muon Trigger

Main upgrades:

- The **Sector Logic** and **NSW Trigger Processor** installed in LS2 will be replaced:
  - New common hardware for Barrel and Endcap Sector Logic (FPGA-based Sector Logic boards)
  - NSW Trigger Processor to perform combined track segment reconstruction by sTGC and MM
- Inclusion of precision hit information (MDT) into Level-0 trigger (**MDT Trigger Processor** will be newly installed) to improve p_T resolution of muon candidates provided by the Sector Logic

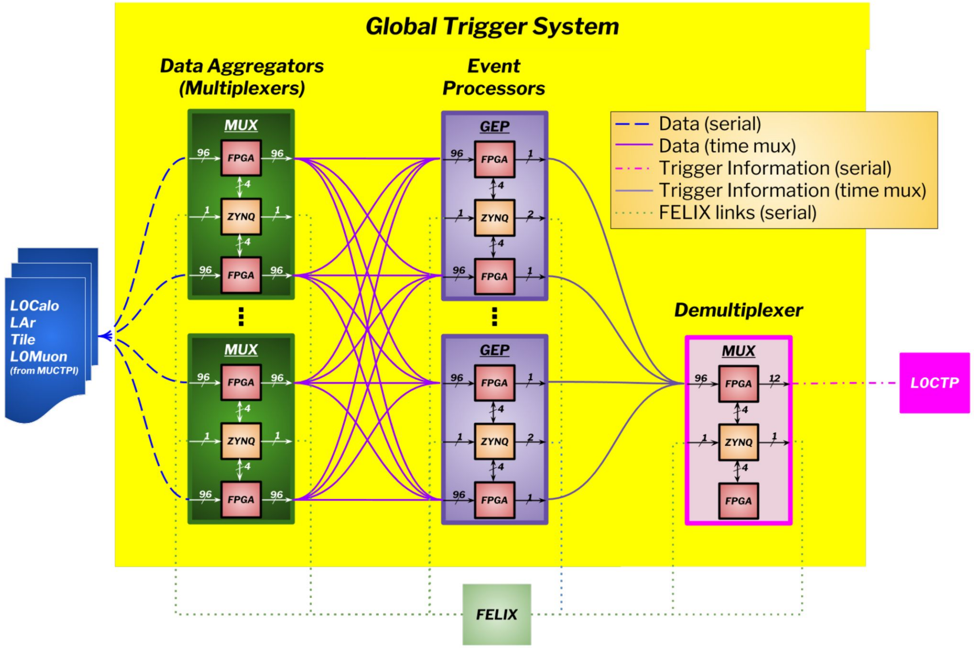


Subsystem	Granularity	Coverage $|\eta|$
NSW processor	Full NSW detector	1.3 – 2.4
MDT processor	Full MDT detector	< 2.4
Barrel Sector Logic	Full RPC and Tile, MDT	< 1.05
Endcap Sector Logic	Full TGC, Tile, RPC, NSW, MDT	1.05 – 2.4

ATLAS Global Trigger

Global Trigger:

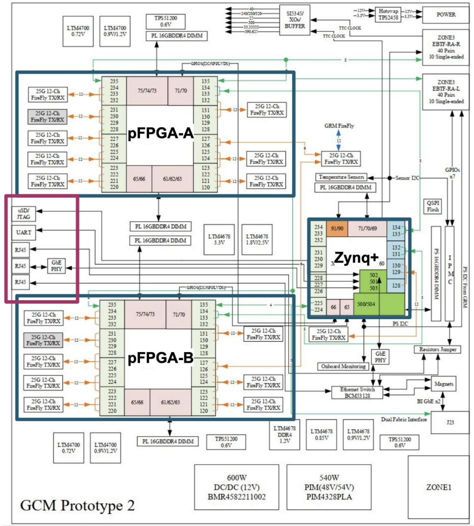
- Replaces and extends the functionality of the Phase-I Topological Processor (L1Topo system)
- Uses full-granularity calorimeter cells to perform algorithms, refines the L0Calo trigger objects and applies topological requirements → **brings Event Filter like capability to Level-0**

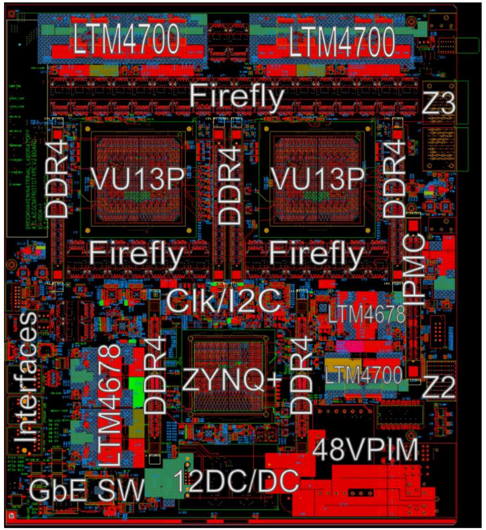


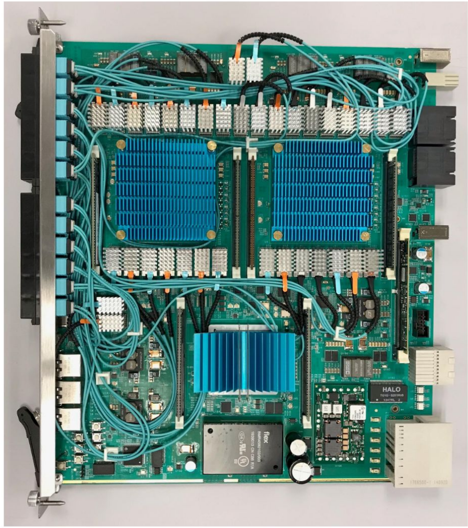
- Emphasis on firmware rather than on hardware:
  - Common hardware
  - Different functions implemented in firmware
- **Global Common Module (GCM)**: common hardware platform and basis of the design, ATCA Front Board with 2 large FPGAs, where each FPGA can be configured as a MUX, GEP or CTPi node as required
- Firmware layers:
  - **MUX:** data aggregation & time multiplexing of events from all sub-detectors (~ 60 Tb/s)
  - **GEP:** Global Event Processing & trigger algorithms (~ x48) → parallelization
  - **CTPi:** Central Trigger Processor interface (demultiplexer to CTP)

ATLAS Global Trigger

- GCM has to provide significant processing resources together with a high input/output bandwidth
- **50 GCMs planned in the system**, each with:
  - 2 Xilinx XCVU13P FPGAs for processing
  - 1 Xilinx Zynq UltraScale+ chip for readout, control, monitoring and debugging
- Board design and fabrication is completed → Ready for framework development
- Prototype hardware tested successfully (including connectivity, thermal and power tests)
- New GCM prototype with two Xilinx Versal FPGAs is upcoming

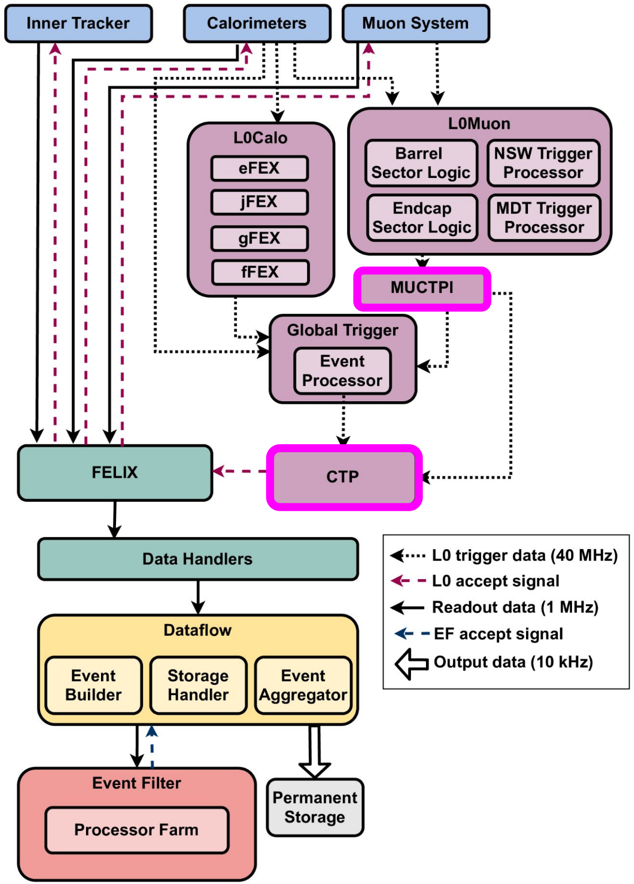






ATLAS Central Trigger System

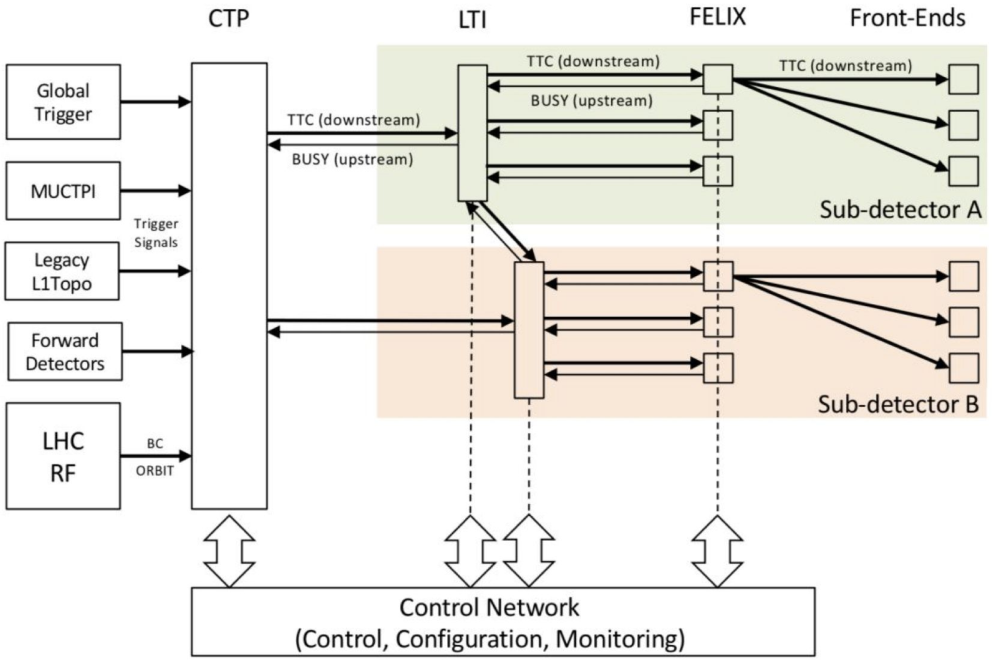
- CTP will be implemented as a single ATCA shelf
- Receives digital trigger inputs from the Global Trigger and the MUCTPI
- Last stage of the processing chain of the Level-0 trigger system, making the final Level-0 accept (L0A) decision
- L0A signal formed as the logical OR of the enabled trigger items
- Responsible for introducing deadtime as required by the detector front-end and readout systems



ATLAS Central Trigger System

The Central Trigger System consists of:

- **Central Trigger Processor (CTP)**:
  New for Phase-II
  Output trigger items increase (512 → 1024) to support bigger trigger menus and exploit the Global Trigger
- **Muon-to-CTP-Interface (MUCTPI)**:
  Upgraded in Phase-I
  MUCTPI merges the trigger information from barrel and endcap before passing it to the Global Trigger and CTP
  Firmware will be upgraded
- **Trigger, Timing and Control (TTC) system**:
  New for Phase-II
  where the Local Trigger Interface (LTI) modules are an integral part, will make use of modern high-bandwidth optical-link technologies



ATLAS Event Filter

Event Filter (EF):

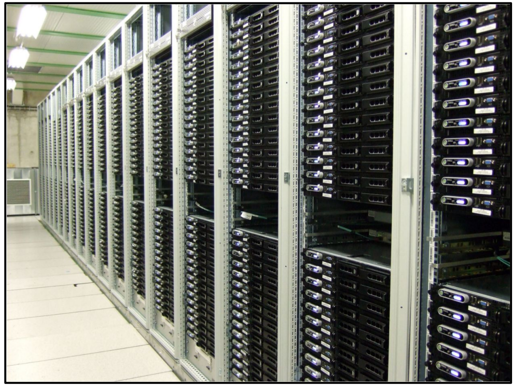
- Responsible for executing sophisticated event selection algorithms at high rate, in a massively parallelised form
- Main goal is to maintain rejection, suppress pileup and keep efficiency high
- The EF will need to make use of more CPU-intensive offline-type selection techniques, including a greater use of full-event tracking
- Representative trigger menu for 1 MHz Level-0 rate
- Thresholds lower than in Run 1
- O(1500) triggers in Run 3

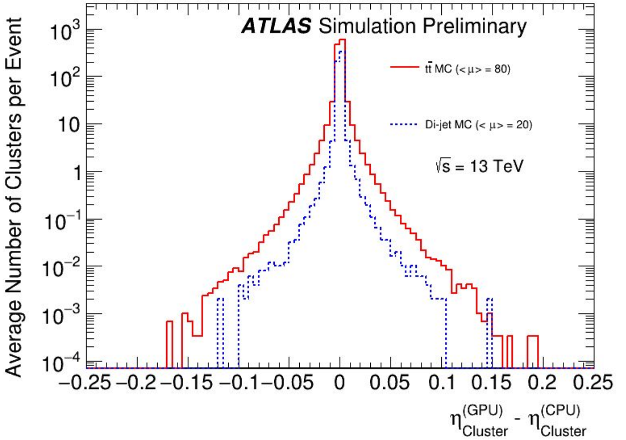
Trigger Selection	Run 1 Offline p_T Threshold [GeV]	Run 2 (2017) Offline p_T Threshold [GeV]	Planned HL-LHC Offline p_T Threshold [GeV]	L0 Rate [kHz]	After regional tracking cuts [kHz]	Event Filter Rate [kHz]
isolated single e	25	27	22	200	40	1.5
isolated single μ	25	27	20	45	45	1.5
single γ	120	145	120	5	5	0.3
forward e			35	40	8	0.2
di-γ	25	25	25,25		20	0.2
di-e	15	18	10,10	60	10	0.2
di-μ	15	15	10,10	10	2	0.2
$e-\mu$	17,6	8,25 / 18,15	10,10	45	10	0.2
single τ	100	170	150	3	3	0.35
di-τ	40,30	40,30	40,30	200	40	$0.5^{\dagger\dagger\dagger}$
single b-jet	200	235	180	25	25	$0.35^{\dagger\dagger\dagger}$
single jet	370	460	400			0.25
large-R jet	470	500	300	40	40	0.5
four-jet (w/ b-tags)		$45^{\dagger}$(1-tag)	65(2-tags)	100	20	0.1
four-jet	85	125	100			0.2
H_T	700	700	375	50	10	$0.2^{\dagger\dagger\dagger}$
E_T^{miss}	150	200	210	60	5	0.4
VBF inclusive			2x75 w/ ($\Delta\eta > 2.5$ & $\Delta\phi < 2.5$)	33	5	$0.5^{\dagger\dagger\dagger}$
B-physics††				50	10	0.5
Supporting Trigs				100	40	2
Total				1066	338	10.4

† In Run 2, the 4-jet b-tag trigger operates below the efficiency plateau of the Level-1 trigger.
†† This is a place-holder for selections to be defined.
††† Assumes additional analysis specific requires at the Event Filter level

Accelerator Hardware for the ATLAS Event Filter

- Original Phase-II ATLAS Event Filter system based on a **CPU farm** and a **Hardware-based Tracking for the Trigger, HTT** (ATLAS-TDR-029, CERN-LHCC-2017-020)
- **Data centers are adopting hybrid systems** that integrate multiple types of computational units:
  - CPUs
  - GPUs
  - FPGAs
- **CMS** and **LHCb** already using **GPUs and FPGAs in Run 3**
- **New baseline for the ATLAS Event Filter Tracking project in HL-LHC** (ATLAS-TDR-029-ADD-1, CERN-LHCC-2022-004)**:**
  - Heterogeneous system **CPU/GPU/FPGA**
  - Better performance/cost and less electric consumption
  - Redesign software in HEP for a hybrid environment

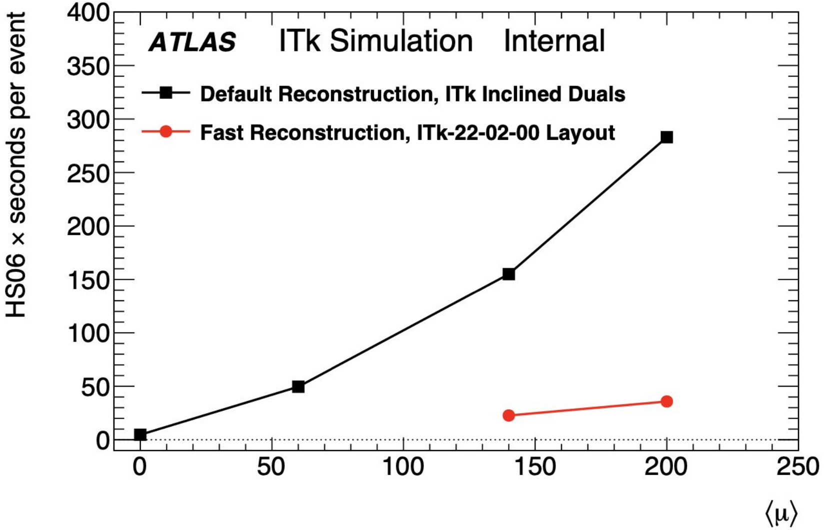


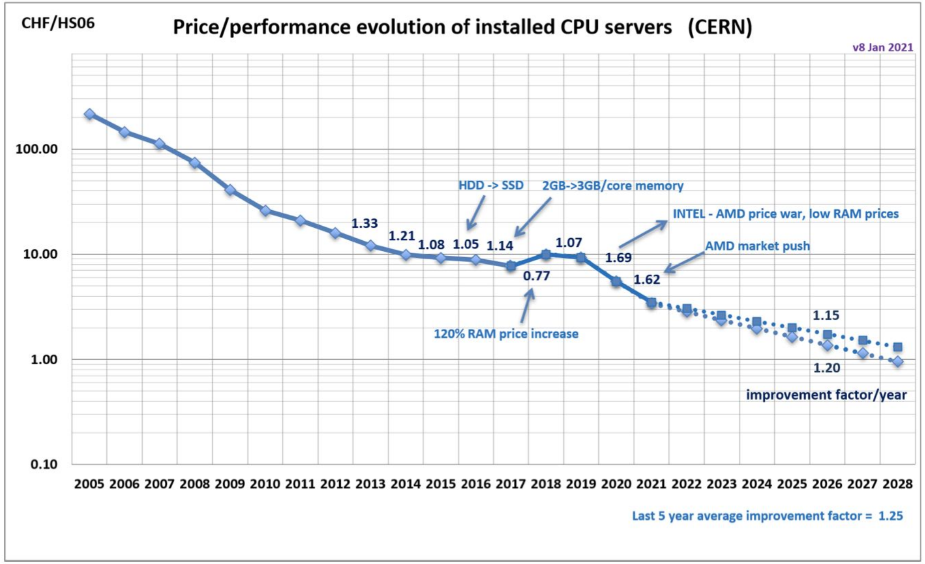


ATLAS Event Filter Tracking Amendment

Main reasons for the revision:

- With the latest **fast ITk reconstruction software** prototype, and with the updated ITk layout, the time for reconstructing an event **went down by more than a factor of 8** without major compromises in tracking performance
- Delays to the LHC schedule and recent developments on the CPU market have resulted in a significant reduction in predicted cost per HEP-SPEC06 (HS06): it is now **1.3 CHF/HS06 in 2027**, compared to the **Phase-II TDAQ TDR prediction of 2 CHF/HS06 for 2026**





Conclusions

- HL-LHC start expected in 2029 with an ultimate instantaneous luminosity of 7.5×10^{34} $cm^{-2}s^{-1}$ and ~200 interactions per bunch crossing
- Ambitious Phase-II Upgrade program for the ATLAS Trigger and Data Acquisition System to cope with the harsh HL-LHC conditions, increased output rate at the first (100 kHz → 1 MHz) and second (1 kHz → 10 kHz) stages
- Improvements include new L0Calo fFEX, L0Muon electronics (including MDT Trigger Processor), Global Trigger and CTP
- Upgraded trigger system will use increased granularity for the calorimeter based triggers and improved efficiency for the muon based triggers
- Continued good progress across TDAQ Phase-II upgrade project areas