



HAXPES to investigate advanced devices for microelectronic applications

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M. Gros-Jean, V. Jousseau, F. Bertin, J. Roy,
J. Zegenhagen and O. Renault



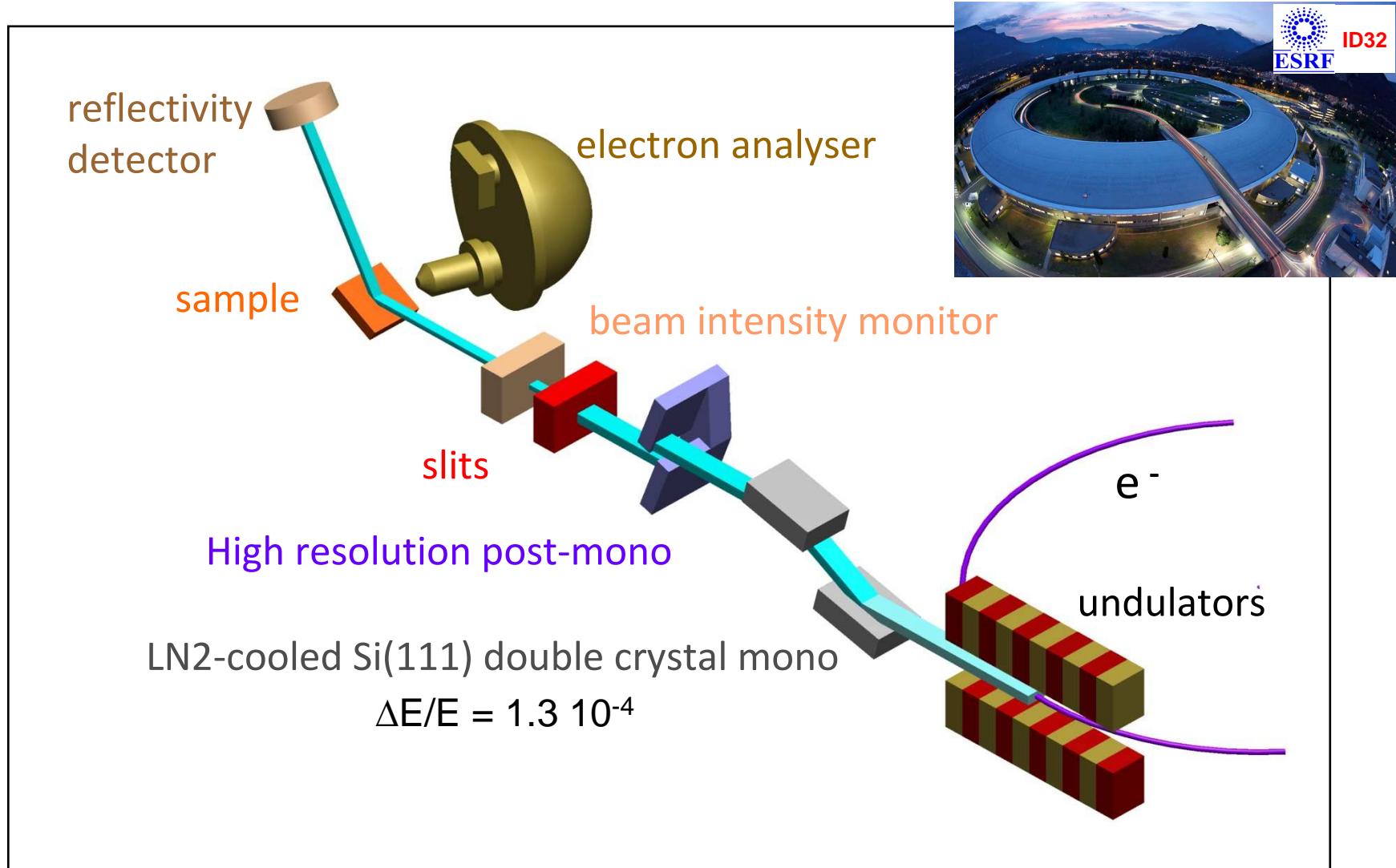
Outline

- The context:
 - The ID32 beamline at ESRF
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- MOSFET - 32 nm node: LaOx control layer
 - Lanthanum diffusion & bonding states
 - Band alignment of the KH/MG stack & interfacial dipole
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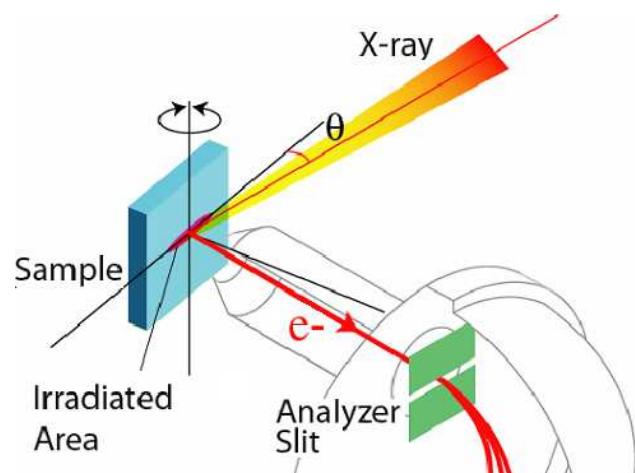
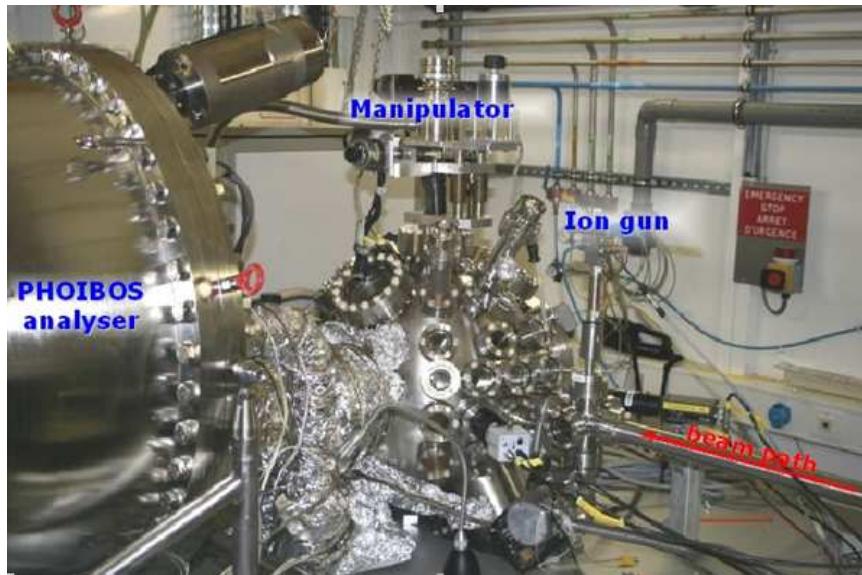
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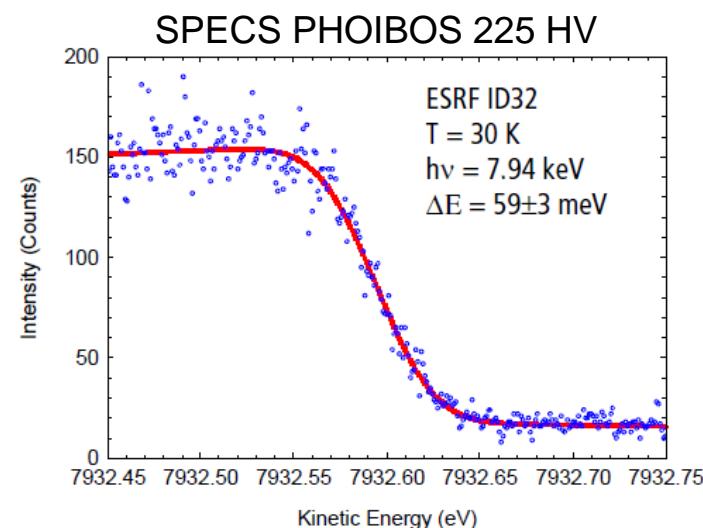
ID32 beamline – HAXPES setup (1)



ID32 beamline – HAXPES setup (2)

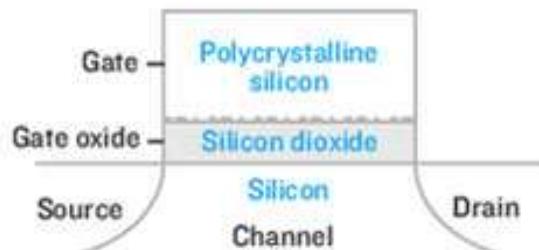


- Energy range from 1.4 to 30 keV
- Beam size : H = 900 μm and V = 20 μm
- Post monochromators & PHOIBOS analyzer – $\Delta E < 400 \text{ meV}$ for $E < 10 \text{ keV}$
- Grazing incidence (10°) and normal collection (90°)

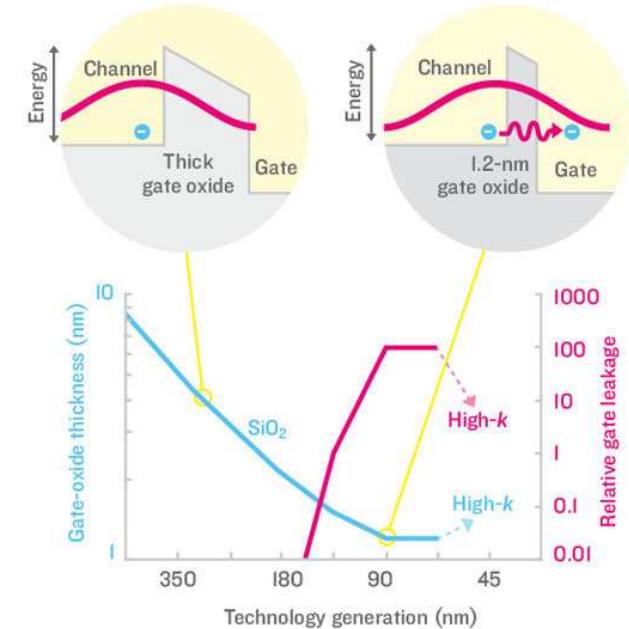


MOSFETs downscaling (1)

CONVENTIONAL TRANSISTORS

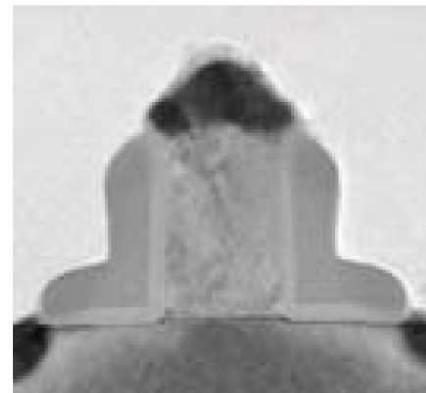


Thin SiO_2 ($< 1 \text{ nm}$): Tunneling leakage current
→ Potential barrier « transparent » for e-

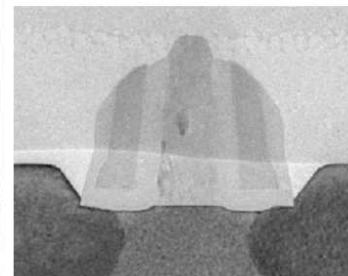


K. Kuhn (Intel), SSDM, Japan, 2009

« The high-k solution » IEEE spectrum, oct. 2007



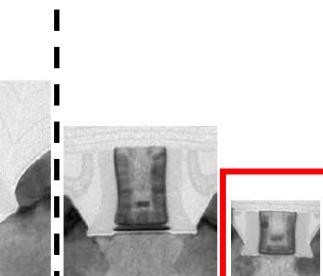
130nm



90nm



65nm



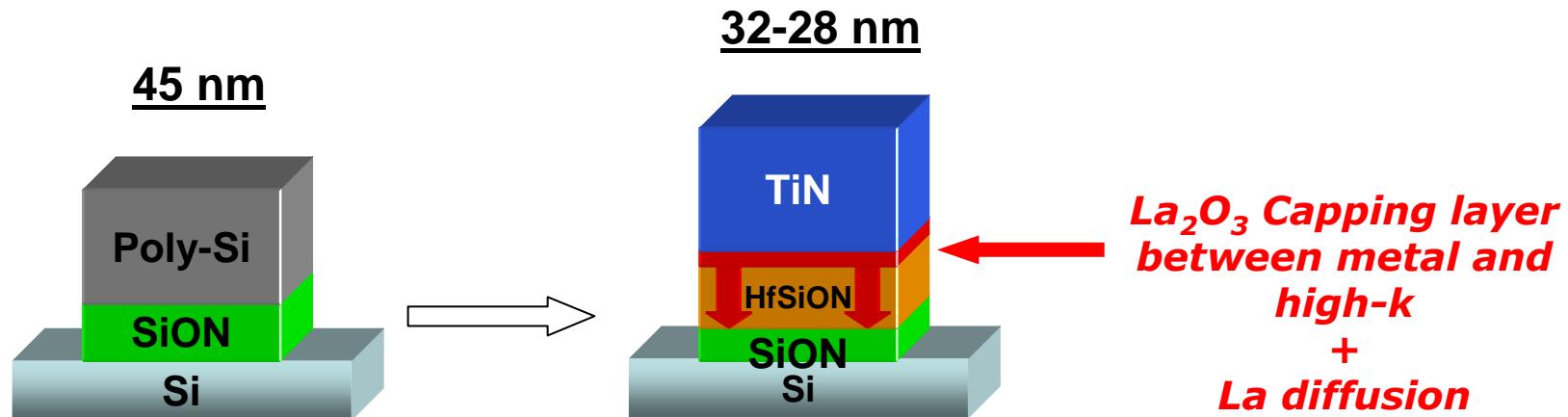
45nm



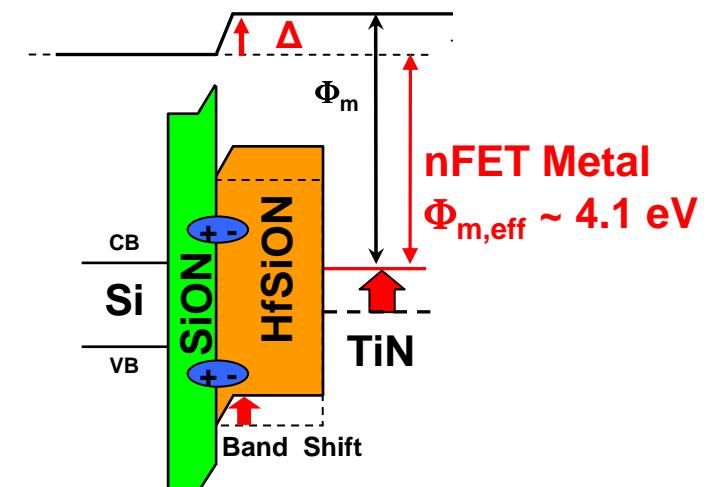
32nm

→ The 32 nm node at STMicroelectronics
First transistor with High-k/Metal gate structures

MOSFETs downscaling (2)

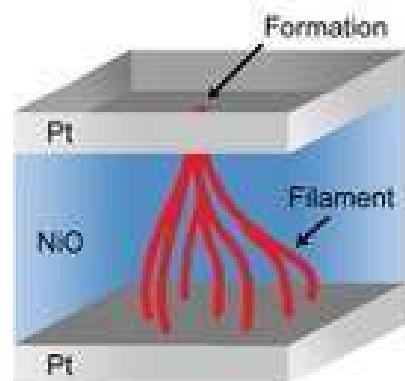
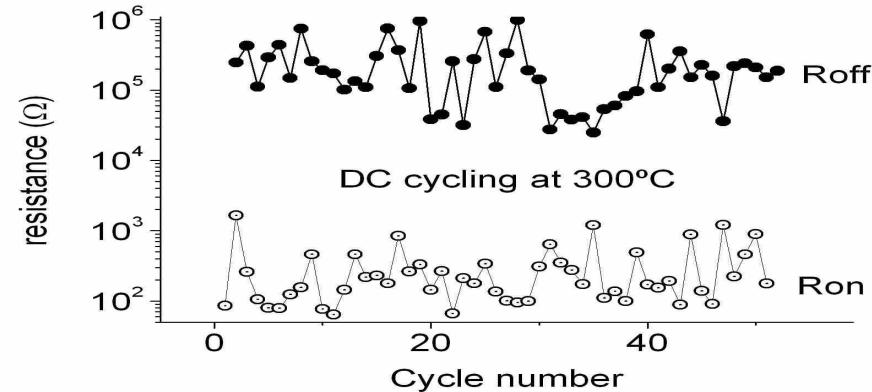
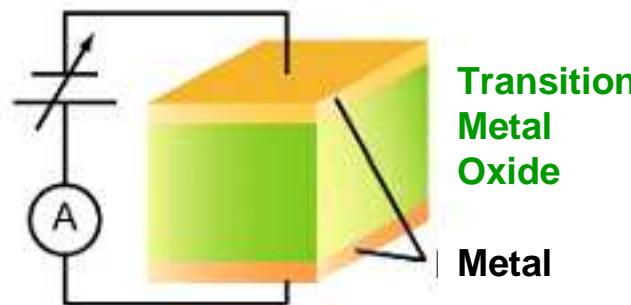


- High-k : HfSiON
 - Reduction of leakage current (x 10 000)
→ $C = \kappa \frac{\epsilon_0 A}{t}$
- Metal Gate : TiN
 - Suppress poly-Si depletion
- Capping layers
 - Tune the gate work-function and V_{TH} voltage
→ La₂O₃ for NMOS stacks



Oxide Resistive memories (OxRRAM) (1)

A. Sawa, materials today, Vol. 11, No. 6, (2008)

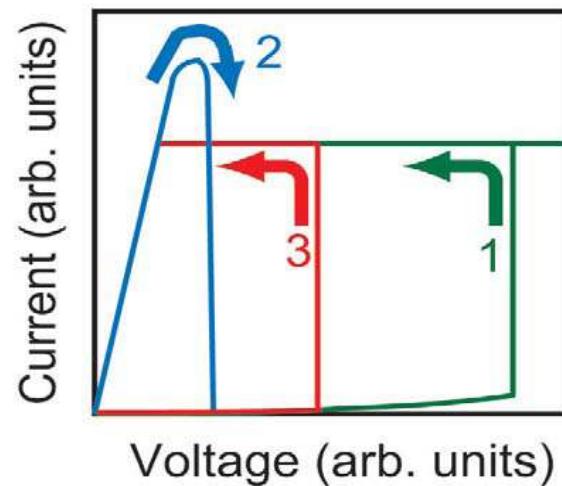


- Scalability, data retention & high speed
- **Pt/NiO promising system**
- HRS to LRS by applying appropriate voltage (~8 V)
- Switching mechanism : filaments, thermal effects...

Oxide Resistive memories (OxRRAM) (2)

A. Sawa, Materials Today, Vol. 11, 6 (2008)

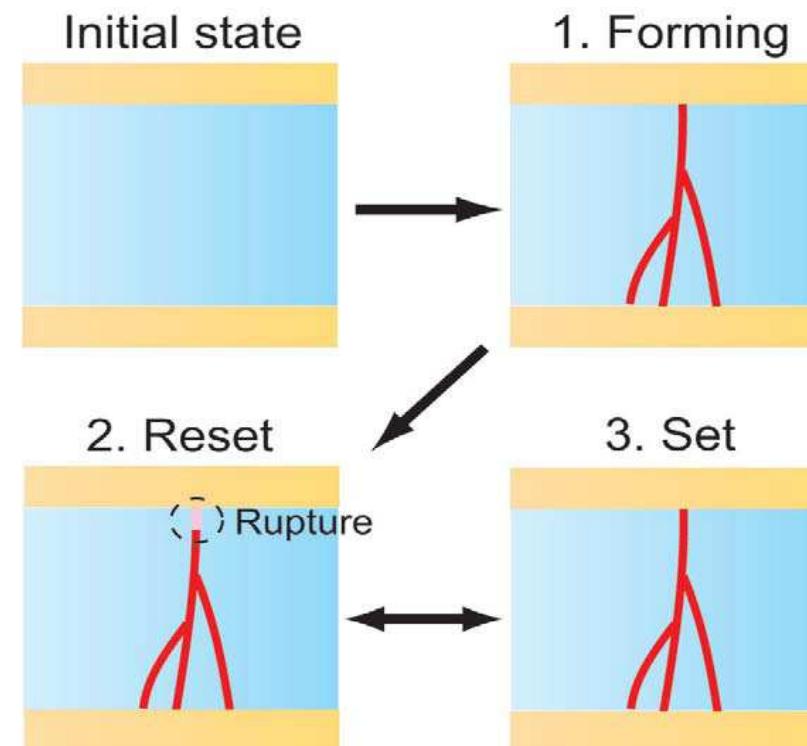
Filamentary mechanism



1 : forming

2 : reset

3 : set



→ HAXPES to investigate forming
→ bulk NiO & buried NiO/Pt interface

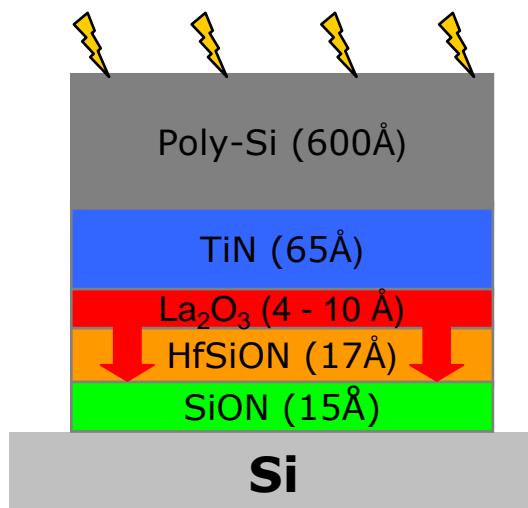
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Objective

- Investigate La diffusion and buried SiON interfacial layer under high temperature anneal (1065°C)
→ HAXPES : *in-depth profiles & bonding states*

Spike anneal (1065°C)



Technologically relevant samples:

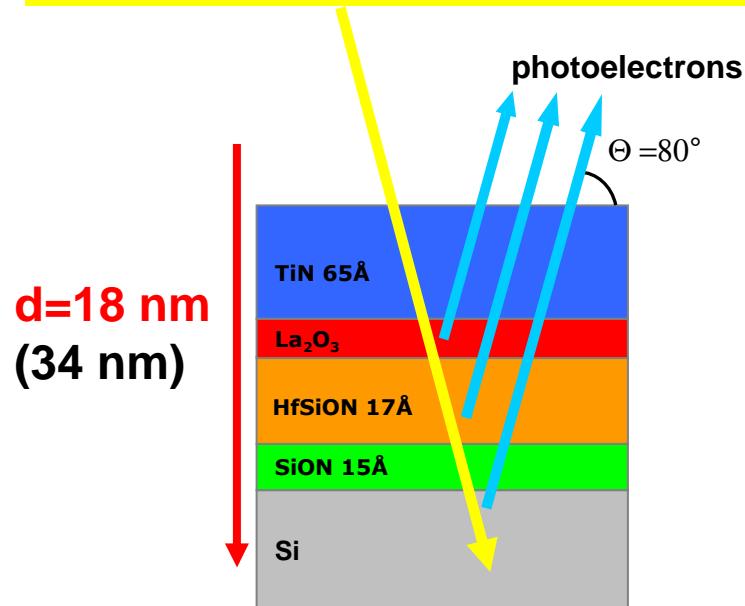
- 300 mm wafers (ST cleanrooms)
- Same integration process (thicknesses, deposition techniques & tools)
- Post deposition spike anneal (1065°C)

Critical points for laboratory XPS:

- Signal attenuation by the gate (TiN + poly Si)
- La instability under air exposure
- Sensitivity to the low amount of La
- Spectral interference between Si2p & La4d

Experimental details

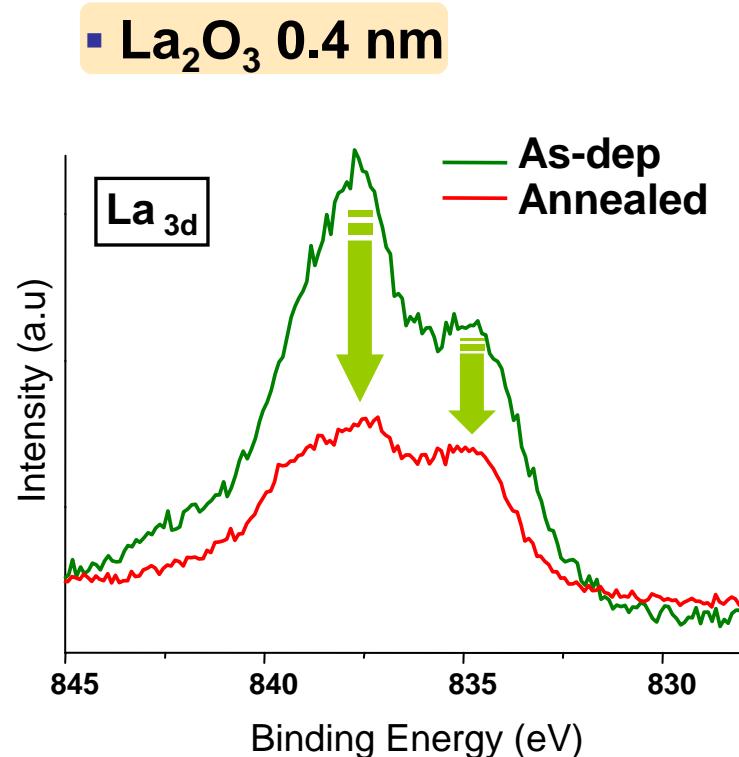
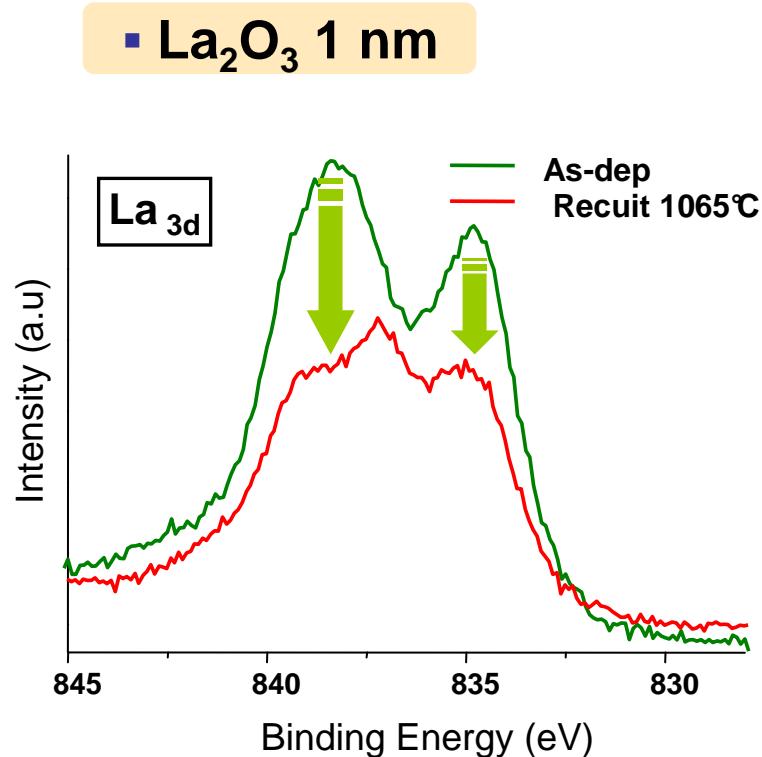
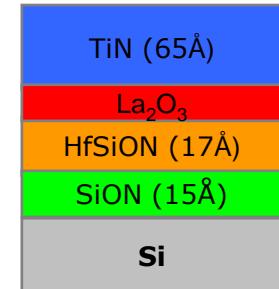
Hard X-ray 3.81 keV (7.95keV)



- Partial removal of the gate (poly-Si)
- Varying La thickness (0, 0.4 and 1 nm)
- w / wo spike anneal (1065°C)
- Analysis of buried interfaces with a larger spectral range (Si 1s)

→ Detailed analysis of La behaviour thanks to HAXPES

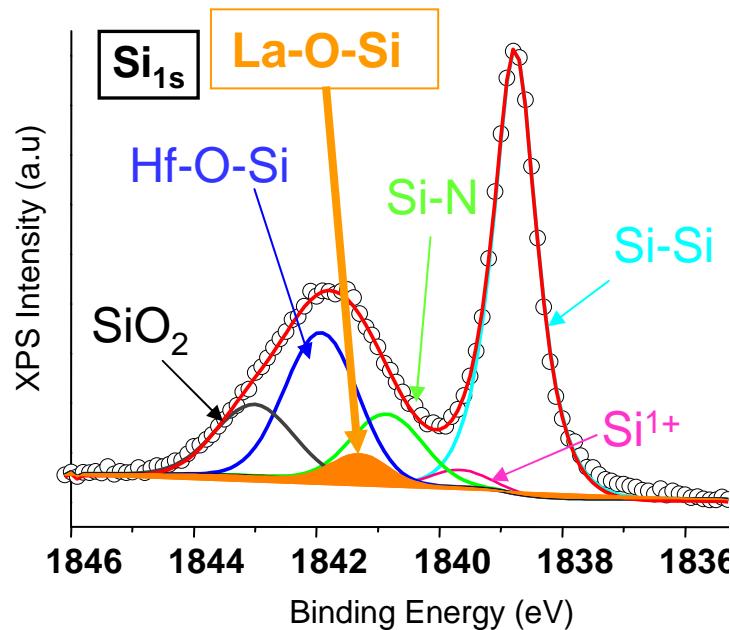
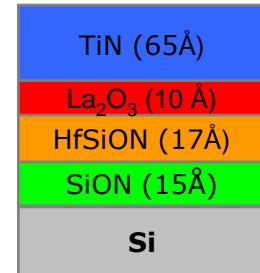
La diffusion through high-K



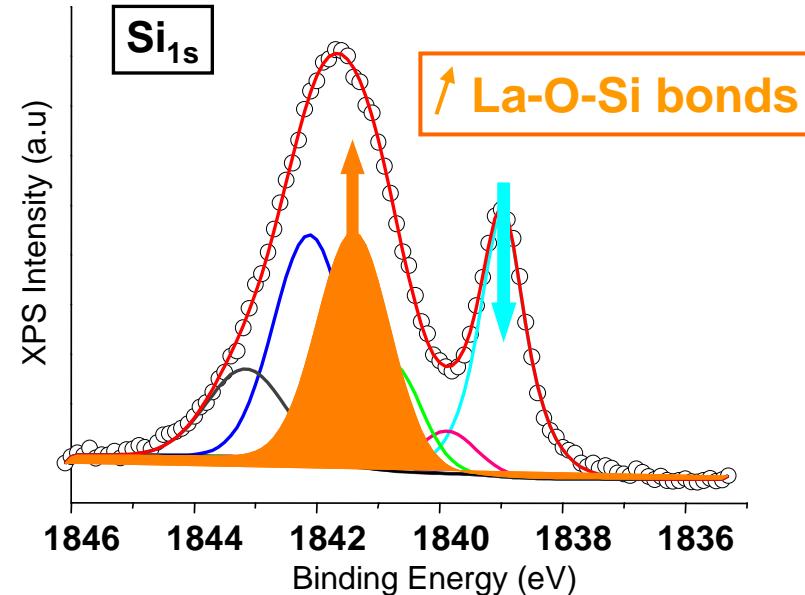
→ La diffusion towards SiON after spike anneal at 1065°C

Bonding states – Si_{1s}

- Stacks with 1 nm-thick La₂O₃



Asdep

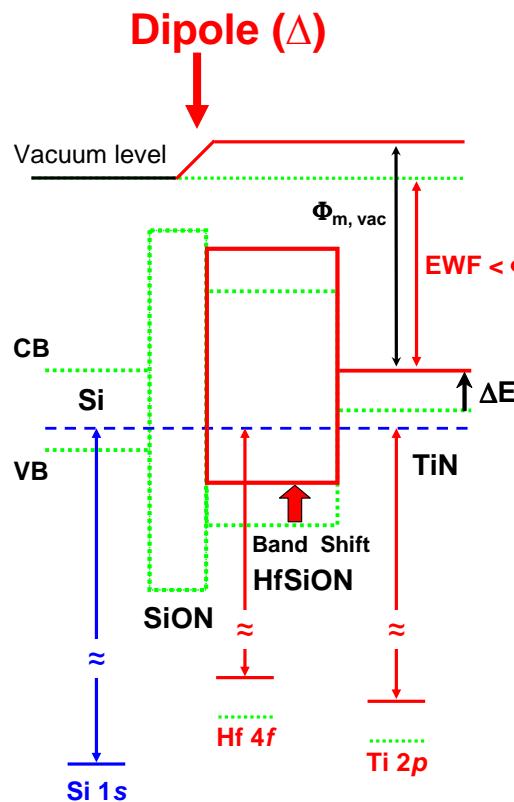


1065°C Anneal

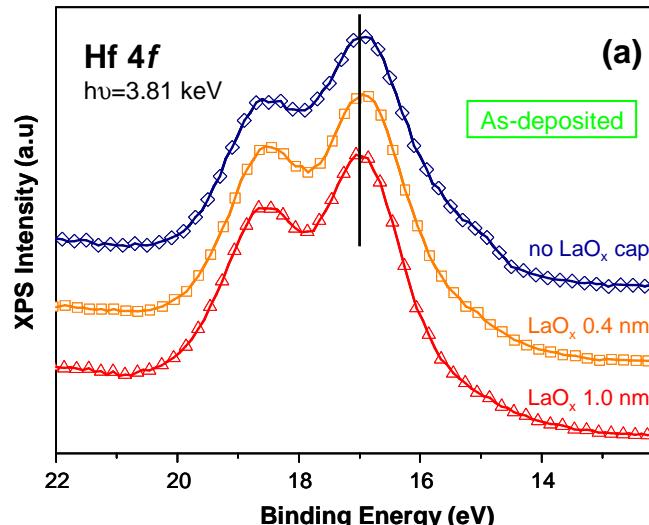
→ LaSi_xO_y component is created after anneal

R. Boujamaa et al., « Impact of high temperature annealing on La diffusion and flatband voltage modulation in TiN/LaOx/HfSiON/SiON/Si gate stacks », submitted to J. of Appl. Phys. (2011).

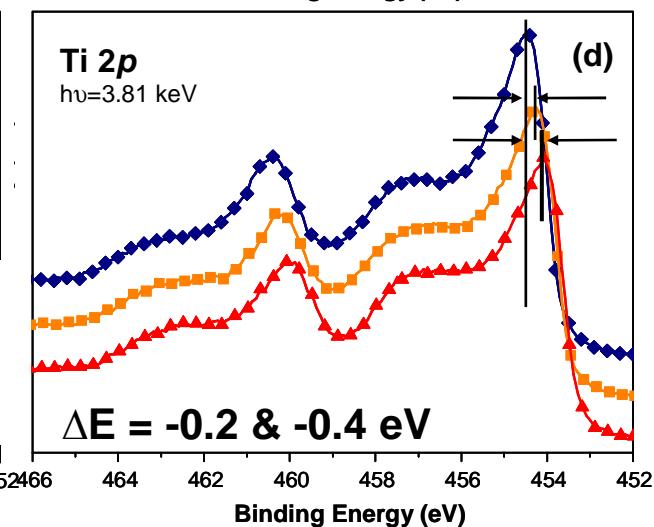
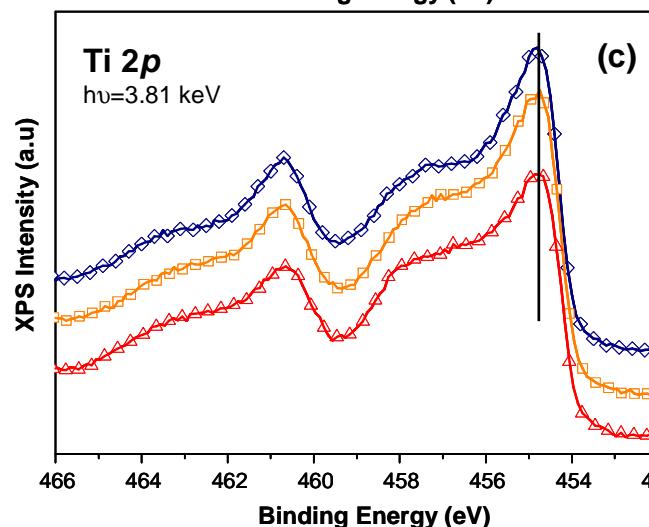
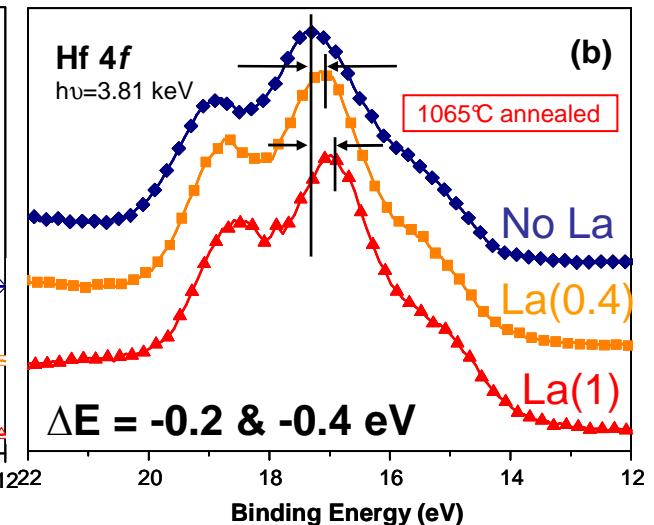
Interfacial Dipole – Hf_{4f} and Ti_{2p}



As-deposited



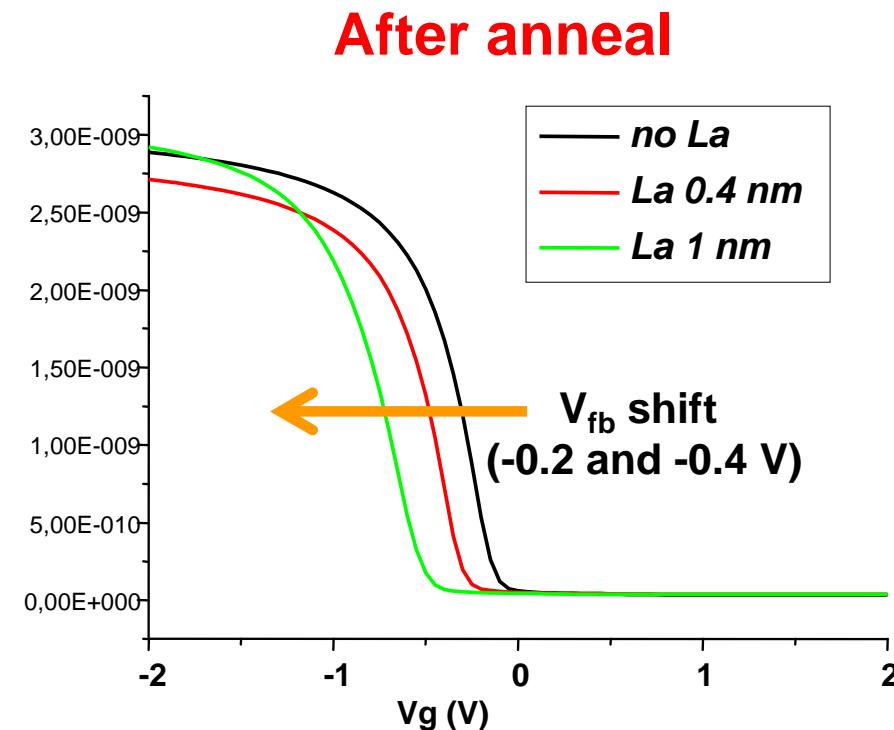
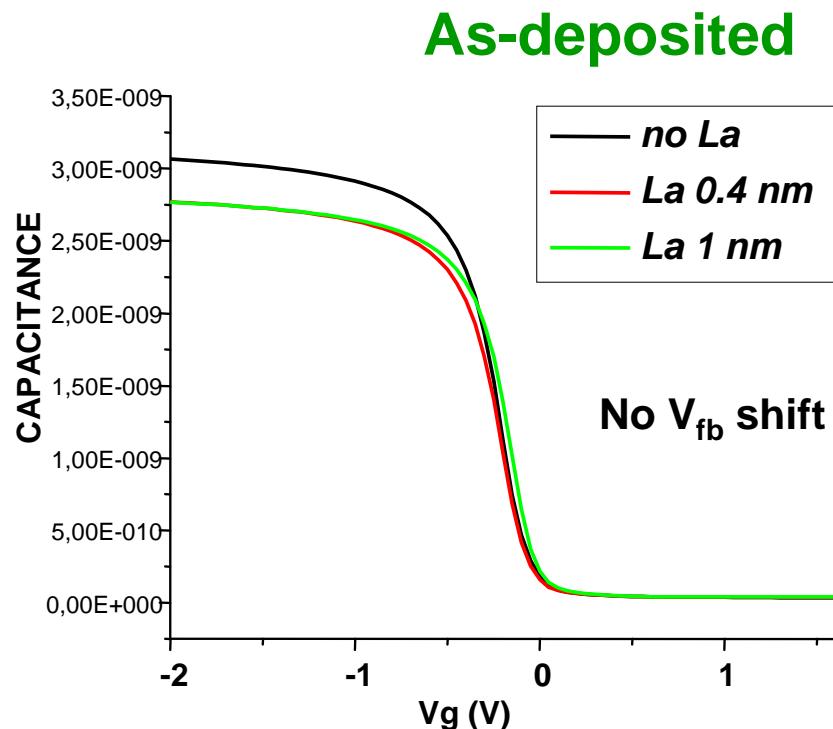
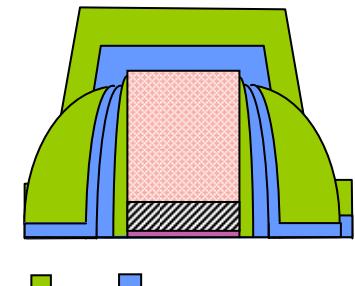
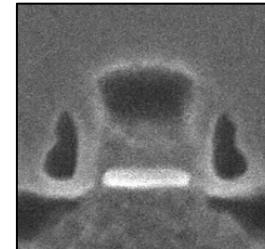
After anneal



R. Boujamaa et al., ECS Transactions
35(4), 805 (2011)

Interfacial Dipole – C(V)

$$|V_t| = |2 \cdot \varphi_f| + V_{fb} + \frac{|Q_D|}{C_{ox}}$$



- V_{fb} shifts after anneal - good correlation with HAXPES core level shifts
- Increasing dipole strength with La thickness

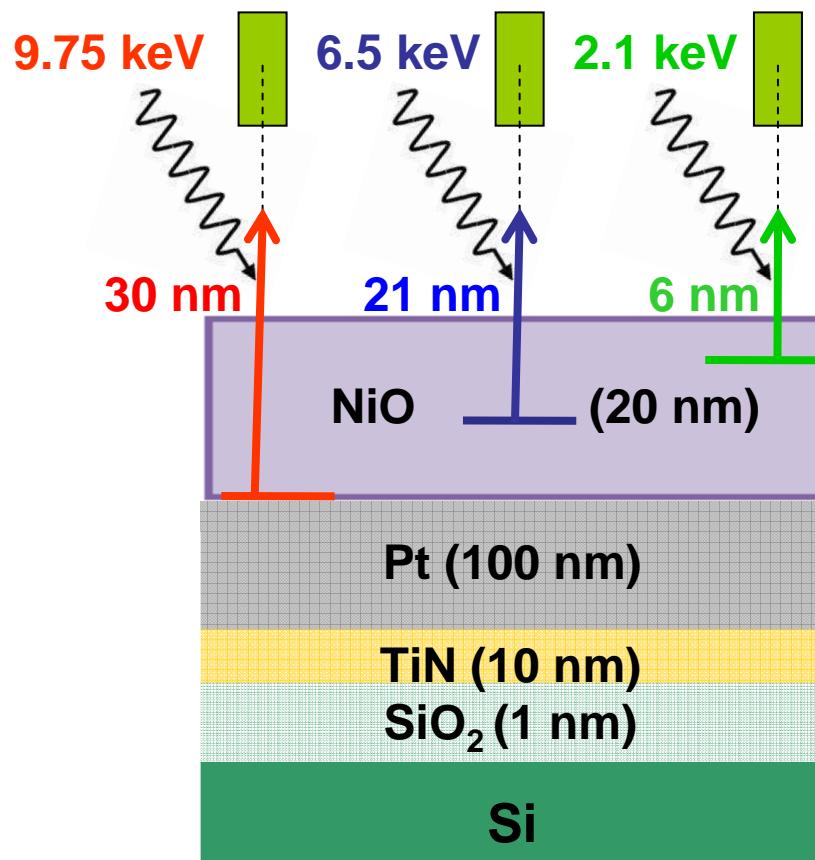
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Objective

- Investigate the conduction mechanism involved in resistance switching

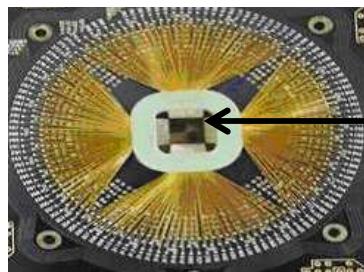
→ HAXPES : bulk NiO & buried NiO/Pt



- $h\nu = 2.1, 6.5$ and 9.75 keV
- Post monochromator – $\Delta E < 510$ meV
- band alignment & bonding states analysis
- Grazing incidence (10°) & normal collection (90°)
- Charging effects corrected via C1s

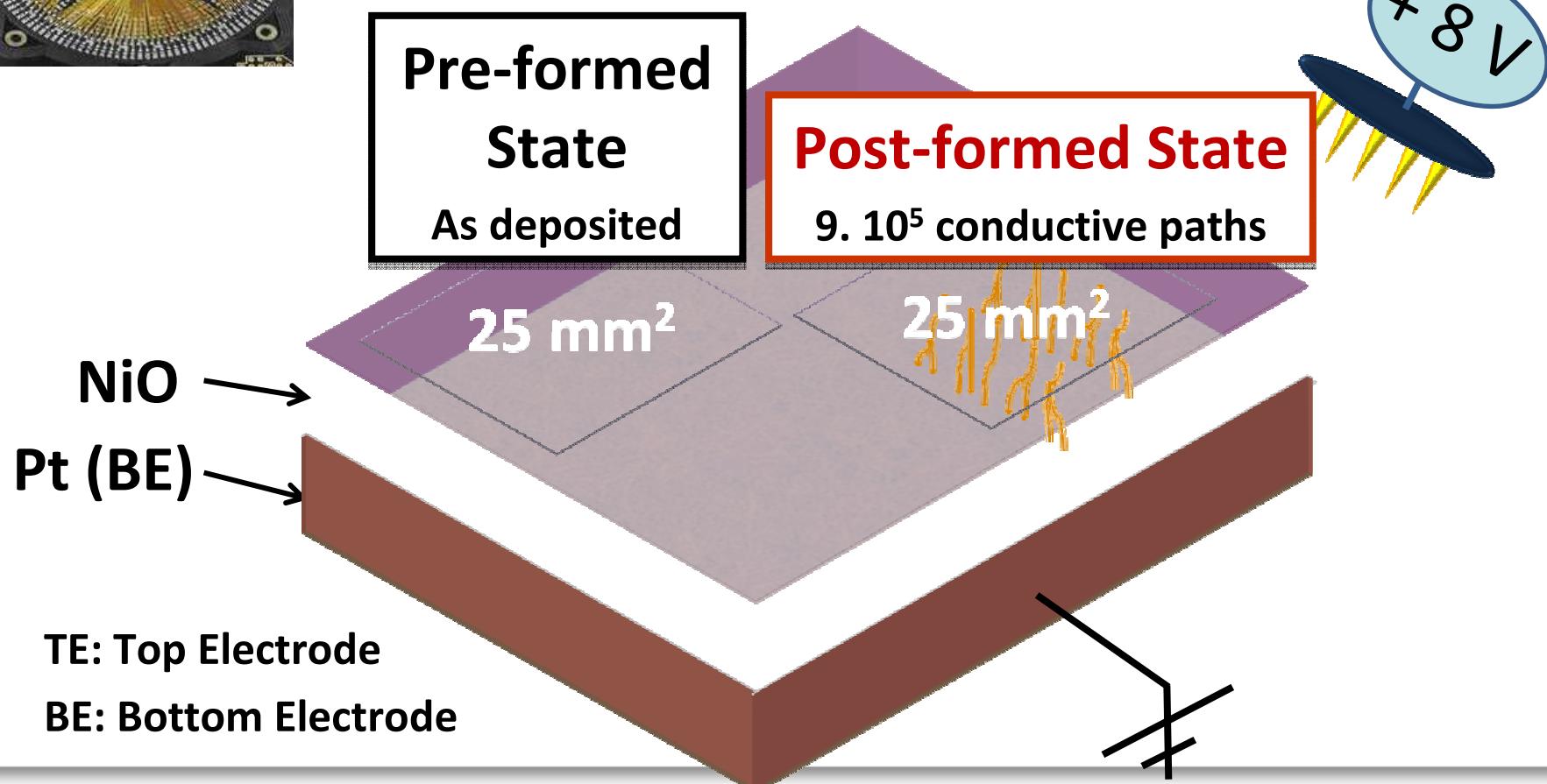
Experimental details

Probe Card

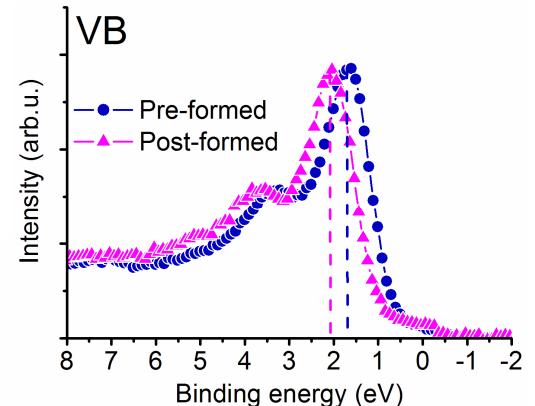
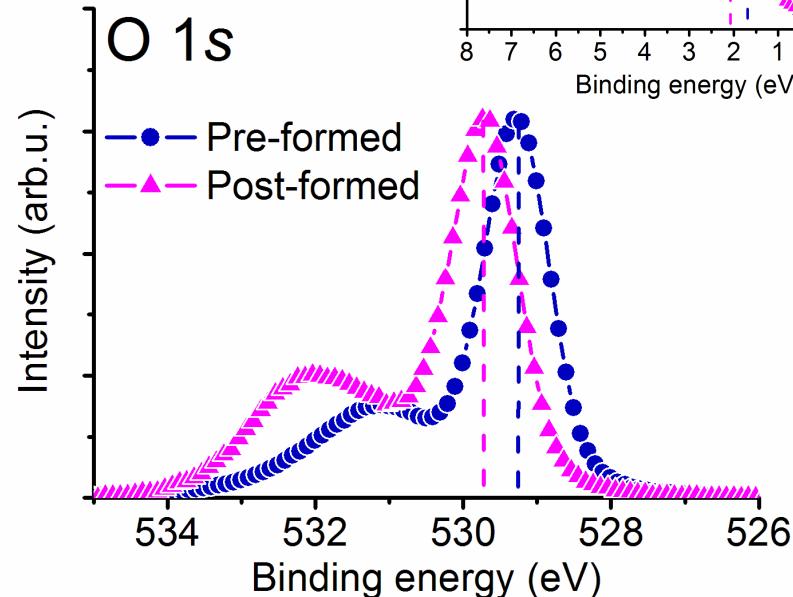
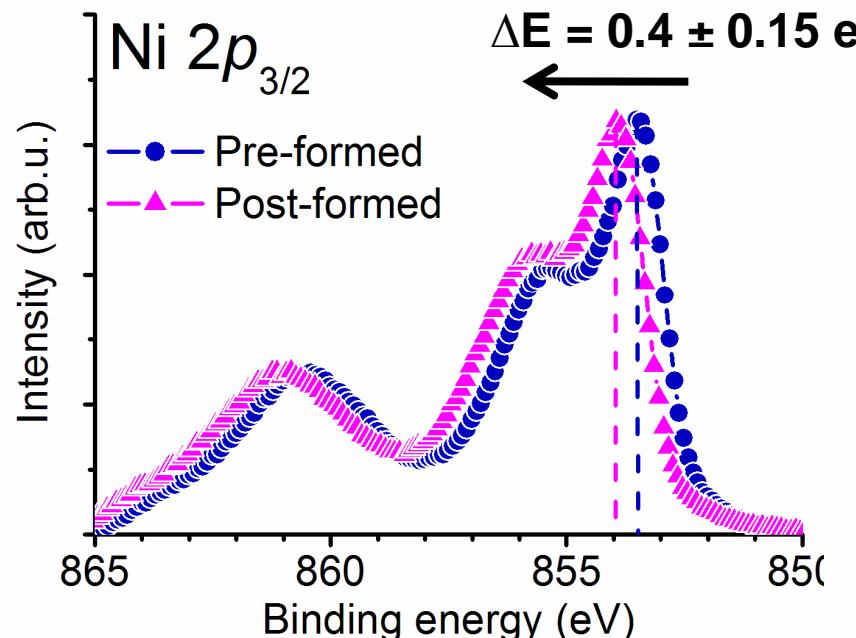


CuBeTips (TE)

- Inducing conductive paths by forming on blanket wafers



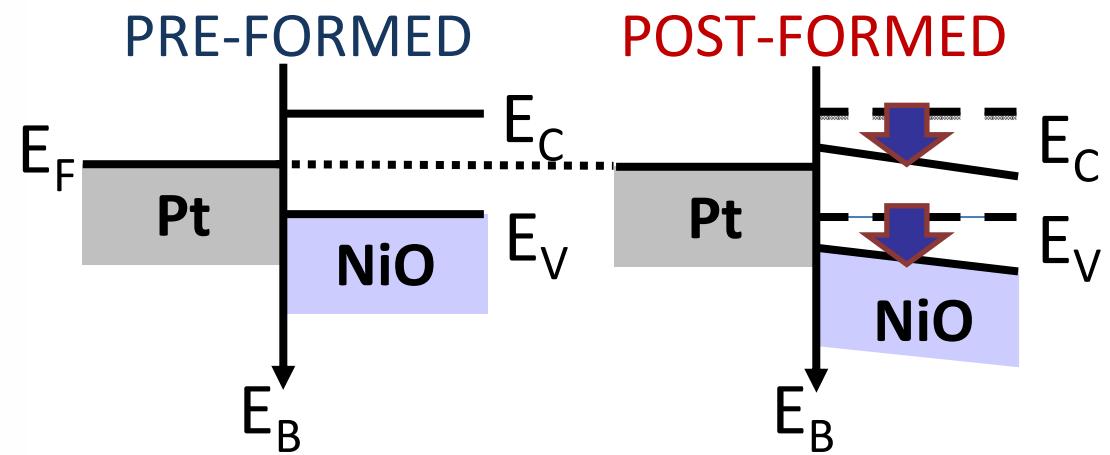
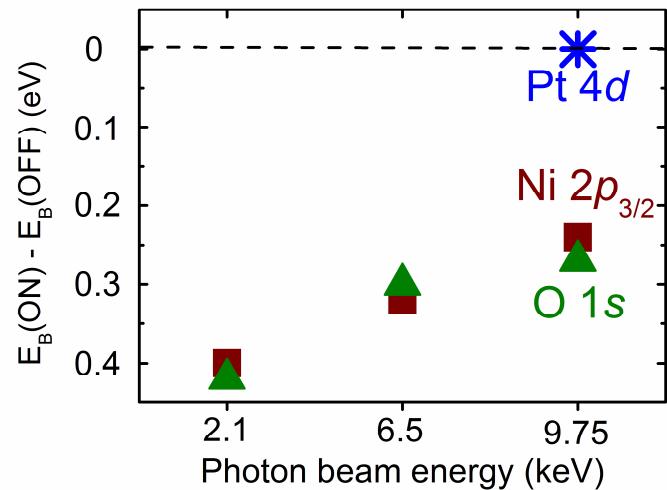
Surface analysis (2.1 keV)



- Similar shifts for Ni2p, O1s and VB after forming
- Band shift towards higher binding energies due to n-type defects (O vacancies)

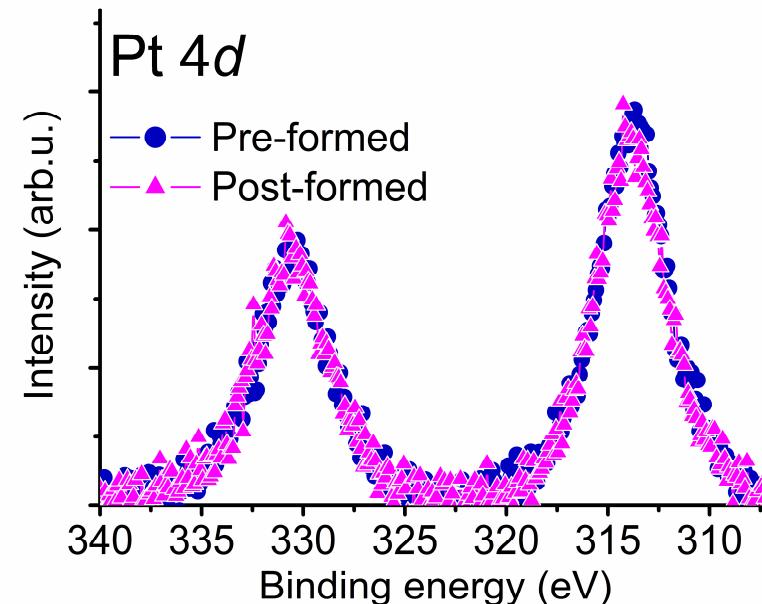
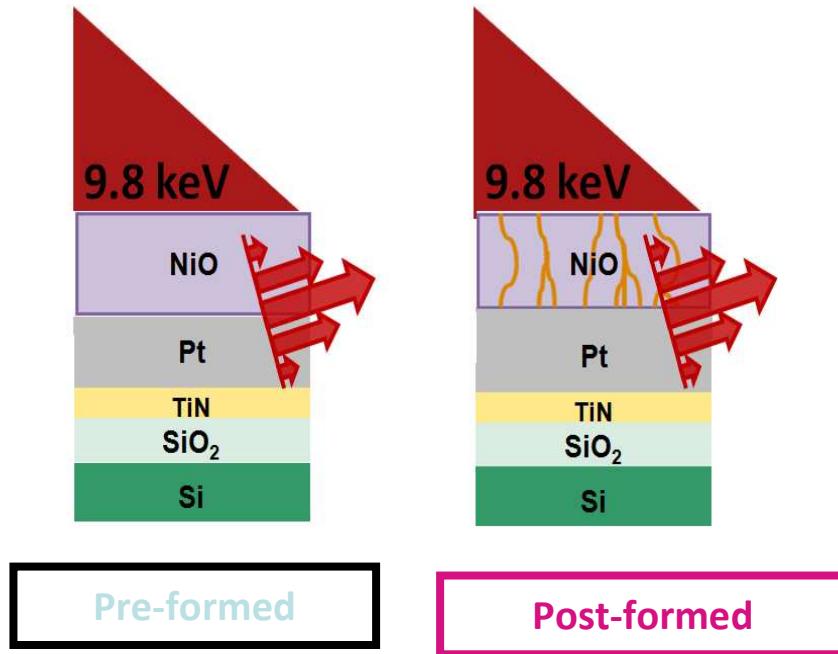
P. Calka et al., J. of Appl. Phys. **109**, 124507 (2011)

In-depth analysis (6.5 & 9.75 keV)



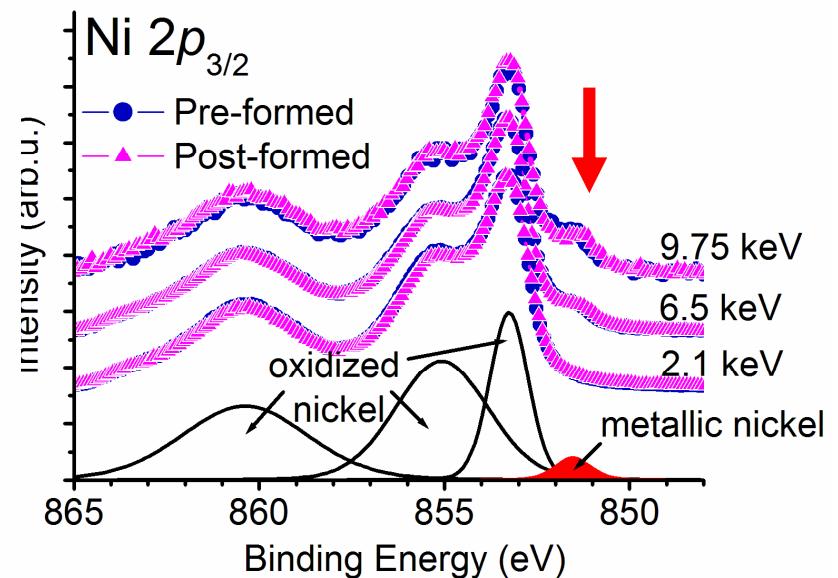
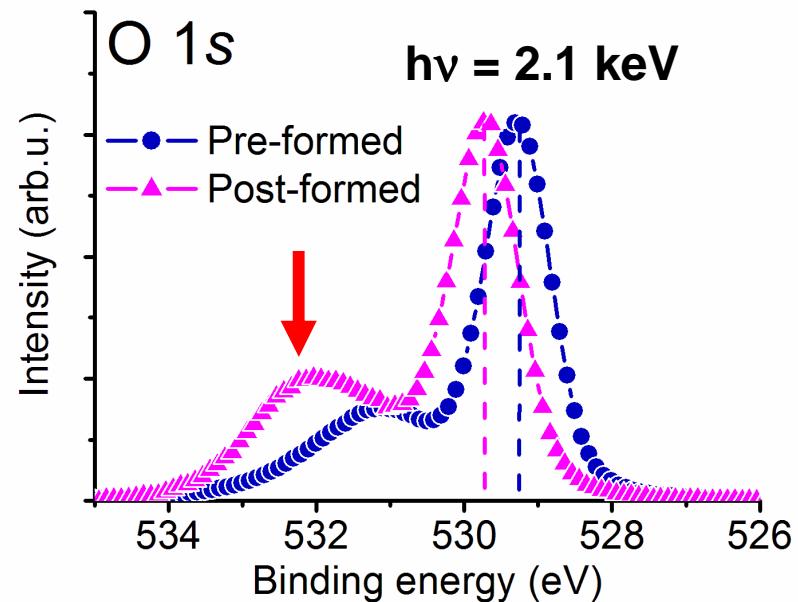
- Increasing band shifts with decreasing depth
- Gradient of defects concentration along NiO

In-depth analysis – Pt_{4d}



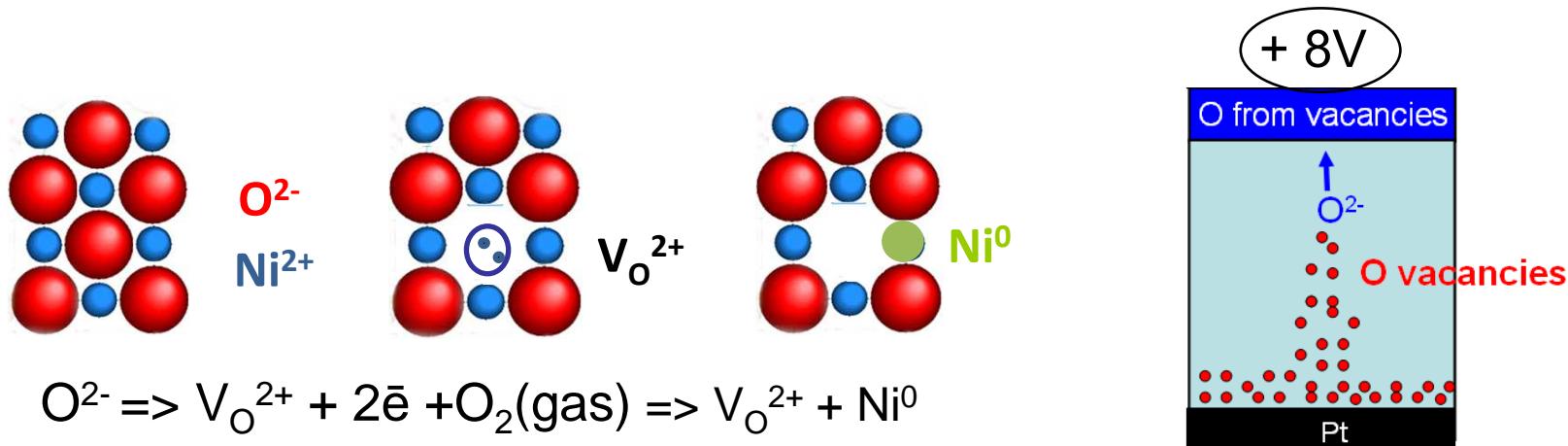
- Non-destructive analysis of the NiO(20 nm)/Pt interface at $h\nu \sim 10$ keV with high S/N ratio
- No chemical changes at the interface

O²⁻ migration & Ni⁰ formation



- New component at 532 eV : O²⁻ in nonlattice position
- Slight increase of Ni⁰ after forming at the Pt/NiO interface (4.4 to 4.6 % of relative area)

Switching mechanism - Discussion



→ O^{2-} migration (Joule heating and/or bias induced) and n-type defects (\bar{e} trapped at O vacancies and Ni^0)

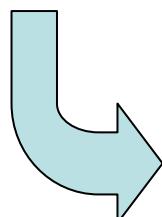
→ The forming step induces conductive paths formation by percolation of these defects

→ In agreement with the models proposed in the litterature

(Lee et al., Phys. Rev. B 81, 193202 (2010))

Conclusion & Prospects

- HAXPES is of great interest for the optimization of a wide range of microelectronic devices
- In-depth analysis of inter-diffusion phenomena, bonding states analysis, electronic properties, band alignments
- No artifacts related to sample preparation (chemical etching, backside preparation, sputtering)



- Background analysis (Quases-Tougaard) coupled with HAXPES ($d \sim 50$ nm)
- Closure of ID 32 at the end of the year !!!

Acknowledgments

- LETI (CEA, Grenoble) : P. Calka, C. Guedj, V. Jousseau, F. Bertin, O. Renault



- ESRF : B. Detlefs, J. Roy, J. Zegenhagen



- STMicroelectronics : R. Boujamaa, M. Gros-Jean



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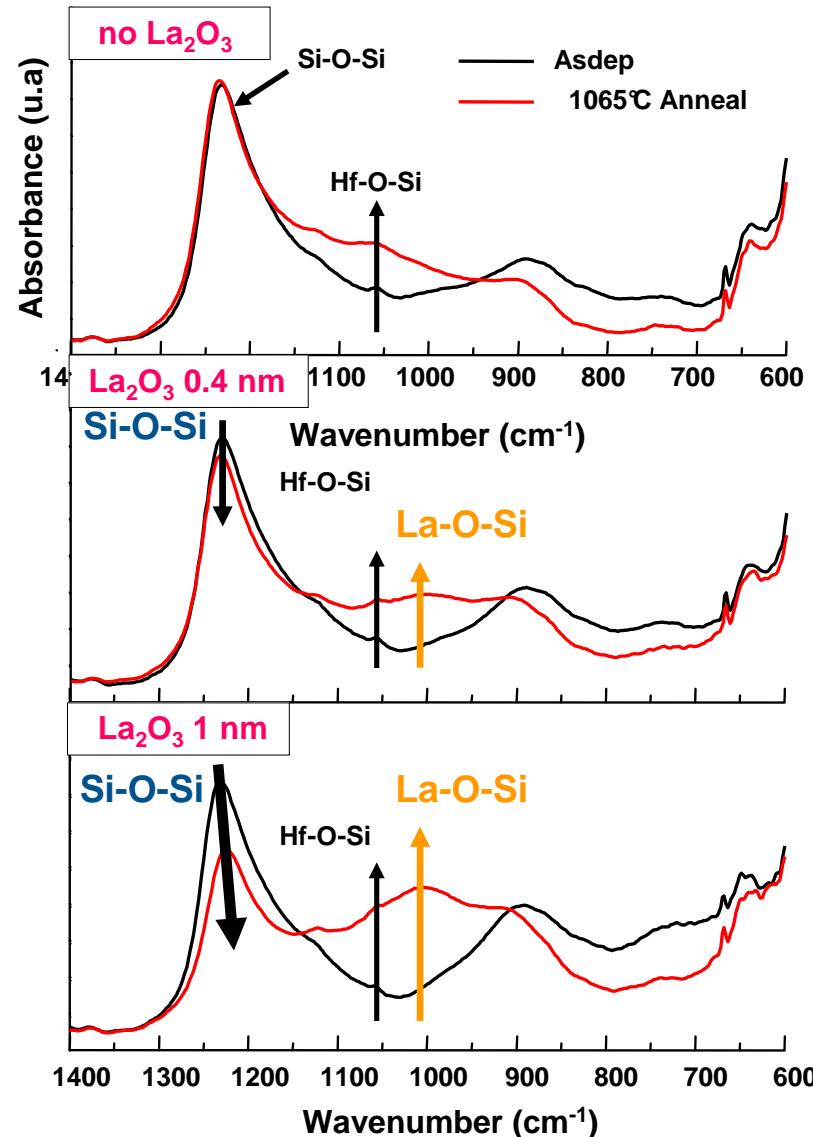
www.leti.fr



Thank you for
your attention



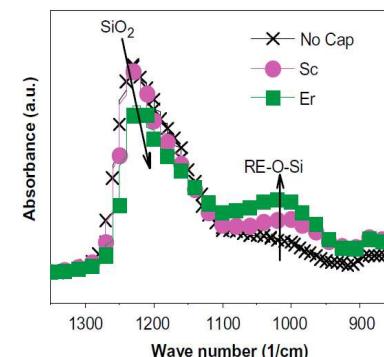
FTIR-ATR complementary results



→ without La_2O_3 capping

- formation of Hf-O-Si bonds

→ with La_2O_3 capping



Hsing-Huang Tseng, Microelectronic Engineering (2009)

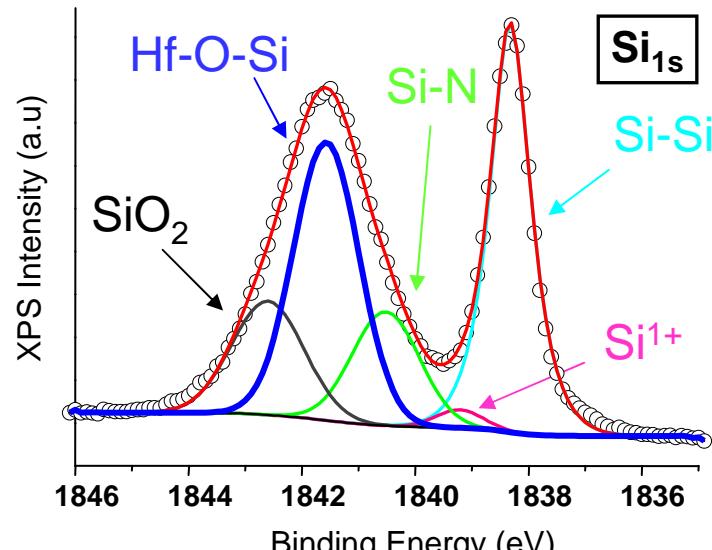
- formation of La-O-Si bonds
- Consumption of the bottom SiON interface

→ La reaches the SiON IL

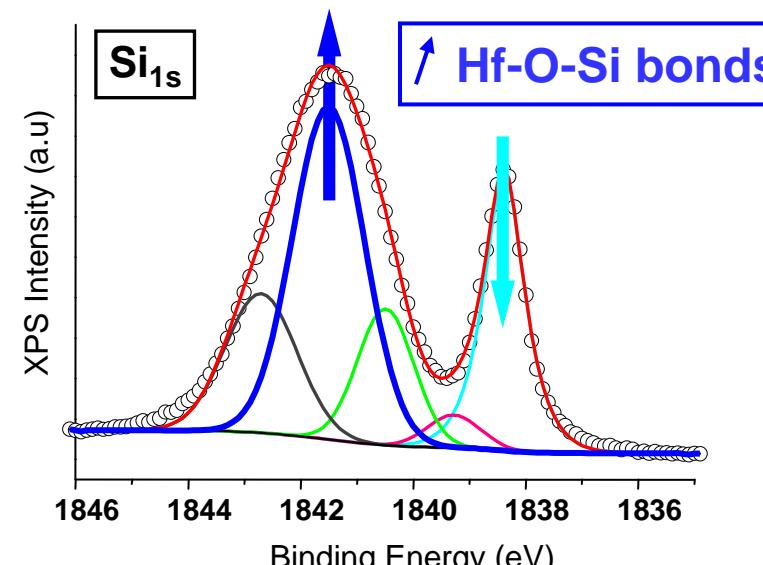
Bonding states – references



▪ Stacks without La_2O_3



Asdep

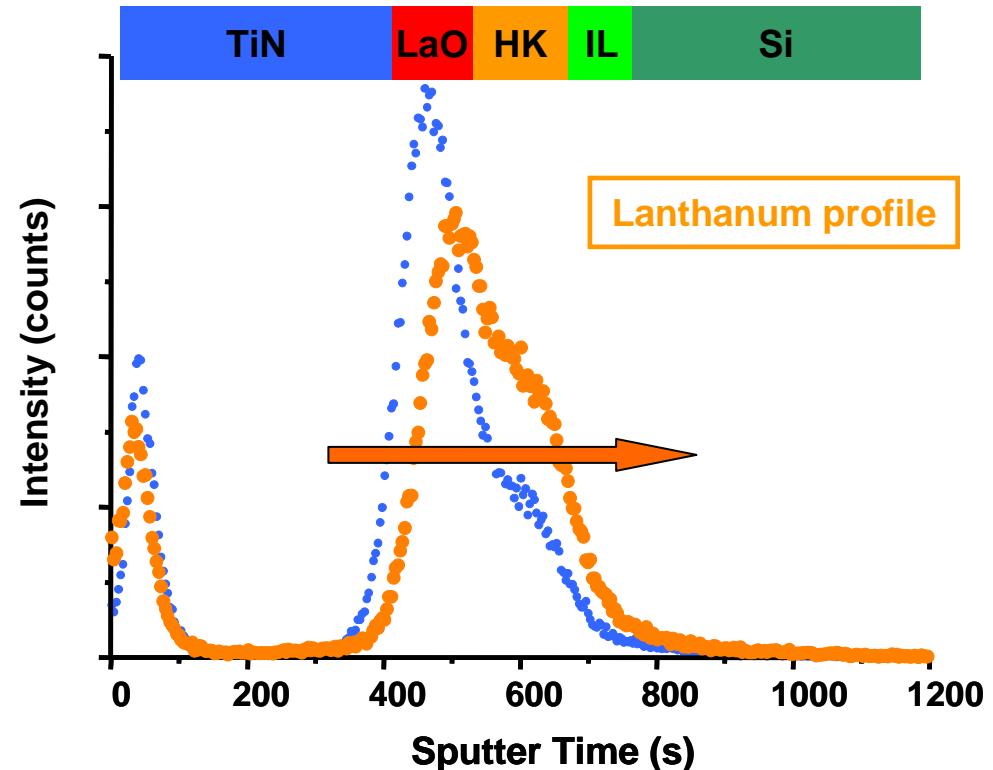
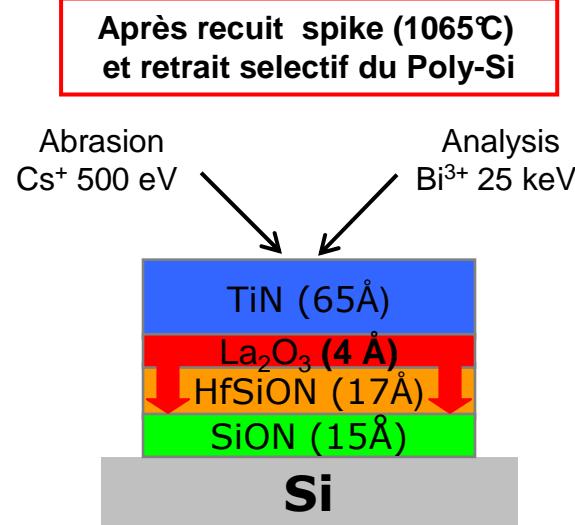


1065°C Anneal

L. Green, JAP 90 (5), 2057 (2001); Vasquez et al., APL 44 (10), 969 (1984);
O. Renault, APL 81, 3627 (2002)

Complementary ToF-SIMS results

- Analyse TOF-SIMS



→ Good correlation between HAXPES results and ToF-SIMS profiles regarding La diffusion through HfSiON

Interfacial dipole – O_{1s}

