WP1.2

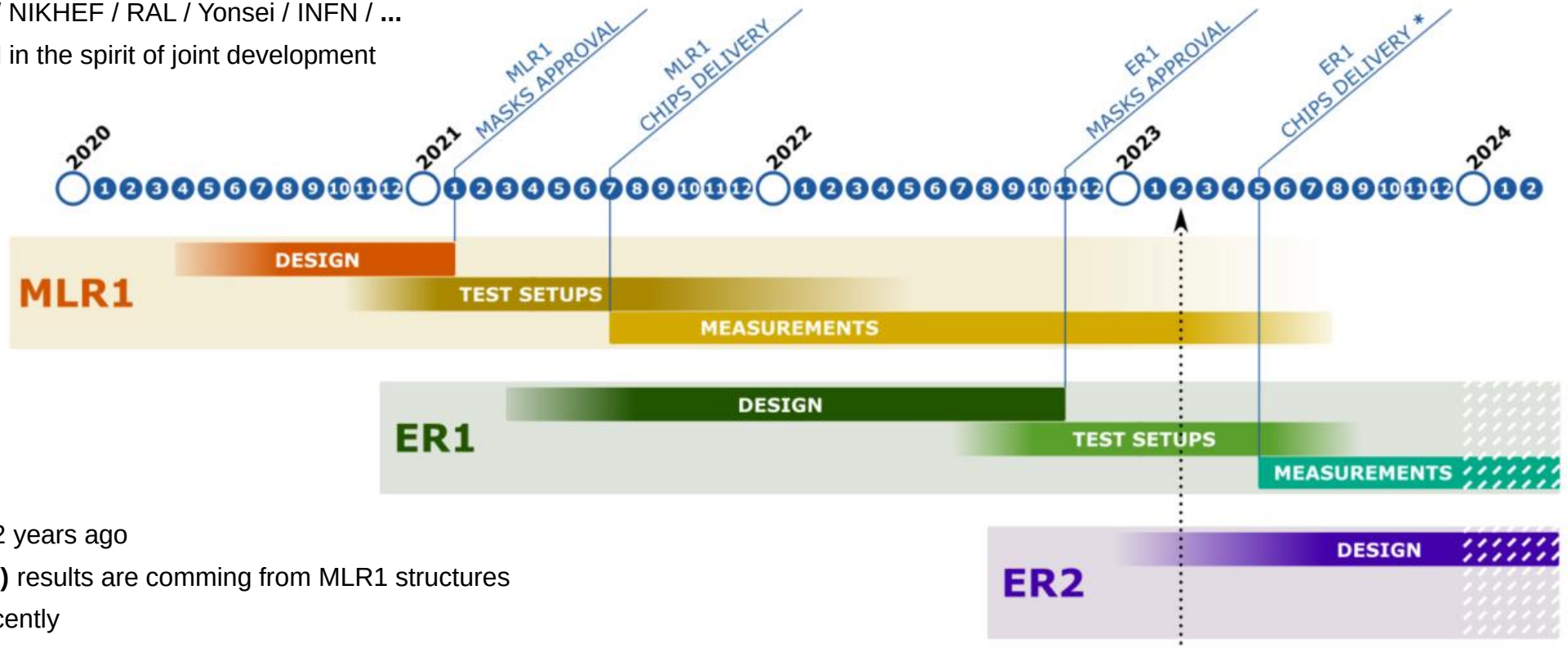
Activities on Monolithic Active Pixel Sensors in 65 nm CMOS technology

Szymon Bugiel

EURIZON meeting 9-10.02.2023

TPSCo. 65 nm development timeline

- **TPSCo. (joint venture TJ & Panasonic) 65nm development done in the framework of WP1.2 EP R&D and ALICE ITS3**
  - 2D stitching possible
  - Initially (MLR1) 5 metal layers, now 7 metals
- **Collaborative effort undertaken by many institutes**
  - CERN / CPPM / DESY / IPHC / NIKHEF / RAL / Yonsei / INFN / **...**
  - Very well coordinated by CERN in the spirit of joint development

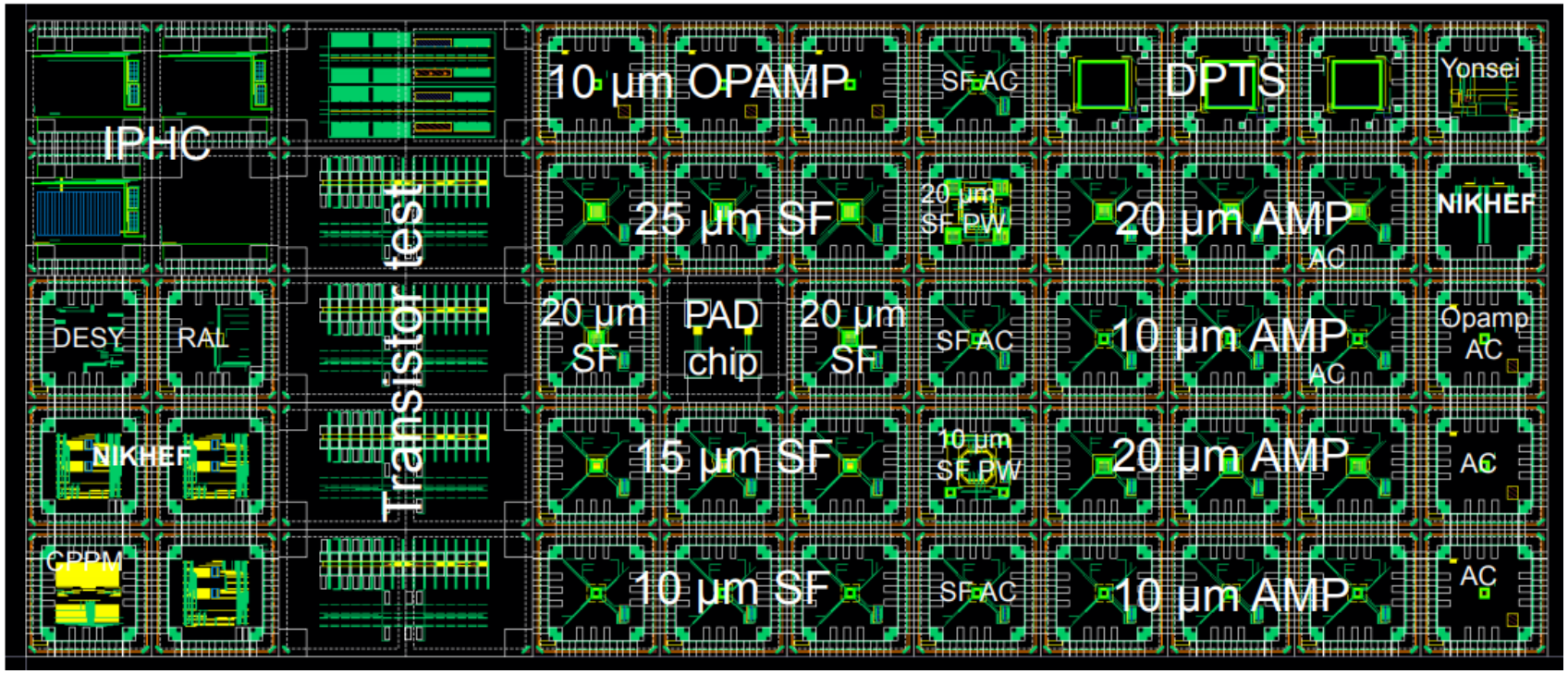


- **Where are we at the moment?**
  - First submission done already 2 years ago
  - Numerous **(very encouraging!)** results are comming from MLR1 structures
  - Second submission finished recently
  - Ongoing activities concentrated around:
    - preparation of the test setups for ER1 chips
    - kicking off the ER2 design (defining specs, collecting ideas, converging on the architecture)

First submission (MLR1)

MLR1 Objectives:

- **Technology validation**
  - transfer 10-year experience from TJ 180nm to 65nm (proces modification: standard / n-gap / blanket)
  - detection performance
  - radiation hardness
- **Design know-how**
  - understanding the design kit limitation/features
  - getting familiarity with IO structure
- **Delivering first batch of common functional blocks**
  - Temperature sensor
  - Bandgap
  - DAC
  - LVDS/CML
  - ....
- **Final approval/masks ordering early January 2021**
  - unified reticle size 1.5 x 1.5 mm^2
  - **55 different chips submitted!**
- **Chip delivered in July 2021**
  - extensive test program started straight away



From: „Ongoing activities and status of the 65 nm MLR1 submission" by W. Snoeys

MLR1: IPHC CONTRIBUTION

FOUR `CE65` CHIPS SUBMITTED:

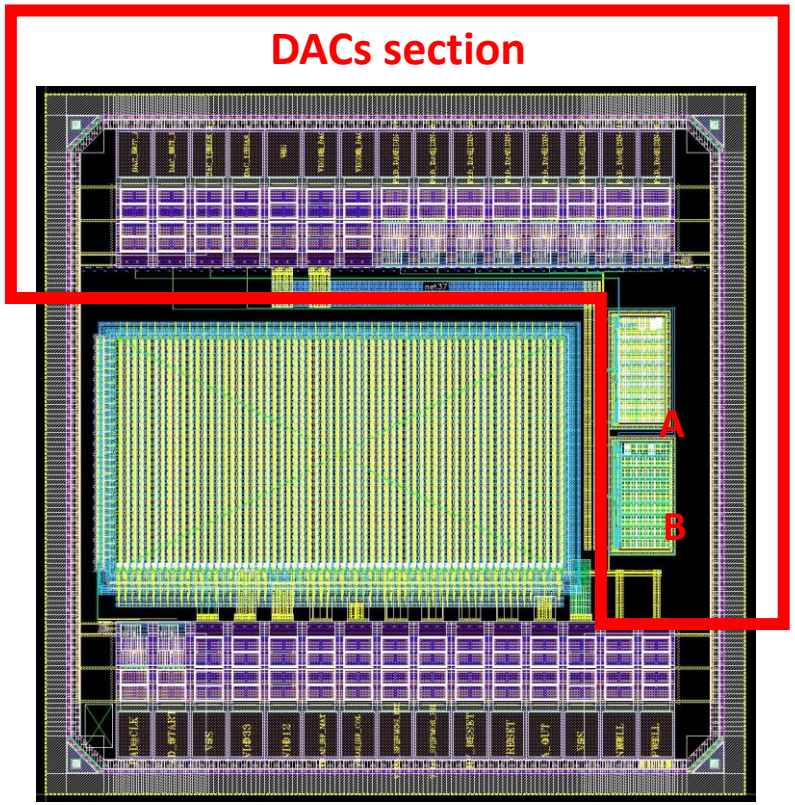
- Each with a relatively small matrix (~0.5 and 1 mm^2), but large enough to be suitable for beam tests
- **Aimed to study:**
  - charge collection properties
  - different front-end options

➢ Variant A/B/C

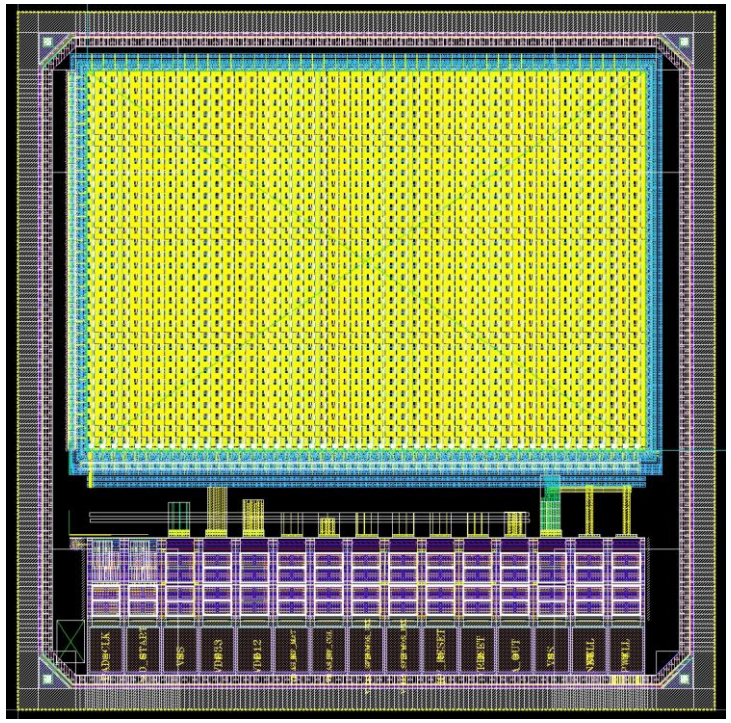
- pixel pitch: 15um
- matrix size: 64x32
- Different sensing node geometries (lessons from TJ180)
  A → standard collection electrode
  B → n-gap
  C → n-blanket
- Hosts also 8`b DAC`s prototypes

➢ Variant D

- pixel pitch: 25um
- matrix size: 48x32
- basic collection electrode geometry



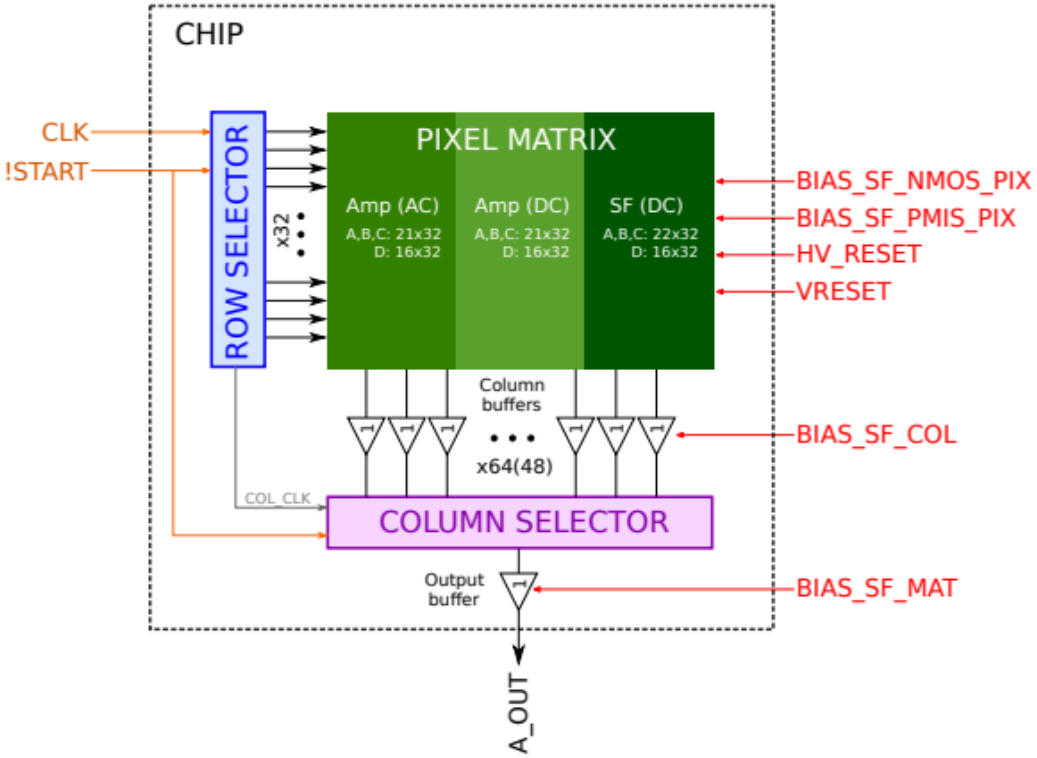
Variants A/B/C



Variant D

CE65 MATRIX DESIGN OVERVIEW

- **Rolling shutter readout**
- **Integration time down to 50 us (@40MHz clk)**
- **External digitization**
- **Three sub-matrices:**
  - AC coupled pre-amplifier [Amp (AC)]
  - DC coupled pre-amplifier [Amp (DC)]
  - DC coupled source-follower [SF (DC)]



SF pixel:

- The simplest approach
- Allows for a direct estimation of input capacitance

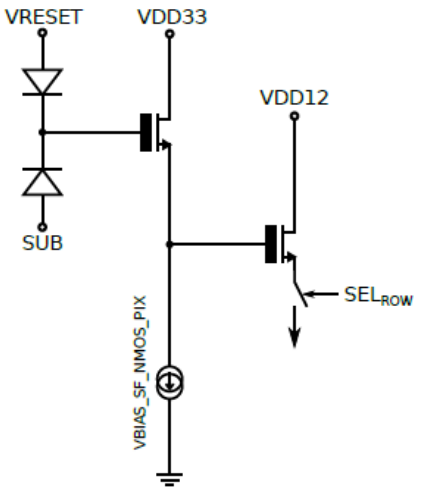
DC AMP:

- Self-biased
- Input node voltage determined by the pre-amp operating point
- In-pixel gain →potencially improved SNR

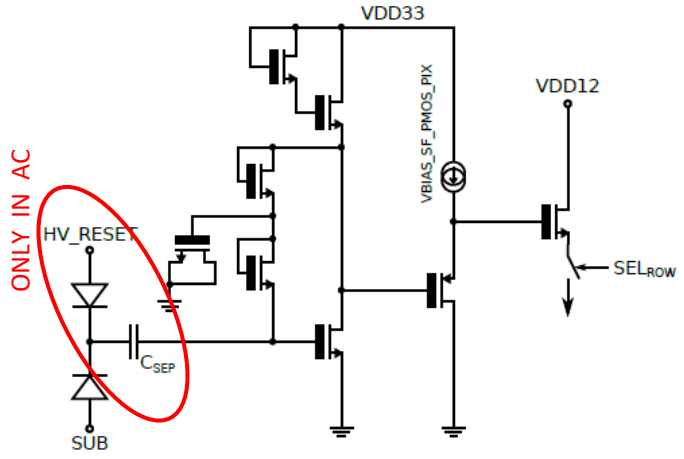
AC AMP:

- Sensing node depletion voltage can be applied independently and go over the supply voltage
- Slightly reduced gain in comparision with DC Amp due to parasitic capacitances

DC SF pixel



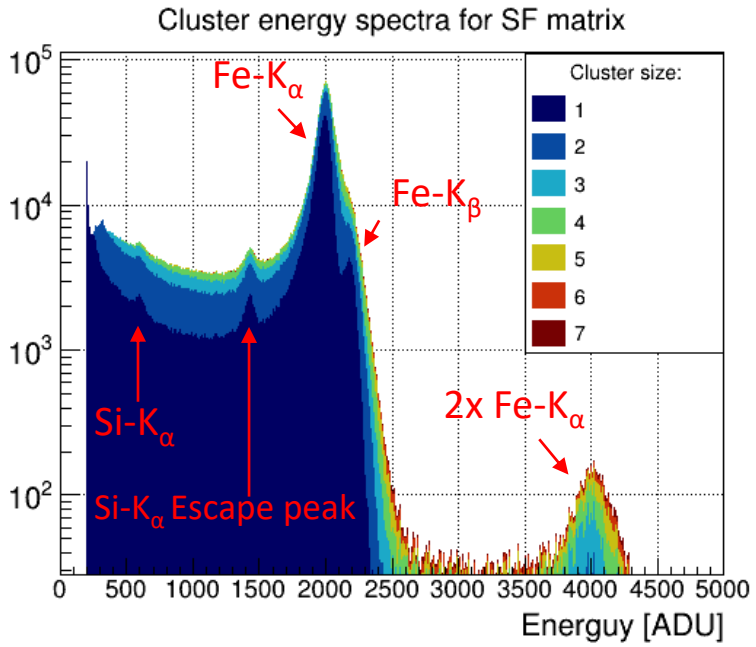
AC/DC pre-amp pixel



CE65: SELECTED RESULTS

➢ **^{55}FeSpectra shown for Source-Followers sub-matrix with n-gap sensor**

- gain correction applied to enchance spectra quality
- resolution limited by the readout frequency (signal discharge between samples)
- **5 peaks clearly visible:**
  - Si(K_α) = 1.74 keV
  - Si(K_α) escape peak (FeK_α – SiK_α=4.16 keV)
  - Fe(K_α) = 5.9 keV
  - Fe(K_β) = 6.49 keV
  - 2x Fe(K_α)= 11.8 keV
- similar behaviour observed on others structures with this sensor geometry
- all peak positions well alligned with respect to theirs energies (linear front-end response)

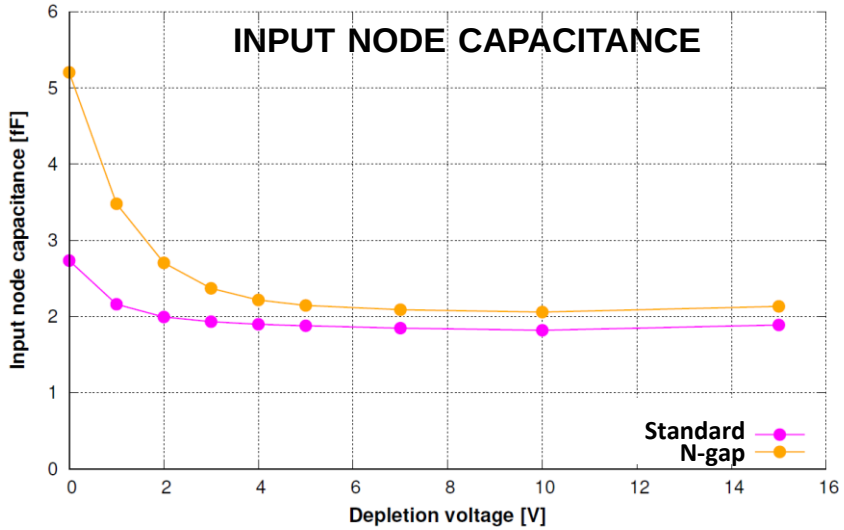


➢ **Input node capacitance for the SF-structre:**

- Indirectly obtained from the measurements by:
  - taking into account gain calibration curve
  - assuming 3.6 eV for e-h pair generation
  - using the ^{55}Fe calibration peak

➢ **Input node capacitance for the SF-structure (@ 3.3V of the depletion voltage):**

- $C_{IN}^{A4} \approx 1.9$ fF
- $C_{IN}^{B4} \approx 2.4$ fF



➢ **By extrapolating this on AC-amplifier structure one can study capacitance evolution with the reverse bias apllied.**

- **Maximal depletion reached around 4 – 5V**
- n-gap diode have gives higher capacitance when not completely depleted
- **in both cases ~2fF is in reach**

CE65: Selected results

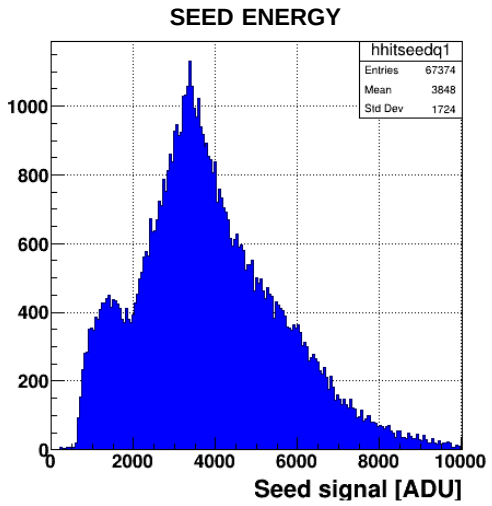
Diode geometries comarision based DC-Amp submatrix:

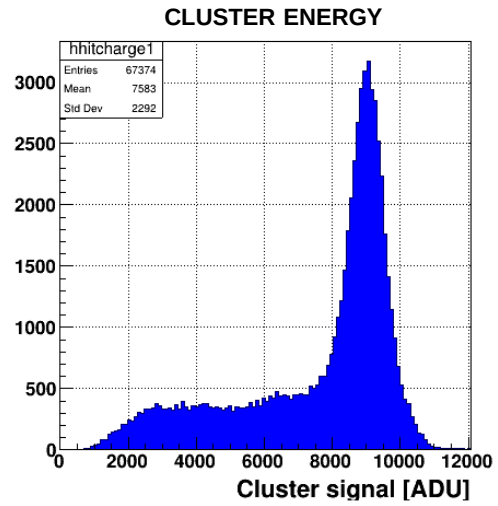
- **Reverse bias:**
  - **1V** (self biased)
  - far from maximal depletion

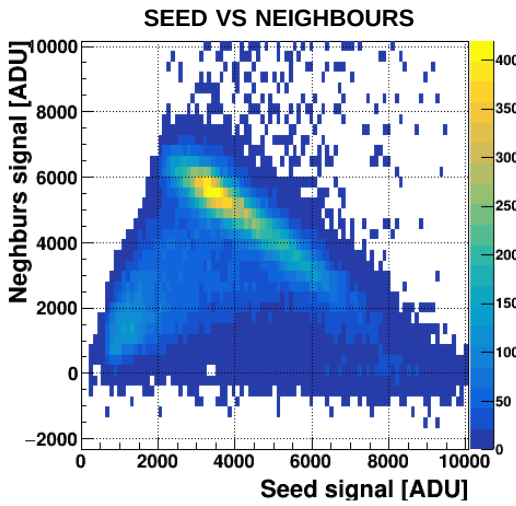
- **Total cluster energy depends on the diode geometry**
  - ~40% larger gain of a standard structure
  - n-gap diode has larger capacitance when not depleted

- **Significant difference in the charge sharing**
  - **n-gap diode:**
    - **dominated by single pixel depositions**
    - seed energy spectrum similar to cluster energy spectrum
  - **standard diode:**
    - **significant charge sharing**
    - almost no single pixel depositions
  - effect very pronaunced because of relatively small depletion voltage

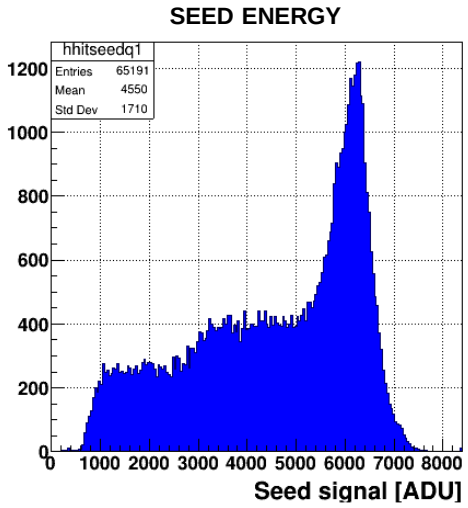
STANDARD DIODE:

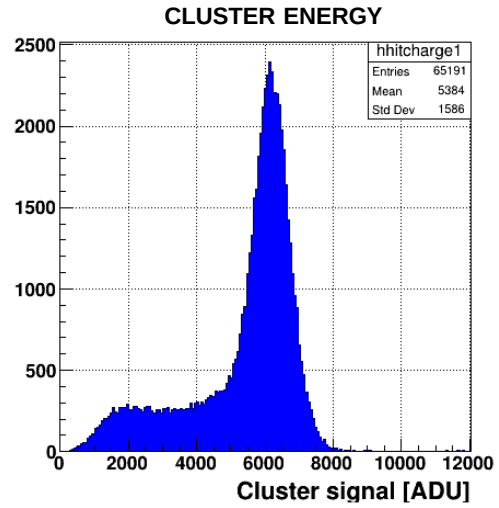


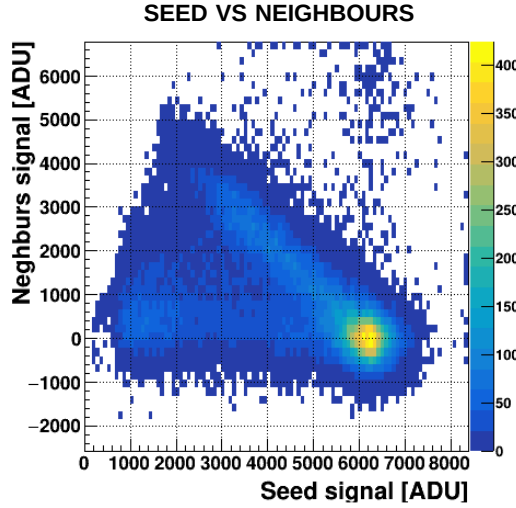




N-GAP DIODE:



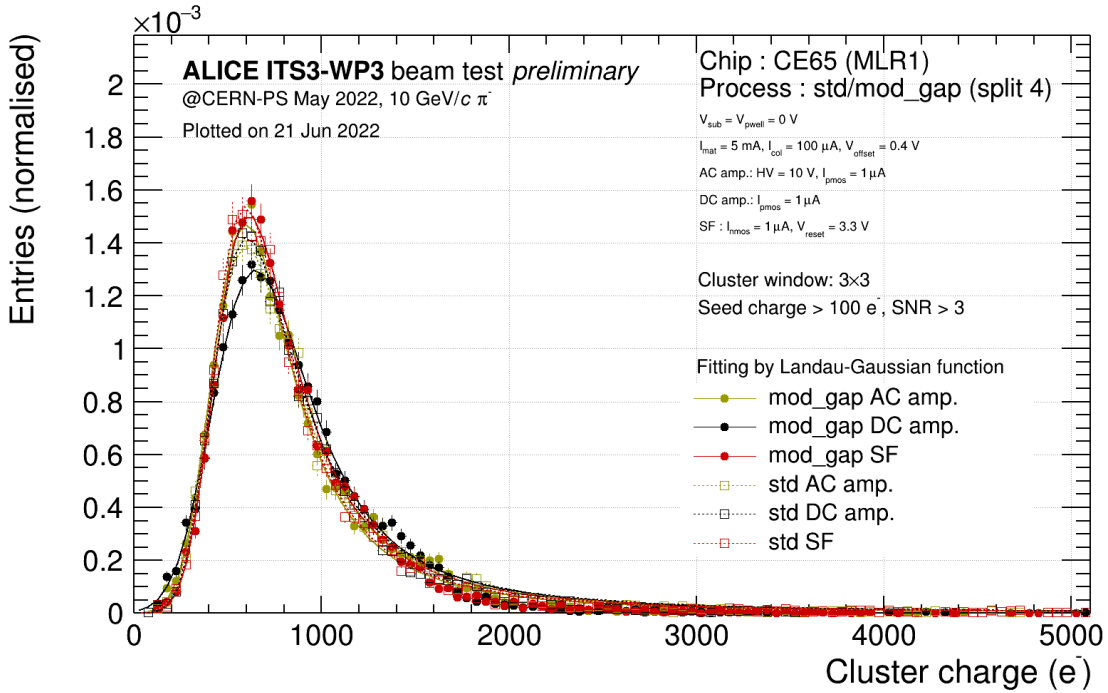




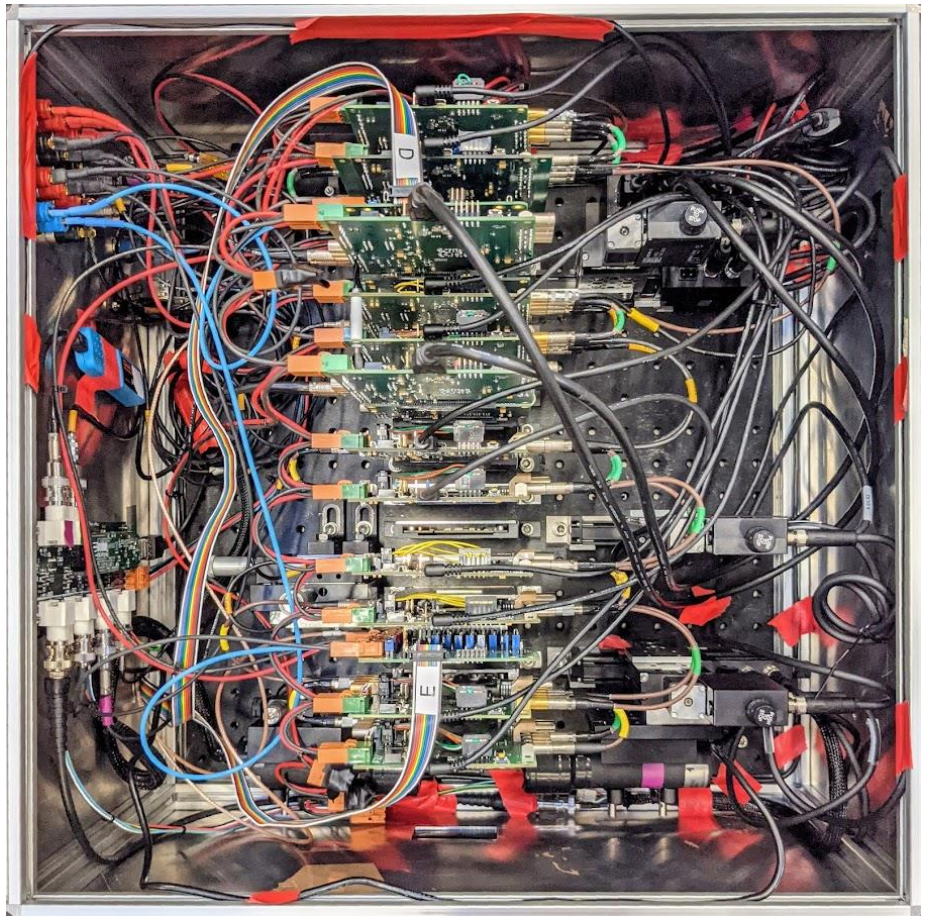
CE65: Beam test

- **Numerous test beams performed:**
  - Significant effort from ALICE ITS3 team
  - Tracking made with Alpide telescope
  - Aimed to measure all different MLR1 devices (including CE65)
  - **CE65 readout integrated with the telescope infrastructure and validated**

- **Beam data analysis is still ongoing:**
  - Cluster charge distribution MPV around 600e$^-$
    → **epi-layer thickness ~11 um**
    → inline with what was declared



- **Excellent detection efficiency already proven with others structures:**
  - **Maintained up to 10^15 1MeV n_{eq} cm^{-2}**
  - See: DPTS paper https://arxiv.org/pdf/2212.08621.pdf
    and APTS https://dx.doi.org/10.1088/1748-0221/18/01/C01065



SECOND SUBMISSION (ER1)

*(more comming up in slide 11.)

ER1 OBJECTIVES:

- **Develop stitching know-how**
  - Yield estimate
  - Defects „masking”
  - Power distribution
  - Sensor depletion
  - Waferscale spreads
  - Methodology

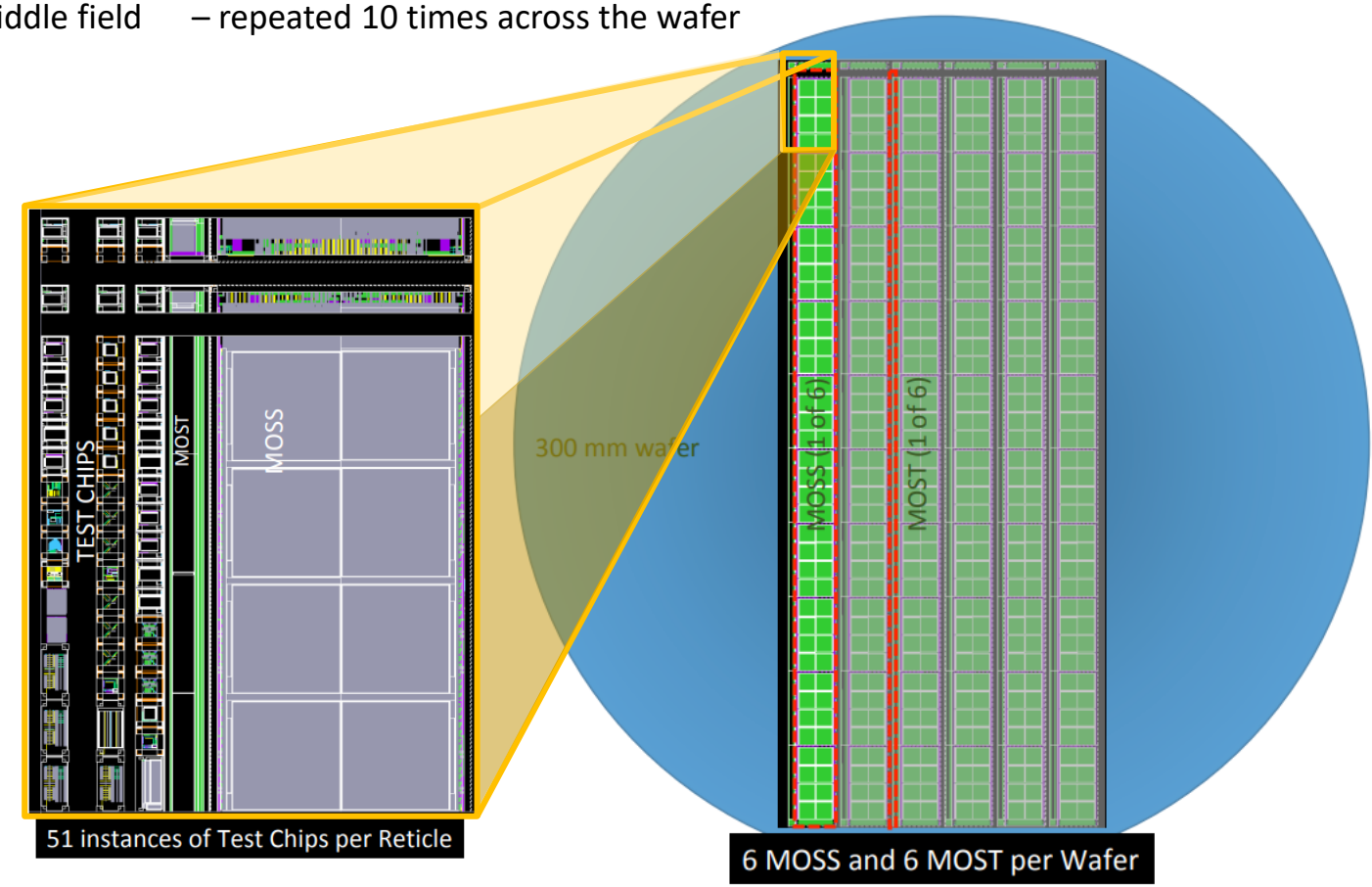
  } MOSS, MOST

- **Continue R&D program**
  - Second batch of small exploratory detectors -- CE65v2, …
  - SEU chip

- **Additional set of functional blocks:**
  - PLL
  - LDO
  - DATA LINKS
  - ....

Wafer-scale detector is a key component for the ALICE inner tracker upgrade

- 1D-stitching is enough (along the beam axis)
- Reticle composed of:
  - endcap fields – printed only on the outer edges
  - middle field – repeated 10 times across the wafer



- **Final masks approval November 2022**
  - Production proces has already begun
  - **Expected delivery date – end of April**

- **Intensive work on tests setups preparation ongoing**
  - Goal is to be ready before chips arrival
  - Essential input for a ER2 design

From: „EP R&D WP1.2 Status Report, 01/06/2022” by W. Snoeys

MOSS, MOST, CE65v2 Highlights

MOSS: (MOnolithic Stitched Sensor)

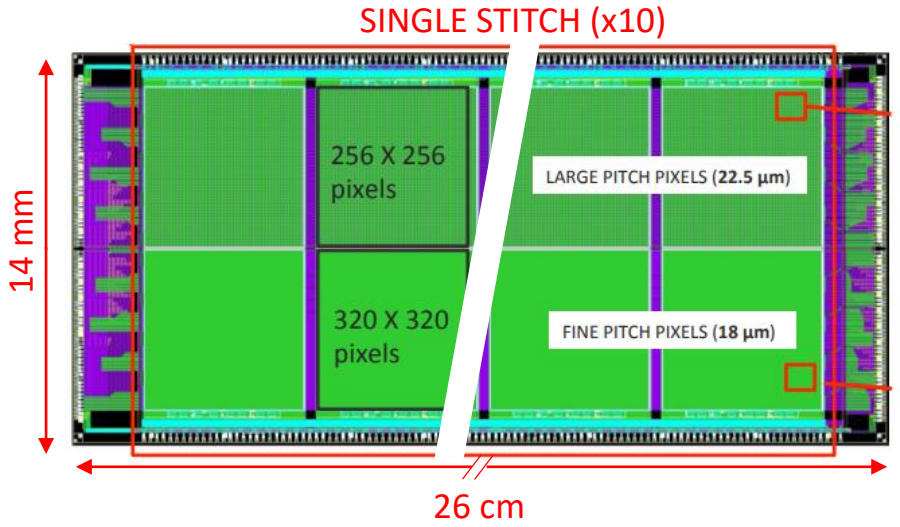
- Design lead by CERN
- **14 mm x 259 mm**
- Two pixel pitches: 18um and 22.5um
- Modification of well established, Alpide-like readout scheme (digital)
- 67 separate power domains
- Local defects mitigated by switching off given power domain (1/20 of full chip)
- Conservative layout (Design For Manufacturing rules fullfiled)

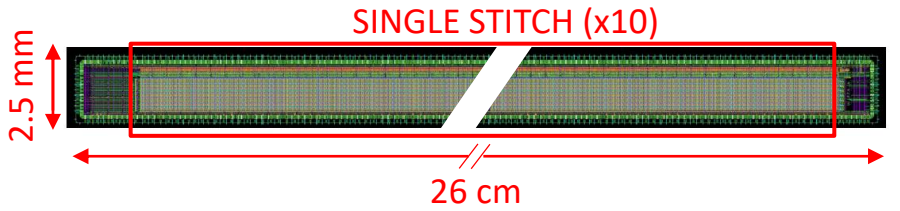
MOST: (MOnolithic Stitched sensor with Timing)

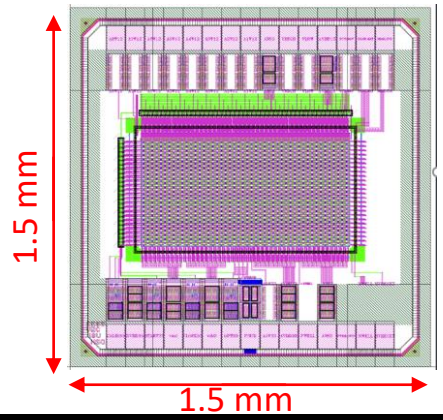
- Design lead by CERN
- **2.5 mm x 259 mm**
- Pixel pitch: 18um
- Asynchronous hit-driven readout (ToA + ToT information)
- 4 power domains
- High granularity local power gating to mitigate defects
- High local density preserved

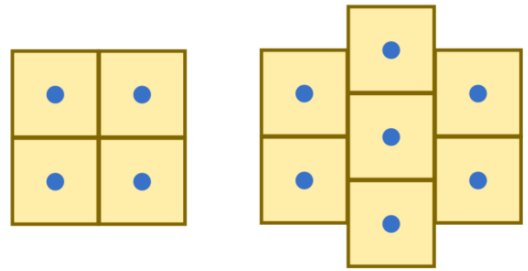
CE65 v2:

- 48x24 pixels (AC Amp)
- Rolling shutter readout
- 15 flawours:
  - pitch 15/18/22.5um
  - 3 sensor geometries (standard, gap, blanket)
  - **squared / hex-squared pixel arrangment**









Squared pixel arrangment

Hex-Squared pixel arrangment

Towards ER2

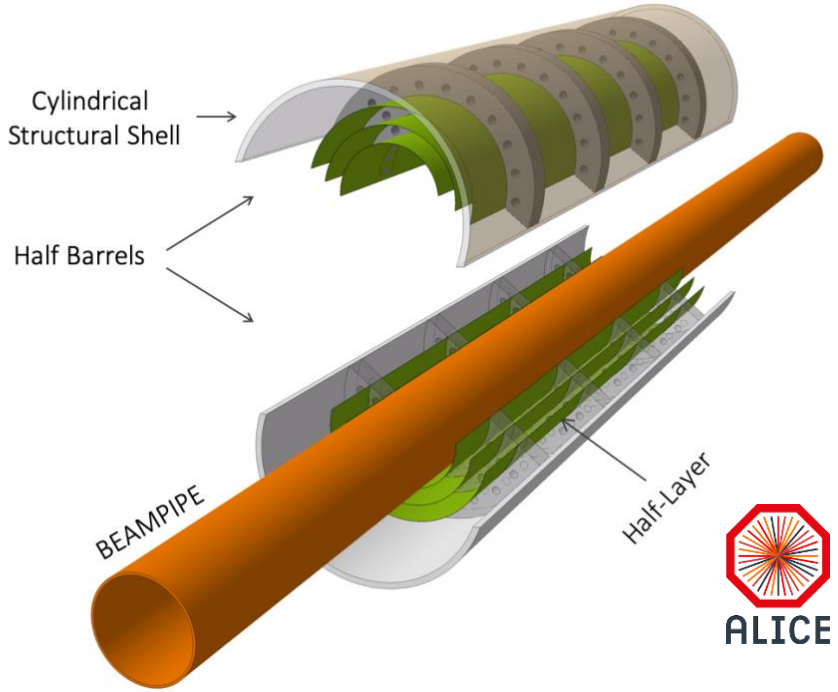
ER2 Objectives:

- Deliver a first prototype targeting ALICE ITS3 (Inner Tracking System)

ITS Upgrade (ITS2 → ITS3):

- Replacement of 3 inner-most tracking layers
- Significant reduction of material budget by:
  - Removing water cooling system → power consumption < 20 mW/cm2
  - Removing flex cabeling → power distribution / data links on chip
  - Removing suport leaders → use stiffness of bend silicon (<50um thick & wafer scale detector)

Only silicon left



- First truly cilindrical tracker
- Many challanges imposed on detector

→ Exploring completely new teritories

- **Input from ER1 structures measurements becomes critical**

Dummy silicon model

From: „ ALICE ITS3 – a next generation vertex detector based on bent, wafer-scale CMOS sensors*" by* M. Mager
https://indico.cern.ch/event/1071914

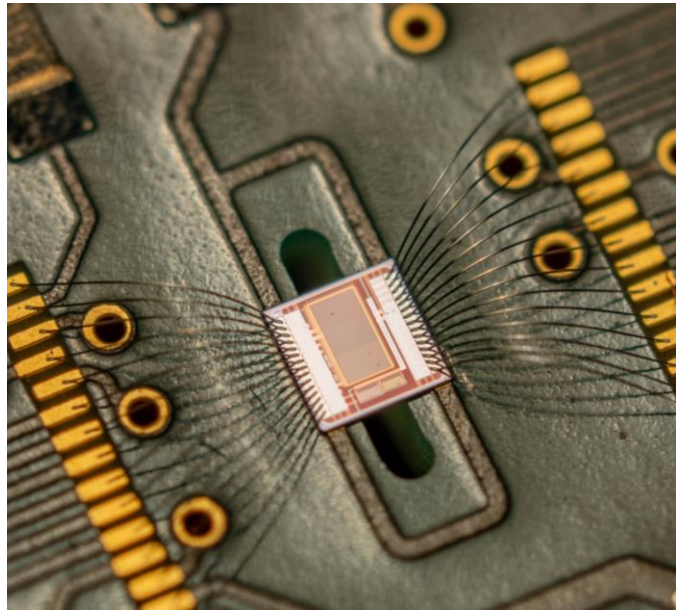
SUMMARY

- **SIGNIFICANT EFFORT MADE TO VALIDATE THE TECHNOLOGY WITH THE MLR1 STRUCTURES:**
  - Lessons learned with TJ180 sucessfully transfered to 65nm
  - No showstopper discovered up to now
  - Radiation tolerance and detection efficiency already proven
  - Spatial resolution below 4 um achieved with the digital pixel
  - Efforts on many different fronts
    → a lot of experience and confidence gained
  - Detailed studies still provide feedback important for the next designs

- **PRODUCTION OF ER1 STARTED RECENTLY:**
  - Gathering stitching know-how
    - Methodology
    - Design
    - Chips handling & testing
    - Yield
  - Very important input for ER2
  - Continuation of R&D activities
  - Widen set of silicon proven functional blocks

- **NEXT STEP - ER2 DESIGN:**
  - Defining specs
  - Collecting all the learnings from ER1
  - Isolating fields for improvement

- **FOR MORE**
  - M.Šuljić at al. *„Digital Pixel Test Structures implemented in a 65 nm CMOS proces”* (https://arxiv.org/pdf/2212.08621.pdf)
  - S. Bugiel et al. „*Charge sensing properties of monolithic CMOS pixel sensors fabricated in a 65 nm technology”* (https://doi.org/10.1016/j.nima.2022.167213)
  - G. Aglieri et al., „*Developments of stitched monolithic pixel sensors towards the application in the ALICE ITS3”* (https://doi.org/10.1016/j.nima.2023.168018)
  - W. Snoeys, „*Optimization of a 65 nm CMOS imaging technology for monolithic sensors for high energy physic”* PIXEL 2022 (https://indico.cern.ch/event/829863/contributions/5053903/)
  - M. Mager, *„ ALICE ITS3 – a next generation vertex detector based on bent, wafer-scale CMOS sensors”* (https://indico.cern.ch/event/1071914)
  - S. Senyukov, *„Exploration of the TPSCo 65 nm CMOS imaging process for building wafer-scale, thin and flexible detection layers for the ALICE Inner Tracking System upgrade (ITS3), iWoRiD 2022”*
  - …



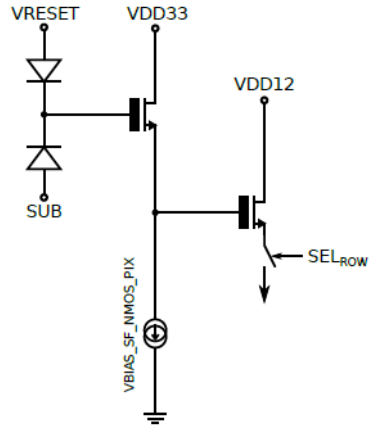
This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No. 871072

BACK-UP

CE65 Calibration

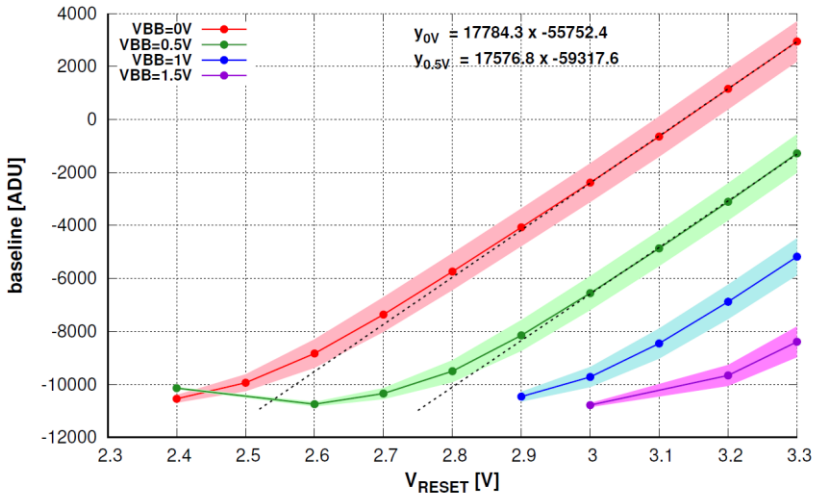
Readout Chain Calibration:

- Precise determinatin of conversion factor between the ADC units and input voltage level made using SF submatrix
- Monitoring baseline shift while scanning over the V_{RESET}

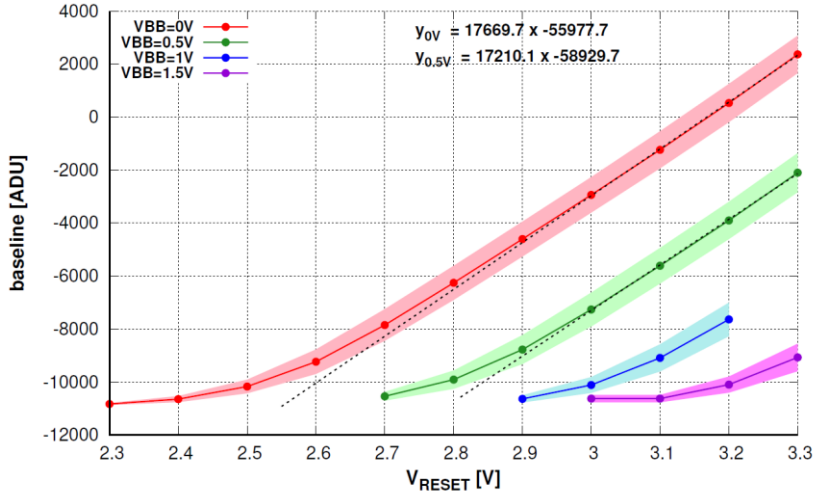


- Very small influnce of the back bias on the readout gain
- Significant shift of the DC levels after applying back bias
  → source followers out of dynamic range at VBB>1V
  → probably even faster for the amplifier based pixels
- Almost impossible to use back bias to enhance the depletion
- All results presented for VBB = 0V

Basic diode [A4]:



Optimized diode [B4]:



CE65 Readout System

DAQ BOARDS:

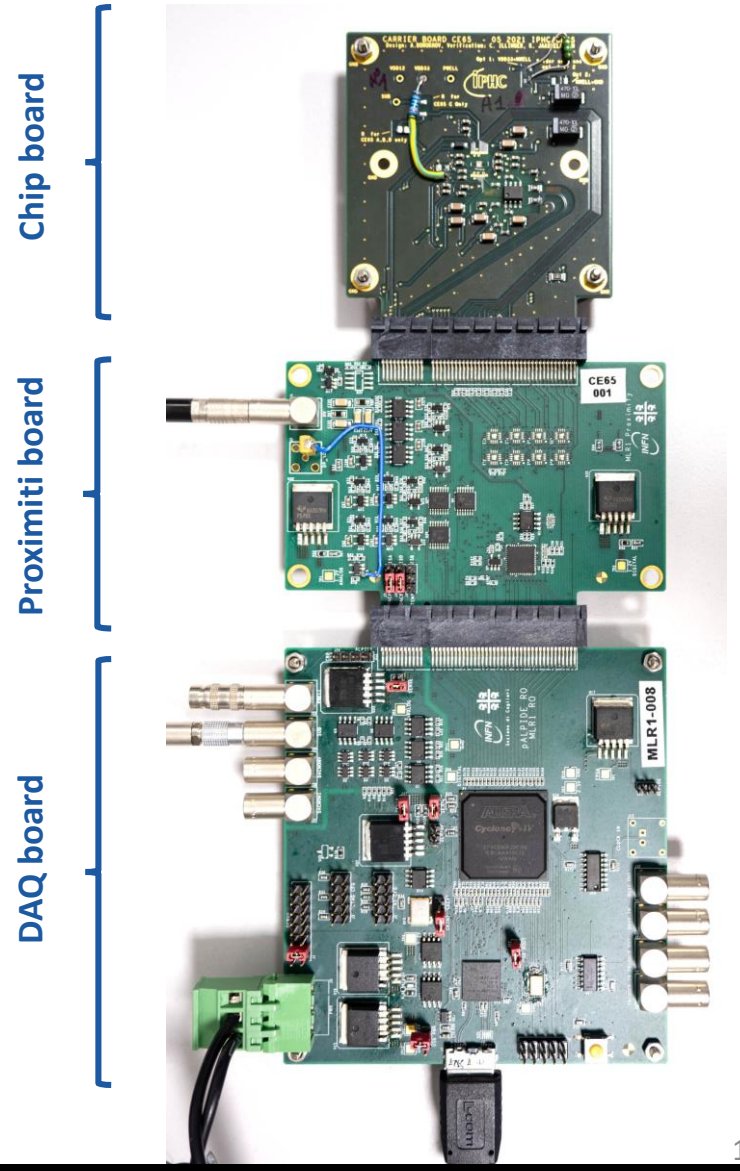
- PCB and firmware developed by the team from Cagliari University & INFN
- Common readout system for multiple MLR1 devices (CE65, APTS, DPTS)
- Based on Altera Cyclone IV FPGA
- Readout speed up to 40 MHz
- USB protocol used for the communication with the PC
- Readout software integrated into the EUDAQ framework (compatibility with the beam test infrastructure)

PROXIMITI BOARD:

- PCB developed by the team from Cagliari University & INFN
- Specific for a given device
- Provides all chip biasing
- CE65 proximity equipped with fast 16-bit ADC

CHIP BOARD:

- PCB developed at IPHC
- Analog output buffering
- Decoupling

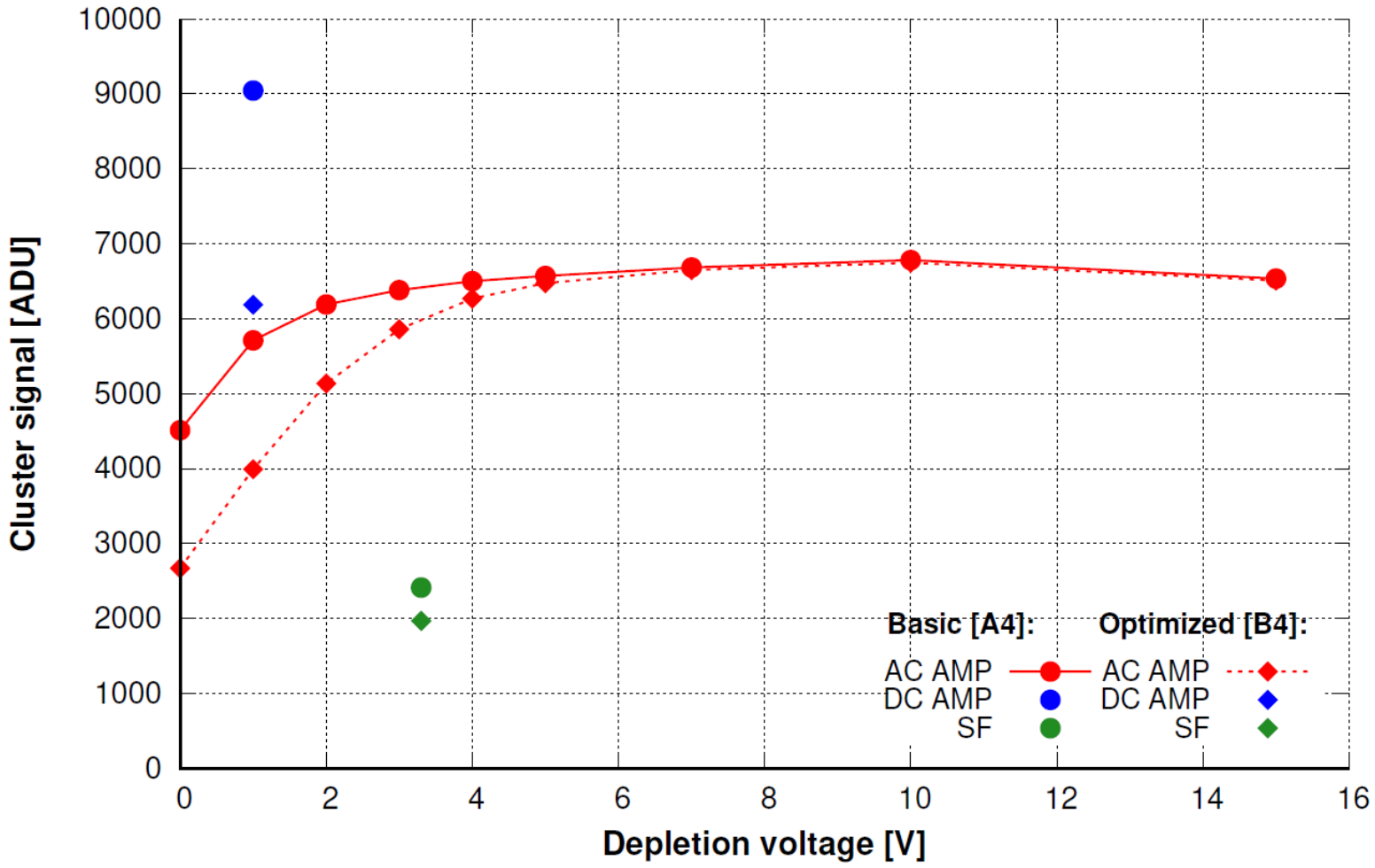


Sensor Depletion Development

- **Sensor depletion can be developed by:**
  - Applying negative voltage to the substrate (back-bias) → not possible for this chip because of accompaning operating point shifts
  - Utilizing AC coupling and directly biasing the collection electrode (HV_RESET)

- **For both sensor geometries depletion develops up to 5V**
  - Above 5V, amplitudes staurates at the same level → for depleted device the detector capacitance does not depend on the sensing node geometry
  - Optimized diode geometry has noticeably larger capacitance when not depleted

- **For DC sub-matrixes only single points available**
  - AC-Amplifier: ~3 times higher gain than SF
  - DC-Amplifier: ~5 times higher gain than SF



Baseline and Noise

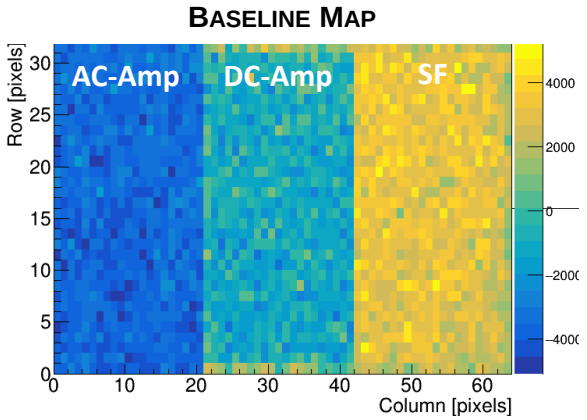
Baseline:

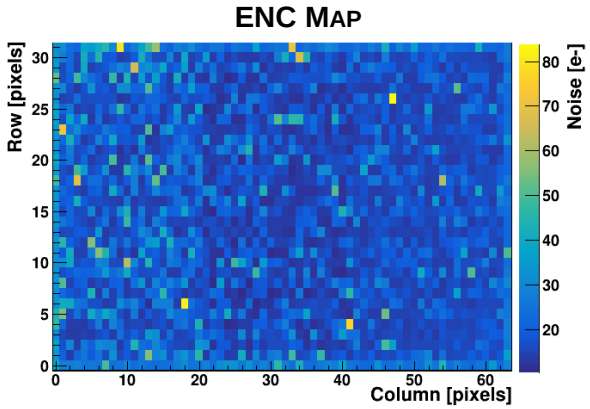
- Clearly visible sub-structure on the baseline map
  → as expected from the design
- No significant differences in the baselines for different diode flavours
- Edge pixels degradation slightly more pronounced for a standard structure

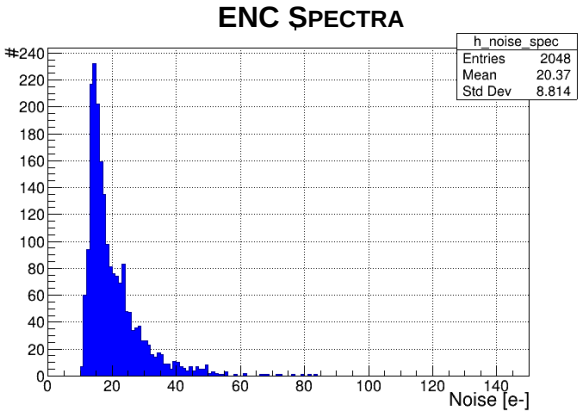
Noise:

- ENC calibrated based on the ^{55}Fe peak position
- No significant differences between the sub-matrices
- ENC measured to be in range **15 e^- : 25 e^-** (depends on the settings optimization, biasing conditions)

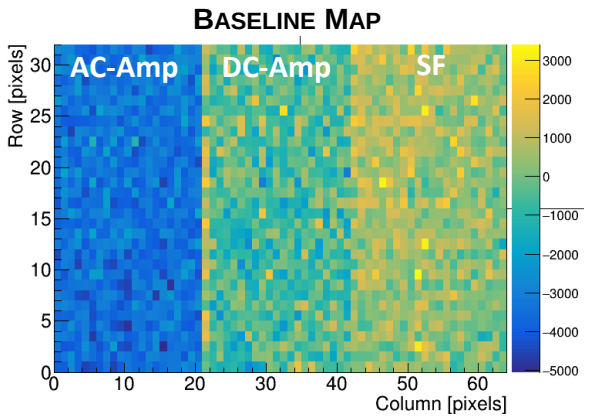
Basic diode [A4]:

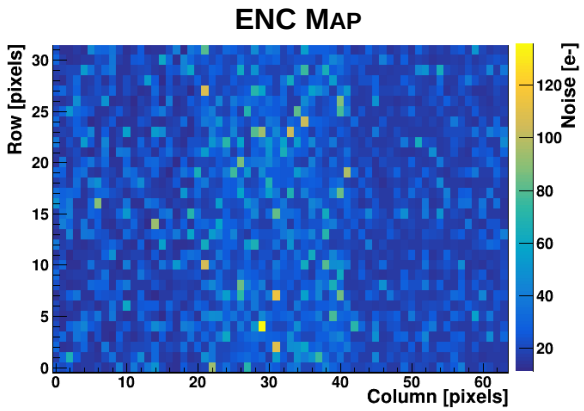


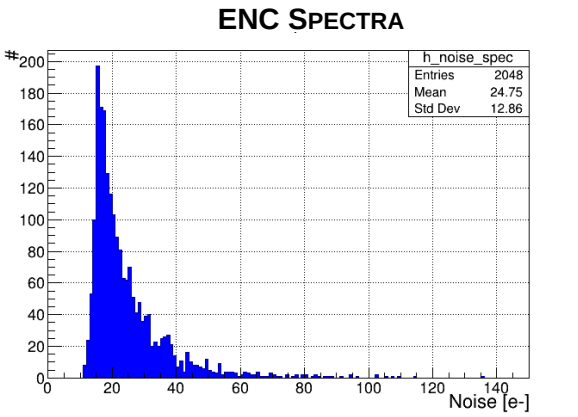




Optimized diode [B4]:







CHARGE SHARING BETWEEN NEIGHBOURING PIXELS

➢ **Exemplary plots shown for DC-Amplifier submatrix**

- Very similar behaviour observed on others structures

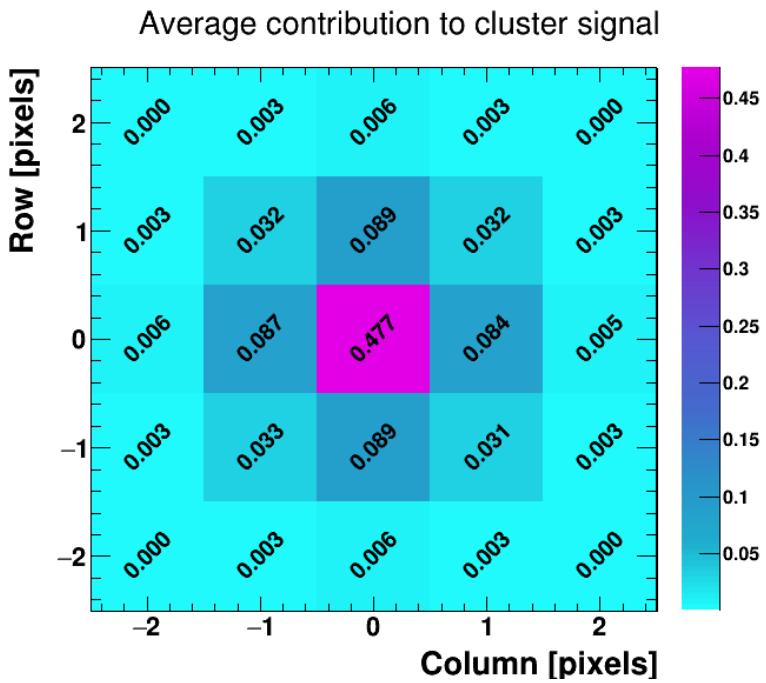
➢ **Results inlined with previous observations:**

- Basic diode:
  - significant charge sharing
  - seed carries less than half of the total charge
- Optimized diode:
  - charge sharing highly suppressed
  - charge concentrated on single pixel
  → more operating margin

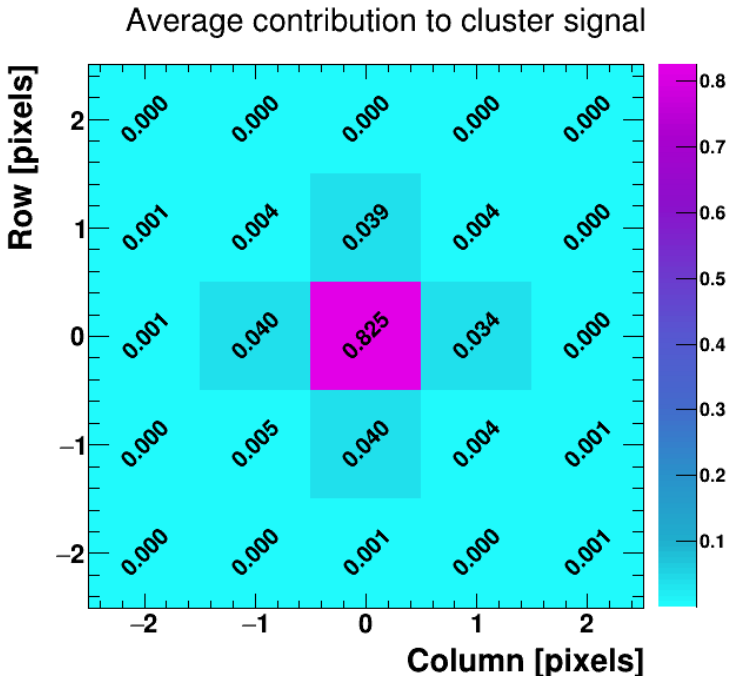
➢ **Consequences:**

- Basic diode:
  - one may expect outstanding spatial resolution
  - harder to maintain high efficiency
- Optimized diode:
  - charges „guided" directly to the closest collection electrode
  that indicates:
  → higher electric field
  → faster collection (higher ToA resolution)
  → more resistant to displacement damages
- Indirect hints → to be verified in direct measurements!

BASIC DIODE [A4]:



OPTIMIZED DIODE [B4]:

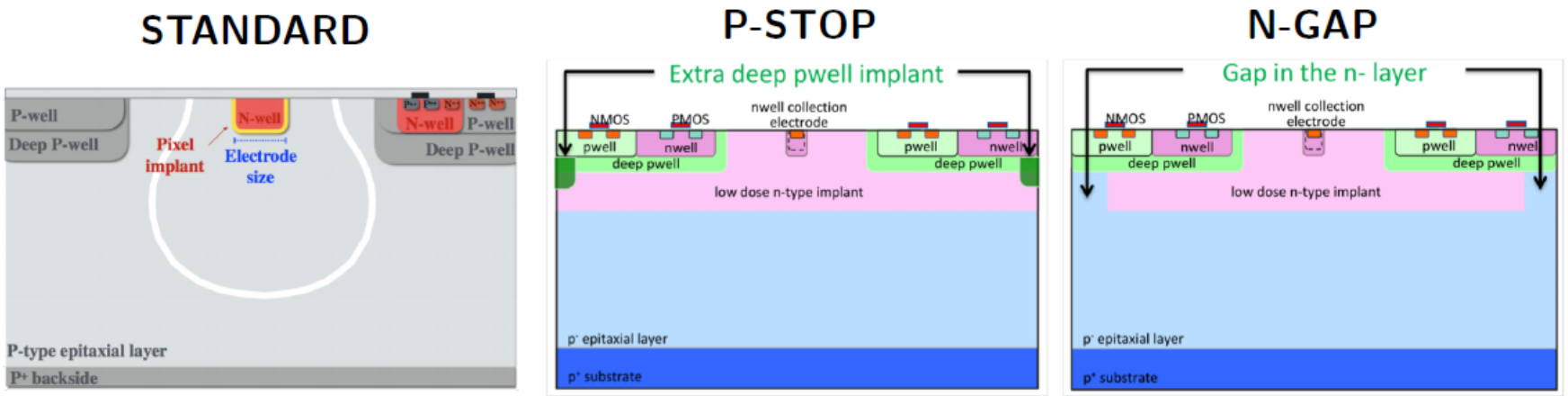


DIODE GEOMETRIES

See the previous talk by R. Bugiel

- TowerJazz CIS 180 nm technology → providing several process modifications and some flexibility on epitaxial layer thickness.
- MIMOSIS-1 available on:
  - **standard process** (3 available wafers)
  - modified process [continuous n+ layer] (3 wafers)
  - **gap in n-layer** [n-gap] (3 wafers)
  - **additional p-implant** [p-stop] (3 wafers)

  → expected improved radiation tolerance
- sensors 300 µm, also thinned to ≈ 60 µm



W. Snoeys et al., NIM-A Vol.871 (2017) 90–96.
Munker, Vertex 2018, Status of silicon detector R&D at CLIC