

# Preparation of the Silicon Tracking System for CBM/FAIR: *progress towards production readiness*

WP2.1

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EURIZON Annual Meeting 2023

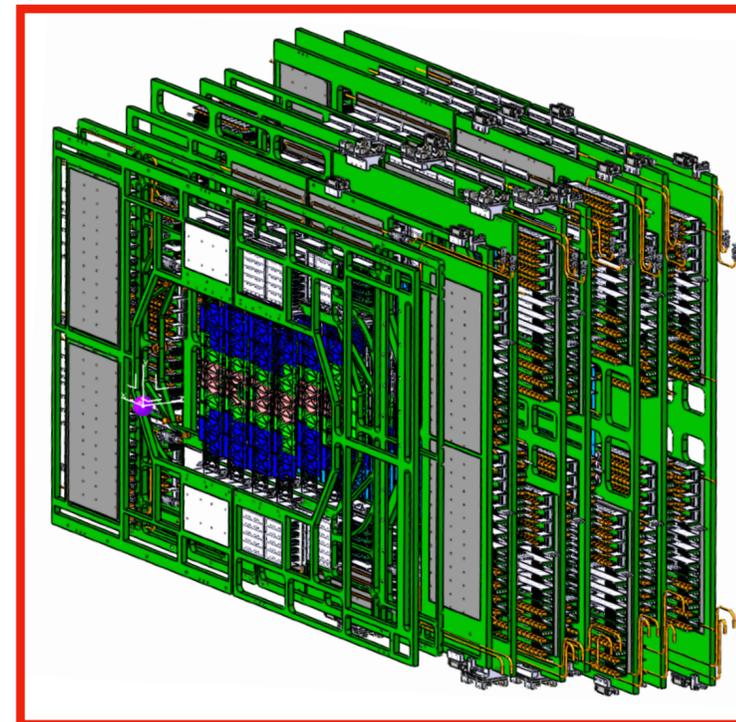
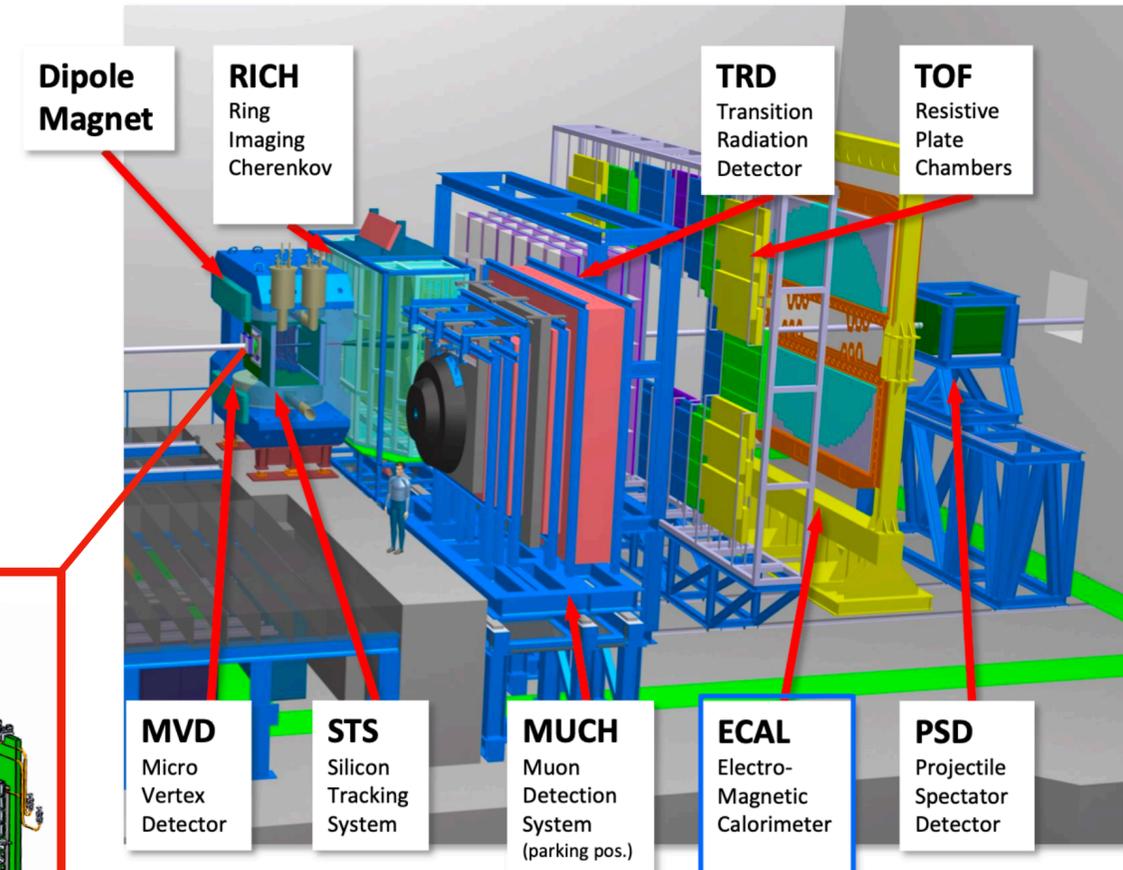
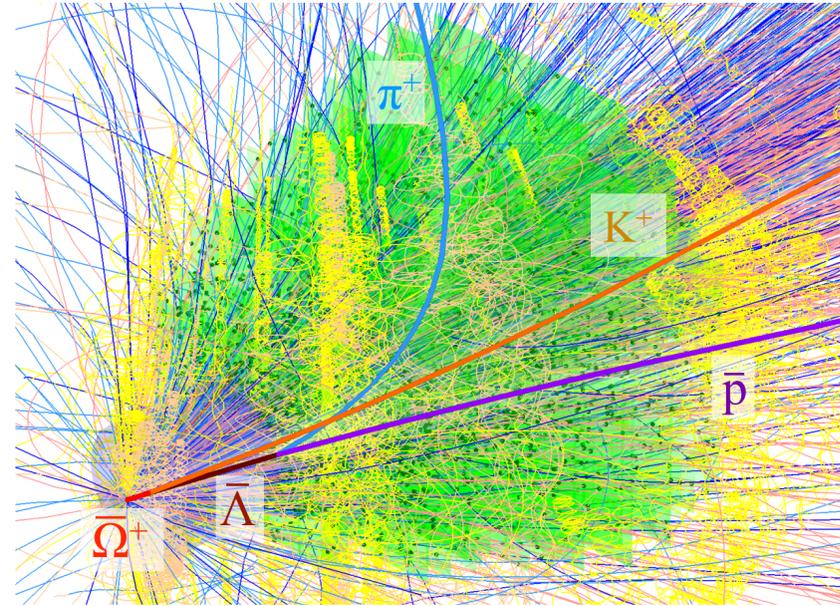
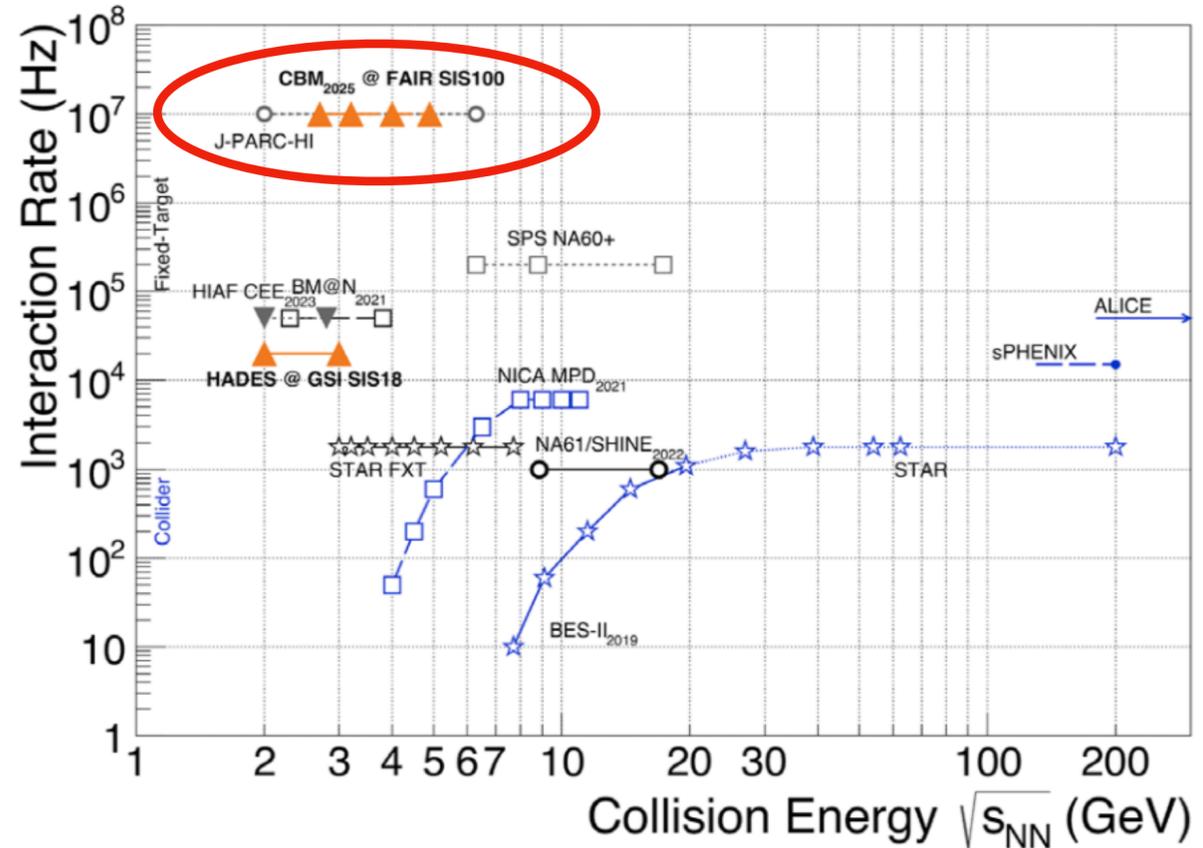


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**eurizon**  
European network  
for developing new horizons for RIs

# Silicon Tracking System of the CBM experiment

key detector for rare probes of compressed nuclear matter in high-rate heavy-ion collisions



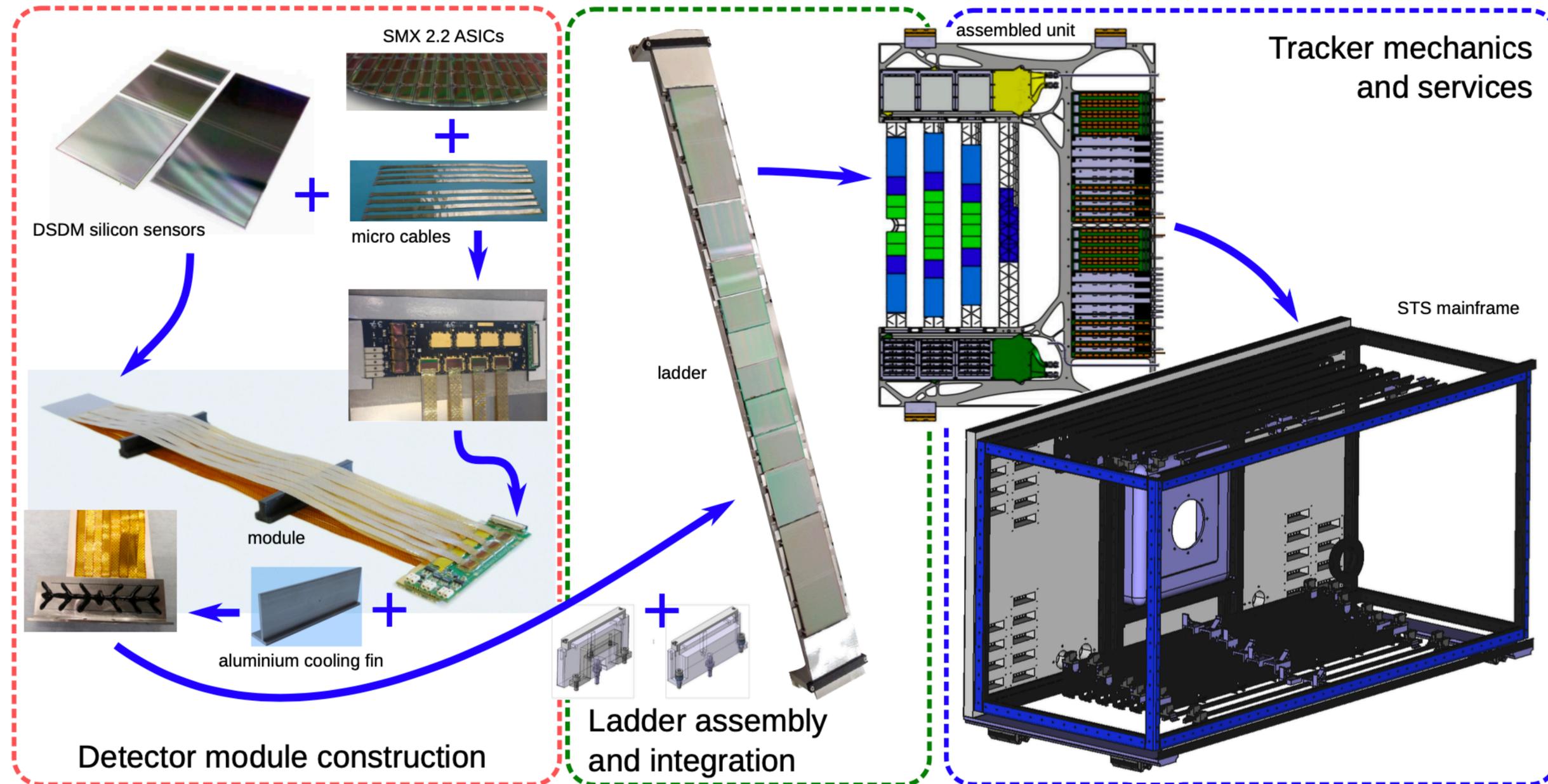
**Silicon Tracking System**

CBM detector setup:

- vertex reconstruction
- tracking
- particle identification
- reaction plane determination

- **Beam-target interactions rates up to 10 MHz**
- Aims at multi-strange hyperon reconstruction
- Tracking challenge:
  - **up to 700 ch. particle tracks/coll. in aperture**
  - **low momentum → low mat. budget (3÷8% $X_0$ )**
  - spatial ( $< 30 \mu\text{m}$ ) + timing ( $< 5 \text{ ns}$ ) + amplitude (15 fC/5 bit) information collected in self-triggering mode

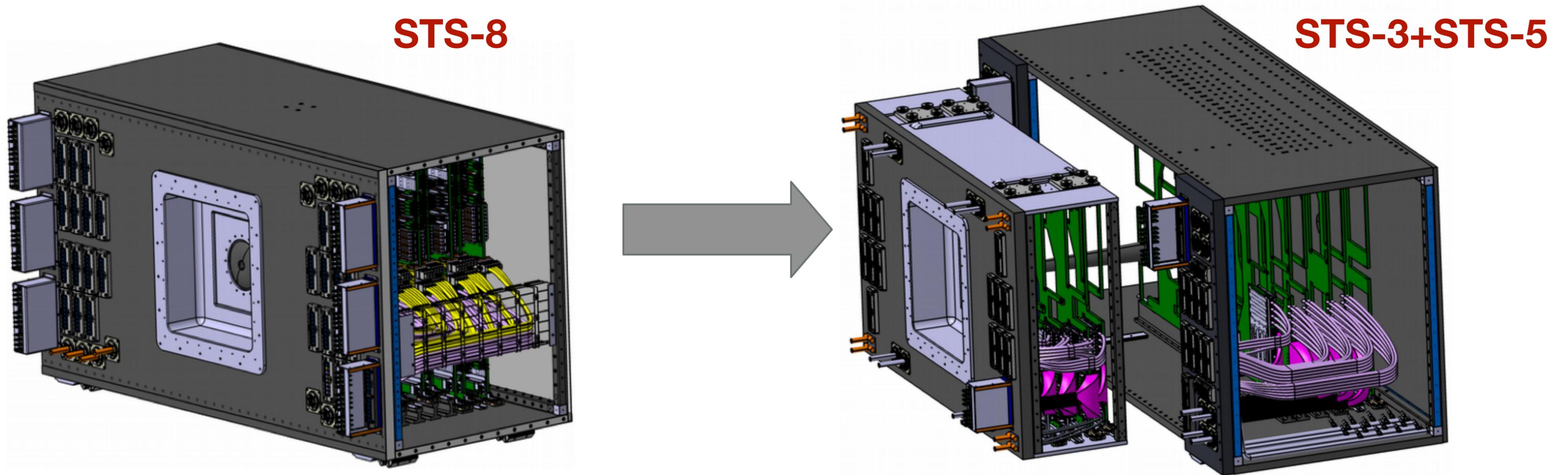
# STS structure and assembly sequence



- 876 modules, 106 ladders, & 14 000 r/o ASICs, & 7 000 LDOs
- Large number of unique components: 199 module variants, 38 ladder types

# Upgradable STS concept

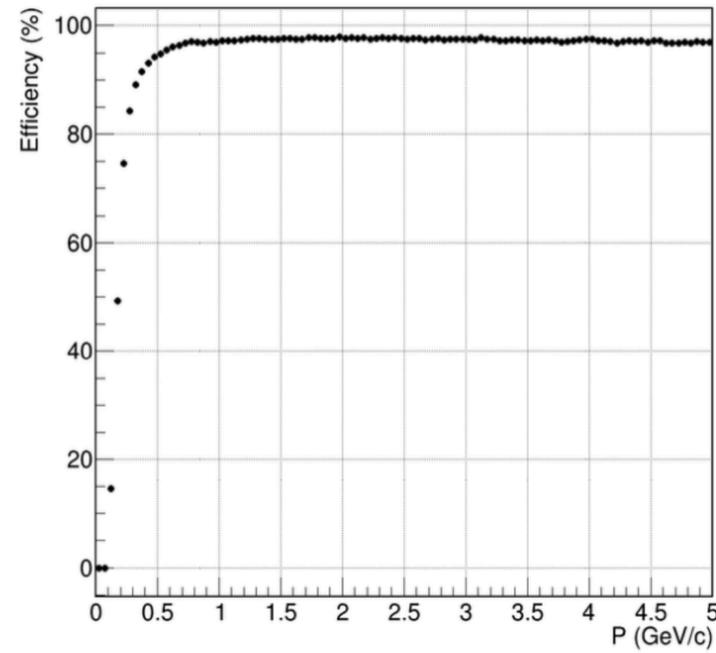
Modular STS setup for improved maintenance, upgradability and replacement



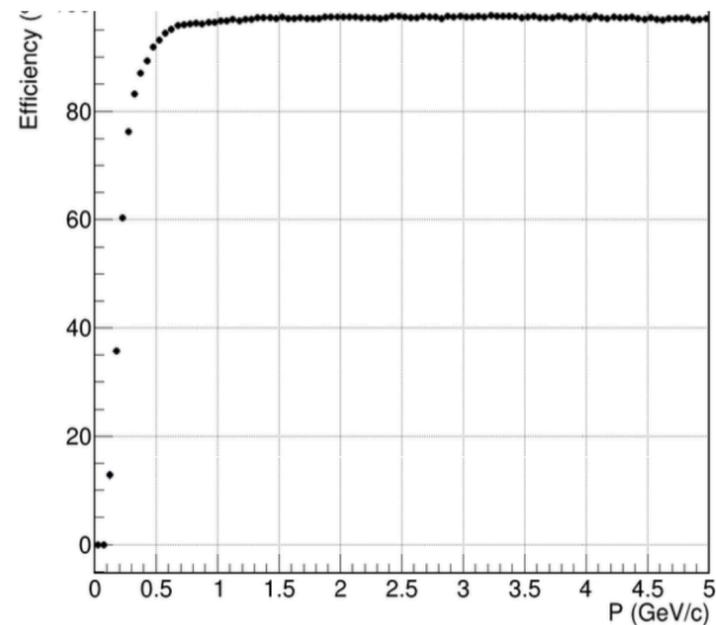
- detailed comparison using a simulation approach:
- updated geometry, acceptance, material budget, tracking performance

# Tracking performance at 12 AGeV/c

Efficiency

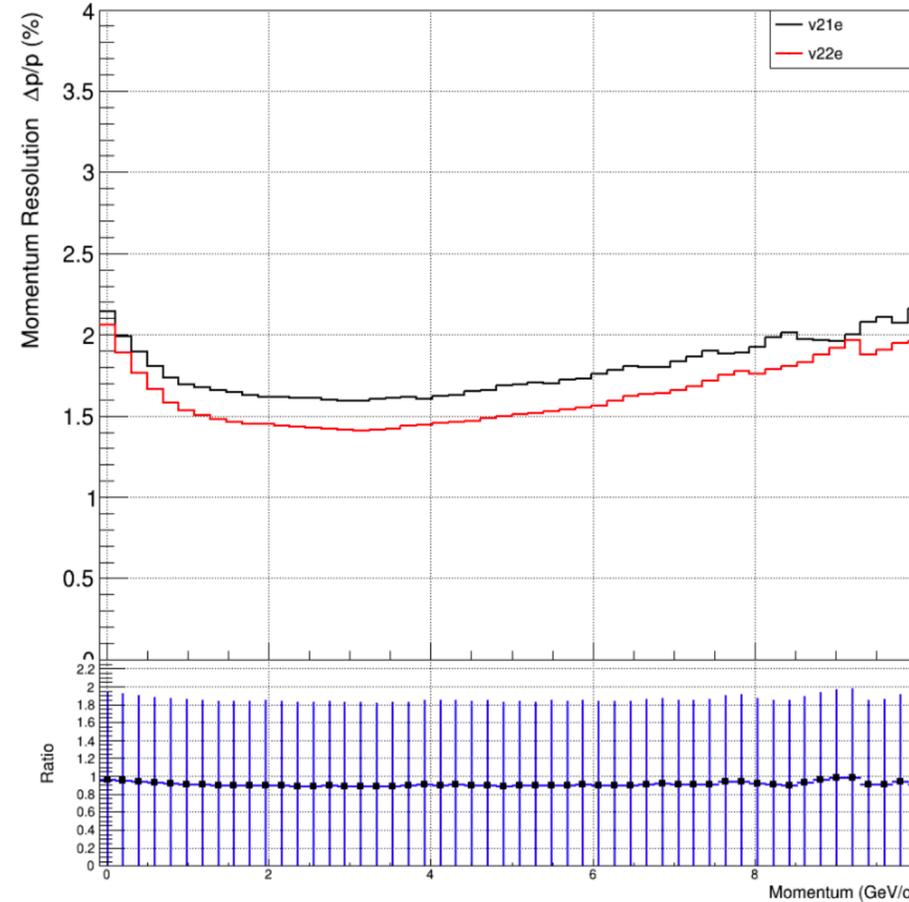


(a) v21e



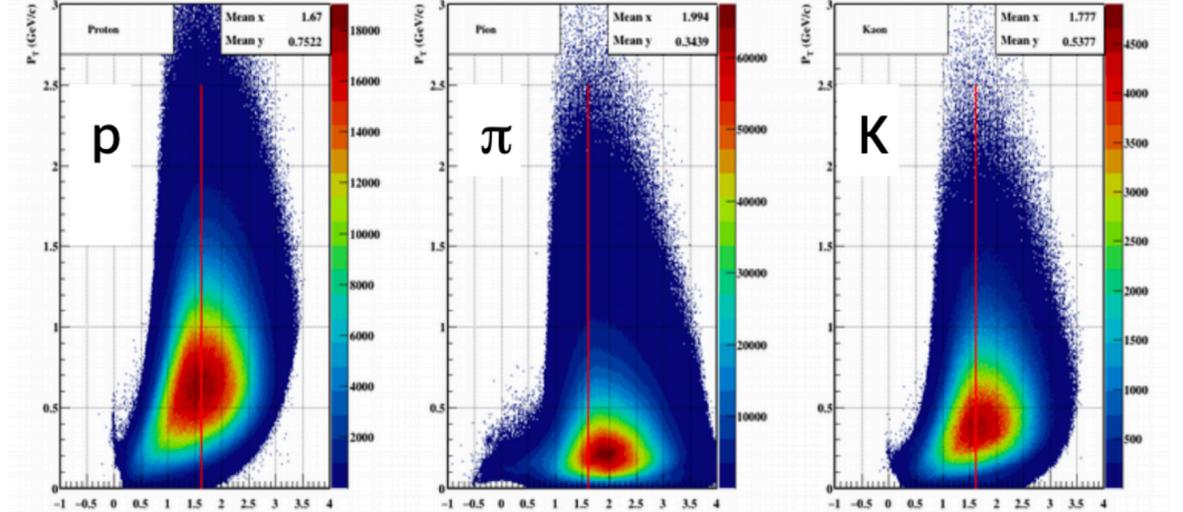
(d) v22e (gap 8cm)

Momentum resolution

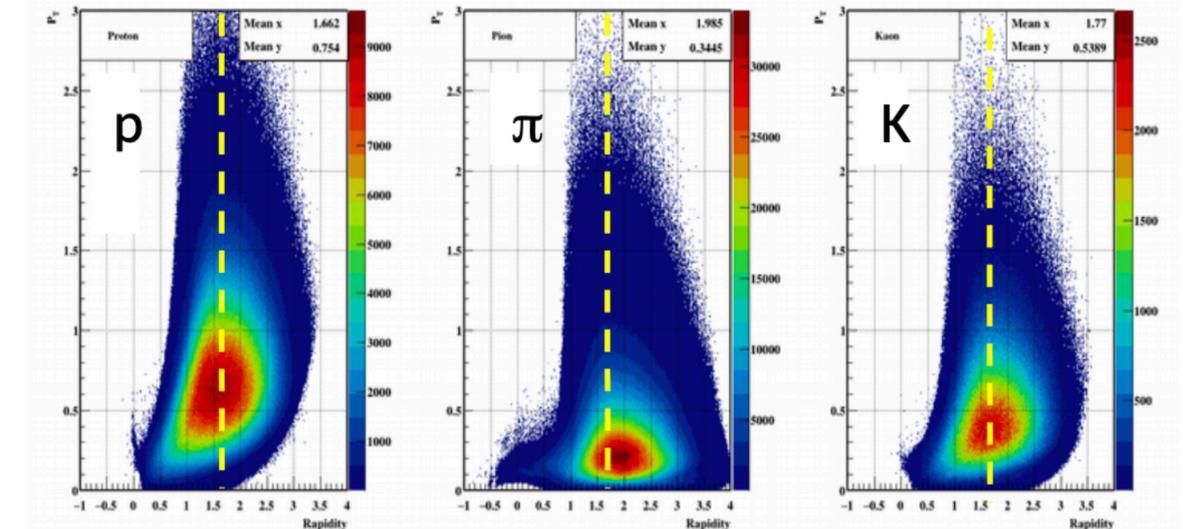


pt-y coverage

STS v22c\*



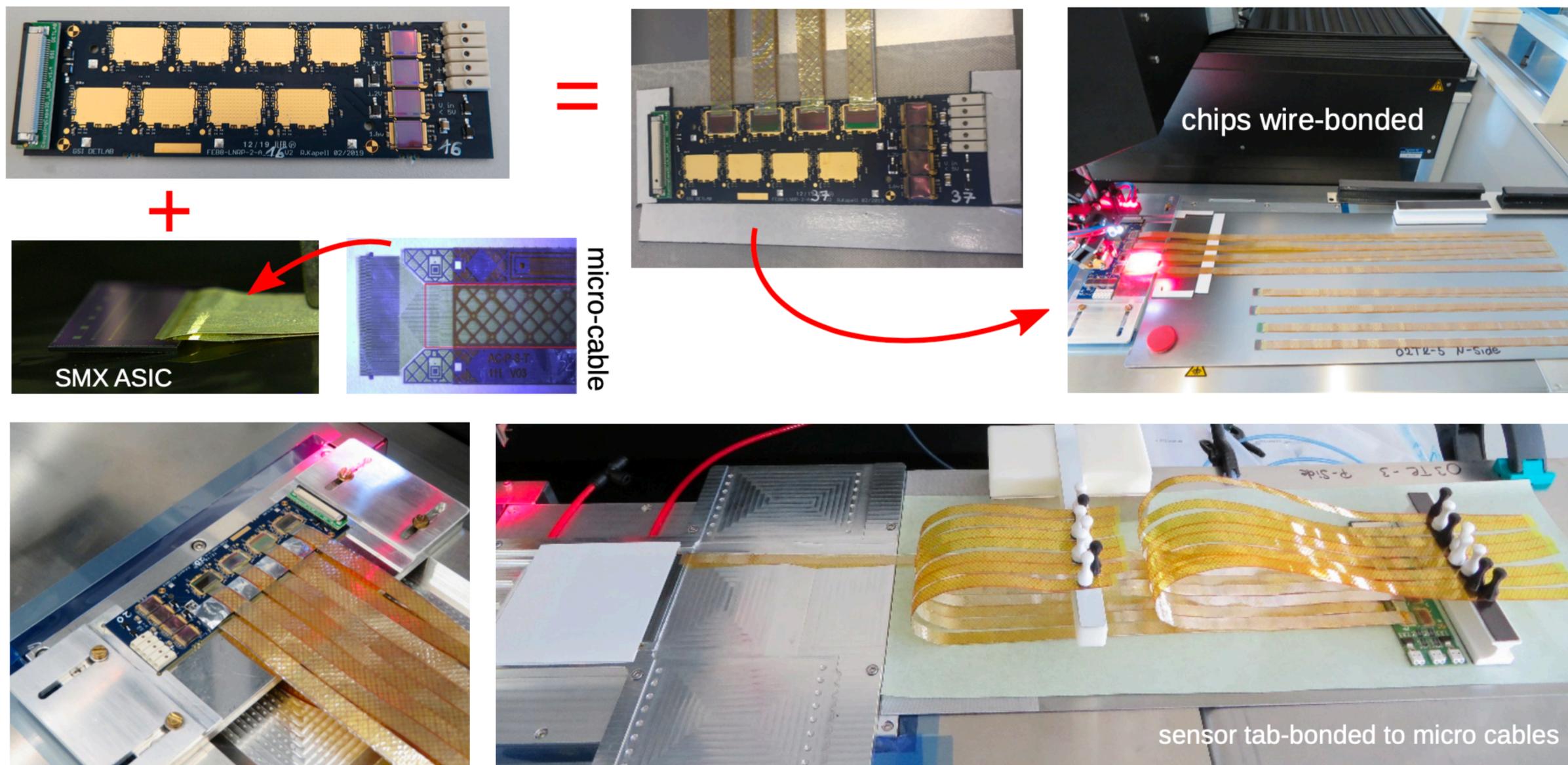
STS v21e



Comparable tracking performance for STS-8 and STS-3+STS-5 setups!

# Module assembly

STS detector modules are produced in the assembly centers at GSI and KIT

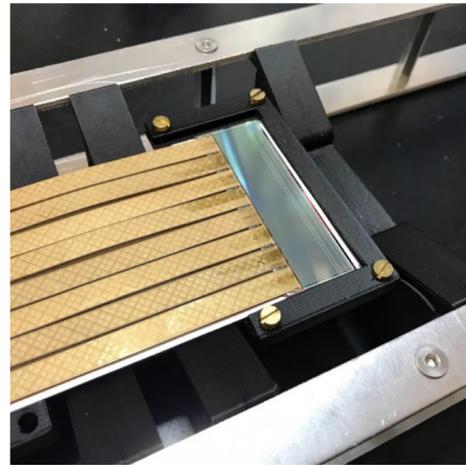
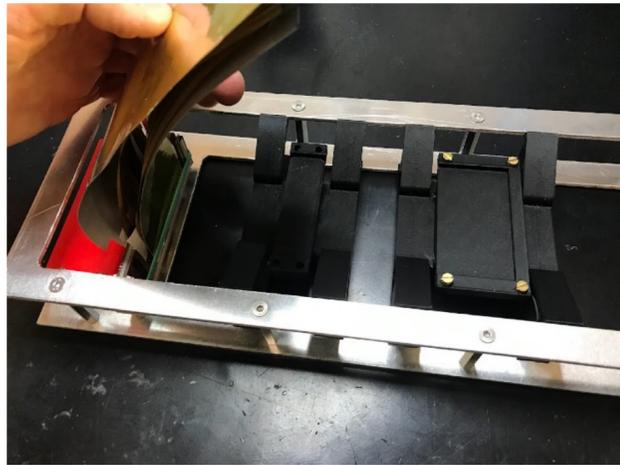


- tools and procedures shared between assembly centers
- highly integrated objects: extensive testing at each step

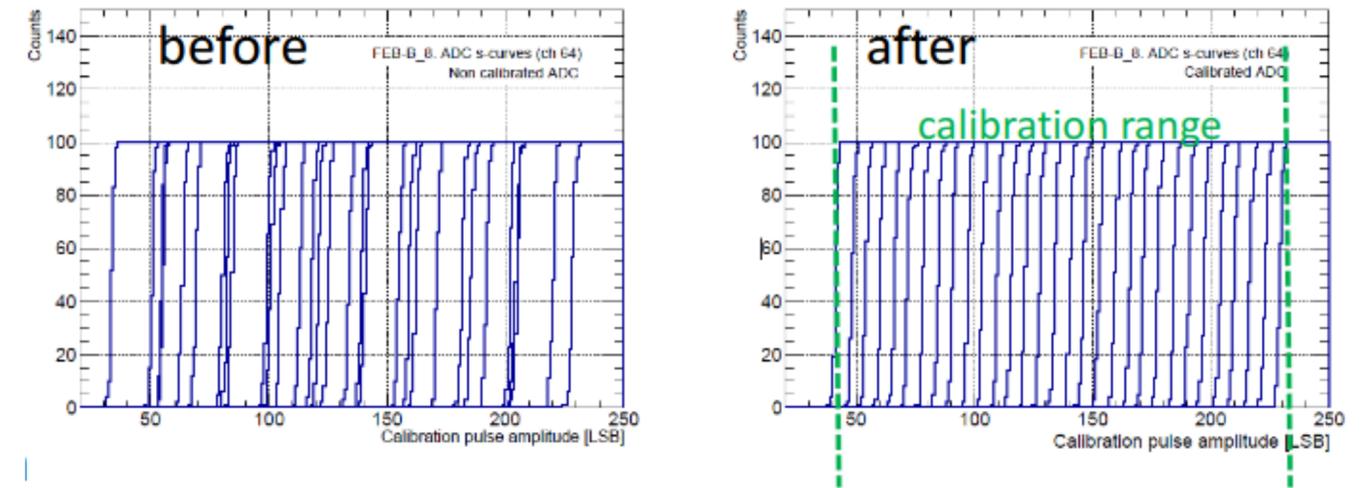
Pre-series production successfully started in early 2022 to validate the sequence

# Module acceptance test: reception, calibration, thermal cycling

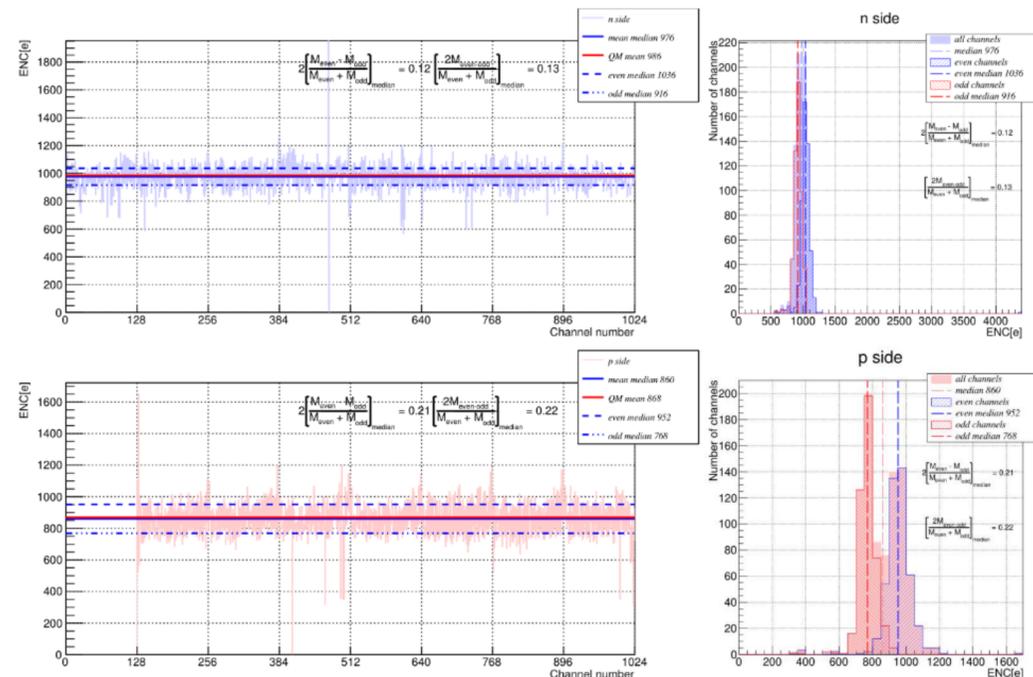
Module installed into the carrier structure with interfaces for testing



ADC calibration of the SMX ASIC



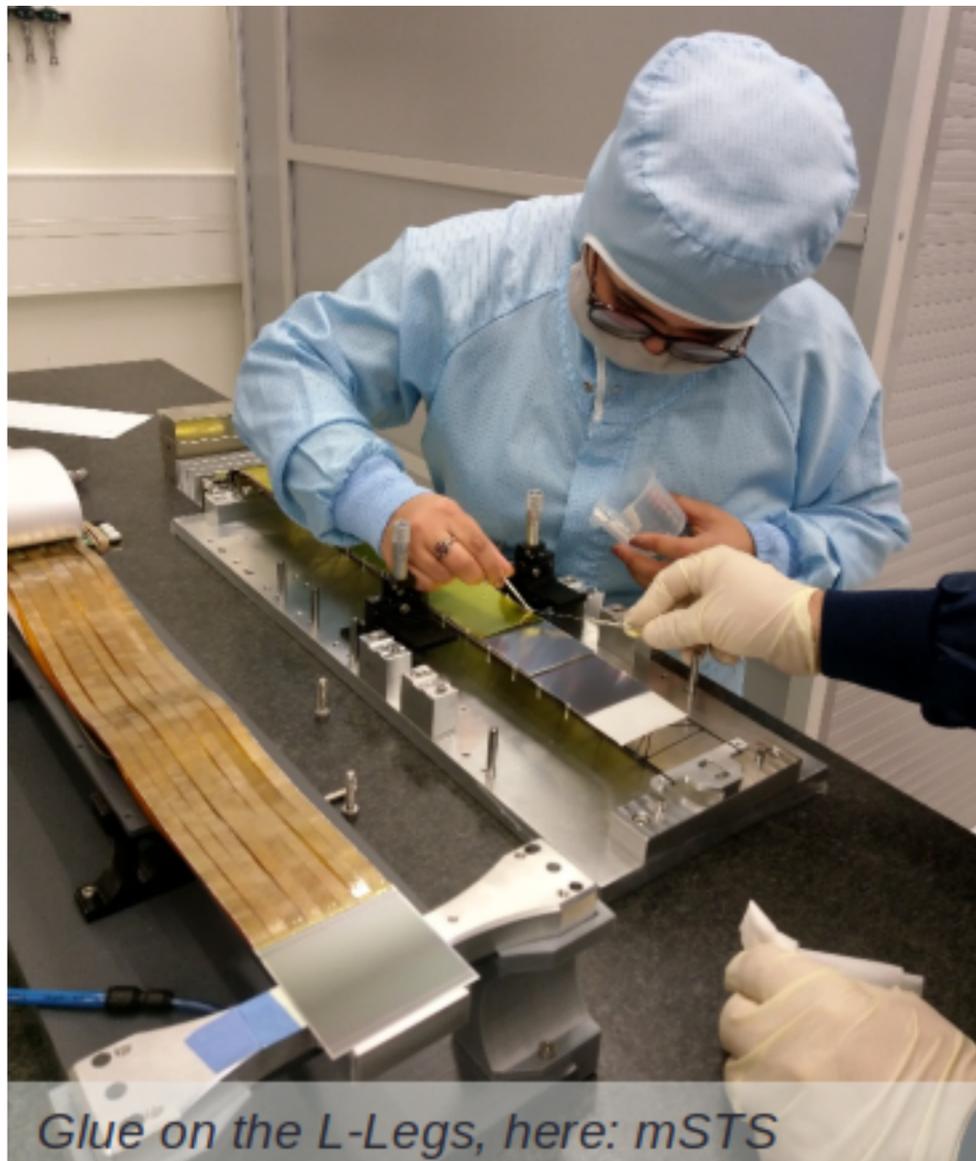
Thermal cycling climate chamber:  
+25°C..-40°C



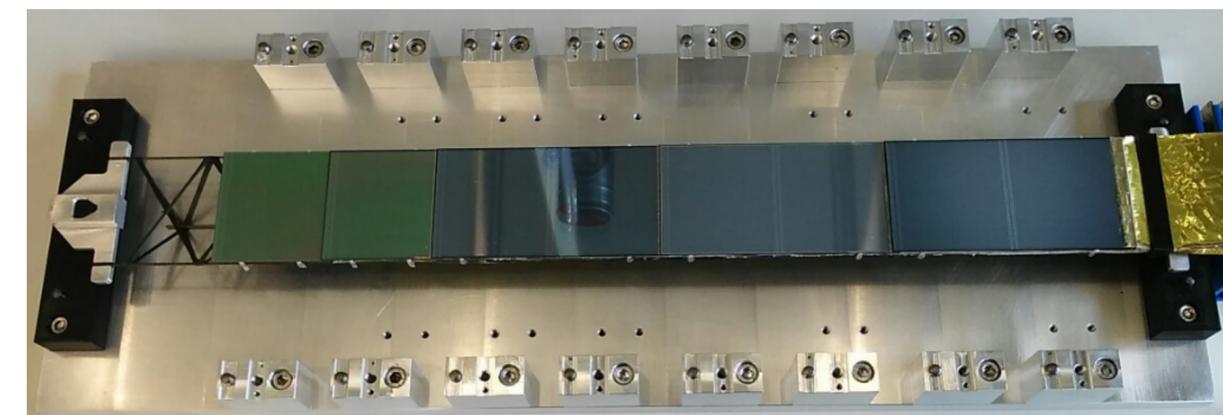
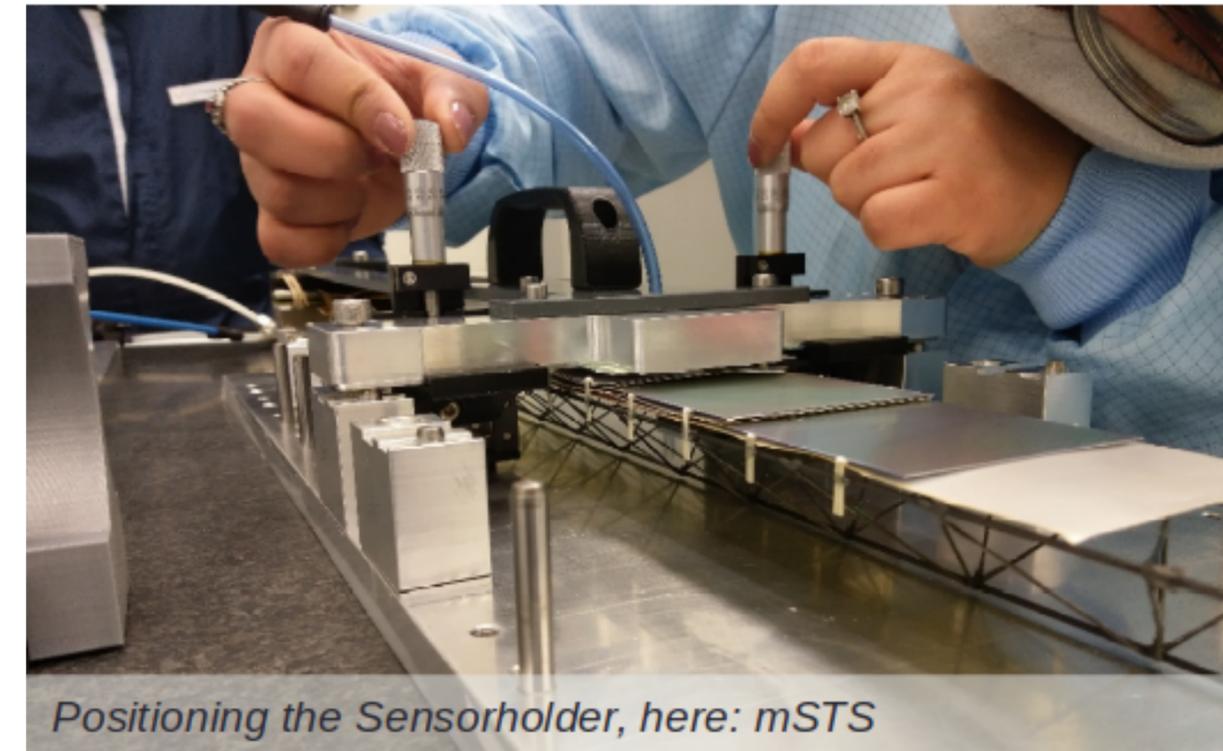
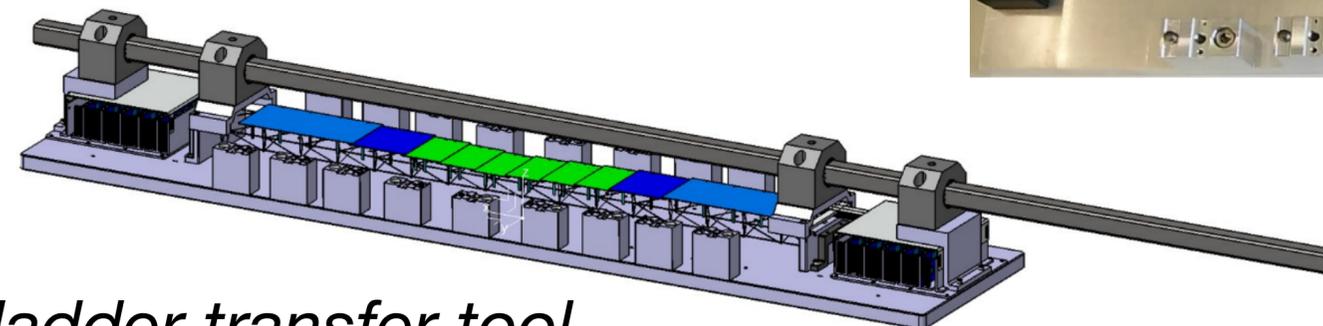
Module baseline  
width measurement

# Ladder assembly sequence

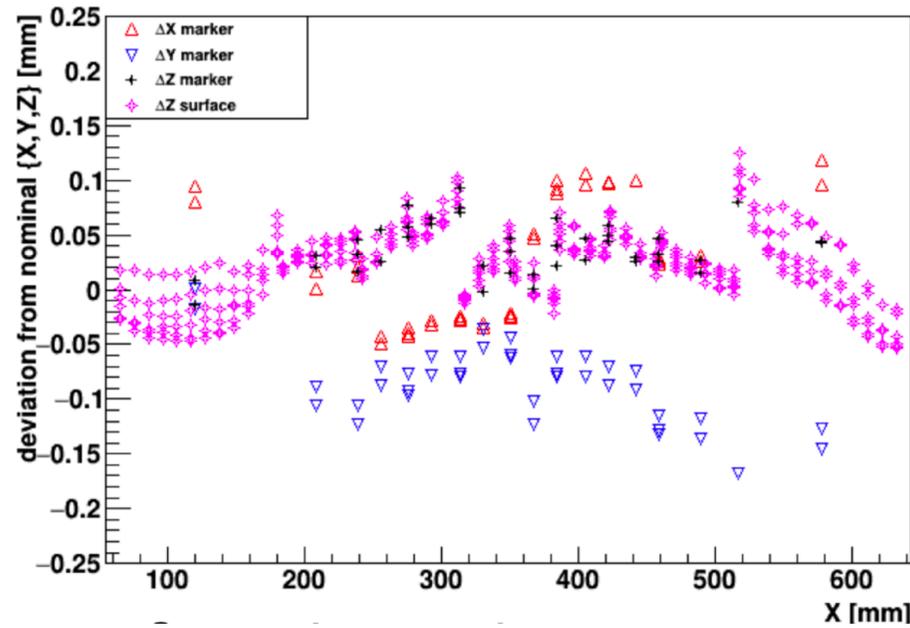
- From 8 to 10 detector modules installed on the light-weight carbon structures: ladders
- Sensors precisely positioned ( $\leq 30 \mu\text{m}$ ) with jigs



- Assembled ladders undergo metrology survey and functionality tests
- After tests ladder is installed on C-frame using transfer tool



# Optical metrology and ladder functionality tests



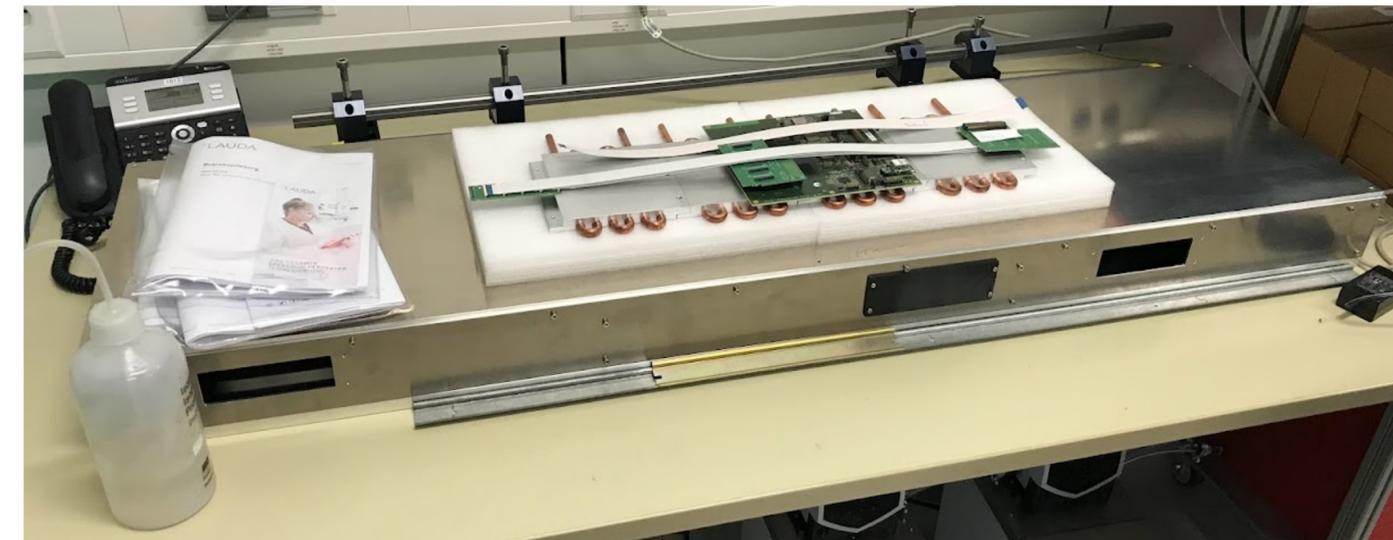
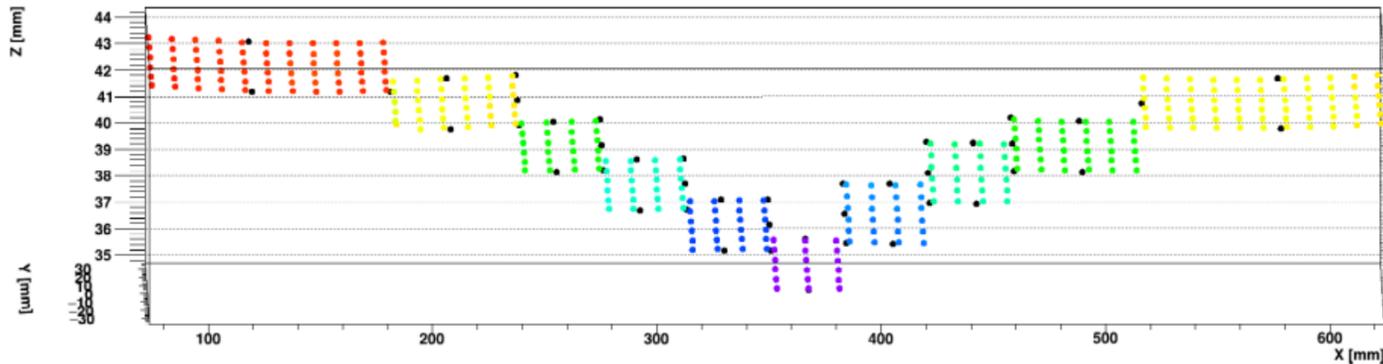
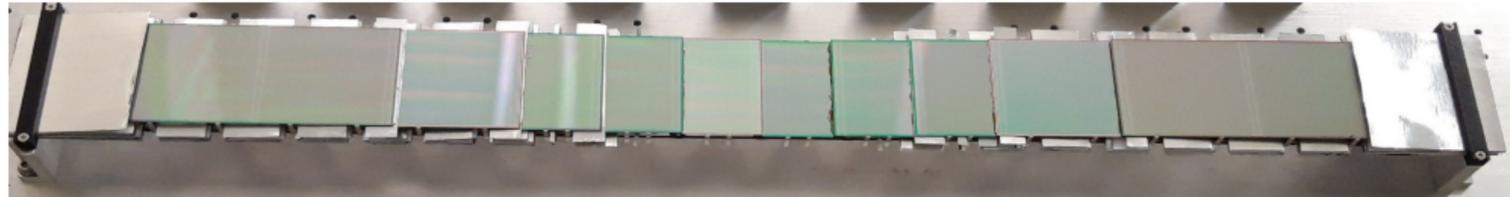
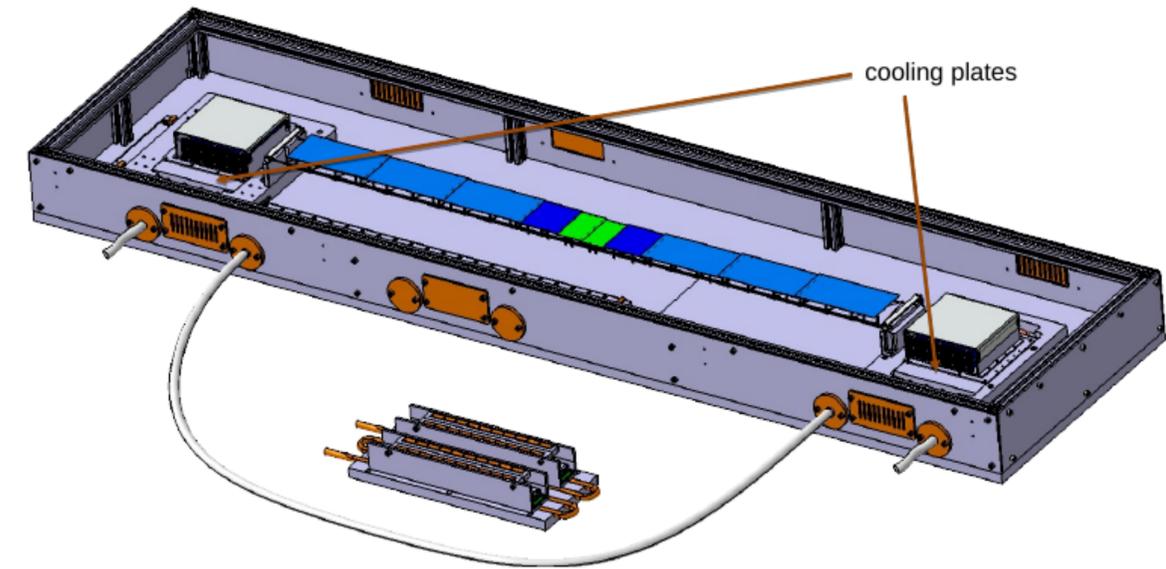
## Optical metrology:

- dedicated table with camera
- $\mathcal{O}(10 \mu\text{m})$  measured precision
- multi-point probing

## QC with assembled ladder:

- DAQ communication test
- HV (spark) test

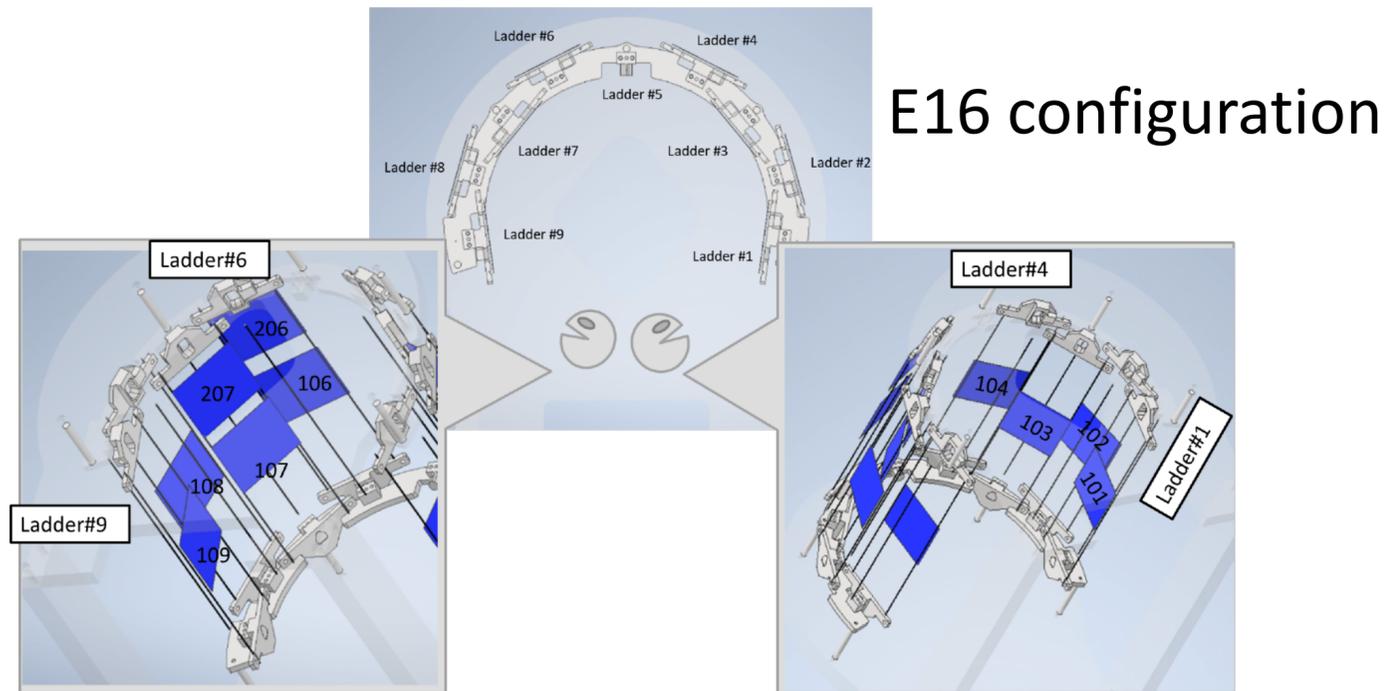
- flexible design to mount every type of ladder
- Dimensions: 1500mm x 400mm x 110mm
- Weight:  $\approx 40\text{kg}$



- Actual sensor position is stored in the database

# Pre-series module assembly

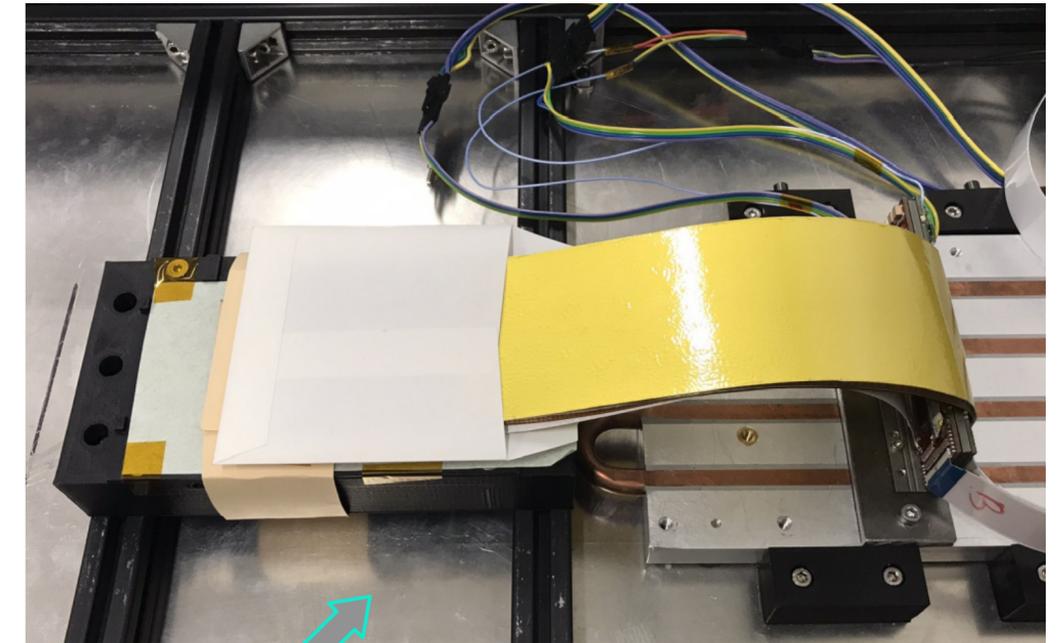
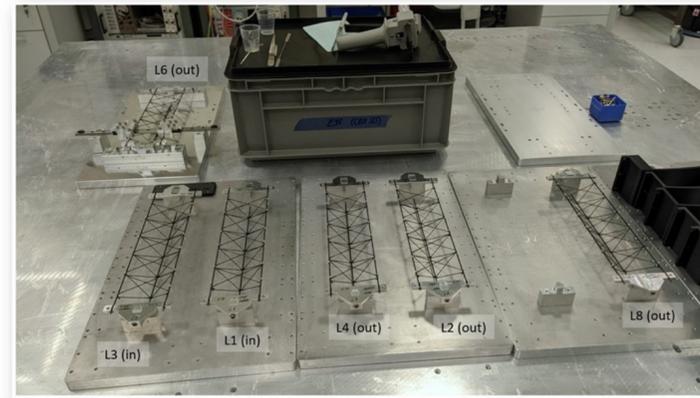
10 STS modules on ladders to be prepared for the E16 experiment (J-PARC).  
Beam test: spring 2023



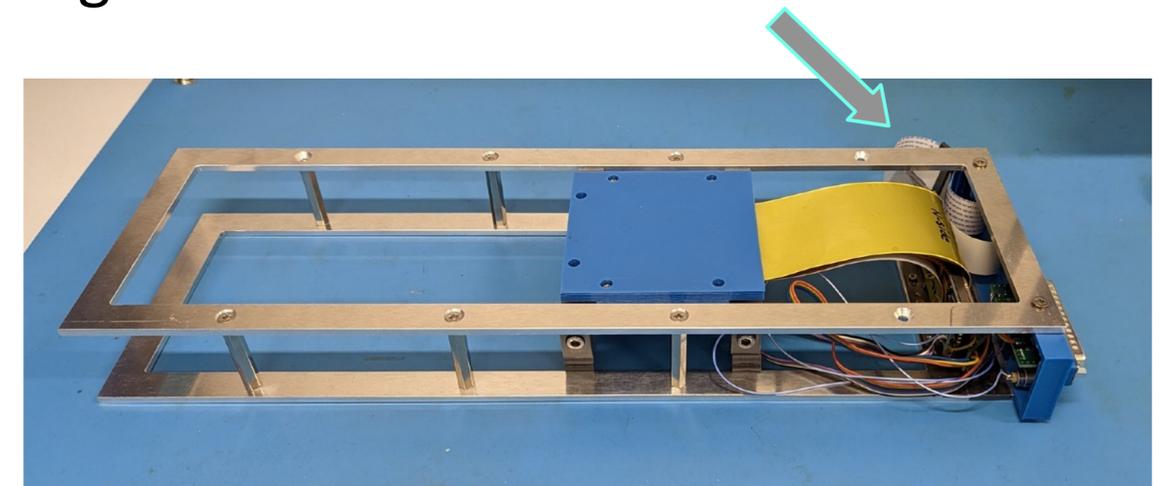
Assembled modules



Ladders

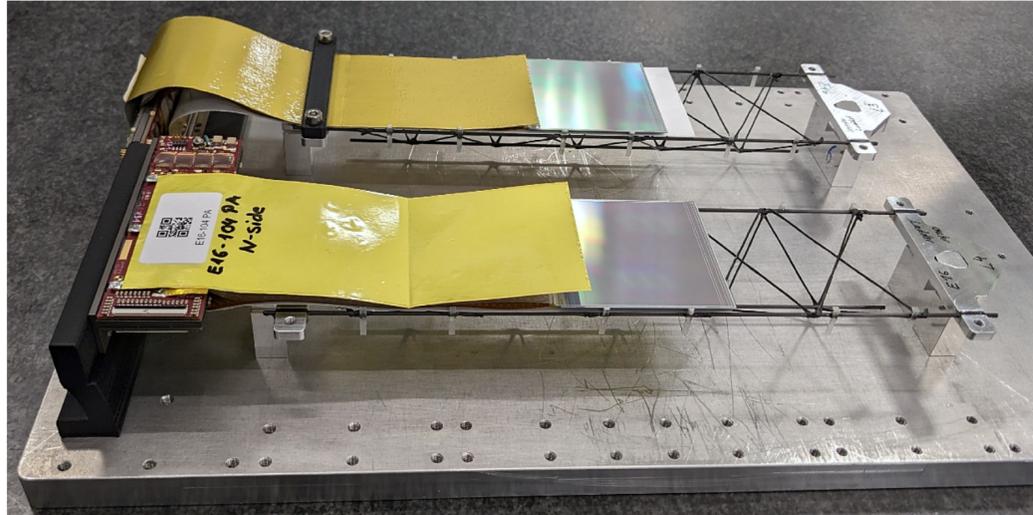


Module testing in the **test box** or in **module carrier**

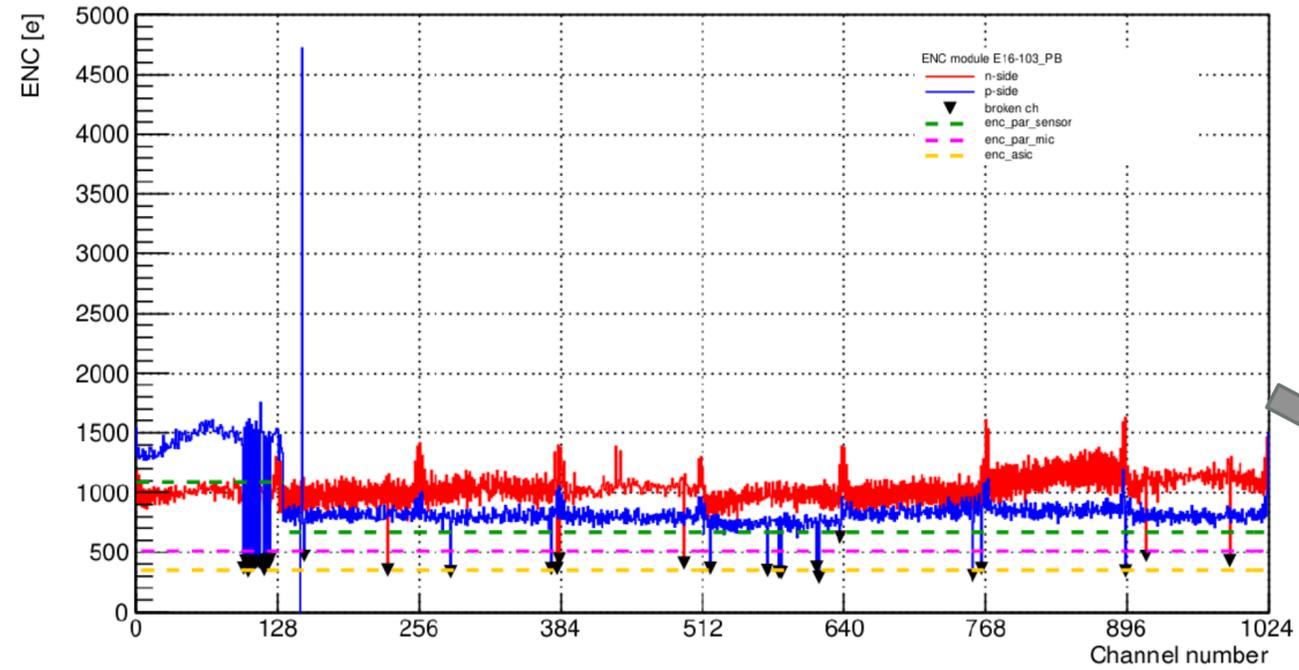


# Module final performance

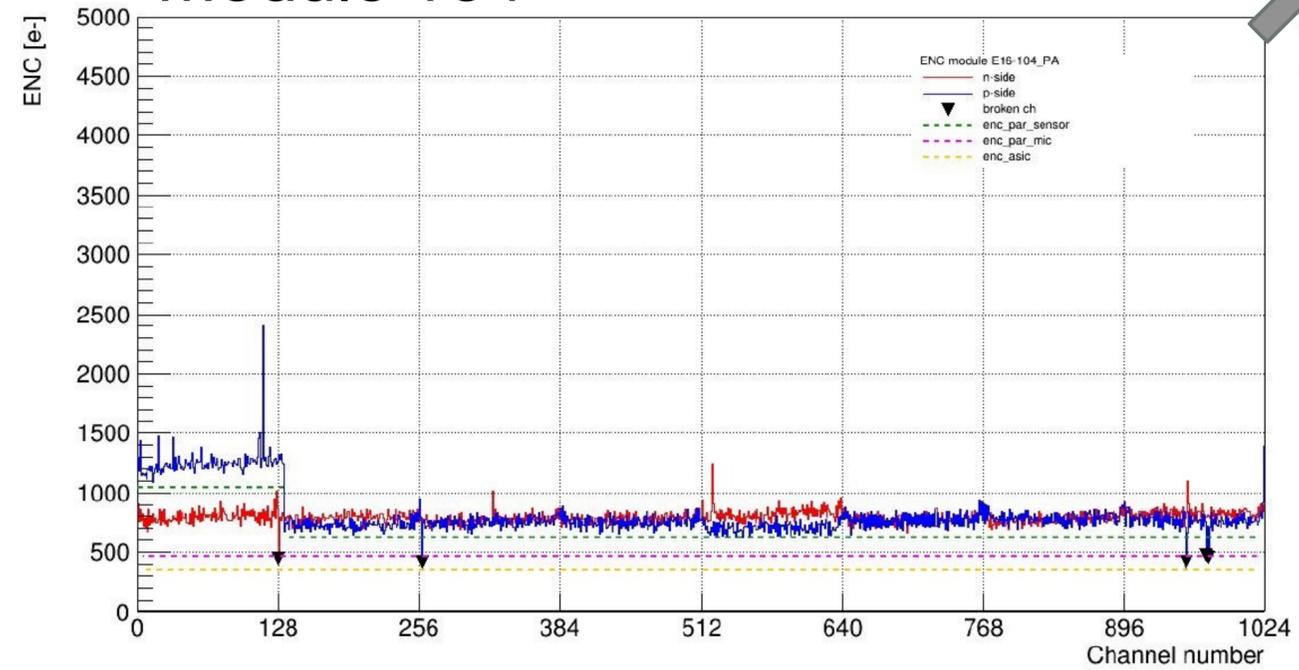
Two module mounted onto ladders



Module 103



Module 104



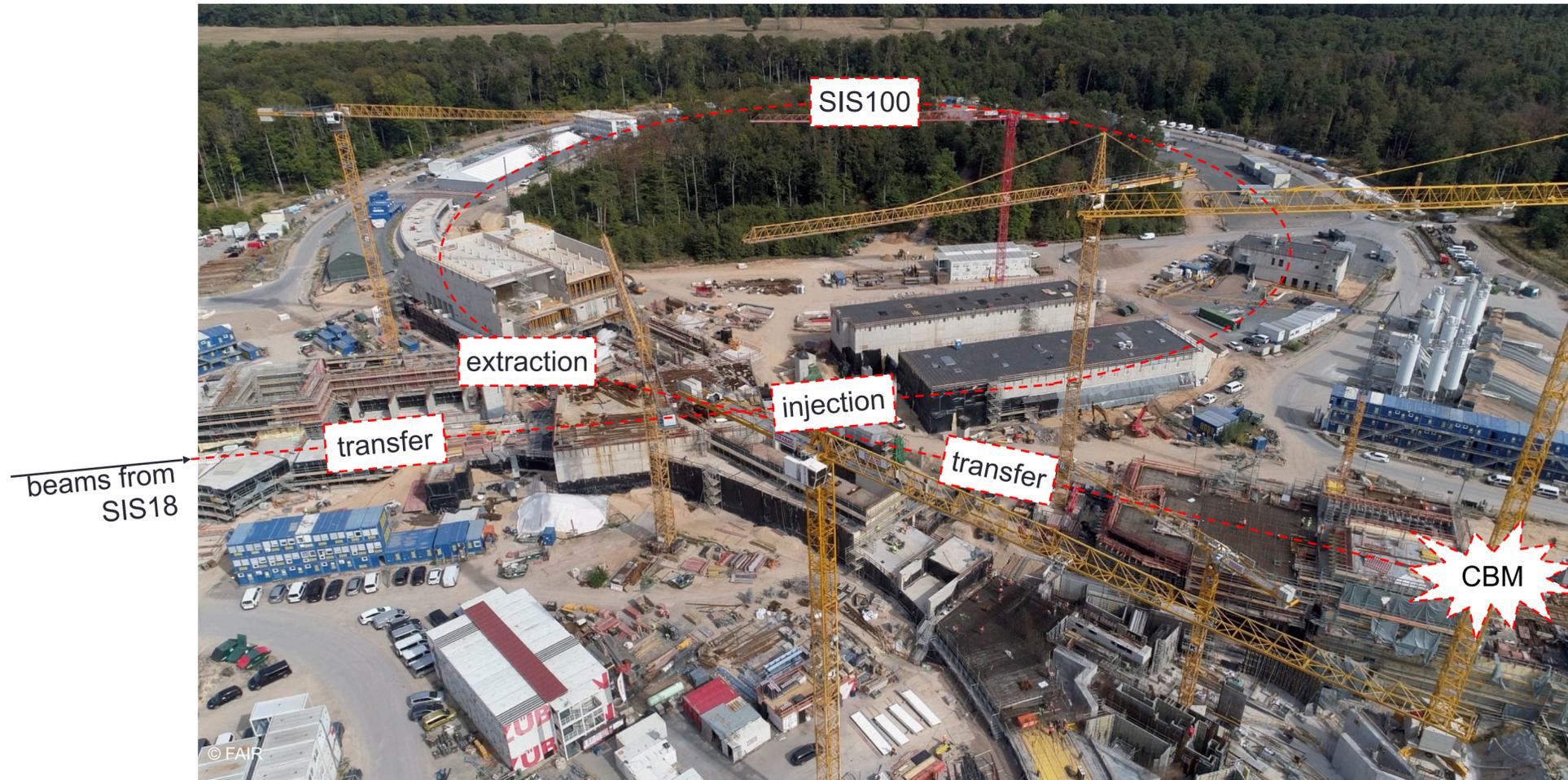
Module ID	Ladder ID	Type
101	L1	inner
102	L2	outer
103	L3	inner
104	L4	outer
-	-	-
106	L6	outer
206	L6	outer
107	L7	inner
207	L7	inner
108	L8	outer
109	L9	inner

- 8/10 tested
- fully functional ✓
- detailed study of all settings done ✓
- installation on ladders ongoing ✓
- first ladders shipped to J-PARC

# Conclusions

- Upgradable/modular setup of STS (3+5 stations): performance estimated, comparable to STS8 setup
- Quality control of system components finished
- Assembly procedure and acceptance tests for detector modules determined
- Pre-series batch of detector modules produced, performance OK.
- Modules integrated onto ladders following optical metrology and electrical quality control.

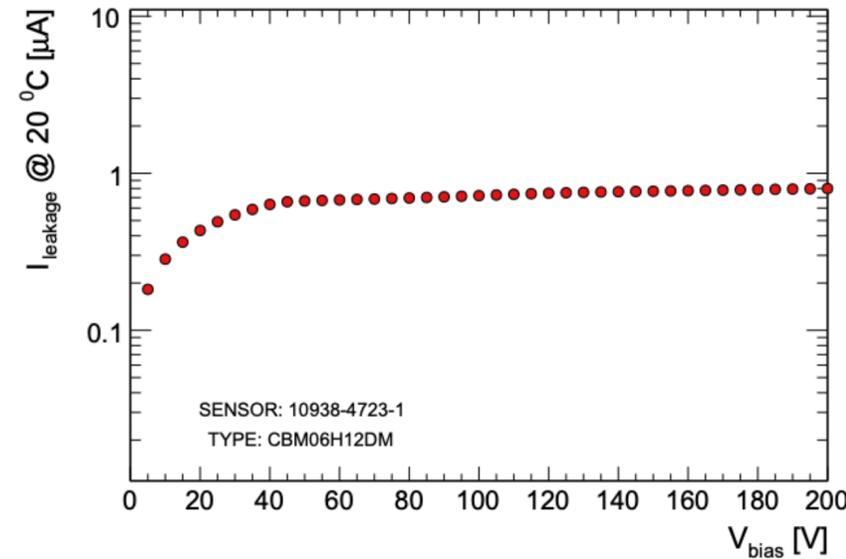
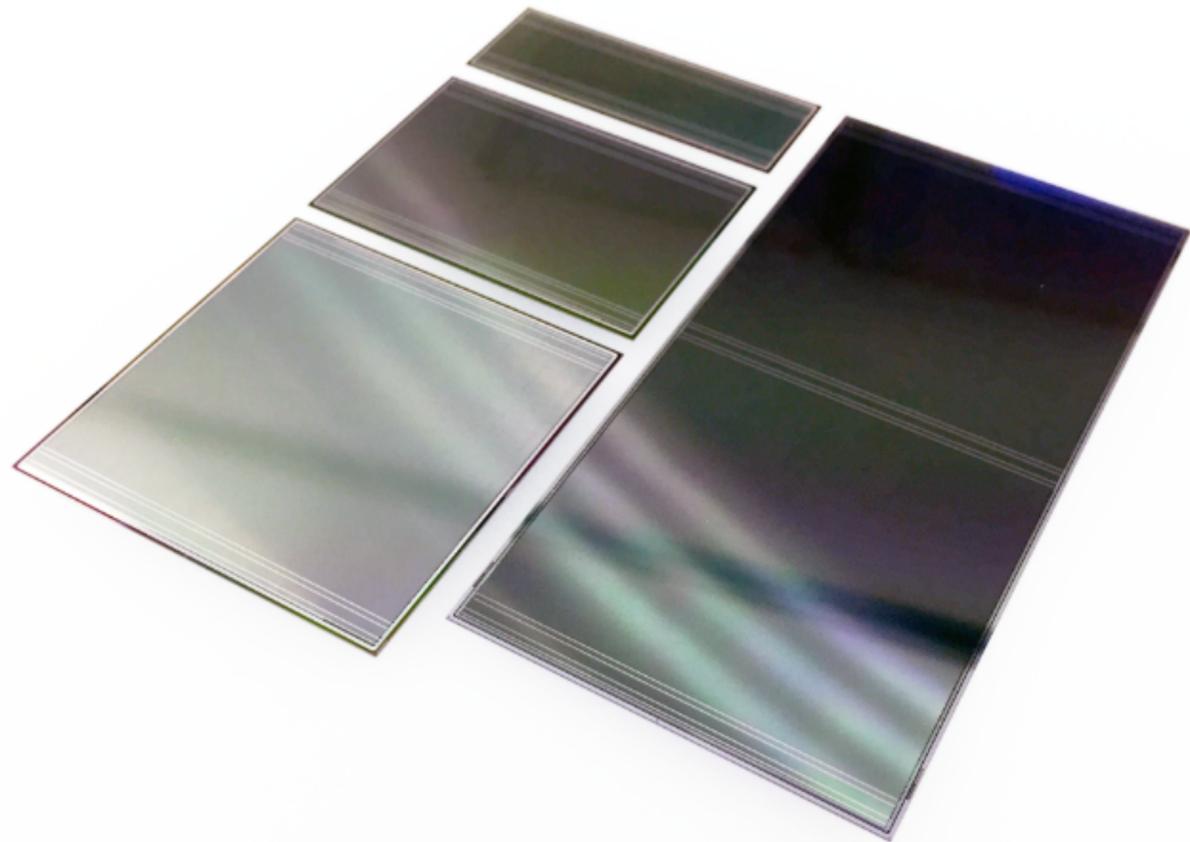
# Construction status



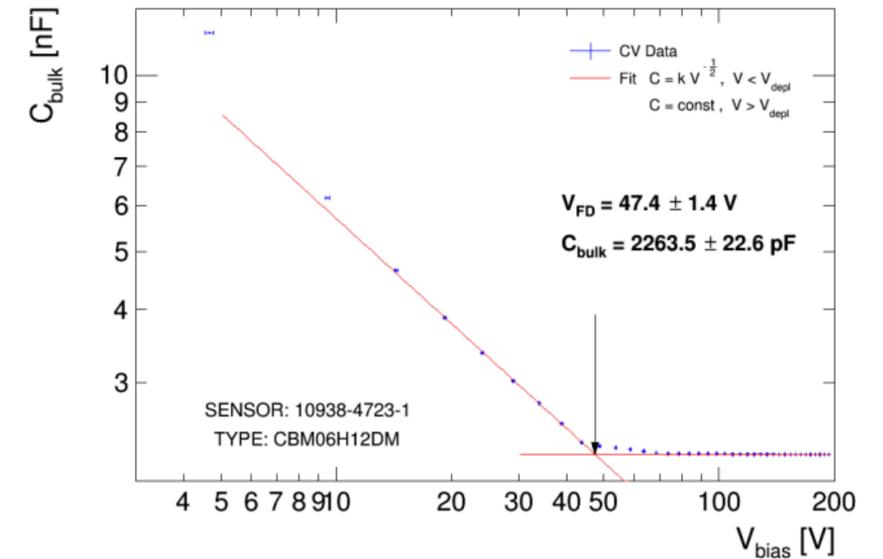
Synchrotron ring SIS100 with transfer line from SIS18 and extraction line to CBM cave

CBM cave

# Double-sided silicon micro strip sensors



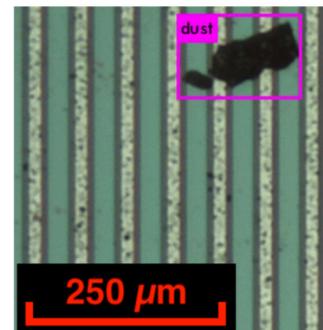
Current-voltage curve



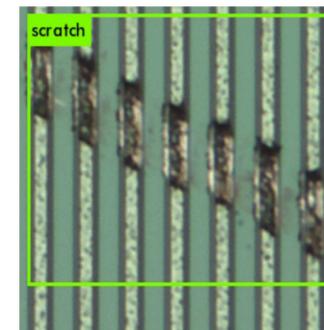
Capacitance-voltage curve

*Sensor characteristics measured at Tuebingen University.*

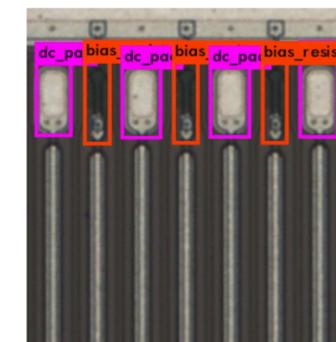
- Four sensor form factors
- All 1100 sensors characterized
- Automated optical defect detection and classification
- Electrical QC (capacitance- and current-voltage characteristics)



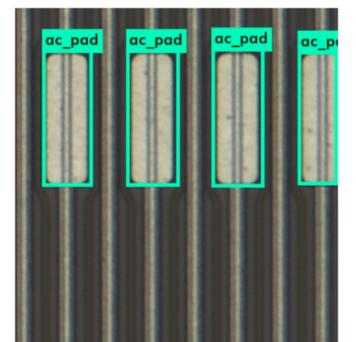
dust grain



scratch



R bias/DC pads



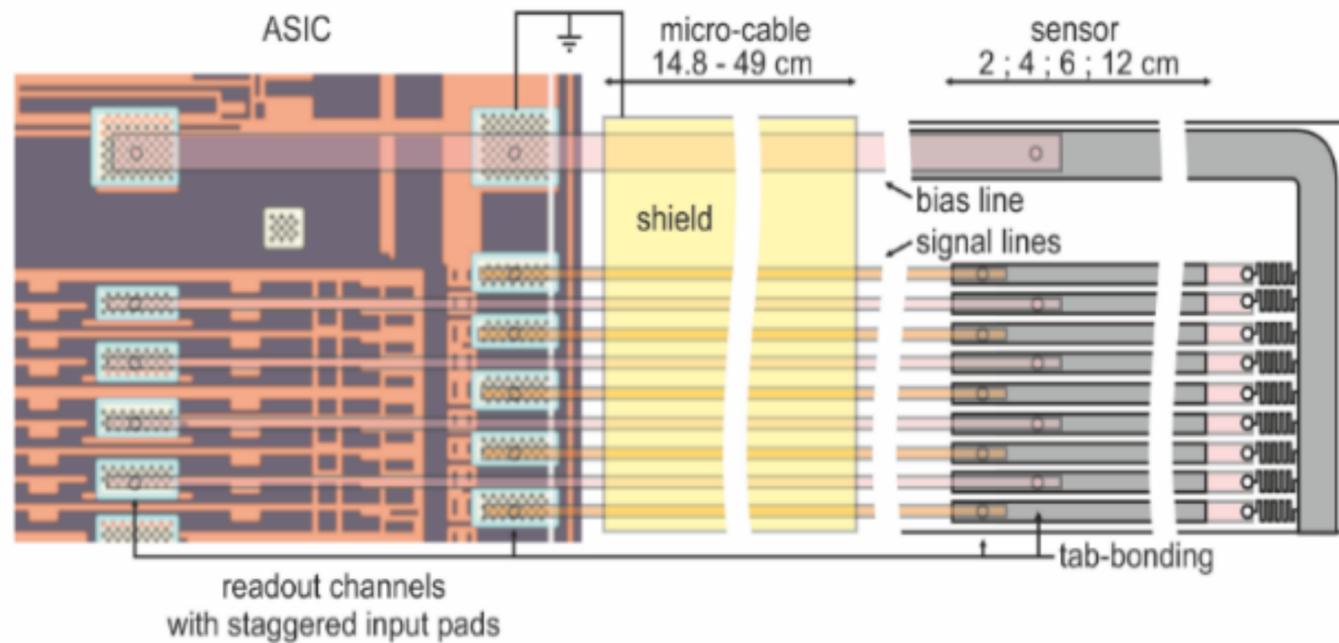
AC pads

Different object/defect classes located and classified with neural networks

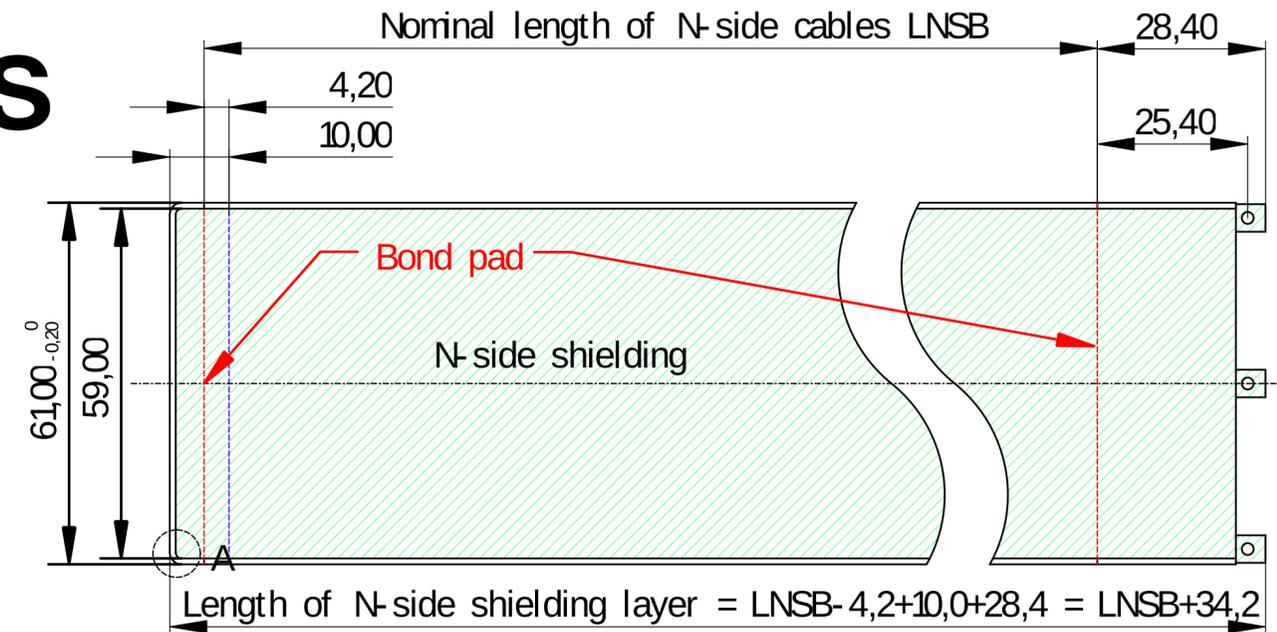
# Ultra-thin readout micro cables

aluminium analog lines on the polyimide base

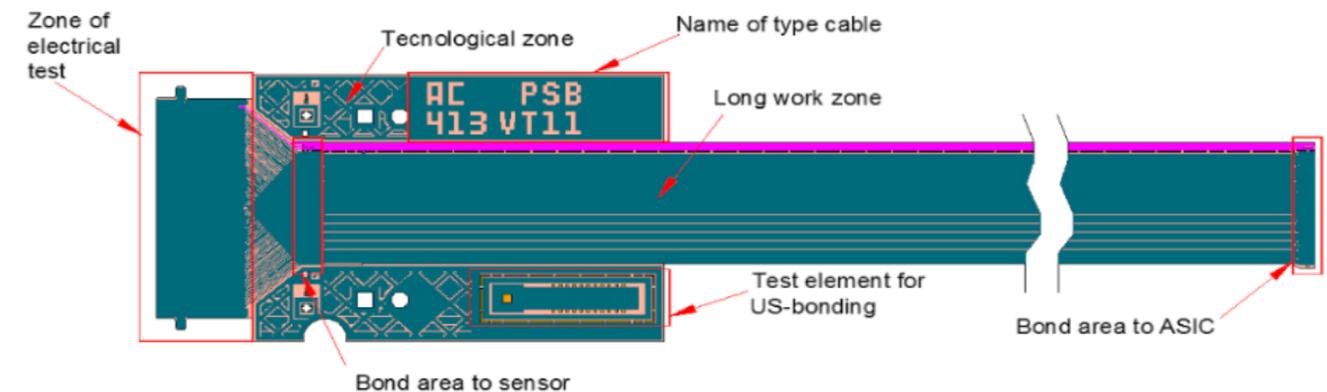
Front-end electronics connected to double-sided silicon sensors via micro-cable lines (64 lines/cable)



- Stack of 32 micro cables per module, 8 subtypes
- Overall length from 160mm to 495mm



Readout lines are protected from EMI by aluminium shielding layers



Micro-cable end with service area



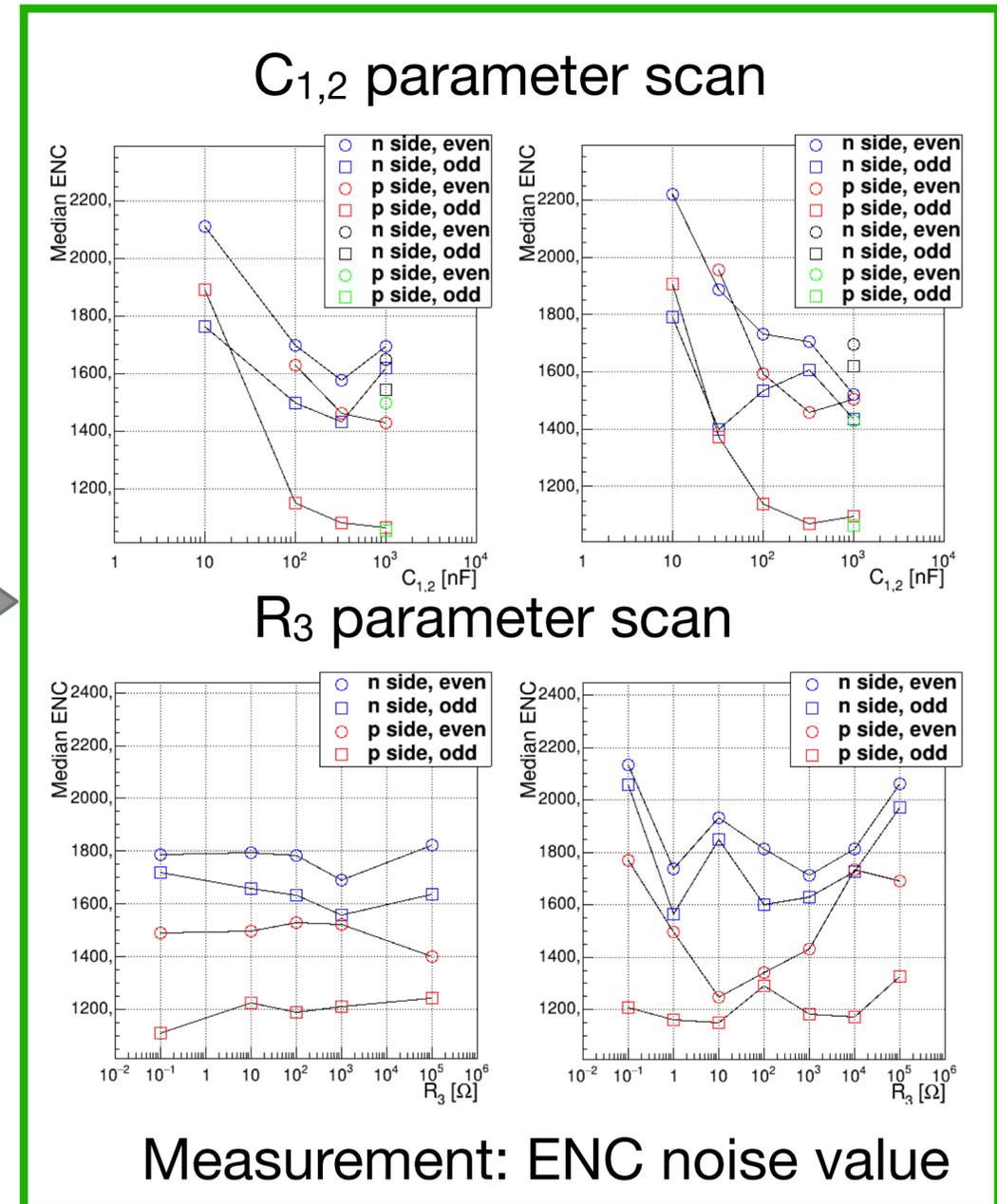
Production/QC ongoing at LTU, Kharkiv (60% of ~15 000 cables already at GSI)

# Front-end electronics

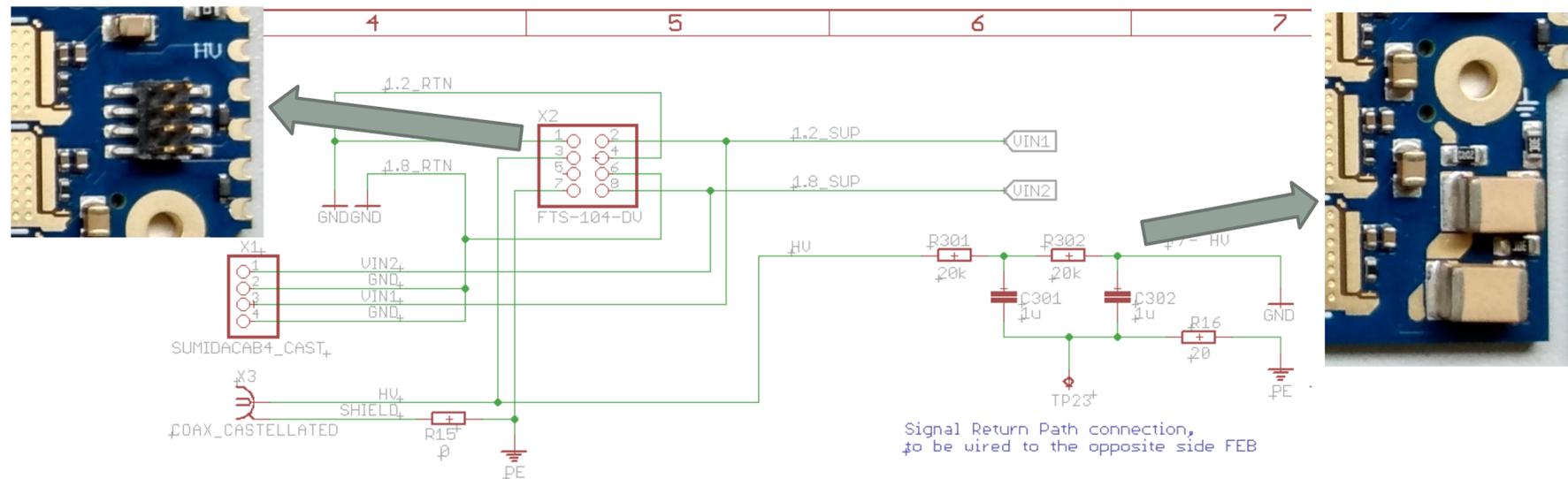
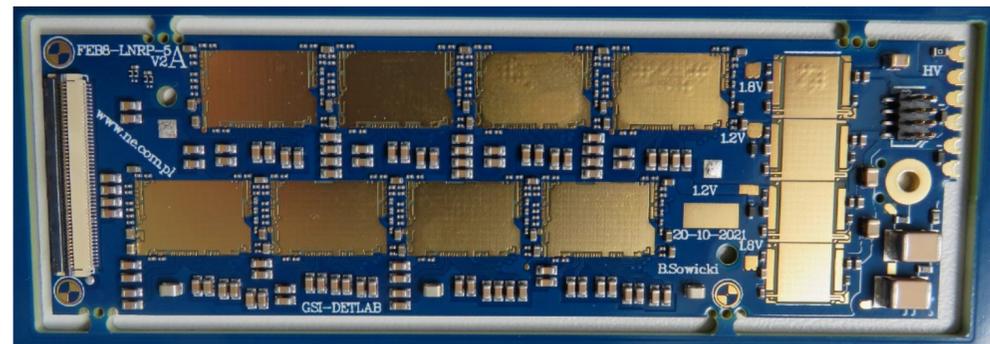
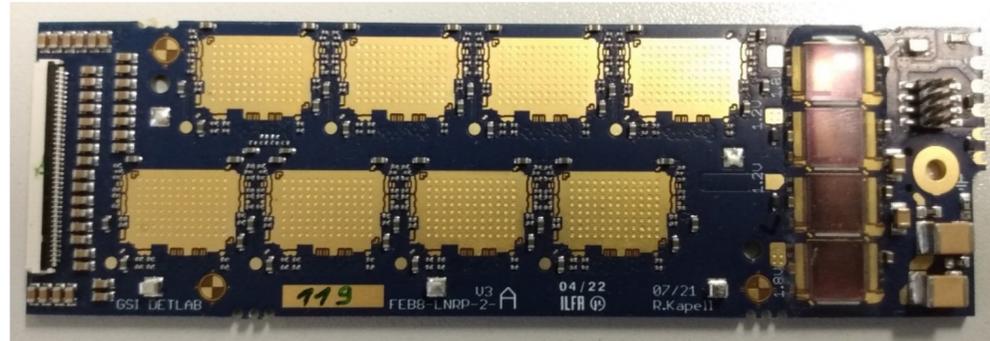
## finalizing the design

- 8 SMX2.2 r/o ASICs (à 128 ch.)
- Custom designed LDOs
- Versions with 2 and 5 data links
- 2 FEBs per module
- HV stability  $\pm 250$  V
- Service connector for fast powering (e.g., module testing)
- Filtering scheme optimized

### Circuit parameter optimization



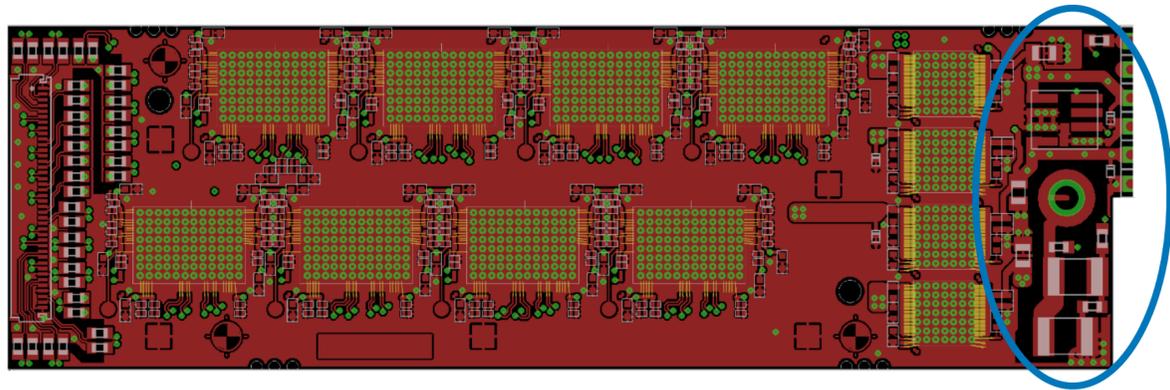
Measurement: ENC noise value



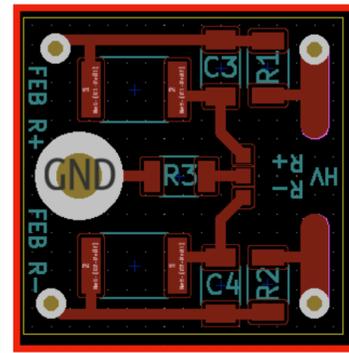
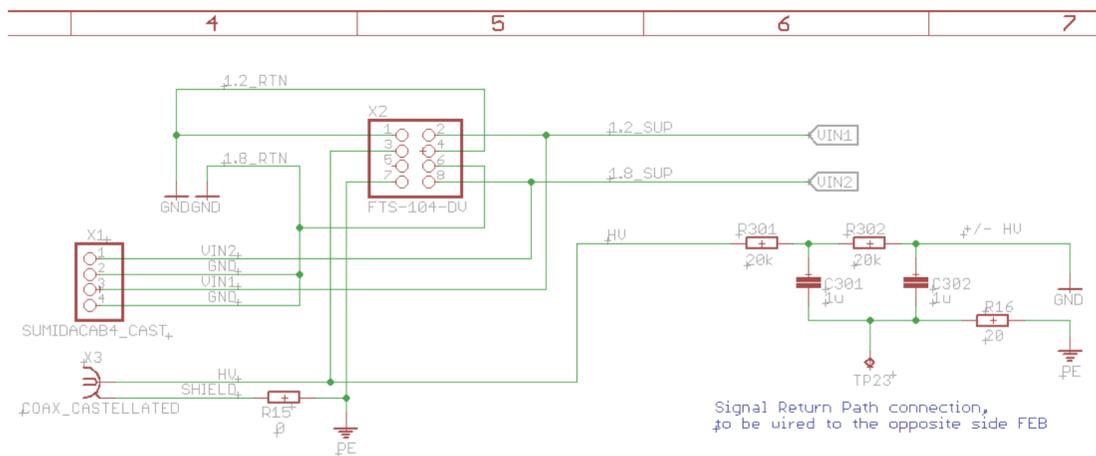
FEB8\_2\_B  
FEB8\_5\_B

Updated FEB schematics with **service connector** + on-board **HV filter**

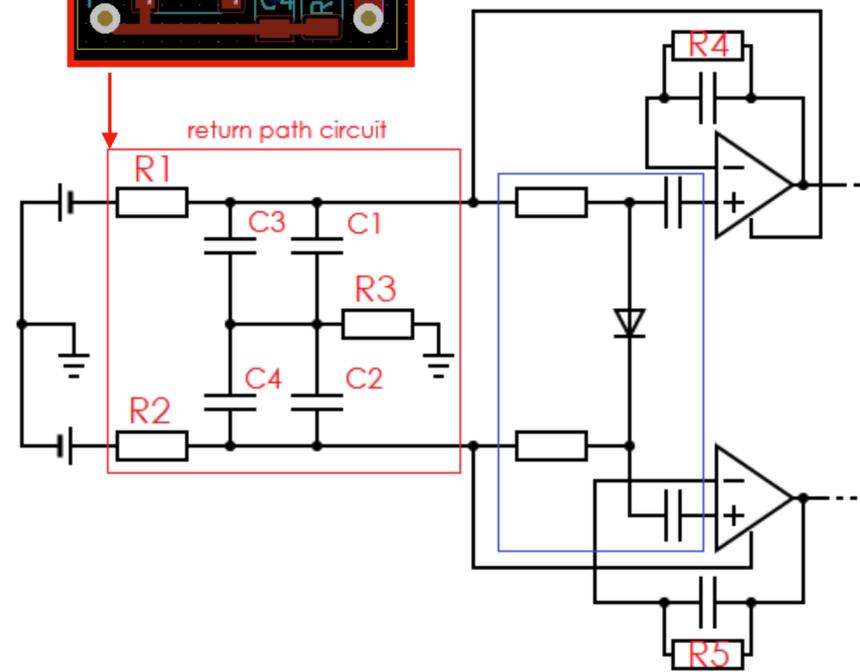
# Circuit parameter optimization



On-board HV filter and return path



Prototype PCB



- 2nd order RC-type filter for HV implemented on the FEB
- Return path circuit with reference to GND
- Signal return path circuit parameters optimised for best noise performance

