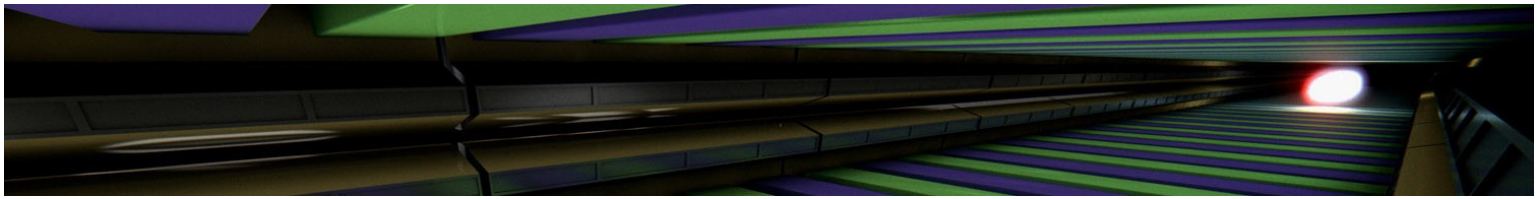
European XFEL



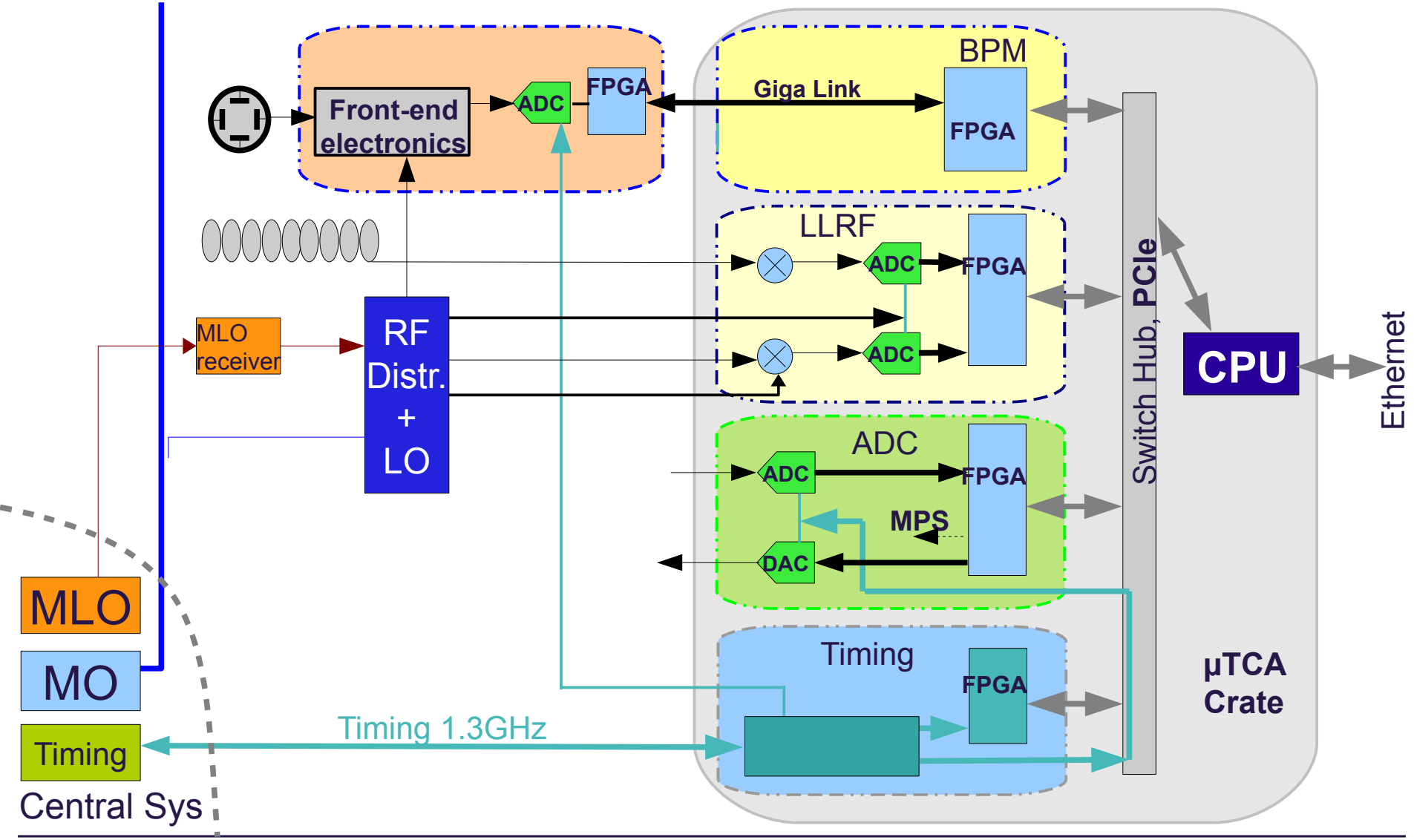
XFEL Timing System

Status 11.2010

Christian Bohm
Attila Hidvégi
Patrick Geßler
Kay Rehlich

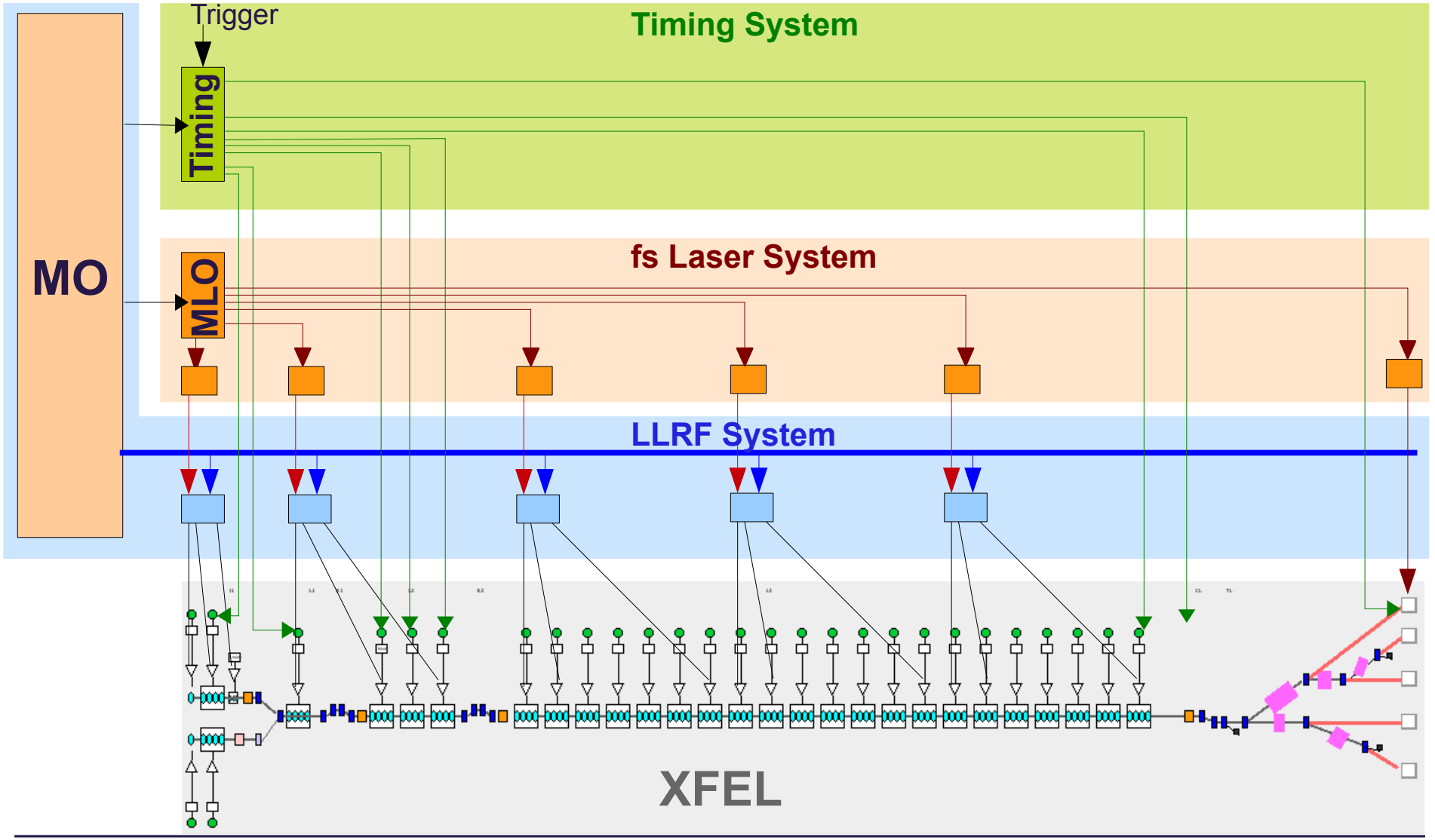
European XFEL

Synchronization and Timing Systems - Local

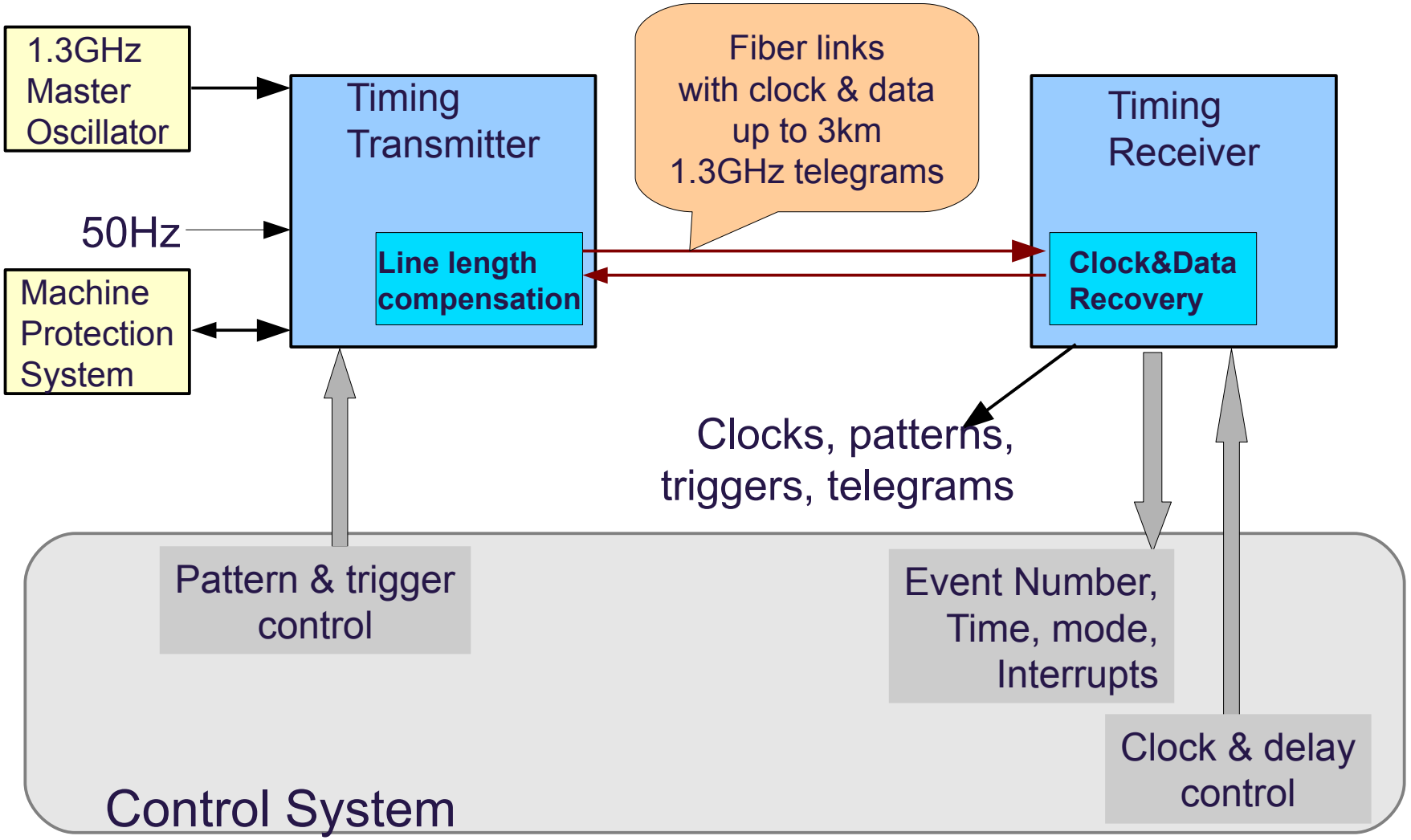


European XFEL

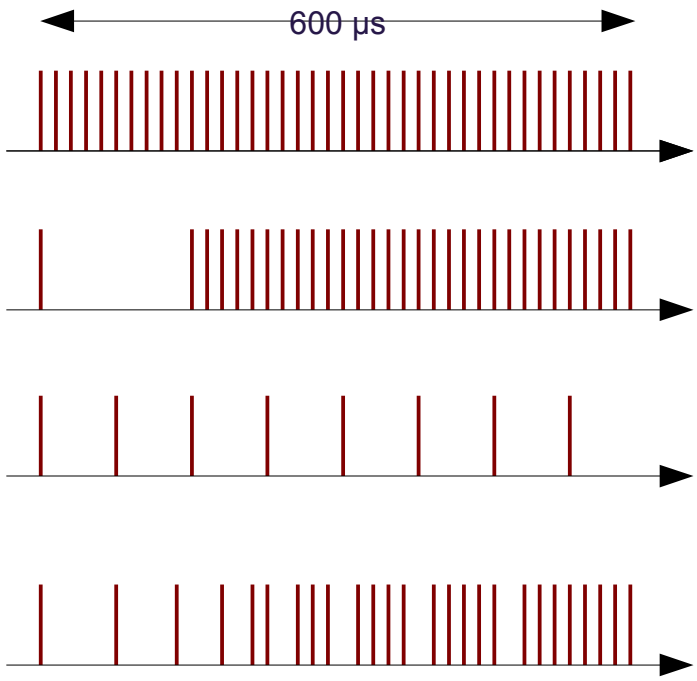
Synchronization and Timing Systems - Global



Timing System Blocks



Possible Bunch Patterns

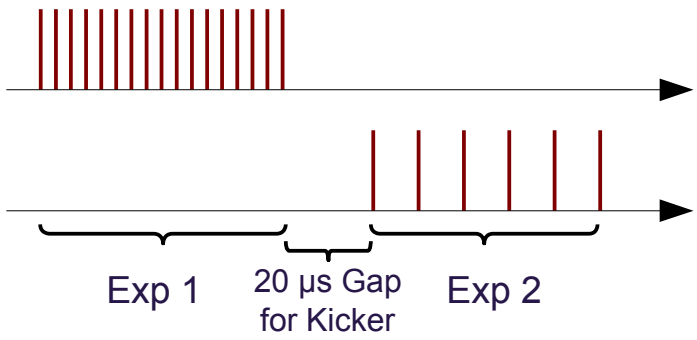


Max: 4.5 Mhz, 2700 bunches

Pre bunch

1 Mhz or lower frequencies

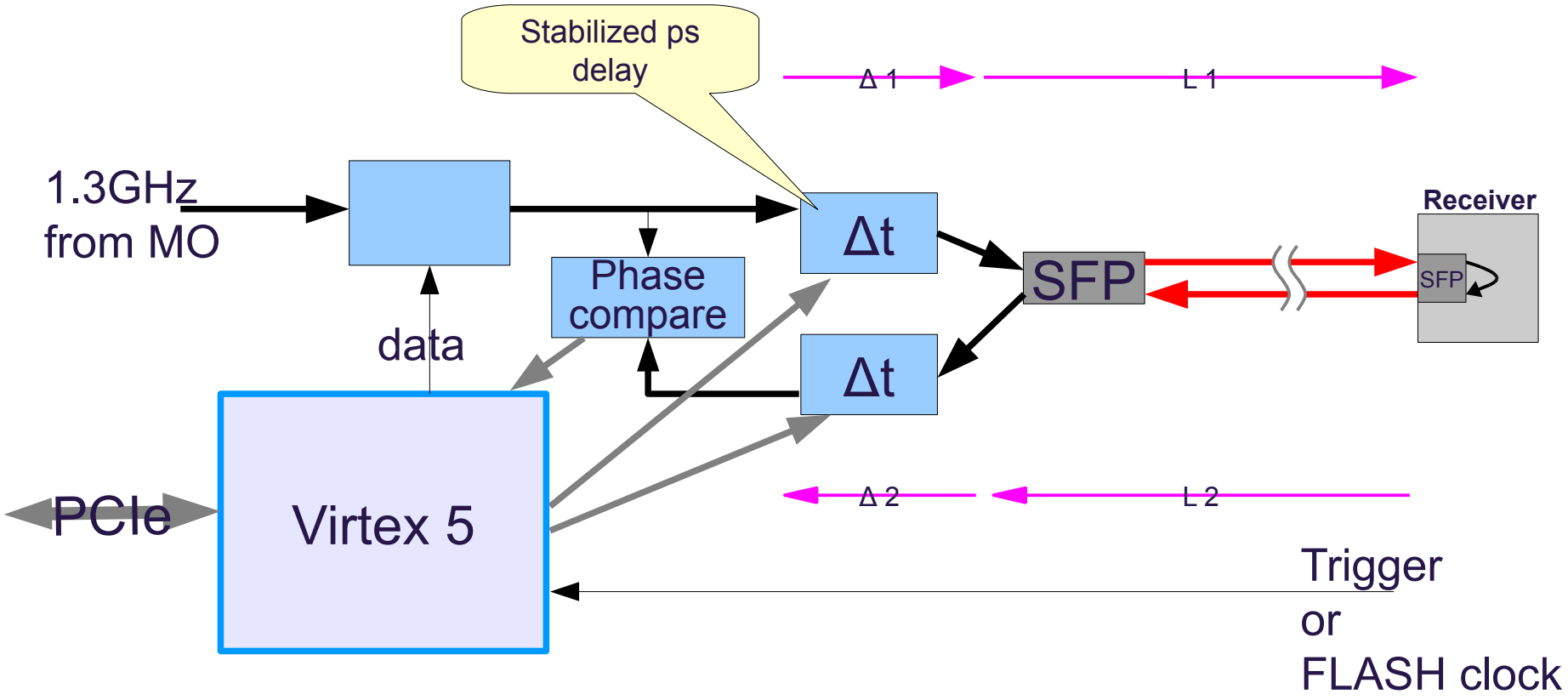
Arbitrary patterns



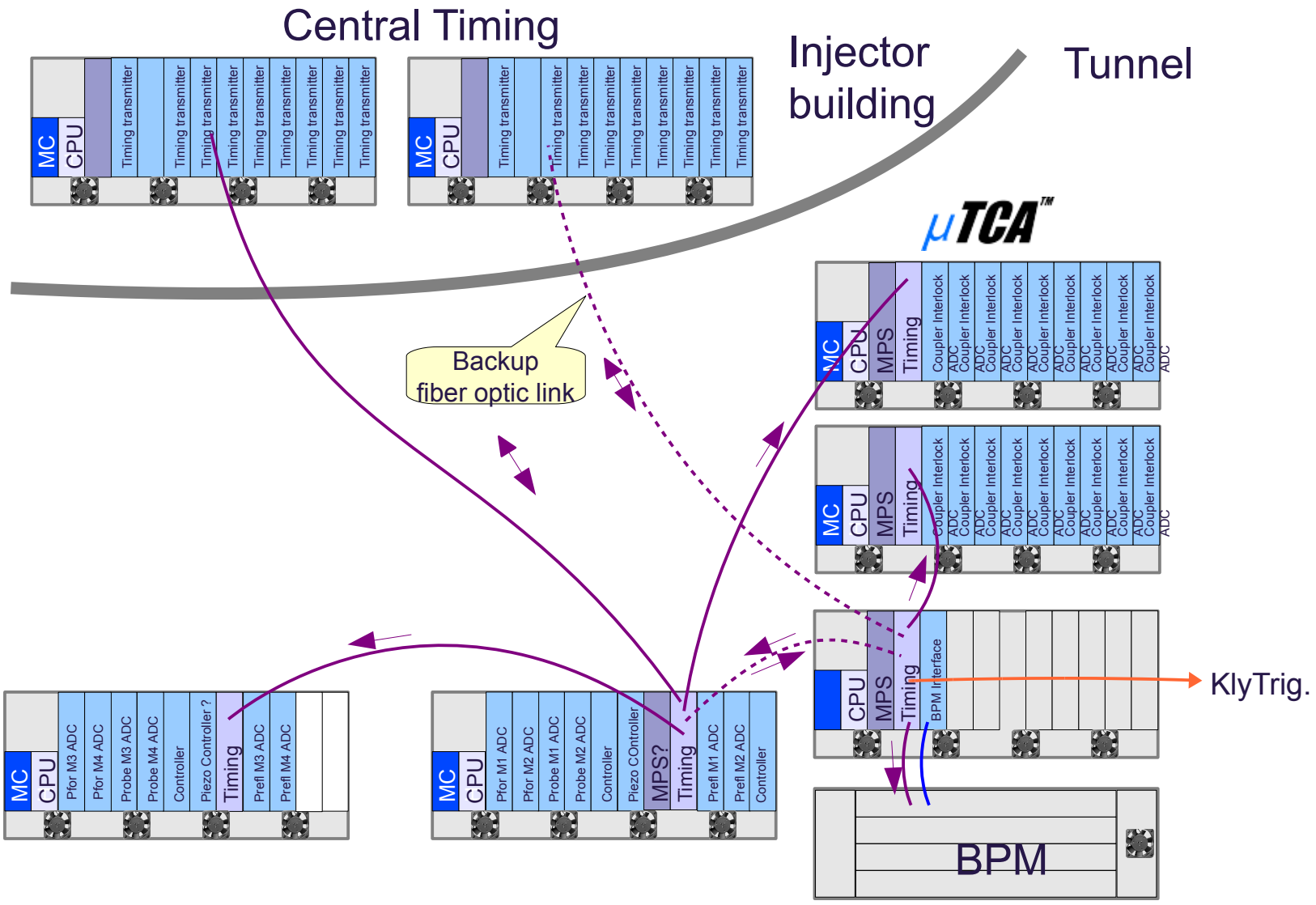
Different patterns @ different beamlines in one macro pulse

or varying patterns from shot to shot

Drift Compensation Schema



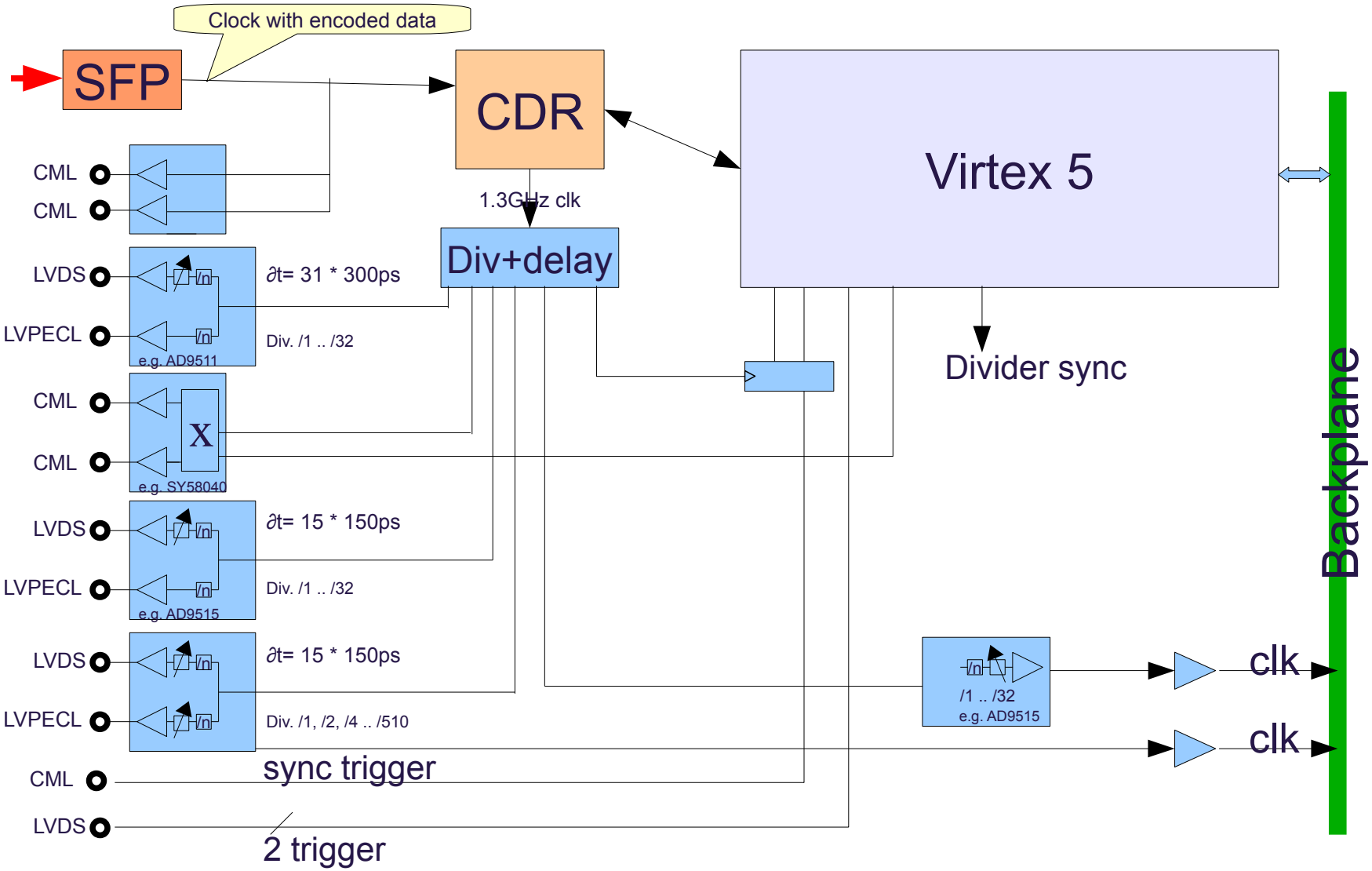
Timing Distribution



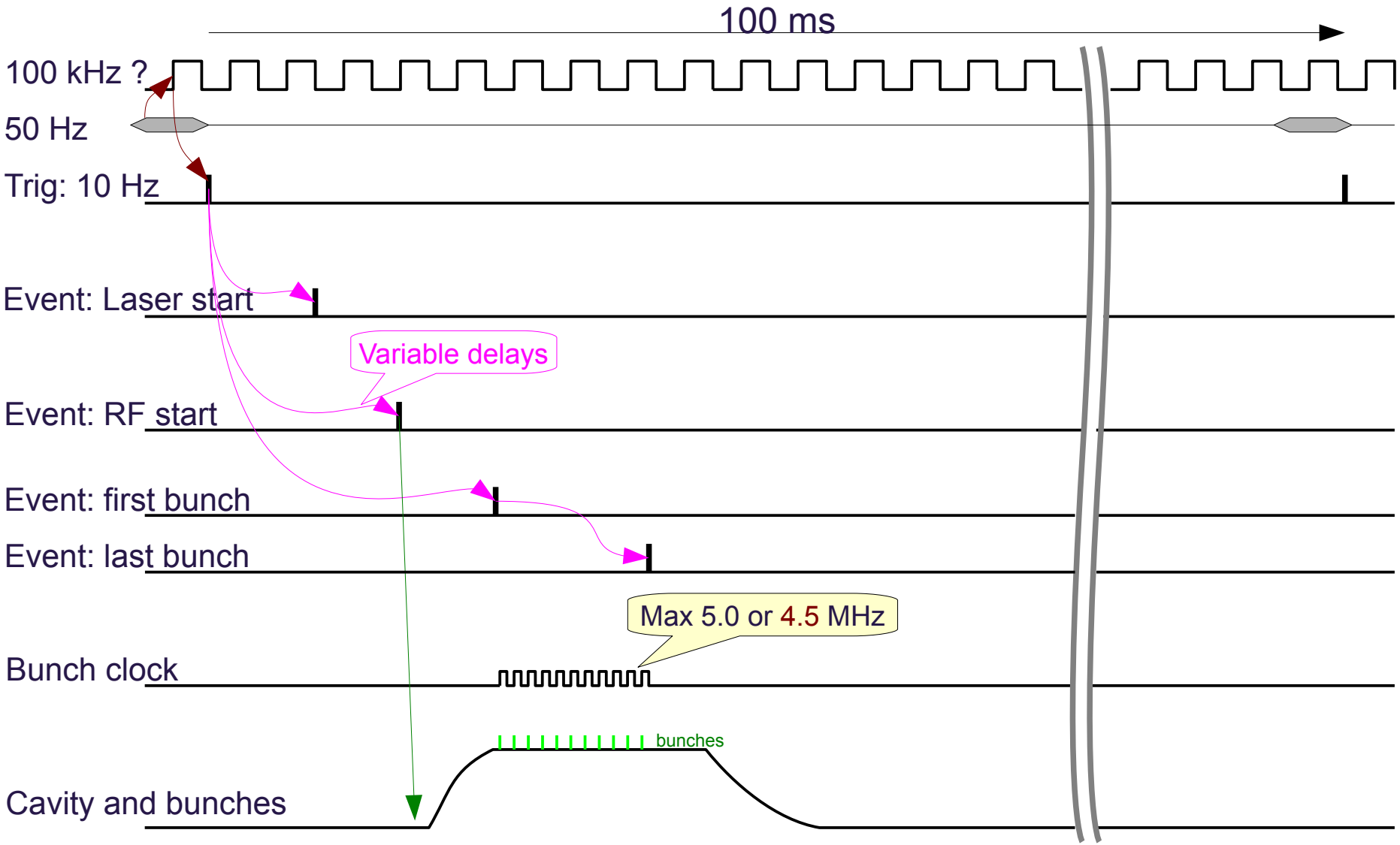
Prototype Status of Combined Xmitter/Receiver

- 2nd prototype AMC boards are ready
- Ready:
  - OS driver and DOOCS server to talk to chips
- ToDO:
  - Implementation of a drift compensation controller

Timing Outputs of the Prototype



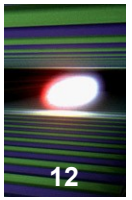
Clock and Trigger Sequences



Preliminary Specs

- Trigger:
  - Timing resolution: 1.54ns
  - Programmable with 32 bits (max delay seconds)
- Clocks:
  - Jitter: < 5ps RMS (goal)
  - Constant or burst (e.g.bunch clock)
  - Automatic adaption of location/beam mode
  - Fixed e.g. 100kHz (with const. Delay to first bunch)
- Raw 1.3GHz telegrams with encoded data
  - Data format is not yet fixed
    (e.g. number of filler words for the clock recovery TBD)

Requirements for the MO



- 20 * 1.3GHz outputs from MO
  - Best: differential --> input is LMK01020, AC coupled
- Optional 100.309kHz as trigger synchronization
  - LVDS, 1300GHz / 12960
  - Could be generated by the timing system