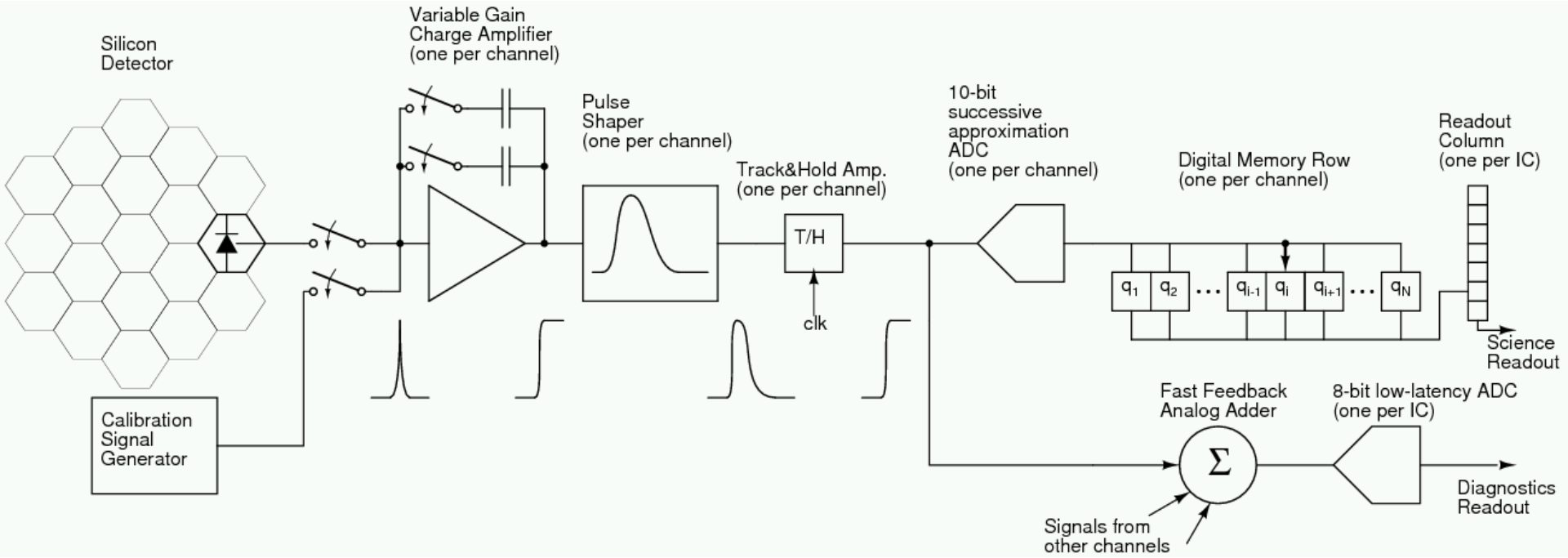
BeamCal electronics challenges

- 32 channels
- Large input signals, up to 40pC
- High occupancy, all data is read out at 10 bits for science purposes
- Low latency output, sum of all channels is read out after each bx at 8 bits, for beam diagnosis (fast feedback)
- Dual-gain front-end (50× ratio), for normal operation and physics calibration
- Radiation hardness requirements
- Parasitics due to wires between detector and chip, detrimental for front-end performance
- Minimum power dissipation
- Prototype in 0.18-μm TSMC CMOS technology

BeamCal electronics operation



- Dual-gain front-end electronics: charge amplifier, pulse shaper and T/H circuit
- Successive approximation ADC, one per channel
- Digital memory, 2820 (10 bits + parity) words per channel
- Analog addition of 32 channel outputs for fast feedback; low-latency ADC

Conservative average power consumption estimation per IC

- Front-end circuits: 1.8mW
- ADC: 0.9mW
- Memory: 0.03mW
- LVDS drivers: 1.8mW

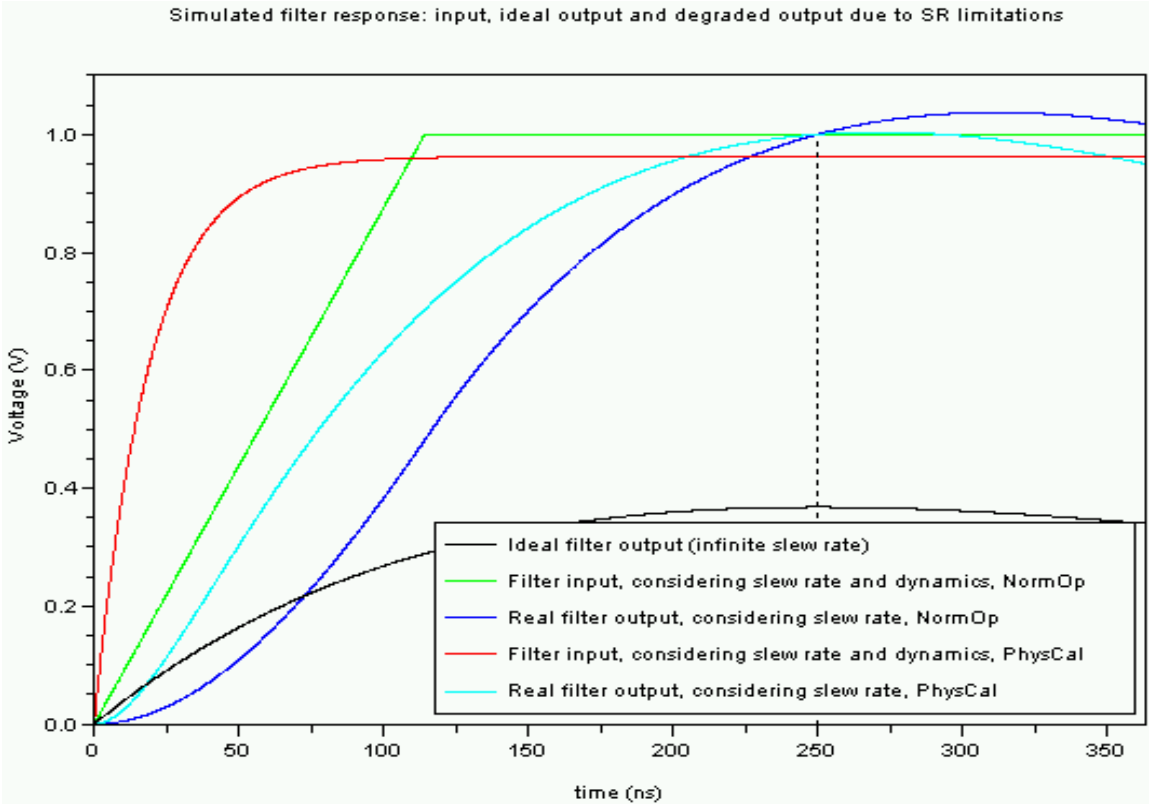
- Average power consumption per IC: 4.5 mW

Front-end design

- Objective: minimize current consumption, while still meeting specifications. But…
- Large input charge → large feedback capacitor (40pF)
- Charge amplifier output current required to charge feedback capacitor
  - High current → large power consumption, very inefficient
  - Low current → low slew rate, ballistic deficit degrades signal, aperture uncertainty due to dV/dt in filter output, nonlinear response…
- Input transistor current set by noise requirements for high gain operation

Front-end design (con't)

Expected front-end waveforms, full-scale input signals

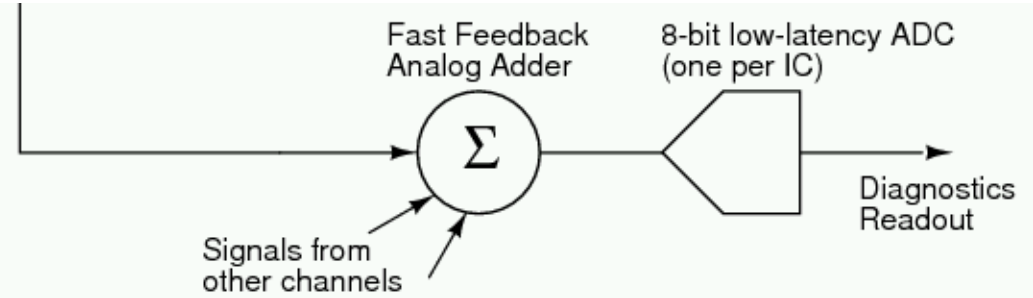


ADC and memory issues

- ADC power consumption is lightly dependent on the number of ADCs
  - one channel per ADC is simple in terms of operation
  - many channels per ADC are efficient in terms of area
  - successive approximation ADCs present a balanced tradeoff, could eventually assign a single channel per ADC without a significant increase in area; currently under study
- Memory choice: analog or digital?
  - Analog memory problems:
    - high droop rate due to switch leakage in TSMC018 (especially after irradiation)
    - radiation-tolerance techniques are not simple nor flexible
  - Digital memory problems:
    - more area
  - Digital memory will be used mainly due to flexibility

Fast feedback design

- Each channel's analog signal is extracted at the track-and-hold circuit output
- Analog adder generates the chip fast feedback signal
- A fast (low-latency) ADC is used to produce the digital output



Radiation hardness requirements

- Chip must be able to tolerate 1Mrad(SiO_2) total ionizing dose (TID)
- TSMC018 is naturally tolerant to TID, but some sensitive circuits in the chip require additional protection
- This can be done by using mitigation techniques:
  - Enclosed-layout transistors
  - Guard rings
- Consequences in circuit design:
  - Power consumption increases by 2× or more, depending on the circuit
  - Chip area increases by 2.5× in some circuits
- First prototype will not be radiation-tolerant, but will allow to:
  - assess the technology tolerance to radiation
  - detect the most radiation sensitive circuits

Planned milestones

- August 2007: Front-end designed
- December 2007: ADC designed
- January 2008: Memory designed
- February 2008: Fast feedback designed
- March 2008: Bias and supporting circuits
- June 2008: Circuit layout complete
- July 2008: Verification complete
- September 2008: Prototype ready
- December 2008: Prototype tests complete