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Summary of the workshop 'Future detectors for the European XFEL'

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Abstract

The workshop 'Future detectors for the European XFEL' took place at the European XFEL in September 2023. Many of the European institutes developing charge-integrating detectors were present. The workshop was focused on three main topics: developments on front-end ASICs, sensor technology and data acquisition and firmware development. The topics were introduced in a session dedicated to a summary of experiences at EuXFEL which included calibrating, operating and maintaining the detectors presently in use (so called “lessons learned”). The workshop was complemented by industry presentations.

This report summarizes the outcome of the workshop in the context of detector development at the European XFEL.

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Introduction

The European XFEL produces exceptionally brilliant and intense X-ray flashes using an advanced temporal pattern, which distinguishes it as a unique X-ray facility. The European XFEL remains unparalleled in its capability to generate up to 2700 pulses at 4.5 MHz within 10 Hz trains. However, owing to this specific time structure and the necessity to capture each pulse within a train, coupled with the requirement to detect from one to several thousand photons in a pixel, the use of commercial detectors is unfeasible. Initially, at the start of the European XFEL operation, customized pixelated detectors capable of operating at a maximum frame rate of 4.5 MHz were developed by external collaborators, and they have been operational for over five years. In order to be able to provide the next generation of detectors for the European XFEL instruments, a recent initiative for new detector development has been initiated.

In this context, the workshop 'Future Detectors for the European XFEL' took place at the European XFEL Company premises on September 18-19, 2023. It served as an opportunity to engage in discussions with potential partners regarding the new detector developments required for the European XFEL. Additionally, as part of the Phase I of the European XFEL detector development project initiated in 2023, the workshop played an important role in conducting a comprehensive survey of existing technologies, with the aim of establishing potential collaborations in the field.

The workshop gathered around 60 participants, with an equal representation of external attendees and those from within the organization. Notably, the workshop attracted participants from virtually all European groups engaged in the development of charge-integrating detectors for Free Electron Lasers (FELs), implying a significant interest. All the main aspects (ASIC, sensors and DAQ) were covered by the invited speakers. Furthermore, a considerable number of participants expressed interest in collaborating with the European XFEL in the upcoming detector development phase.

During the workshop, various technologies were presented, each accompanied by an assessment of its potential benefits and current level of maturity. This comprehensive overview is a valuable achievement as it enables a thorough evaluation of these technologies and will help in determining their suitability for the European XFEL program.

In the following sections, we will outline the European XFEL plans for detector development and discuss the necessary specifications for the next generation of detectors. We will also provide a concise summary of the presentations made during the workshop, beginning with an explanation of our future strategy. This strategy is aimed at ensuring the continuous and efficient operation of detectors at the European XFEL while enabling the development of a new generation of detectors with improved specs and performance, satisfying the future needs of the user community.

1 The European XFEL detector development program 2023-2030

1.1 Structure of the detector development program at the European XFEL

In late 2023, the first R&D phase for the Detector Development Program at the European XFEL was approved with associated funding. This program and budgetary provision aims to facilitate development initiatives and feasibility studies within the Detector (DET) Group at the European XFEL, which had primarily been focused on operational functions until that point.

Consequently, a significant portion of the funds have been allocated for the creation of new positions to foster the growth of expertise within the group.

The strategic plan outlines the start of detector development efforts in the following four key areas:

- detector mechanics and cooling;
- detector backend electronics;
- high-Z materials for hard X-ray detection;
- sensor and ASIC.

A budget has been allocated for the initial three-year phase, referred to as Phase 1. The objectives of Phase 1 are as follows:

- to evaluate ongoing projects within the detector development community, identifying those that align with the requirements of the European XFEL;
- to enhance the expertise of the Detector Group in the aforementioned key areas through specific projects aimed at strengthening the scientific capabilities of the European XFEL and initiating preliminary detector development activities;

- to identify a small number of key projects, taking into account the available technologies, solutions, and ongoing developments, to carry forward into Phase 2.

Phase 2, planned to commence in 2025-26, will mark the start of a broader detector development effort. This phase is expected to start in 2026, last five-six years, and is focused on producing one or a few fully functional detector prototypes including all the features of the final detectors. These prototypes may resemble, for instance, an AGIPD single module, a DSSC ladder, a Jungfrau 500k module, or an LPD mini module. The budget for Phase 2 is currently under discussion between the European XFEL Management and the governing bodies of the facility and is expected to be significantly larger than that of Phase 1. The realization of a large-area detector will follow the successful completion of Phase 2, starting 2031-2032. From past experience, it could take 3-4 years to build up a large-scale detector from the module prototype.

1.2 Role of the European XFEL in Phase 1 of the project

The level of European XFEL participation in various key areas will vary based on the expertise available within the organization and the facility requirements. The European XFEL is committed to assuming overall responsibility for mechanics and cooling design of the new detector systems. Consequently, the in-house design and assembly of extensive systems from individual detector modules is a task that will be led by the European XFEL.

Concerning the backend electronics, the European XFEL intends to actively engage in electronics and firmware design. This effort will involve close collaboration with external partners and ASIC designers.

This collaborative approach will see the European XFEL involvement move away from a customer-provider model, to a peer-based model. Clear interface documents will be prepared in this initial phase of the detector development program to support this approach.

In terms of ASIC and sensor development, most of the expertise and personnel will remain with our development partners. At the same time, the European XFEL has now developed the necessary competence to define the specifications and functionalities of the required ASICs, and to take an active role in the decision on the technology choices. Together with fellow collaborators, the European XFEL will work to set-up ASIC development plans. In addition, EuXFEL will actively contribute to part of the designs with a dedicated ASIC designer (currently in the hiring phase) and with the experience and know-how already present in the DET group.

This know-how can also contribute to the development and definition of CMOS sensors (DEPFET or standard CMOS) for soft X-ray applications.

Finally, the European XFEL's role in qualifying high-Z materials for detection of harder X-ray will primarily focus on data collection and analysis. Our commitment involves granting access to beam time for strategic detector development, to test both current prototypes and possibly novel materials or novel implementations, at the high frame rates and photon fluxes which can be presently reached only at our facility.

The European XFEL can also develop a dedicated setup including existing MHz rate ASICs and DAQ components to test novel materials. This would allow collecting data with different sensor materials using the same electronics and readout, decoupling the effect of the electronics to better determine sensor properties.

An additional objective of Phase 1 is to establish collaborations and agreements that will be carried forward into Phase 2, which is dedicated to prototype detector development. Phase 1 will, therefore, play a crucial role in defining the specific responsibilities of the European XFEL and its partners in the subsequent development phase.

2 Detector specifications

The tables below outline the primary detector specifications for the prototypes intended to be developed during Phase 2 of the European XFEL detector development program and eventually for the next generation detectors. It is worth noting that the majority of these specifications are already satisfied by the currently installed MHz detectors that were initially developed for the European XFEL, with the exception of the pixel size. A smaller pixel pitch has been a longstanding requirement from the scientific instruments at the European XFEL. However, in the pursuit of achieving this smaller pixel size, which is a major challenge, compromises may be necessary in other specifications, depending on the specific scientific application.

2.1 Performance parameters for hard X-rays

For the next generation of hard X-ray detector(s), the target performance parameters are summarized below. The term "possible variants" refers to a set of parameters or ranges of parameters that can be considered and agreed upon to accommodate different scientific requirements.

	Target values	**Possible variant**
Sensitive Energy Range	5 – 13 keV[1] with Si 13 – 50 keV with high-Z	3 – 13 keV[1] with Si 13 – 50 keV with high-Z
Dynamic range in photons	> 5 x 10^3 12 keV ph./px	500 – 1000 12 keV ph./px, one gain
Noise (ENC)	< 300 el. rms. ~1 keV photon in Silicon	
Frame rate	Burst mode, 1.1 MHz	Burst mode, 1.1 – 4.5 MHz
Sensor type	2D pixelated	
Pixel size	80 – 100 µm pitch	
Pixel count	Move away from fixed large detectors, modular approach	
Operating pressure range	Both ambient and vacuum (below 10^{-3} mbar) versions needed	

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[1] *Defined by QE of the sensor. Operation above/below is possible with reduced performance.*

2.2 Performance parameters for soft X-rays

For the next generation of soft X-ray detector(s), the target performance parameters are summarized below. The term "possible variants" refers to a set of parameters or ranges of parameters that can be considered and agreed upon to accommodate different scientific requirements.

	Target values	
Sensitive Energy Range	0.4 – 3 keV, possibility to extend to hard X-rays	
Dynamic range in photons	> 5 x 10^3 1 keV ph./px	500 – 1000 1 keV ph./px, one gain
Noise (ENC)	< 30 el. rms ~0.125 keV photon in Silicon	
Frame rate	Burst mode, 1.1 MHz	Burst mode, 1.1 – 4.5 MHz
Sensor type	2D pixelated	
Pixel size	80 - 100 µm pitch	
Pixel count	Move away from fixed large detectors, modular approach	
Operating pressure range	< 10^{-6} mbar	

2.3 General considerations

The main difference of the new generation of X-ray detectors compared to the existing detectors is the reduced pixel size. To accommodate different sizes and shapes of the detection plane, the detector must be designed in a modular fashion that allows for flexible assembly configurations.

Currently, the dimensions of the European XFEL large area detectors range from approximately 20 × 20 cm^2 to 50 × 50 cm^2. For the forthcoming generation of detectors, similar dimensions are expected to be employed. Consequently, the detector modules should permit the assembly of detectors with various shapes and sizes while minimizing dead areas between the modules. As mentioned above, the European XFEL is committed to assuming responsibility for mechanics and cooling design. Consequently, the in-house design and assembly of extensive systems from individual detector modules will be led by the European XFEL.

While the future repetition rate of the European XFEL (EuXFEL) is under discussion, burst mode operation will continue into the mid-2030s. It is anticipated that a Conceptual Design Report (CDR) for the new machine will be prepared in 2025-2026, followed by the development of a Technical Design Report (TDR) by 2028-2029. These reports will define how the machine will operate in the 2030+ timeframe, as well as outlining the detector specifications required for operation during that period.

A potential change in operating mode that could be introduced before 2030 without major machine modifications may involve longer bunch trains (up to a factor of 4) and a lower repetition rate (2.25 or 1.125 MHz). In any case, in order to fully exploit the specific features of the European XFEL time structure, it is imperative for the next generation of detectors to adhere to the following specifications: the ability to collect frames at a rate of MHz is a fundamental requirement that must be met to fully leverage the unique capabilities of the EuXFEL; the new detectors should possess a minimum data collection capability of a 1.125 MHz repetition rate in burst mode at 10 Hz; and provide readout of 400-800 frames per burst.

To ensure as much common use as possible, detector technologies should strive to remain the same, even if the sensor material is altered. For example, for hard X-rays there is the necessity for the ASIC to function effectively, even with the use of high-Z materials for the sensors.

3 The workshop

The workshop 'Future Detectors for the European XFEL' served as an opportunity to engage in discussions with our potential partners regarding the new detector developments required for the European XFEL. Additionally, as part of Phase 1 of the European XFEL detector development project initiated in 2023, the workshop played an important role in conducting a comprehensive survey of existing technologies, with the aim of establishing potential collaborations in the field.

The workshop took place at the European XFEL premises on September 18-19, 2023, with approximately 60 participants. The attendance was evenly split between external participants and those from within the organization. The decision to hold the workshop in person was made to encourage direct and open communication. The agenda and the presentations of the workshop can be found under

https://indico.desy.de/event/37831/

3.1 Goal of the workshop

The objectives of the workshop, 'Future detectors for the European XFEL,' can be summarized as follows:

- build upon lessons learned and experiences gained from the previous generation of detectors and other systems;
- highlight the criteria for the next generation of detectors based on scientific needs and facility upgrades;
- showcase ongoing development projects, with a particular emphasis on sensors, front-end ASIC technologies, and data acquisition;
- showcase state of the art technologies in ASIC development, sensors (including CMOS sensors, DEPFETs, LGADs, high-Z sensors) and DAQ technologies

- explore the potential benefits of these developments and technologies for both the European XFEL and the developers involved;
- promote communication and initiate discussions regarding potential collaborations.

3.2 Lessons learned from the present generation of detectors

Currently, the European XFEL operates three unique types of detectors. The 1-megapixel AGIPD [1] detector was deployed in its first version at the SPB/SFX and MID instruments of the European XFEL in 2017 and 2018, respectively. The 1-megapixel LPD [2] detector has been in use at the FXE instrument since 2017. The 1-megapixel DSSC [3] detector has been used interchangeably at the SCS and SQS instruments since 2019. Starting from 2020, a new version of the AGIPD detector, featuring a 500-kpixels prototype with enhanced electronics, has been operational at the HED instrument. Over the coming years, several more detectors from the previous development phase are set to be installed at various instruments, including a 4-megapixel AGIPD at the SPB/SFX instrument, a 1-megapixel AGIPD at the HED instrument, and a new version of the DSSC detector, incorporating DePFET sensors, at SCS and SQS (1-megapixel).

Six years of operation in the demanding conditions presented by the European XFEL have allowed precise characterization of the present detectors. The detectors are able to operate at MHz frame rates, reaching a high dynamic range of some thousands of photons per pixels allowing also single photon sensitivity. Their specifications are unprecedented and allow effective use of the European XFEL photon beam, including its very specific time structure. The experiments conducted with these detectors have yielded excellent results, published in leading scientific journals.

Extensive use of these detectors has also led to a list of potential enhancements to be incorporated into the next generation. Specifically:

- A detector can undergo comprehensive testing only under actual operational conditions. This means testing it at its full size, with the final installation infrastructure, and, in our case, with the European XFEL beam. The absence of the beam during the detector development phase inhibited the identification and correction of certain features before the final detector was fully assembled and installed.

- Integration of the detector at the beamline is a complex process, and the convenience and ease of operation for the detectors are paramount. Ensuring simple access to cables, connectors, and the inner components of the detector is crucial.

- Notably, the sensitive components of the detectors are prone to damage, making the availability of spare parts and straightforward repair procedures essential. Simple access to inner detector components for replacement and repair is essential.

- Detector safety has to be ensured with a simple, reliable and robust interlock system which can reduce risks.

- Operation should be user-friendly and straightforward. The detector should operate reliably and for an extended period with minimal human intervention.

- Defining interfaces is a critical task that needs to be addressed as early and accurately as possible. This applies to various aspects, including mechanical and cooling interfaces, as well as electronics, firmware, software, data formats, and data acquisition. Clarity and precision in these interface definitions, as well as proper accompanying documentation, are essential.

- Standardization plays a crucial role in reducing the operational workload. Developing variants of the same detector for diverse applications, such as different front-end options utilizing the same back-end, helps saving resources when it comes to integration and operation.

- The volume of generated data is at the GigaBytes/s level, and sustaining long-term raw data storage is impractical. Therefore, it is essential to develop efficient and reliable data reduction algorithms and methods.

- Going into more detail regarding the ASIC architecture:
  - Dynamic gain switching has demonstrated limitations, especially in the transitional region between different gain stages. Thus, it is essential to explore different calibration techniques or alternative implementations and solutions to achieve a high dynamic range;
  - the inclusion of analog memory cells complicates detector calibration and negatively impacts data quality. For the next generation of detectors, implementing digital memory as already done in the DSSC detector or eliminating memory altogether should be considered, provided that it is possible to transfer the data off the detector in real time;
  - it is essential to incorporate in-situ calibration sources at least at the ASIC level to facilitate fast, reliable, and efficient detector calibration.

3.3 Front-end ASIC development

Various institutes and groups presented ongoing developments for their own facilities and future plans. The Photon Science Detector Group at DESY is primarily driven by the developments for PETRA IV and introduced the **CoRDIA** [4] detector development. It features a small pixel pitch (110µm), high-speed readout (>= 100 kHz CW), high dynamic range, and low noise, similar to AGIPD. The ASIC, designed in 65 nm TSMC technology, includes on-chip digitization (>= 10-bit ADC) and enables fast data transfer based on the Timepix4 design (up to approximately 10 Gb/s off the ASIC). The readout system allows for the use of various sensor types (Si, LGAD, CZT). The initial version of the ASIC is expected to be available in 2027, with the first detector version around 2029, followed by a second version featuring an improved ASIC after 2030.

Additionally, there is consideration for a possible 1 MHz burst-mode version of CoRDIA, which would require additional development. Expectations regarding achievable pixel sizes for different numbers of frames were also presented, ranging from approximately 100 μm to about 165 μm for different technologies, with a varying number of collected frames per burst between 350 and 660.

The PSI Detector Group discussed potential developments for the **Jungfrau** [5] detector that could be suitable for the European XFEL. In the short term (ca 2027 in production), they are considering creating a version of Jungfrau with 32 cells instead of 16, capable of operating at a MHz frame rate. This version would be fully compatible with the existing backend electronics, making integration relatively straightforward. The option of implementing binning at readout level, increasing the dynamic range at the cost of reduced spatial resolution, was also presented.

On a medium-term horizon (2030+), they are exploring the possibility of integrating an ADC at the ASIC level and implementing fast digital data transfer at approximately 3 Gb/s. However, this would necessitate a complete redesign of the current backend electronics used with Jungfrau.

The PSI Detector Group is working on upgrading the **Gotthard** [6] detector to achieve a continuous frame rate of over 1 MHz. This represents a 2.5-fold improvement over the existing Gotthard-II detector. Alongside this enhancement, they will optimize the ADC performance. To enable fast data transfer from the ASIC, they are considering the implementation of a 1.6 or 3.2 Gb/s serializer directly on the chip. However, it is worth noting that this decision will have impact on the backend electronics, with the faster serializer potentially necessitating a complete board redesign.

Additionally, PSI detectors, including Mönch [7] and Jungfrau, are being used with various types of sensors to cover a wide range of photon energies, spanning from 0.25 keV to several tens of keV. PSI is actively engaged in the qualification of new sensor materials and technologies for both soft X-ray (between 0.2 and 2 keV) and harder X-ray (> 20 keV) photons. For the soft X-rays, they are collaborating with the Fondazione Bruno Kessler (FBK) to develop Low Gain Avalanche Diode (LGAD) sensors. In the case of harder X-rays, their focus is primarily on CZT and GaAs sensors, depending on the specific application requirements.

The **XIDyn** collaboration is dedicated to developing a detector tailored for hard X-rays within the range of 30 – 100 keV. It employs high-flux CZT as its active material and brings together expertise gained from the XIDER [8] and Dynamix [9] projects involving various partners such as the European Synchrotron Radiation Facility (ESFR), the University of Heidelberg, the Science and Technology Facilities Council (STFC), and Diamond.

The detector key specifications include a pixel pitch of 100 µm, aiming for single photon sensitivity, and a dynamic range of approximately 1000 – 2000 photons per pixel per pulse. The detector is designed to operate in both continuous and pulsed modes to align with the ESRF bunch structure. The detector features on-pixel digitization, and a version suitable for the European XFEL could achieve a frame rate of 1 MHz with around 200 memory cells.

To achieve its high dynamic range, the detector uses incremental digital integration, effectively 'pumping' charge away fast during the exposure period. This approach also helps mitigate the effects of afterglow, which is common with sensors used for harder X-ray detection. The actual dynamic range achievable depends on the speed of the charge pump and the size of the packets. However, it is important to note that the speed of the charge pump directly impacts power consumption, which is anticipated to be relatively high.

On the path to enhancing soft X-ray detection capabilities, ideas to upgrade the **DSSC** [3] detector for improved performance in its next generation have been presented. The design of the DSSC detector already meets all the specifications required for the new soft X-ray detector at the European XFEL, with the exception of the pixel size. However, the DEPFET-based detector has not yet been deployed in user operation. Once in operation this will provide an excellent opportunity to assess and qualify its performance under real conditions. The DSSC detector features very low noise, a high dynamic range, and implements analog-to-digital conversion with 800 digital memory cells. Additionally, it features pixel-wise sub-gain trimming for a large variety of photon energies to facilitate rapid optimization for specific scientific applications. These performance characteristics are achieved through various methods, including implementing an active pixel sensor with an entrance window tailored for soft X-ray detection and using filtering instead of correlated double sampling at the ASIC level. Furthermore, power cycling between bursts significantly reduces average power consumption.

While reducing the DEPFET pixel size should not imply major issues (prototypes are already available), the shrinking of the ASIC pixel size requires scaled CMOS technologies (65 or 28 nm). This might not be sufficient to allow achieving the required 100 µm pixel size and the desired quantity of frames to be gathered per train. Compromises or new architecture and/or new interconnection techniques might be necessary. A reduction of the number of memory cells or of the frame rate from 4.5 to 1.125 MHz cannot be excluded a priori. Other options to be studied are the possible clusterization of pixels (at sensor level with DEPFETs or CMOS active pixels) or the use of TSVs (through-silicon vias)

Given that gain switching is a critical feature of the first-generation detectors that has not fully realized the expected performance, it is essential to revisit the concept or explore new ideas to achieve a high dynamic range. One approach could be the utilization of **predictive gain switching**, where the required gain for a specific signal can be predicted by analyzing the rise time of the output voltage. This approach reduces the need for multiple transitions among various gain stages and allows for the decision on which gain stage to use to be made relatively early in the integration window.

This concept has already been implemented in the readout of real detectors and could potentially be integrated into an ASIC. Studies have started, focusing on 65 nm technology, with the aim of developing front-end electronics for a new detector designed for the European XFEL.

In an effort to reduce pixel size, the **PixFEL** [10] project was initiated in a collaboration including INFN Pavia/Bergamo, Pisa and Trento. This project uses 65 nm CMOS technology and envisions a 4-side buttable ASIC. It incorporates in-pixel digitization at a 5 MHz sampling rate and utilizes TSVs to enable the use of active edge sensors, minimizing dead areas. The sensor is designed with an entrance window optimized for soft X-ray detection (< 1 keV) while still allowing detection up to 10 keV with a sensor thickness of 450 µm. The pixel pitch is set at 110 µm. In this case, achieving a high dynamic range is made possible through signal compression within the ASIC. The design used for the ASIC allowed the implementation of the digital memory. This should have been placed on a third layer using TSVs. A complete prototype has not been realized and also TSVs have not been manufactured yet.

Additionally, the **FALCON** [11] project is focused on developing a detector for X-ray ptychography. This detector boasts a high frame rate of 1 MHz in continuous operation but with a moderate dynamic range of a few hundred photons. The Bergamo group is also involved in designing ASIC blocks using 65 nm CMOS technology for the RD53 collaboration in high-energy physics.

The Bergamo group has been involved in projects conducted in the more scaled **28 nm CMOS** technology, including the Falaphel [12], IGNITE, and PiHEX initiatives. During their presentation, one of the key takeaways was a comparison between the 28 nm and 65 nm CMOS technologies, highlighting their respective advantages and disadvantages. In the 28 nm technology, the analog cell area is reduced compared to the 65 nm technology, enabling the implementation of more complex pixel digital designs. However, it is important to note that the design rules in the 28 nm technology are more stringent, and costs associated with this technology both in terms of manufacturing and person-power for the design tend to be consistently higher.

3.4 Sensor development

In the discussion on sensor development, the primary focus was on sensors for both soft X-rays (< 2 keV) and hard X-rays (> 20 keV).

The MPG Semiconductor Laboratory, HLL, is a center specializing in cutting-edge silicon-sensor development. They produced the **miniSDD** silicon sensors, which have been integrated into the DSSC 1 Mpixel camera used at the SCS and SQS instruments of the European XFEL. In addition to miniSDD sensors, they also manufacture pnCCDs and DEPFET sensors, with the DEPFET sensors designed to be compatible with the DSSC.

The laboratory is involved in sensor mounting, integration, and testing, and they have contributed to projects such as pnCCD, ATHENA WFI [13], and EDET [14]. Currently, they are embarking on new developments related to the so-called German LGAD sensors, used for the MARTHA project, which incorporate an internal gain layer capable of amplifying signals by up to a factor of 20. Their expertise extends to interconnection, sensor module design, and assemblies.

The **DEPFET** sensors for the new version of the DSSC detector have been designed by PNSensor, a non-profit company specialized in sensor and detector development and fabrication. The production has been accomplished partially by the CMOS foundry of the Fraunhofer Institut in Duisburg and partially by PNSensor for the backside process of the entrance windows. The DEPFET sensors have an internal floating charge collecting anode (the so-called internal gate) that provides unequalled low noise for single photon sensitivity and intrinsic signal compression for a high dynamic range. The DEPFET sensors for DSSC are 725 µm thick, ensuring safe operation up to 8 keV due to the silicon shielding effect. They are covered with 150 µm of aluminum, which serves as visible light blocking filter, e.g. from lasers, but has an impact on the sensor quantum efficiency. In future productions the aluminum thickness can be reduced according to the experimental needs, if necessary.

As mentioned previously, the design of the DSSC detector meets the specifications for future European XFEL detectors, except for the pixel size. The pixel size could potentially be reduced to 75 – 100 µm either by implementing pixel-by-pixel bump bonding or by sharing one output node among 4 pixels, without the need for a change in bonding technology. This would require the implementation of CMOS switches or a CMOS MUX on the sensor, increasing the complexity of the sensor fabrication. However, before proceeding with the sensor fabrication, a feasibility study must be conducted on the ASIC. Furthermore, simulations of smaller pixels need to be performed to assess aspects like charge sharing and their impact on the science program.

The **ARCADIA** [15] R&D project focuses on the development of versatile Monolithic Active Pixel Sensors (MAPS) using 110 nm CMOS technology provided by LFoundry, particularly for large area detectors. This project has resulted in the production and qualification of several prototypes featuring various pixel pitches, sensor thicknesses, and layouts. Additionally, test arrays incorporating a gain layer have been manufactured.

For applications related to detectors for FELs, it is possible to increase the sensor thickness to the required 400 – 500 µm, and the backside terminations could, in theory, withstand high radiation doses. However, further comprehensive testing is needed to ensure their robustness in such environments. In general, more in-depth studies are required to better understand the effects of high photon fluxes and the specific conditions within the FEL environment on these MAPS detectors. With this technology it is in principle possible to implement pixels with on-sensor amplification, e.g., implementing the preamplifier on the sensor itself. This could be an alternative to the DEPFET even if the level of maturity is still uncertain. The intrinsic signal compression would then require some special circuit topology to be developed.

The Fondazione Bruno Kessler (FBK) presented its capabilities in sensor development and fabrication, including a wide range of sensor technologies. These technologies include planar strip and pixel detectors, SiPMs (Silicon Photomultipliers), SDDs (Silicon Drift Detectors), 3D sensors, and LGADs, which were mentioned in one of the PSI presentations. Applications of each of these technologies were shown. SiPMs are used both in large area high energy physics experiments, like those at CERN, and in industry, e.g. for medical applications. SDD arrays are implemented in e.g. the ARDESIA [16] detector, developed for high brilliance synchrotron light sources. The REDSOX [17] projects aims at developing a SDD-based detector for soft X-rays spectroscopic applications and for X-ray astronomy.

For applications in soft X-ray imaging, FBK is working on enhancing detector performance by focusing on sensor improvements. They aim to make it possible to extend detector capabilities by merely changing the sensors. In collaboration with PSI, they are working to optimize the entrance window for improved quantum efficiency and are exploring charge multiplication techniques to increase the signal-to-noise ratio. As part of this effort, they have developed LGAD sensors in various designs. In particular, inverted LGAD sensors have already demonstrated excellent performance when used with the EIGER [18] detector. Looking ahead, FBK is researching new designs with the goal of further improving LGAD performances, driven by new projects in high energy physics and photon science. Regarding their technological developments, FBK is investigating also TSVs and new materials, such as SiC or SiGe. Moreover, FBK plans to upgrade their clean room to include additional mounting capabilities in-house, further expanding their capabilities in sensor development and fabrication.

STFC provided insights based on their experience in developing sensors suitable for high photon energy detection. They utilized the LPD system to conduct tests on various sensor materials in different extreme conditions, particularly high pulse repetition rates and high flux levels. Their investigations with **Chromium-compensated GaAs**, using both LPD and Jungfrau detectors, revealed issues related to hole mobility. These issues resulted in shifts of the pixel pedestal and the appearance of halos in neighboring pixels.

The introduction of **High-Flux CdZnTe** material by REDLEN has opened up new possibilities in this field. This material was subjected to testing using LPD at LCLS, enabling high-flux measurements, although this was limited to a pulse rate of 120 Hz. Subsequently, it was tested at MHz rates using the Hexitec$_{\text{MHz}}$ [19] chip at the Diamond Light Source. More recently, it has been tested at MHz rates at the European XFEL using LPD. Thorough analysis of these results will help determine the applicability of this material for use at the European XFEL or identify the need for further testing.

3.5 DAQ and firmware development

ESRF introduced the **RASHPA** [20] platform, which serves as a data-transfer platform for high-performance DAQ (Data Acquisition) applications. The primary goal of RASHPA is to efficiently transfer data from detectors to processing nodes in a standardized manner. This platform implements remote direct-memory access (RDMA) and is specifically designed and optimized for modular detectors. RASHPA seamlessly integrates into the DAQ system and operates without the need for software intervention; it simply pushes the data into the destination buffers.

One of the key advantages of RASHPA is its flexibility. It can accommodate any number of processing nodes, and data can be dispatched in a configurable manner based on the specific application's requirements. RASHPA is a versatile package that is independent of the detector and adapts to the detector and computing node during configuration.

Furthermore, RASHPA's low-latency data transfer capabilities offer the potential for fast experimental feedback. For example, it can be used to make real-time adjustments to experimental conditions, such as correcting the sample position or tuning the intensity to reduce radiation damage to the sample, ensuring more efficient and effective data collection.

STFC has been involved in various areas of development, including **microelectronics, sensor technology, and data acquisition (DAQ)**. Their ASIC team has placed particular emphasis on achieving high-speed data transfer capabilities, with test structures for serializers reaching speeds of up to 14 Gb/s in 65 nm CMOS technology. They have also been engaged in advanced pixel design, with developments in both 65 nm and 28 nm technologies. Notably, 65 nm test structures have been created for high dynamic range applications at 1 MHz speed, and they have produced the Hexitec$_{\text{MHz}}$ full ASIC for high-speed spectroscopic detectors working at MHz rates.

In the domain of CMOS sensor development for MHz detectors, STFC has worked on projects such as PERCIVAL [21] and Kirana [22], and is now exploring stacked technology for future sensor designs.

On the DAQ front, the STFC approach involves separating the control path from the data path. The control path encompasses functionalities related to control, timing, power management, and data acquisition, while the data path handles various processing layers, ranging from simple data unscrambling to more complex tasks like data reduction. A key objective is to rapidly and effectively convert data from the chip to an optical format, optimizing data handling and processing. A stack of FPGA-based readout boards then processes the data, optimizing the information that is written to disk.

DigiLab was established in 1992 at Politecnico di Milano and features expertise in various areas, including hardware such as PCB design and enclosure/mechanics, firmware development, and software. They collaborate with numerous external partners on detector development and instrumentation projects. Specifically, they have an ongoing collaboration with the European XFEL on the DSSC project, focusing on optimizing the firmware.

Looking ahead, within the context of the DSSC project, DigiLab plans to initiate a redesign of the **DSSC Patch Panel Transceiver** (PPT) and input-output board (IOB) to incorporate significant improvements. This redesign aims to enhance the control of the interlock board on the detector control, explore the feasibility of upgrading the mounted FPGA, and consider how this could lead to a more compact design of the DSSC boards, which would be particularly beneficial for single modules. This study will also provide insights into the performance requirements for the next generation of detectors, encompassing aspects such as data processing and data reduction at the FPGA level, power consumption, and the type and capabilities of FPGA systems needed for these advanced detectors.

3.6 Industry presentations

Companies were also invited to illustrate which of their products or development could contribute to next generation detectors for the European XFEL.

DECTRIS stated that one of its key objectives is to broaden access to dependable detector systems within a larger user community by constructing durable and user-friendly detectors intended for deployment at various facilities. They stated that their commitment in the European XFEL detector development program would focus on a collaborative effort on the creation of a dependable MHz detector for the European XFEL. In addition to providing advanced technology, they are prepared to deliver spare parts and offer long-term support, ensuring the sustained operation of the detector.

Their primary objective would be to achieve a pixel pitch below 150 µm, enabling high-speed MHz operation while maintaining low noise and a wide dynamic range. To achieve this, DECTRIS proposes to organize the project into distinct phases. This phased approach helps mitigate risks and ensures the progressive development and maturation of various subsystems at each stage. Notably, one of the key challenges they are focused on addressing is the efficient management of high-rate data transfer associated with such fast detectors.

X-Spectrum, established in 2014 as a DESY spin-off, specializes in delivering fast X-ray detectors utilizing existing chip developments. Unlike some other entities, X-Spectrum stated that it does not engage in ASIC design themselves but offer customizable products tailored to the specific requirements of users. They showed that their product offerings are built upon technologies like Medipix (LAMBDA [23]) and AGIPD [1] (SPARTA).

X-Spectrum stated that it recognizes the substantial challenge of developing a detector from scratch. Thus, they position themselves as collaborative partners, particularly in select areas such as electronics, firmware design, sensor qualification, system production, and the provision of spare parts. They stated that their approach aims to facilitate the development of next-generation detectors by leveraging existing chip technologies and tailoring solutions to the unique needs of their users.

ADVAFAB and REDLEN are sensor providers with a strong presence in the X-ray community, particularly for high-energy photon detection. **ADVAFAB** presented detailed results using GaAs sensors. They showed that they have processed Cr-compensated GaAs wafers both in-house and in collaboration with partners, which involved wafer-level processing steps, lithography, and dicing. These sensors were subsequently bump-bonded to various versions of Timepix chips at ADVAFAB.

The results showed that ADVAFAB sensors exhibited good uniformity in comparison to commercial sensors and delivered good spectroscopic performance. ADVAFAB stated that it envisions itself as a potential sensor provider for the European XFEL and is open to collaboration as a partner for sensor manufacturing and hybridization. Additionally, receiving feedback on sensor performance under high repetition rates and high-flux conditions at the European XFEL would be valuable for ADVAFAB continued development efforts.

REDLEN is the leading provider of high-flux CdZnTe (CZT) sensors, particularly known for its high-quality CZT materials. Their high-flux process involves the use of wafers that are 2-2.5 mm thick and have been optimized to facilitate balanced electron and hole transport within the sensor. In 2021, REDLEN was acquired by Canon. During their presentation they expressed a strong commitment to supporting the global use and high-volume supply of premium-quality CZT sensors. REDLEN's stated primary focus is on sensor production and, although they do not specialize in ASIC development, they are working to reduce their standard pixel pitch to align more closely with the requirements of the scientific community.

4 On the path of new detectors for the European XFEL

During the development phase of new detectors for the European XFEL, it is essential to ensure the continued operation of the present detectors. Therefore, mitigation strategies to address the effects of detector aging must be implemented to prevent the need to divert resources away from the development program with tight deadlines.

4.1 Detector aging: mitigation strategy

The issue of detector aging should be addressed separately from the detector development program. The first pixelated MHz detectors were installed at the European XFEL in the second half of 2017. The designs predates this by 8-10 years. Aging of materials affects detectors in various ways:

- firstly, the most common aspect is the gradual deterioration caused by usage and the time based aging of individual components. This eventually leads to electronics and mechanical components becoming non-functional;
- specifically concerning the replacement of electronics components, which tend to become obsolete within a few years, eventually going out of production. For instance, some components of the electronics boards designed for the currently used detectors are now no longer in production. Consequently, producing spare parts based on the existing design is no longer feasible, necessitating at least a partial redesign. This introduces complications such as potential incompatibilities in functionality and possibly different form factors;
- frequent use also contributes to aging. Frequent mounting/dismounting, mechanical stresses, and notably, damage caused to sensors and

electronics due to the intense radiation generated by the European XFEL are factors that impact the expected lifespan of detectors;

- furthermore, infrastructure linked to detectors, such as coolers and power supplies, which are typically commercial components, encounter similar challenges. These include going out of production and the unavailability of spare parts, among other issues.

Mitigation strategies need to be implemented to:

- guarantee the availability of detectors at the European XFEL, enabling high-level scientific output at all times;
- ensure that the detector development program remains unaffected by detector aging and the absence of suitable detectors at the instruments, allowing the program to progress without any compromises necessitated by the need to replace an aging detector.

These objectives can be accomplished through various methods, with one of the most direct and costly approaches being the procurement of a large quantity of spare parts to be held in reserve until they are required. However, this procurement needs to occur timely to prevent component or technology obsolescence. There is a risk associated with this approach, as having an excessive number of spares can result in unnecessary expenses if they are not used or needed, or conversely, there may not be enough spares to ensure the detector lifespan until a replacement becomes available.

An alternative approach strikes a balance by partially redesigning obsolete components, making procurement more cost-effective and, in some cases, improving performance. This approach is feasible for components like electronic boards and FPGA systems. For instance, the boards could be redesigned to accommodate a more advanced FPGA to replace an obsolete FPGA. However, this approach is less feasible for ASICs, as a significant redesign or a change in technology can be just as costly and time-consuming as developing an entirely new design.

All of this assumes that old design files are available to the European XFEL in a format that facilitates swift modifications and adaptations. Furthermore, the European XFEL should possess the capability to review and modify boards internally and have the expertise to test the produced boards in-house.

If the previously mentioned strategies prove to be ineffective or if the timeline for new developments is significantly delayed, it would be prudent to investigate the option of integrating intermediary detectors at the European XFEL instruments. These intermediary detectors may offer reduced performance but should maintain stable and low-maintenance operation. They would serve as replacements for the obsolete detectors until the fully fledged next generation developments are available. It is essential to ensure that these intermediary detectors still guarantee high-quality scientific data collection at the facility.

Conclusions and outlook

The 'Future Detectors for the European XFEL' workshop took place on September 18-19, 2023, at the European XFEL Company premises. Its main goals were to discuss potential new detector developments for the European XFEL and to conduct a comprehensive survey of existing technologies, with the aim of establishing potential collaborations in the field. The workshop hosted about 60 participants, equally split between internal and external attendees, including representatives from various European charge-integrating detector development groups for FELs. This diverse participation indicated a successful start to the process. Furthermore, many participants expressed interest in future collaborations with the European XFEL. The workshop featured presentations on different detector technologies, each assessed for its potential benefits and current level of maturity, providing valuable insights for future evaluations in the European XFEL program.

The detector specifications for the next generation detectors are given in Sections 2.1 and 2.2. The future operational modes of the European XFEL are under consideration. Burst mode operation will continue until the mid-2030s. Plans include preparing a Conceptual Design Report (CDR) in 2025-2026 and a Technical Design Report (TDR) for the accelerator by 2028-2029. These reports will define the European XFEL operation beyond 2030 and specify detector requirements. Until then, the European XFEL will operate similarly to now. Potential changes that may be introduced before 2030 involve longer bunch trains and a lower repetition rate. A MHz frame collection rate is essential to fully utilize the European XFEL capabilities, requiring a minimum 1.125 MHz repetition rate in burst mode at 10 Hz, with 400 – 800 frames per burst. In addition to that, the primary change in specifications, compared to the current MHz detectors, is the requirement for a reduced pixel size, preferably around 100 µm. The current generation of detectors already fulfills all the other specifications for the next generation detectors; as such reducing the pixel size while, as much as possible, maintaining the rest of the present specifications represents the major challenge of the next detector development program.

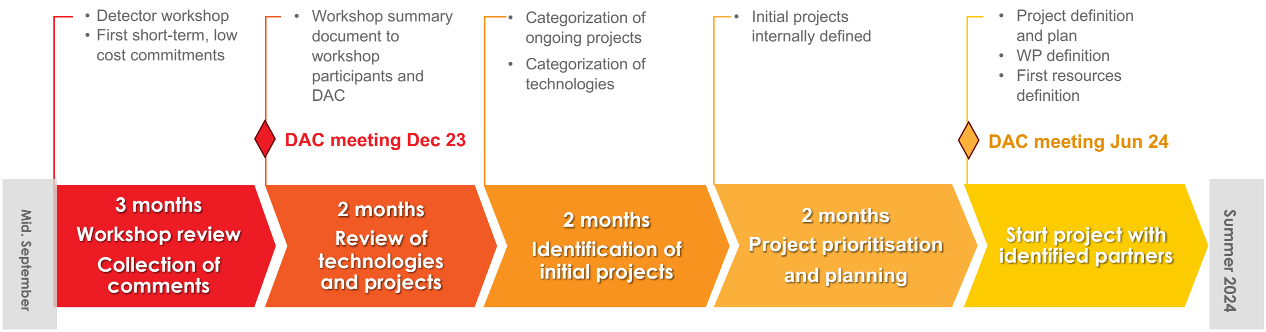
In order to ensure sustained detector operation, several mitigation strategies against detector aging must be employed. One approach is the procurement of spare parts, but this must be done swiftly to avoid obsolescence. However, this carries a risk of oversupply or shortage. Another strategy involves partially redesigning obsolete components, which can be cost-effective for items like electronic boards but less so for ASICs. In all cases, old design files must be transferable and adaptable. If these strategies are ineffective or new developments are significantly delayed, intermediary detectors with lower performance but stable operation can be explored as replacements for obsolete detectors, thus ensuring high-quality data collection.

It is essential to ensure that the aging of existing detectors does not impede the progress of new detector development: effective strategies must be in place to address aging, so as to prevent undue operational load which in conjunction with over-ambitious deadlines could compromise the quality of the new detectors.

Following the successful workshop, our next steps include:

- Distributing this summary document to partners and gathering feedback (by December 2023);
- categorizing ongoing projects based on their potential applications and timelines at the European XFEL (January-February 2024);
- categorizing state of the art technologies in ASIC development, sensors (including CMOS sensors, DEPFETs, LGADs, High-Z sensors) and DAQ technologies (January-February 2024);
- identifying a small number of key projects taking into account the available technologies, solutions, and ongoing developments (April 2024);
- internally prioritizing projects and formulating plans for upcoming developments (June 2024);
- Initiating contact with developers to establish collaborations (summer 2024).

These actions will help us progress toward our goals effectively.


Mid. September
• Detector workshop
• First short-term, low cost commitments
3 months
Workshop review
Collection of comments
• Workshop summary document to workshop participants and DAC
DAC meeting Dec 23
2 months
Review of technologies and projects
• Categorization of ongoing projects
• Categorization of technologies
2 months
Identification of initial projects
• Initial projects internally defined
2 months
Project prioritisation and planning
• Project definition and plan
• WP definition
• First resources definition
DAC meeting Jun 24
Start project with identified partners
Summer 2024

A Abbreviations and acronyms

ADC	Analog to Digital Converter
AGIPD	Adaptive Gain Integrating Pixel Detector
ASIC	Application Specific Integrated Circuit
CdZnTe or CZT	Cadmium Zinc Telluride
DAQ	Data Acquisition
DET	Detector group
DePFET	Depleted P-channel Field Effect Transistor
DSSC	DePFET Sensor with Signal Compression
FEM	Front End Module
FPGA	Field Programmable Gate Array
GaAs	Gallium Arsenide
LGAD	Low Gain Avalanche Detector
MAPS	Monolithic Active Pixel Sensor
MUX	Multiplexer
LPD	Large Pixel Detector
PCB	Printed Circuit Board
PLC	Programmable Logic Controller
SDD	Silicon Drift Detector
SiC	Silicon Carbide
SiGe	Silicon-Germanium
SiPM	Silicon Photomultiplier

B Definitions

Backend electronics: the part of the (detector) electronics which starts at output of the Front End Module (FEM) and ends when the interfaces to the European XFEL infrastructure starts (e.g.: plug to connect the optical fiber to the DAQ, plus to Karabo and / or timing system, plug to PLC system).

Front End Module (FEM): a complete detector unit that includes essential components such as the sensor, ASIC and the initial interface electronic board, along with any necessary mechanical parts to maintain the unit's structural integrity. Notably, the FEM functions as a unified entity, and any replacement or modification of individual components within it requires the disassembly of the entire module.

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