PAUL SCHERRER INSTITUT

PSI

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Overview of Jungfrau improvements in the short and ~~long~~ medium term: a EU-XFEL perspective.

Future Detectors for the European XFEL - Sept. 2023

Outlook

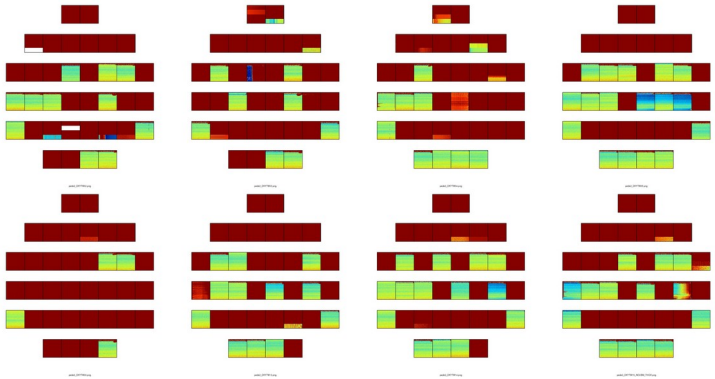
Current PSI JUNGFRAU development plan

- JF 1.2 – improved linearity, uniformity and calibration
- JF 2.0 – 10kHz frame rate, on chip ADC.

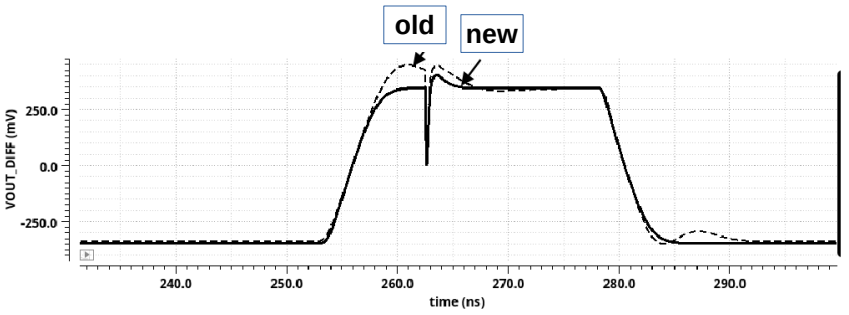
a JUNGFRAU dedicated to EU-XFEL ?

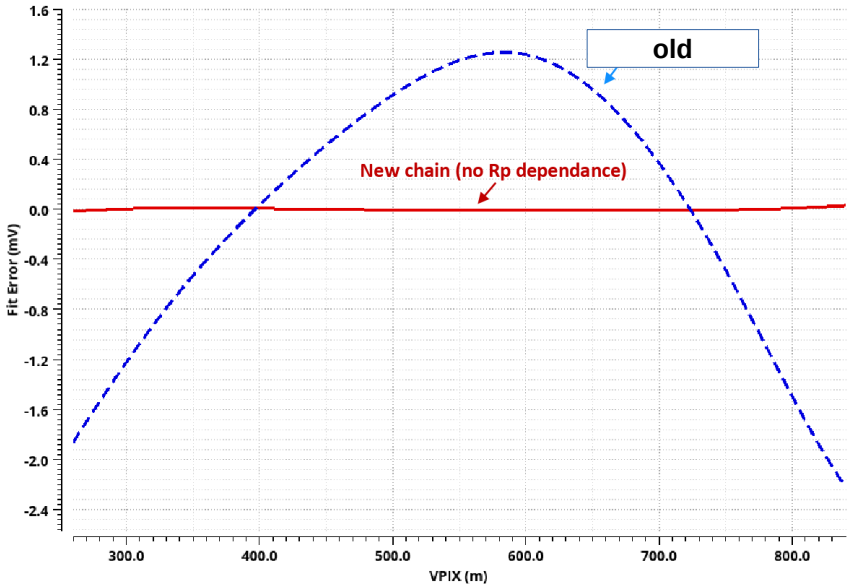
- storage cell (SC) optimization
- FE designed for 1MHz speed
- increase SC number.
- 2x2 binning

JF 1.2 readout ASIC



- main motivation: terrible yield for JF1.1
- occasion to improve the analog readout chain
  - linearity ~1% → <0.05%
  - speed – phase margin
- Tape-out Oct ‘23
- Drop in replacement for JF10-JF11.

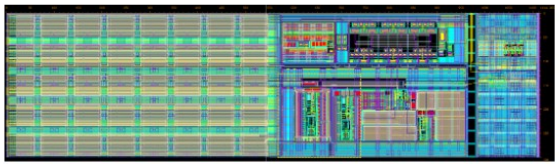




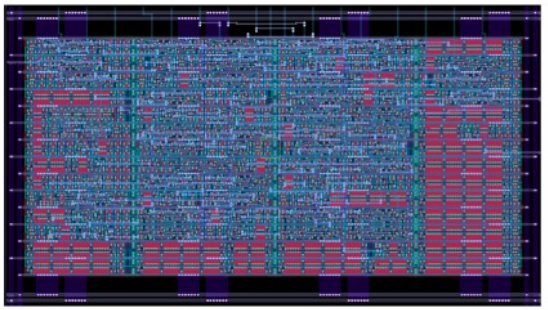
JF 2.0 towards higher frame rate

- 10kHz frame rate target
- On chip ADCs
  - preliminary specs:
  - 12b 10Ms/s
  - every 8 columns
- High speed serializers and transceivers for off chip communication
  - 3.125 Gb/s
  - 10/8b encoding
- Requires complete back end and DAQ redesign – synergies with Matterhorn.
- On the FE side, we are evaluating:
  - lower noise at long exposure times
  - higher DR for FELs (4x higher)

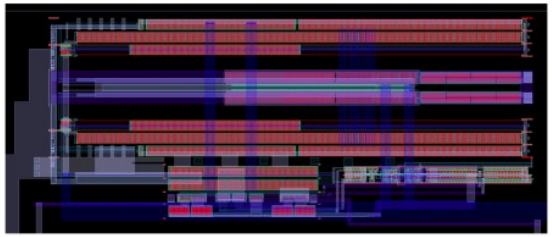
PLL



Serializer



CML driver



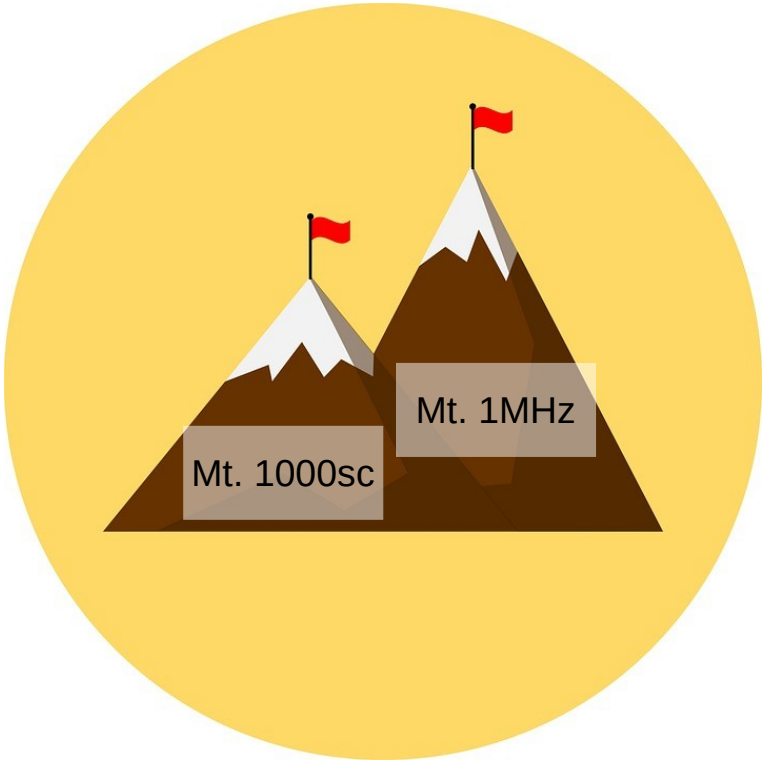
JF for EU-XFEL? a modest proposal

110nm technology and constrained manpower:

- no ambition to climb the 1MHz CW /1000 cells mountains.
- shift the focus to provide a dependable, 32image per bunch, 75um pitch, 1MHz burst rate, multiMp detector.
- can be delivered on a short timeline!
  - Not exciting, but:
    - Useful
    - Soon
    - “cheap”

On our standard 500k pixel sensor module, 1MHz means ~1TB/s.

A staggering 256 5Gbps links per ASIC!



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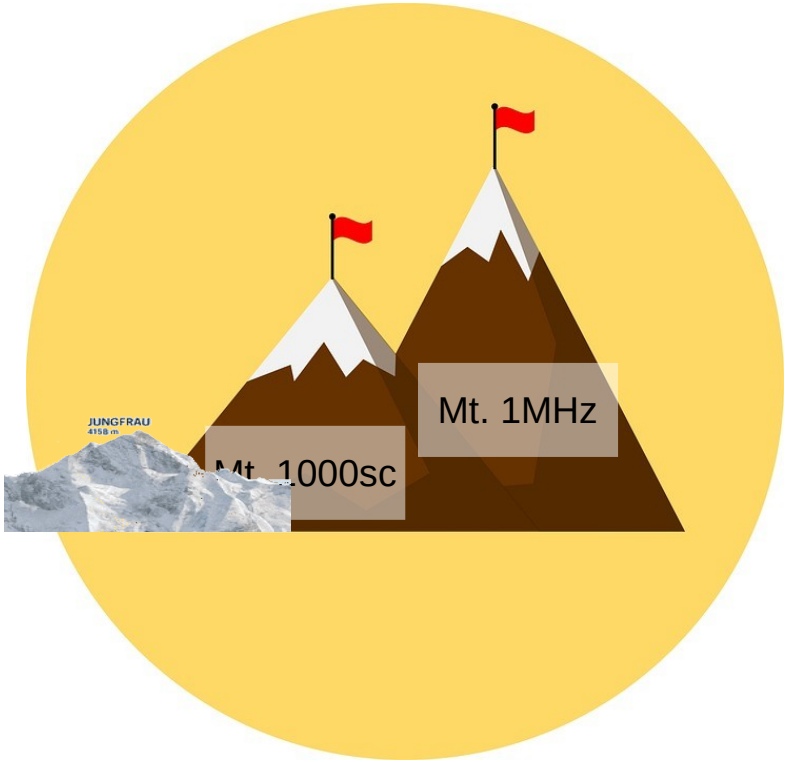
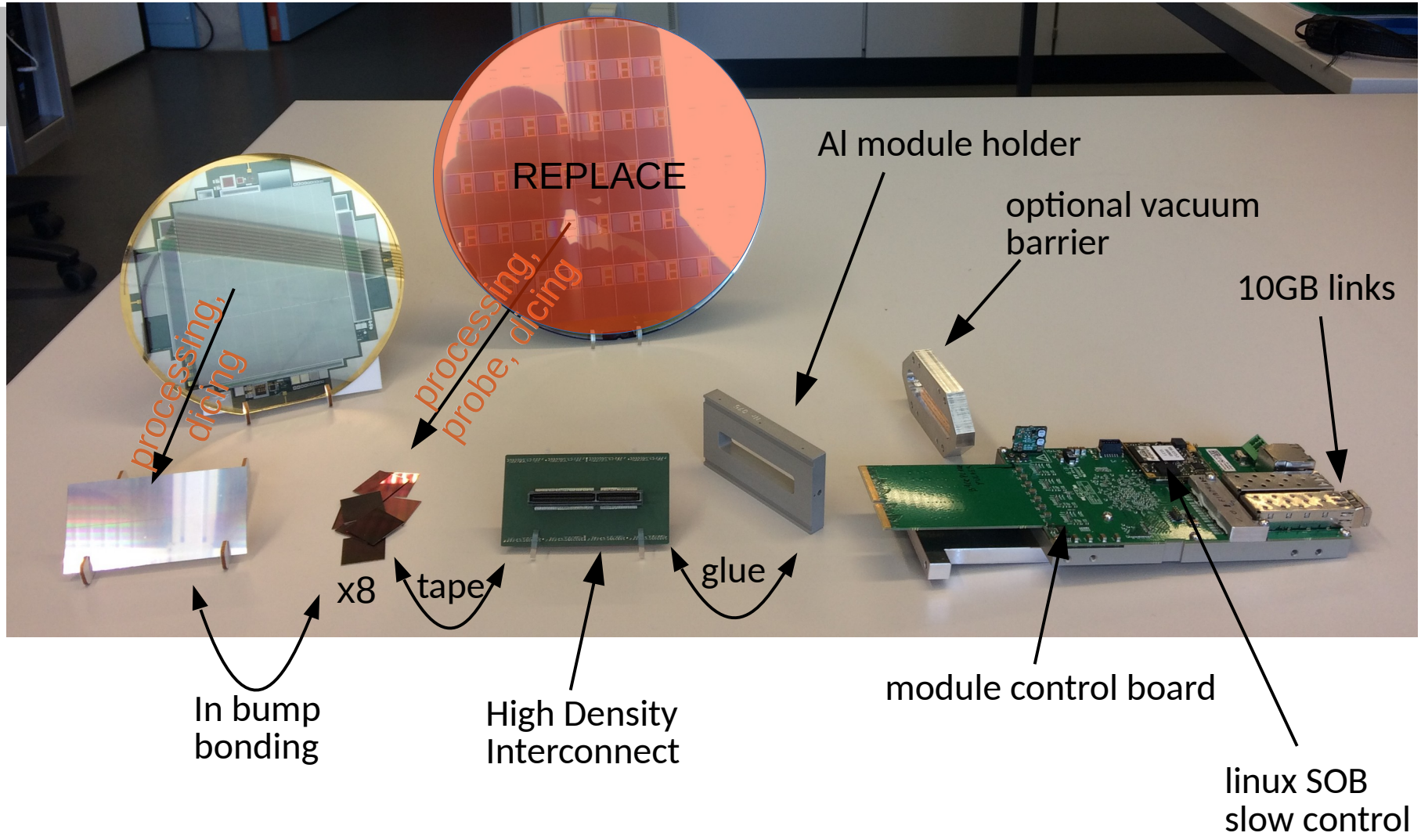


Drop in replacement

Sensor, HDI, readout, mechanics, DAQ all stay the same

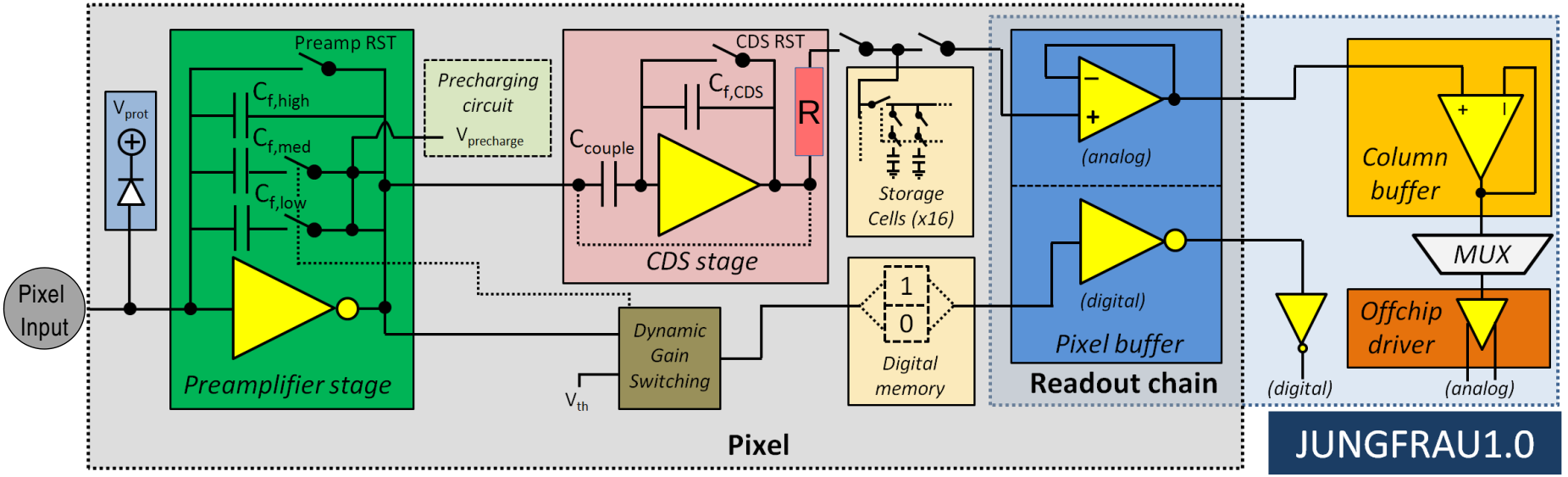


1MHz operation

- Burst speed today limited by
  - SC bandwidth, due to filtering resistor,
  - CDS reset after PRE reset

resistor removal, cap reduced

CDS stage pipeline OR complete CDS bypass (noise in G0 will increase by ~2.5x) in fast-burst mode



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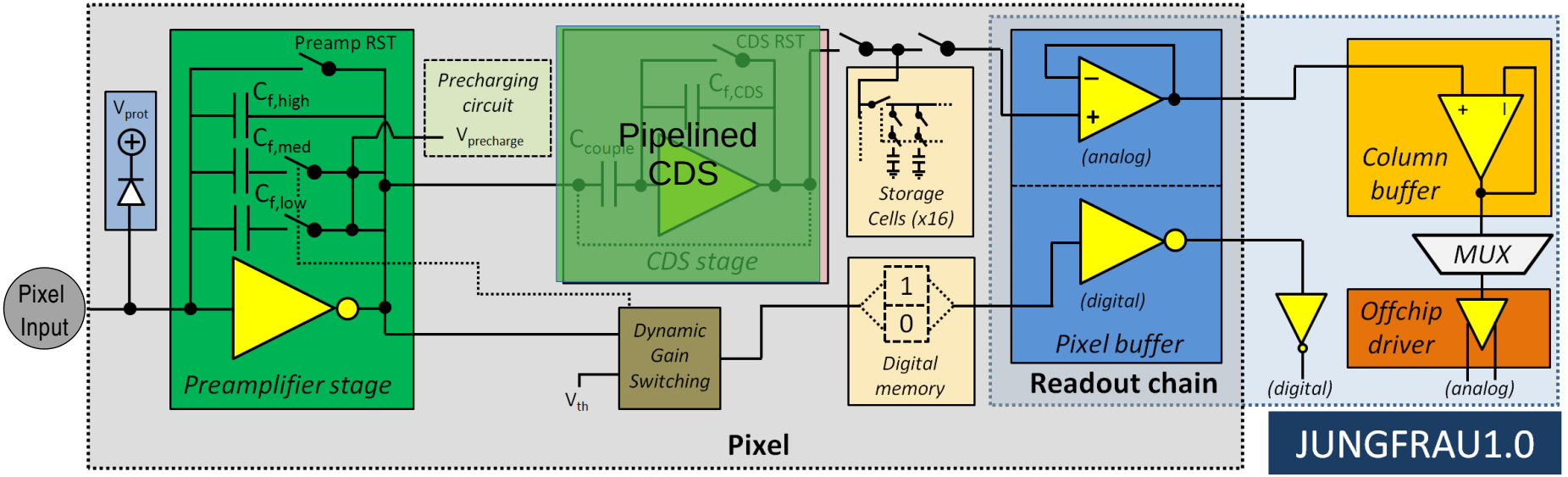
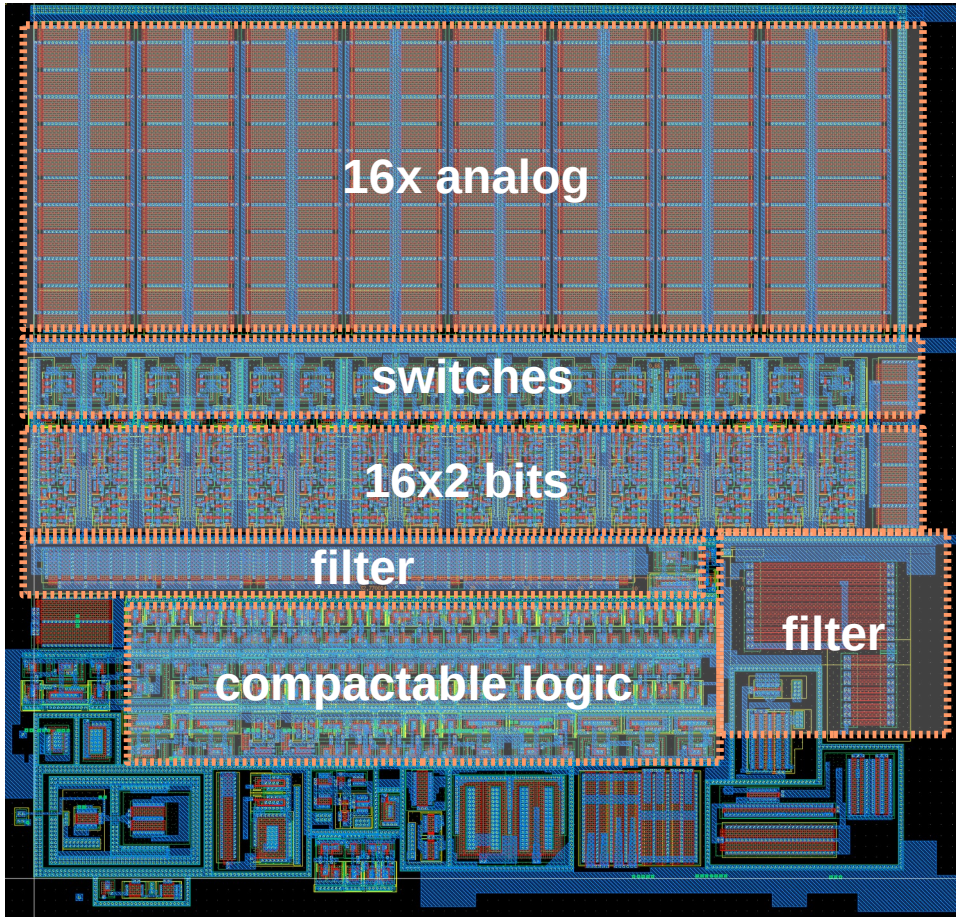


Number of storage cells.

- current JF: 15x500fF + 800fF

- reduce to 400fF, improve layout
- more compact switches
- logic in linear vs enclosed
- Filtering (decoupling) capacitors removed

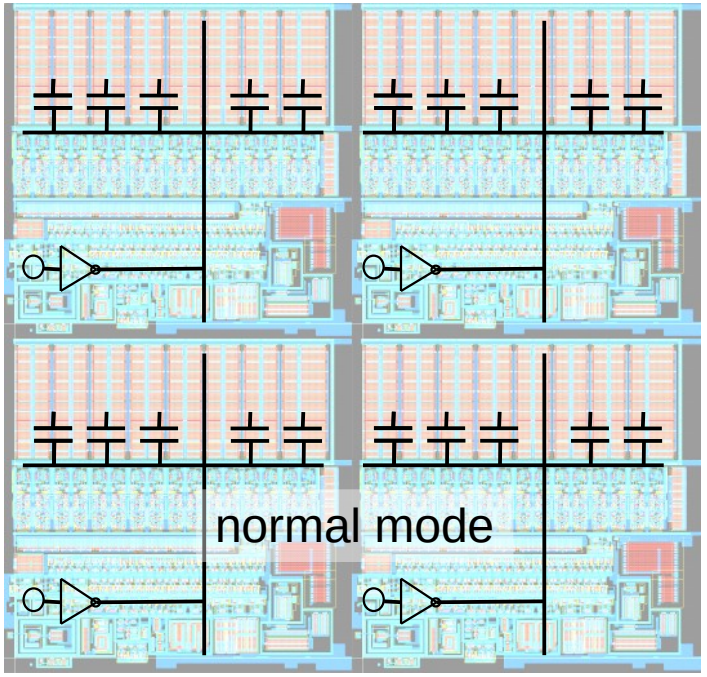
- fitting 32 caps does not look too difficult.
  - Still 60% of AGIPD SC area density which was aggressive.

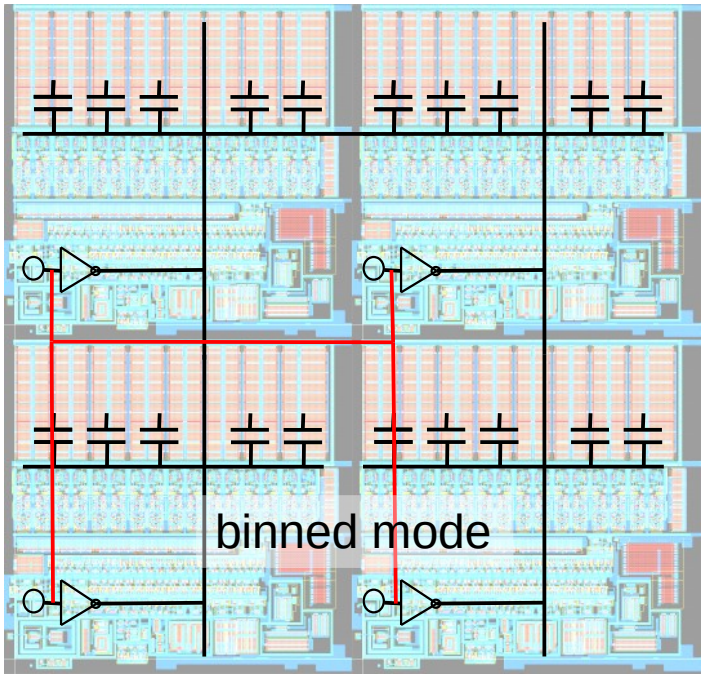


Binning

- pixels are part of a 2x2 pixel cluster.
- when configured in binning mode, the SC busses are connected together to the same pixel output
- amplifiers inputs also connected
- only one comparator/digital block enabled
- readout unaffected (bus split)

normal	binned
pitch 75μm	pitch 150μm
noise 0.3keV	noise 1.5keV (est.)
DR 10000 γ	DR 40000 γ
SC# 32	SC# 128





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END.