XIDyn collaboration

a new approach to high-energy 2D detection for 4th generation synchrotrons

Paolo Busca[1]
on behalf of the XIDyn collaboration

1. European Synchrotron Radiation Facility

ESRF The European Synchrotron

UNIVERSITÄT HEIDELBERG ZUKUNFT SEIT 1386

diamond

UKRI Science and Technology Facilities Council

Future Detectors for the European XFEL. Sep 18 – 19, 2023

Outline

1. Introduction

- Motivation
- DynamiX and XIDER projects
- XIDyn collaboration

2. Front-end architecture

- Readout concept
- Continuous and pulsed illumination
- Data handling and telegram protocol

3. Experimental results

- Prototypes and characterisation
- High-flux CZT

4. XIDyn collaboration

- Common MPW design
- Scale-up plans

Motivation

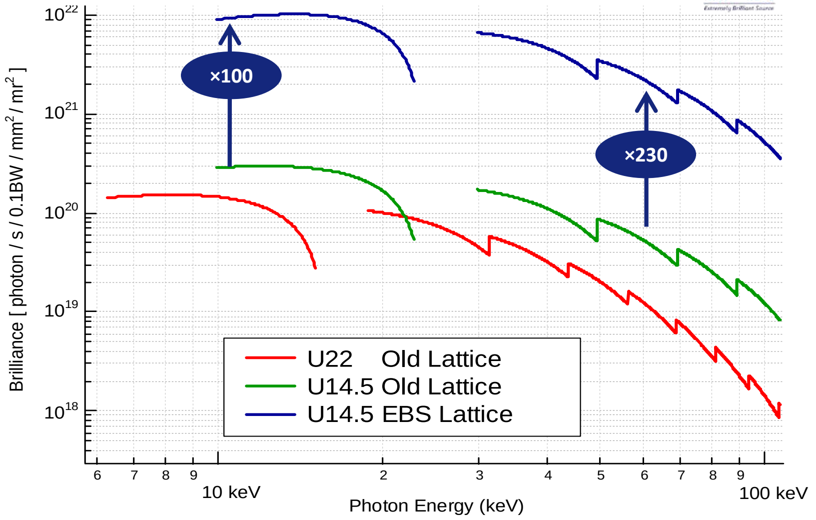
New generation (4^{th}) of synchrotron and FEL facilities

- Diamond II
  - Planned upgrade
- ESRF Extremely Brilliant Source (EBS)
  - In user mode since 2020

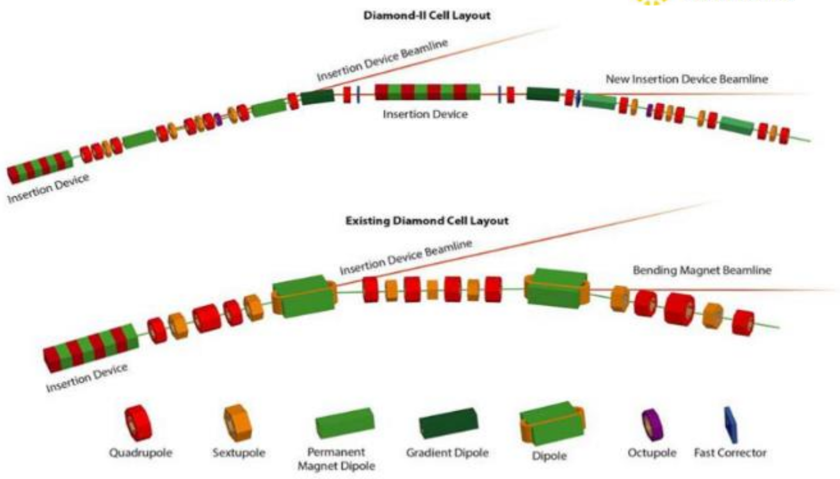
New science opportunities require improved instrumentation

- X-ray detectors
  - Extended dynamic range
  - Shorter time domains: intrinsic time resolution and frame rate
  - Detection of high energy photons

Example of ESRF brilliance gain [photons/s/0.1BW/mm2/mr2]

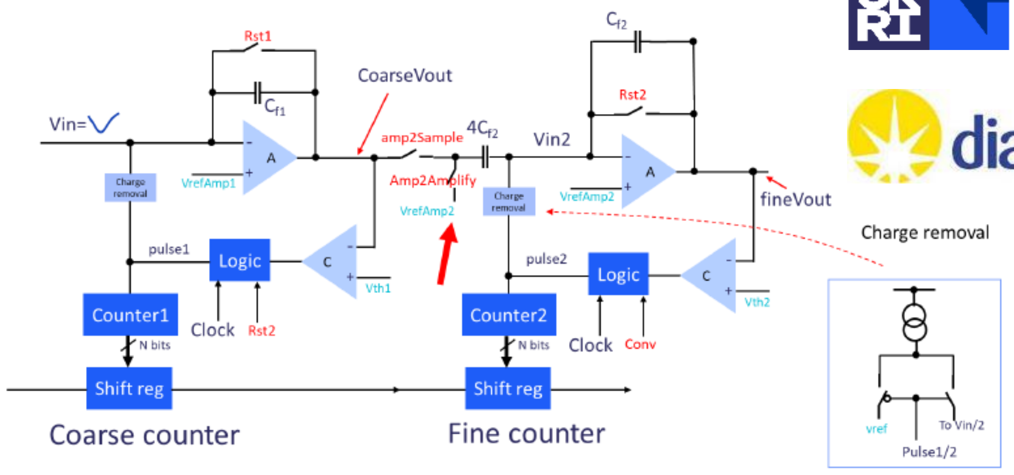


Schematic of current Diamond and future Diamond II lattice

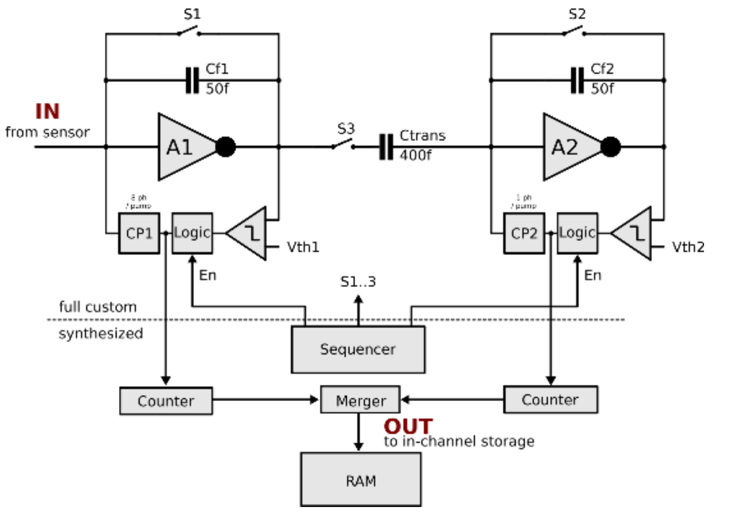


DynamiX and XIDER projects

DynamiX



XIDER



“Low energy” single-crystal diffraction

- “Soft” organic samples (e.g. protein crystals)
- Energy range: 15 to 30 keV
- Data accuracy is a must (crystal structure determination)
- “Long” integration times: ~10 µs to (many) ms
- Frame rate determined by integration time

“High-energy” time resolved diffraction

- “Hard” inorganic samples (often polycrystalline)
- Energy range: 30 to 100 keV
- Sensitivity to fast changes is crucial
- Sub-µs repetition (limited by beam time structure)
- Continuous and burst mode readout (memory)

Different target applications and parameter space!

XIDyn collaboration

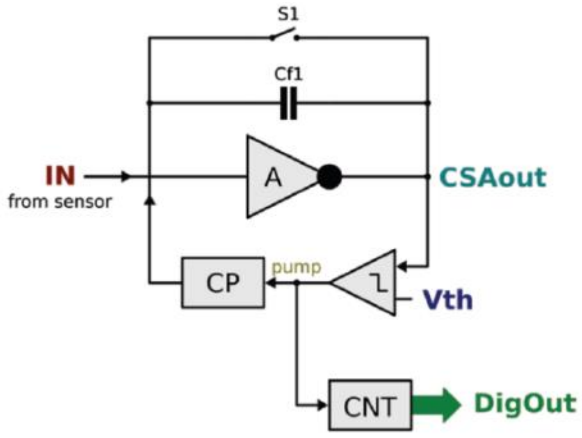
Common technical choices

- Readout concept
- High-flux CZT
- Data Acquisition Framework

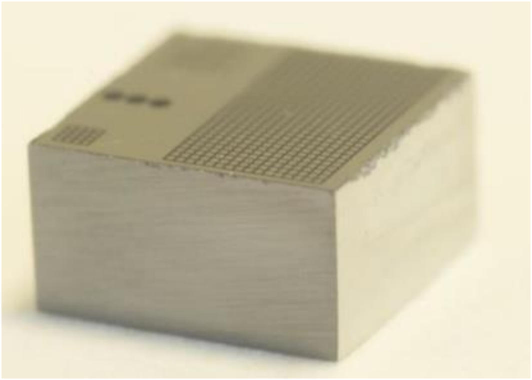
XIDyn collaboration

- Started in 2022
- Development of a common platform
- Attempt to merge both designs

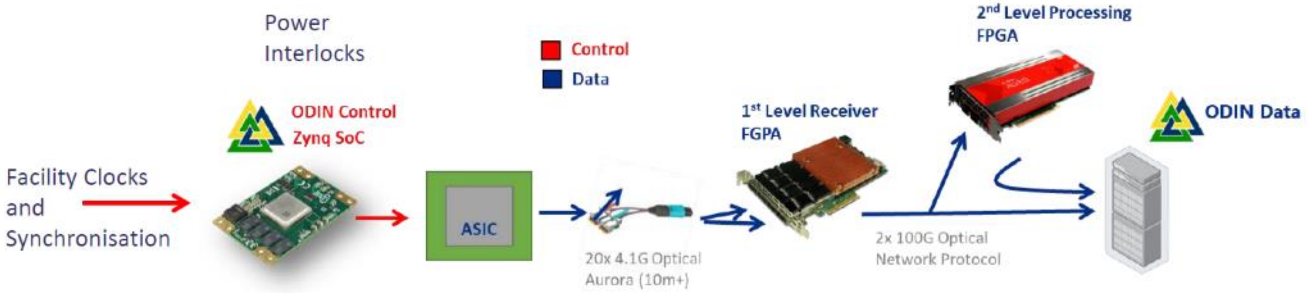
Front-end concept



High-flux CZT
(Redlen & Due2Lab)



Data Acquisition System



Outline

1. Introduction

- Motivation
- DynamiX and XIDER projects
- XIDyn collaboration

2. Front-end architecture

- Readout concept
- Continuous and pulsed illumination
- Data handling and telegram protocol

3. Experimental results

- Prototypes and characterisation
- High-flux CZT

4. XIDyn collaboration

- Common MPW design
- Scale-up plans

Readout Concept

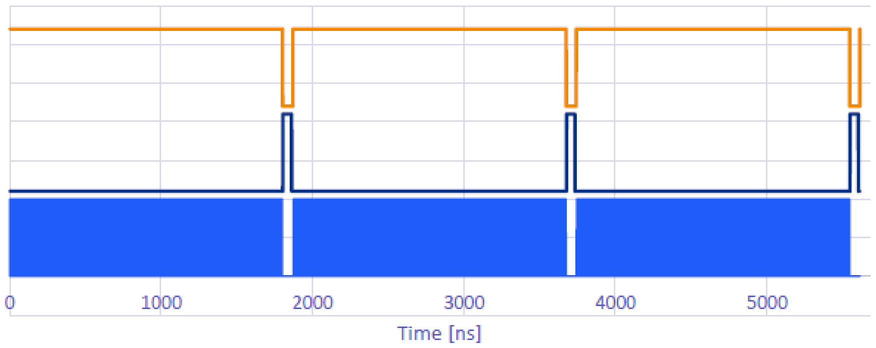
Common "pixel" requirements

- Pixel size: 100 µm
- Conceived for high-Z sensors → Cd(Zn)Te
- High dynamic range:
  - Single photon sensitivity
  - Up to ~ 10^9 photons/s/pixel (or above if possible)
- Operation with "continuous" and "pulsed" beams
- Nearly 100% duty-cycle operation should be possible

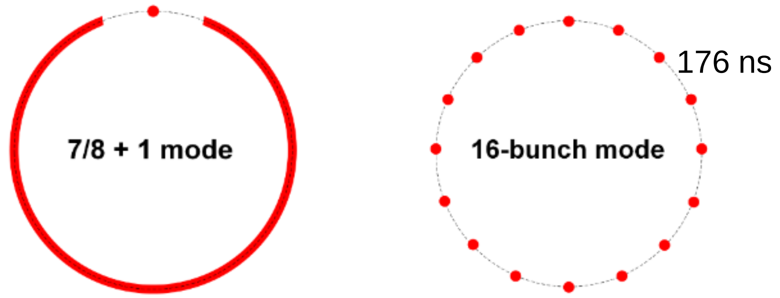
Focus on XIDER architecture

Similar considerations for DynamiX

Example of Diamond II fill pattern



Example of ESRF-EBS fill patterns



Continuous mode (high flux)

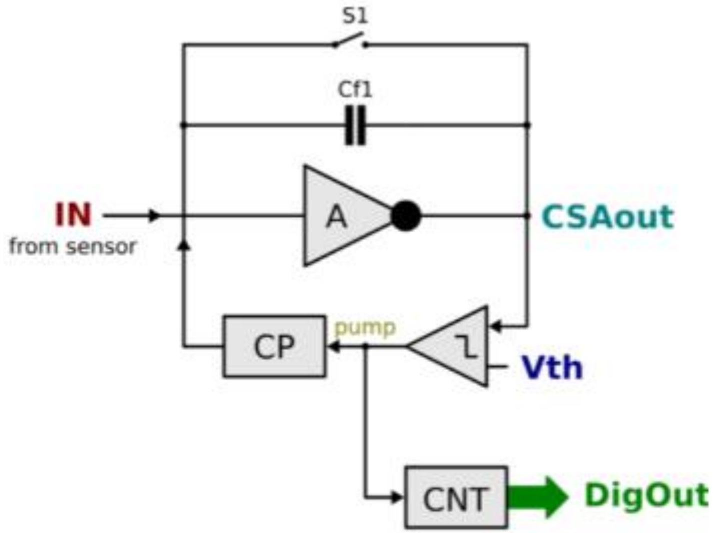
Pulsed mode (time resolved)

Readout Concept

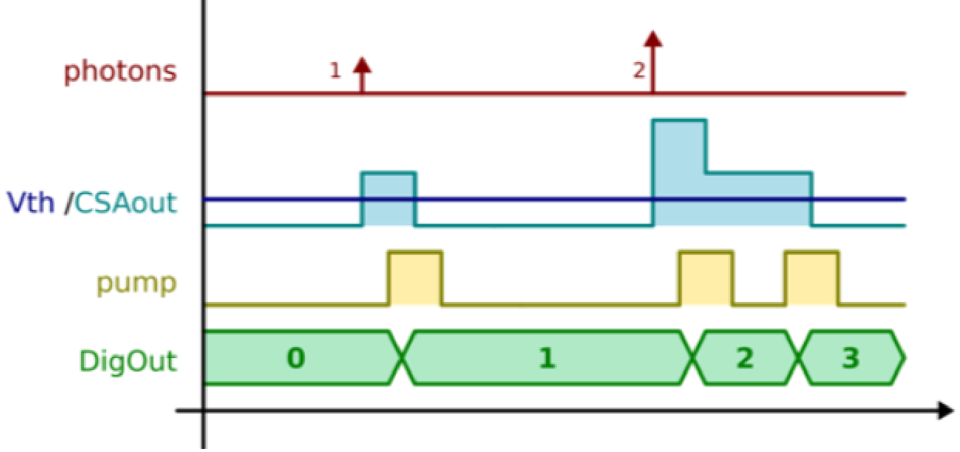
Continuous conversion front-end with one stage

- Charge-sensitive amplifier (CSA) collects charge
- Charge pump removes well-defined charge packets (eq. to n photons) from the input node
  - Single photon sensitivity
  - Infinite dynamic range (ultimately limited by counter depth)
  - Pumping must be fast enough to handle the photon rate
  - Mostly insensitive to CSA saturation
- Data output is digital

Schematics



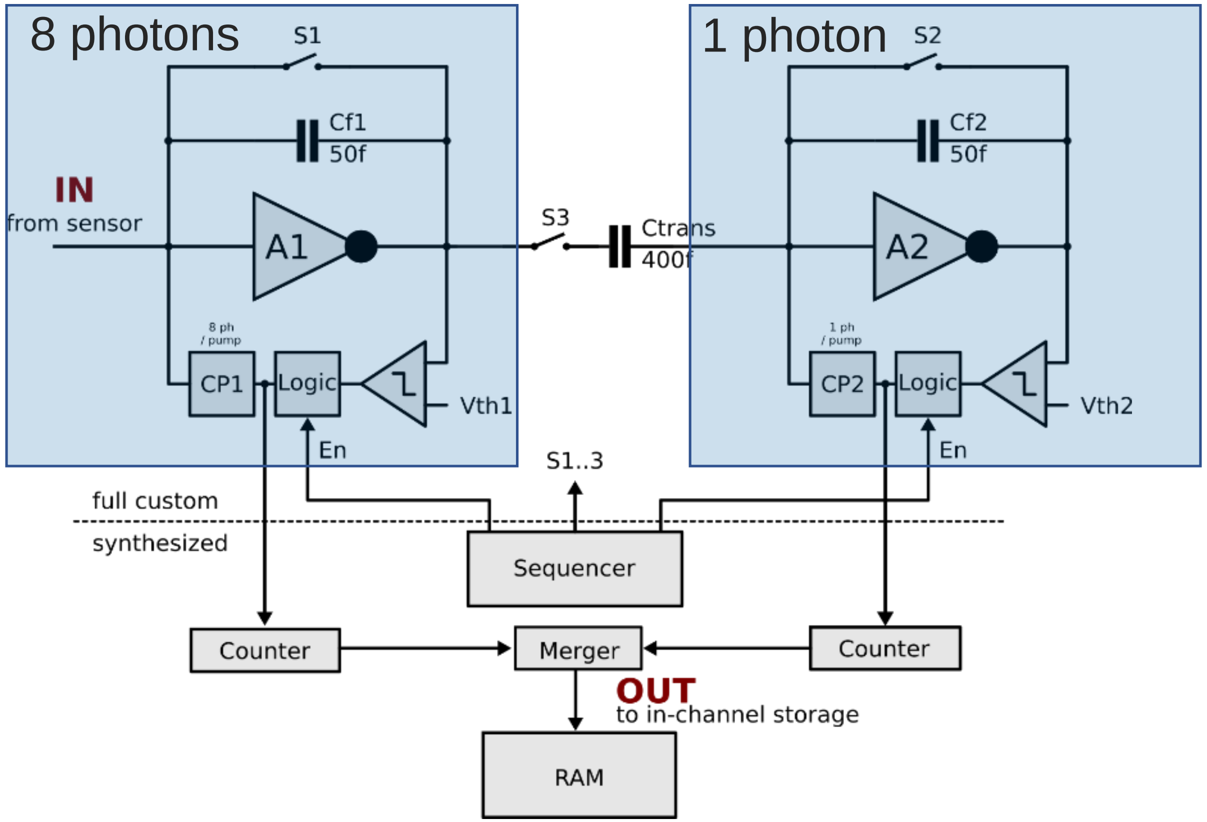
Signal sequence

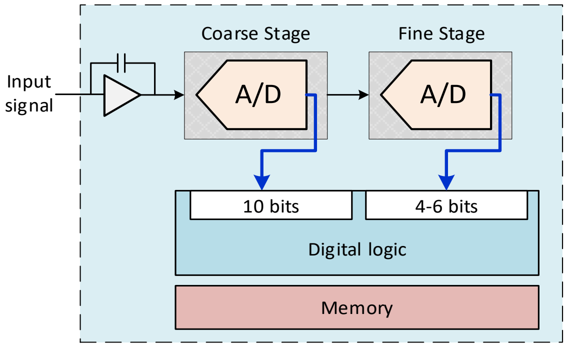


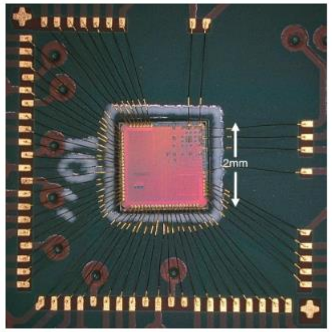
Readout Concept

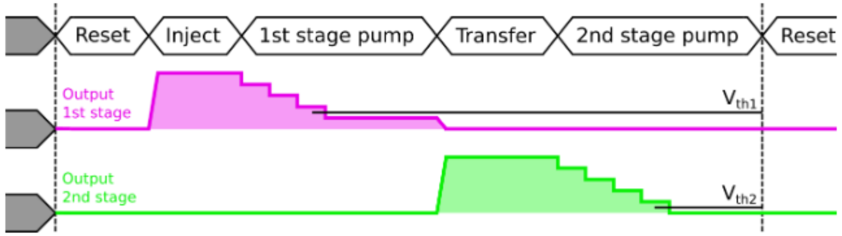
Continuous conversion front-end with two stages (pipeline)

- First stage (coarse) → high dynamic range
- Second stage (fine) → single photon (or sub-photon) resolution
- Transfer stage in between





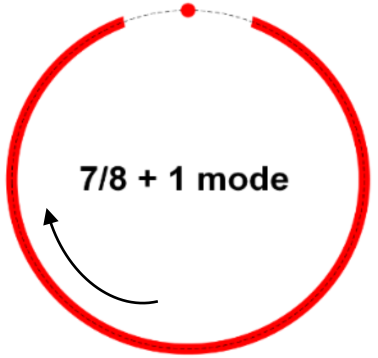




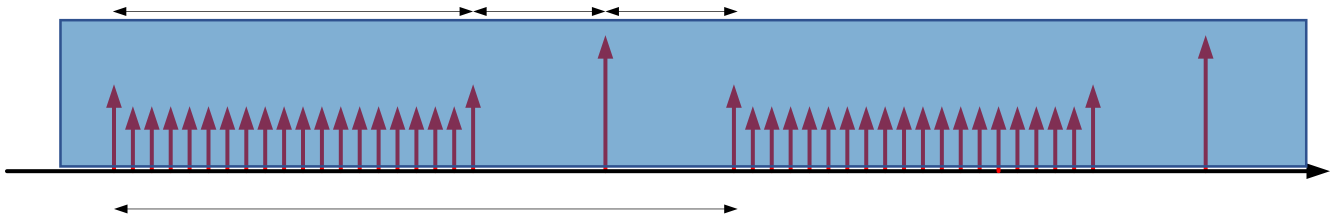
Readout implementation discussed in: *J. Inst.* **16** P03023
https://doi.org/10.1088/1748-0221/16/03/P03023

Flexible front-end

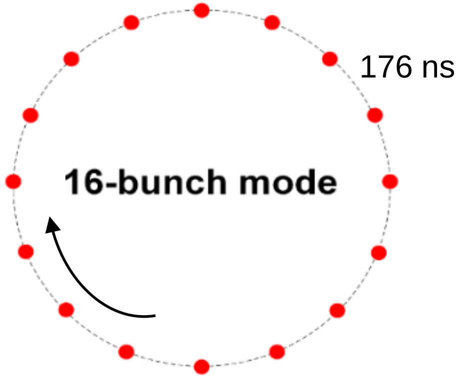
Continuous mode
(high flux)



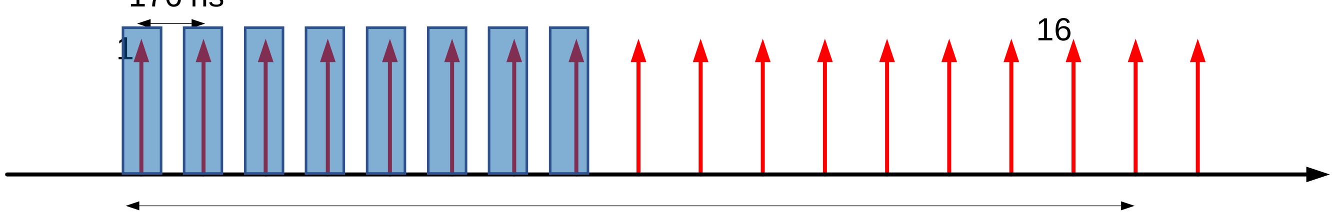
Filling Mode: 7/8 + 1



Pulsed mode
(time resolved)



Filling Mode: 16 bunch

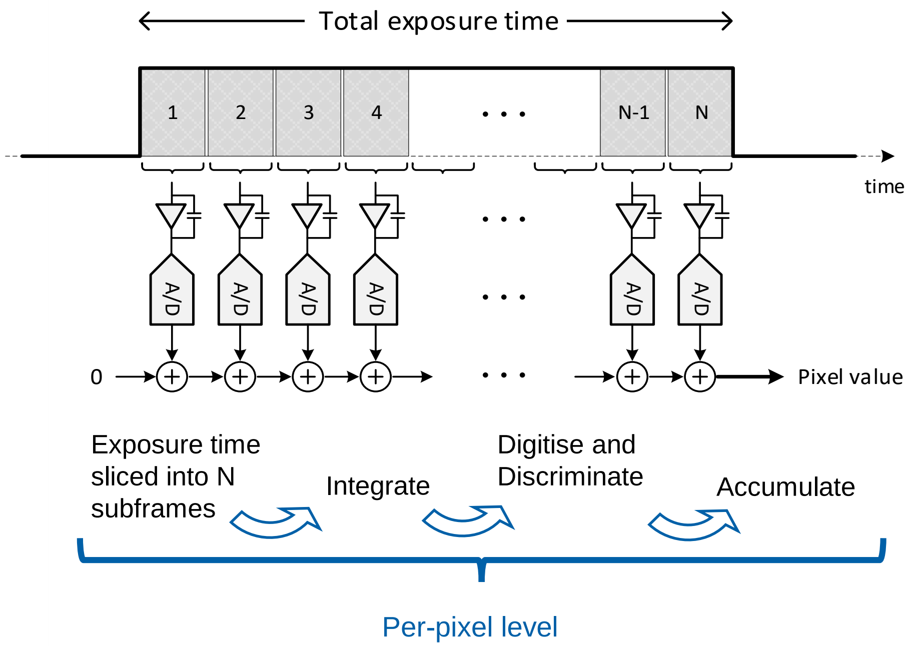


5.7 MHz

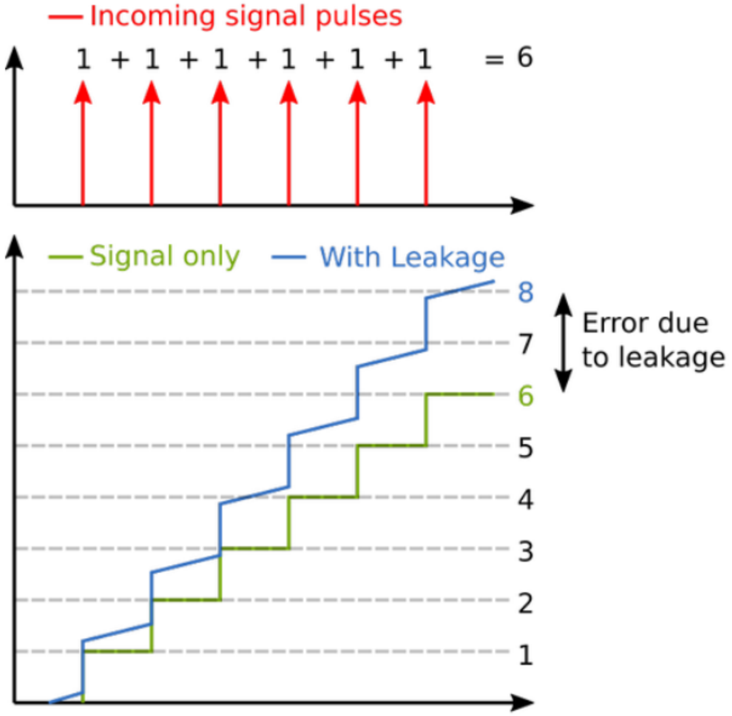
Flexible front-end to cope with both modes

Continuous illumination

Incremental digital integration concept

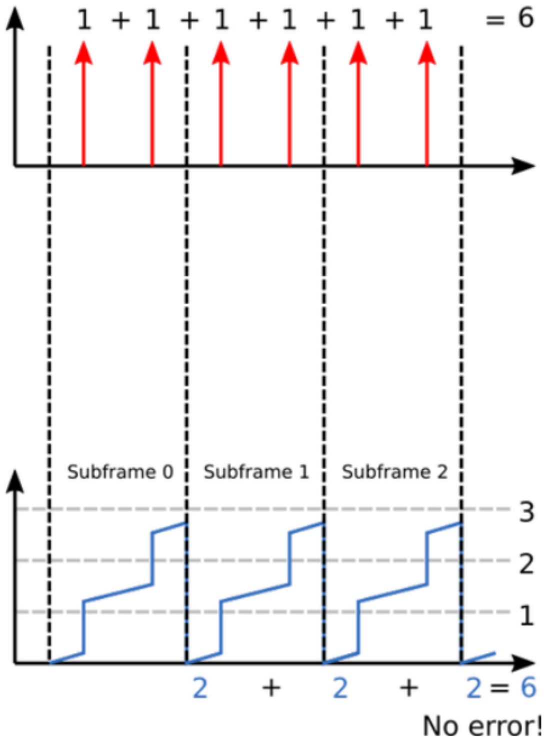


Incremental digital integration discussed in: *J. Inst.* **15** C01040
https://doi.org/10.1088/1748-0221/15/01/C01040



Standard integration

- Leakage accumulated



Digital Integration

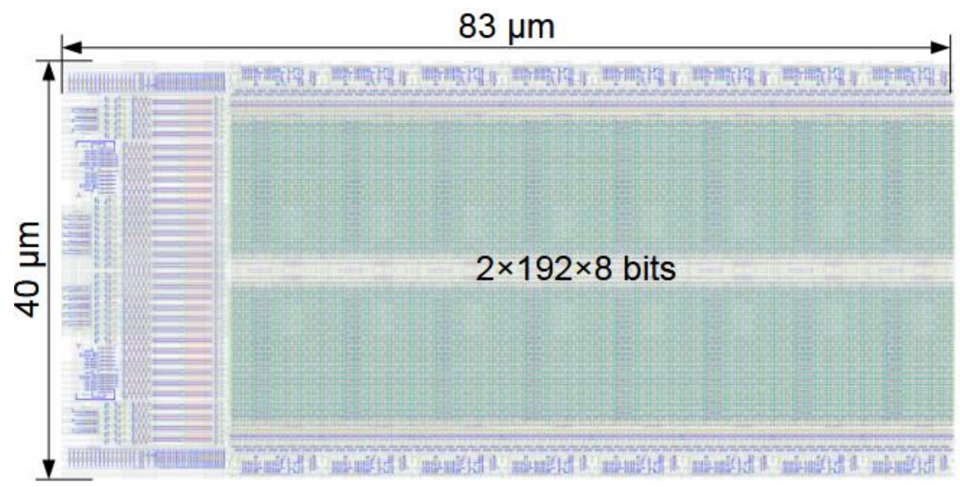
- Integration
- Digitization
- Accumulation

Pulsed illumination

Features

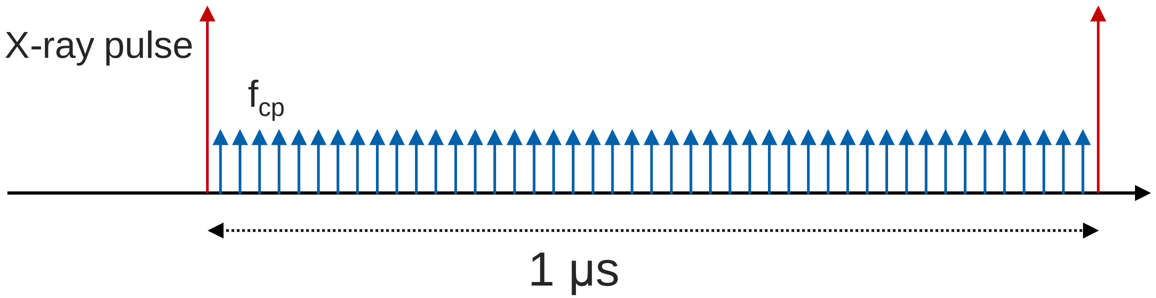
- Fast front-end (rise time ~10-20 ns)
- 192×16 bit RAM storage per pixel
- Dynamic range limited by charge pump frequency
- Major limitation: reset and transfer time

Full-custom RAM design



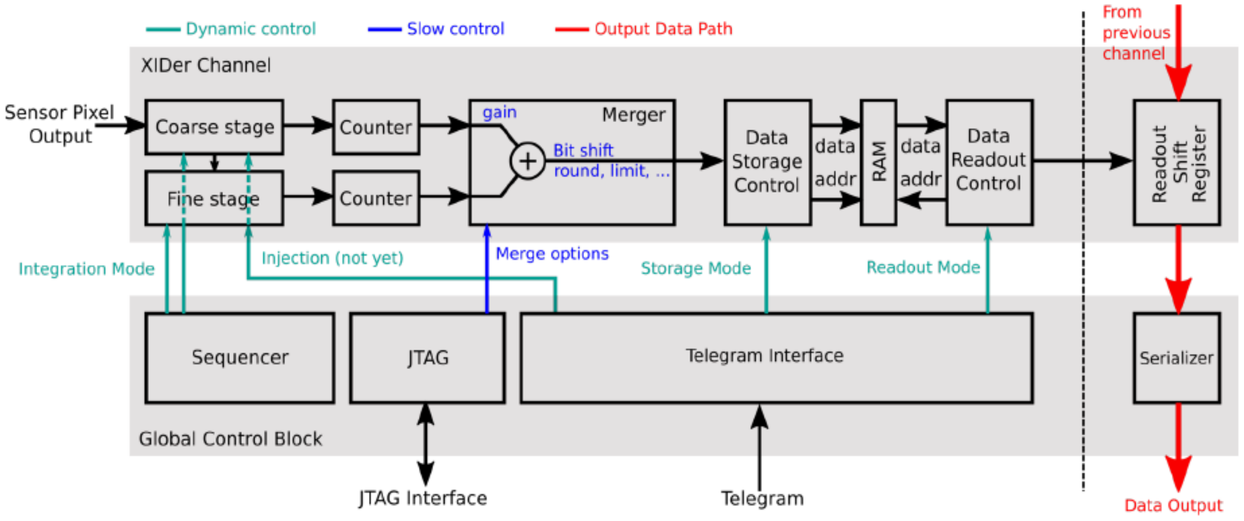
Example for XFEL

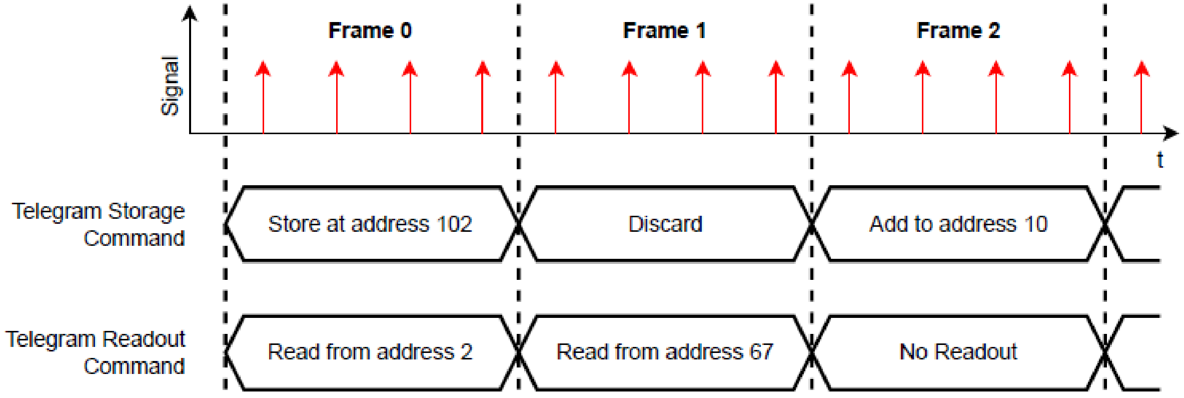
- f_{burst}: 1 MHz
- f_{cp}: 200 MHz
- N_{ph}: 8 ph
- DR: 8×200MHz/1 MHz ~ 1600 ph



Dynamic range can be easily adapted with bigger packet size

On chip data handling



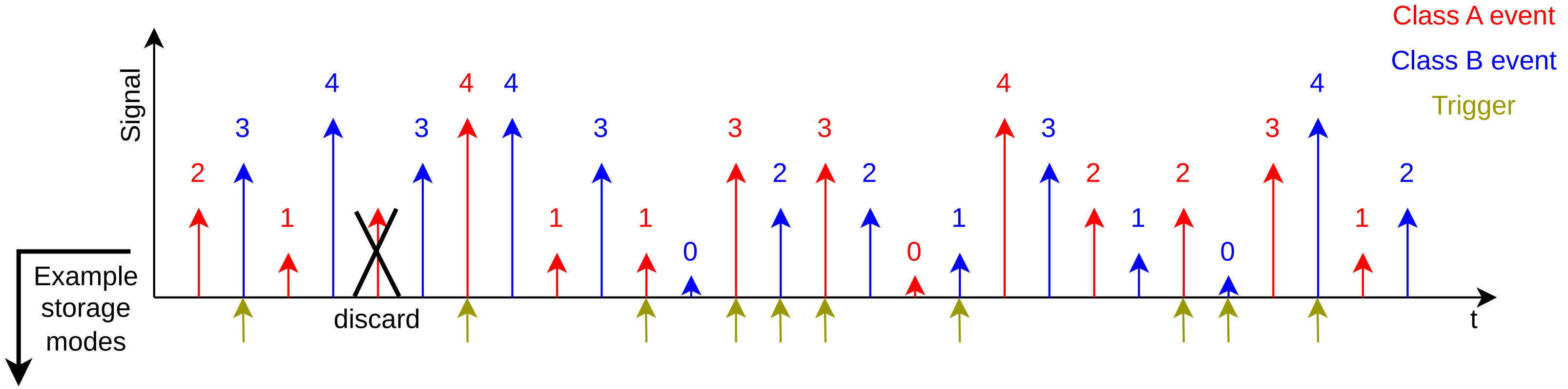


Telegram concept discussed in "*Concepts for the Data Flow Control on the XIDer Readout ASIC*" D. Schimansky, conference record ULITIMA 2022, under publication

Custom-designed telegram protocol

- Maximum flexibility in data taking
- Sends commands to the ASIC channels on frame-level for data storage and readout
- Allows for event-by event decisions, like triggering or data rejection.

Telegram protocol storage mode examples



RAM Address	Consecutive	Accumulated & consecutive	Histogram	Classified histogram	Triggered & consecutive
...	...	...	...	...	...
9	1	3+2=5	0	3	4
8	3	1+4=5	0	4	0
7	1	2+0=2	0	3	2
6	4	2+3=5	0	2	1
5	4	0+3=3	0	2	3
4	3	3+1=4	5	2	2
3	4	4+1=5	7	3	3
2	1	3+4=7	6	3	1
1	3	1+4=5	6	4	4
0	2	2+3=5	3	1	3

- There are many more modes
- Actual choice depends on the user's requirements

Outline

1. Introduction

- Motivation
- DynamiX and XIDER projects
- XIDyn collaboration

2. Front-end architecture

- Readout concept
- Continuous and pulsed illumination
- Data handling and telegram protocol

3. Experimental results

- Prototypes and characterisation
- High-flux CZT

4. XIDyn collaboration

- Common MPW design
- Scale-up plans

Prototypes

2018
T1
T2
T3
T4
T5
XIDER

2022
T6
T7
XIDyn

ASIC design

The XIDER pixel functionality is particularly **complex**

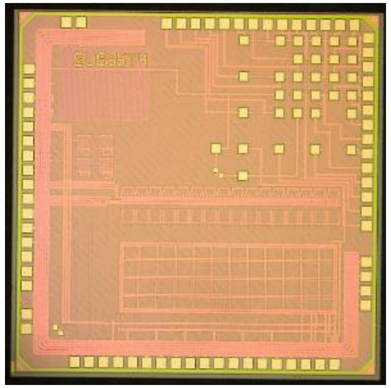
- ✓ Fast analog front-end
- ✓ In-pixel analog-to-digital conversion
- ✓ Digital logic, sequencer, multiple modes of operation
- ✓ Built-in memory
- × Power hungry

The pixel design has **progressed incrementally**

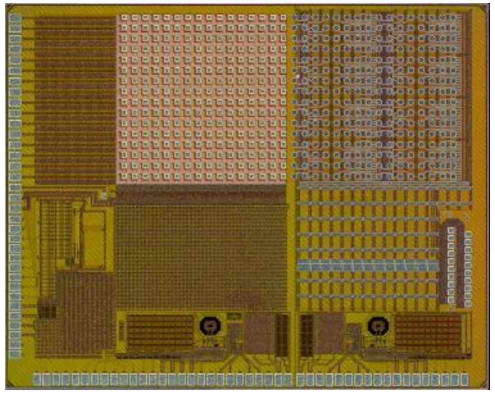
- Six chips (T1 to T6) designed so far
- Not all the chips have used for X-ray testing
- Last X-ray measurements with T4: investigation at the pixel level
- T7 is planned

More info on T6&T7 in the last section

ASIC T4: 4×4 pixels



ASIC T6: 16×16 pixels



TSMC CMOS 65nm

Prototypes

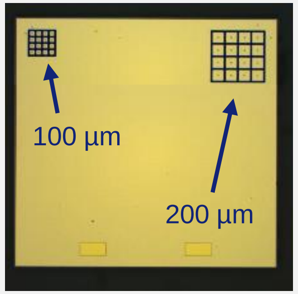
Prototypes T4

- CdTe-ohmic (Acrorad) or CZT (Due2Lab & Redlen)
  - 1 mm thick CdTe (ohmic contacts)
  - 2 mm thick high-flux CZT
- 4×4 matrices of 100 or 200 µm pitch
- TSMC CMOS 65nm technology (version T4)
- Interconnection by Polymer Assembly Technology

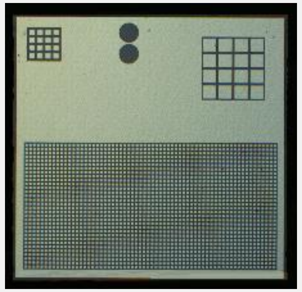
Characterization

- The initial investigation work was done with CdTe assemblies
- CdTe devices perform poorly
  - Instability and irreproducibility of dark/leakage current
- High-flux CZT assemblies available only very recently
- Measurements taken both with 30 keV X-rays at BM05/ESRF and with LED sources at the lab

Cd(Zn)Te sensors

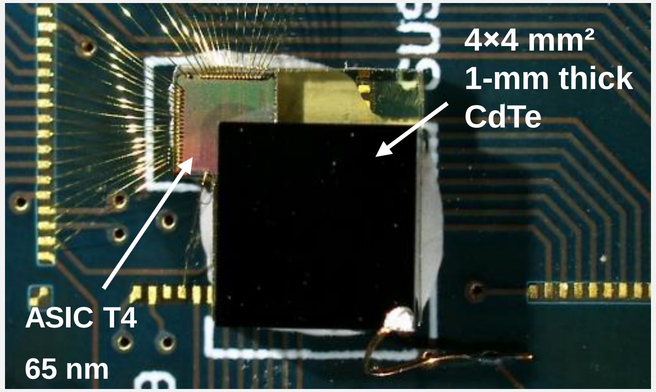


CdTe
(Acrorad)



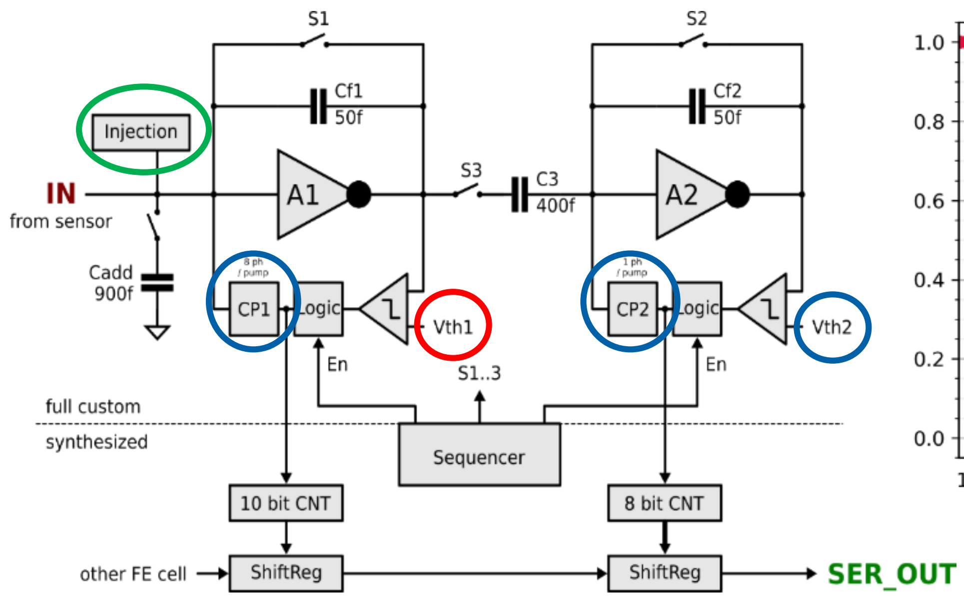
High-flux CZT
(Redlen / Due2lab)

Sensor-ASIC prototype

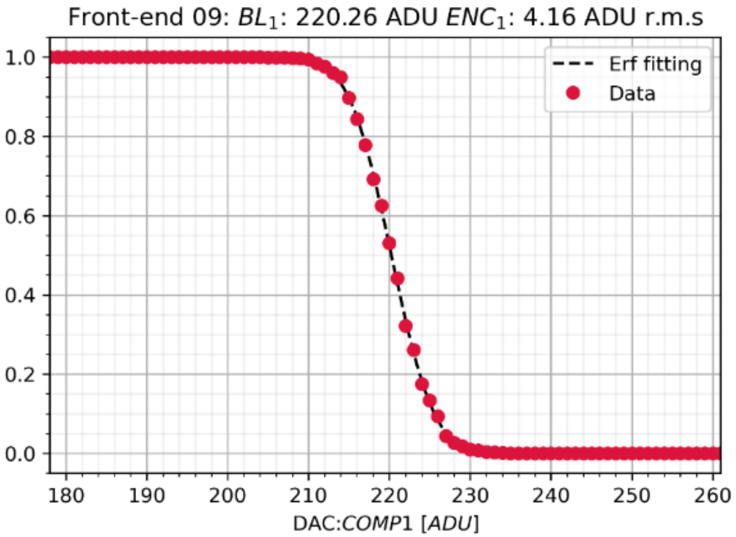


Calibration

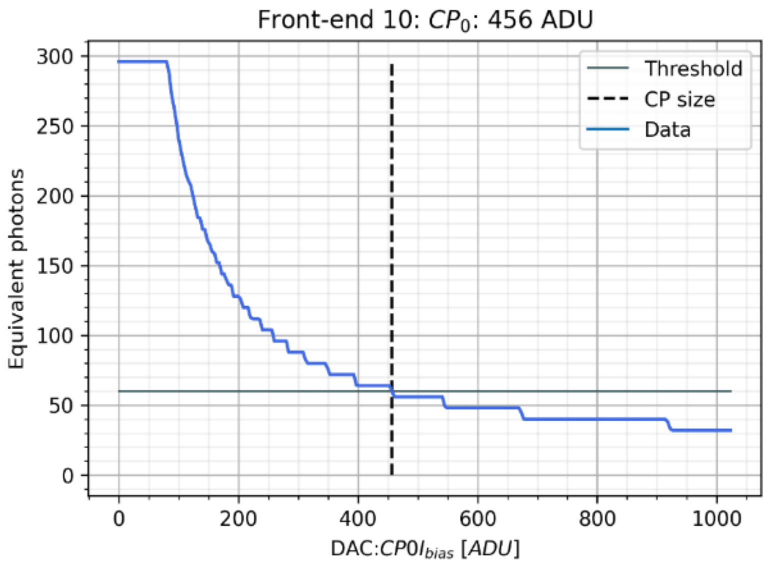
Parameters to be calibrated



Threshold calibration



Charge packet calibration

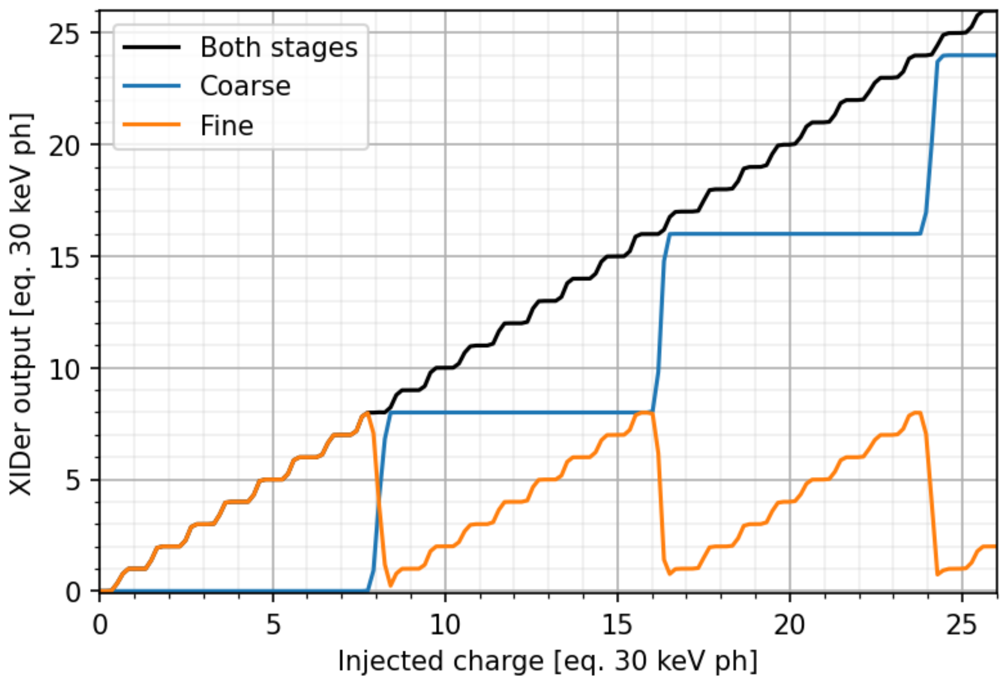


Parameters to be calibrated

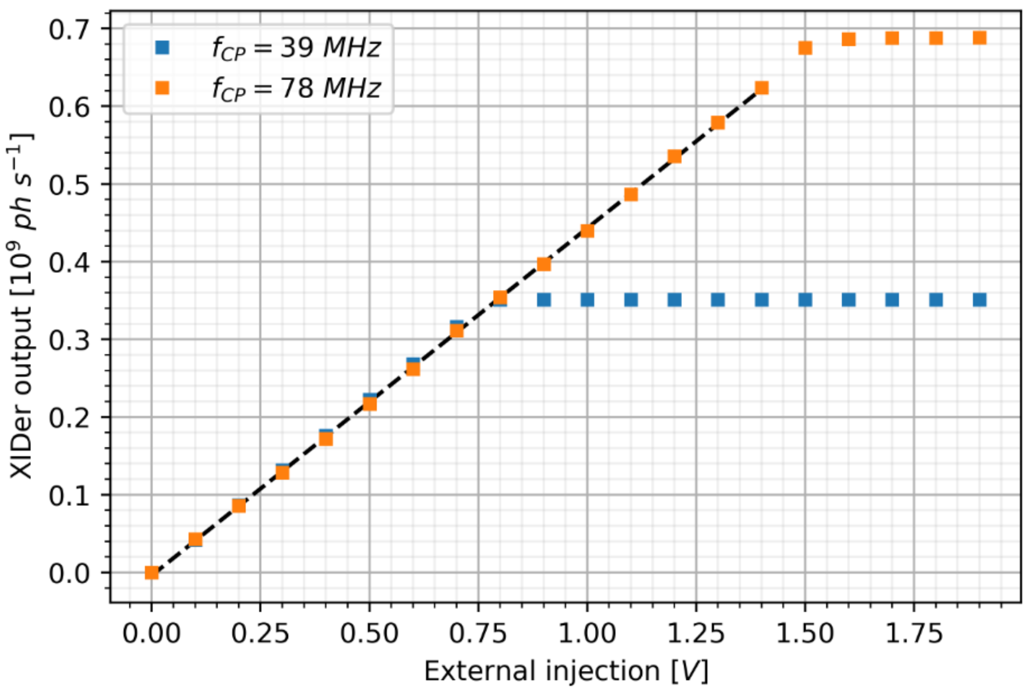
- Thresholds and charge pumps (×2)
- All trimmable with 10-bit DACs
- Using internal (or external) charge injection

Characterisation

Example of calibrated channel



Dynamic range vs charge pump frequency

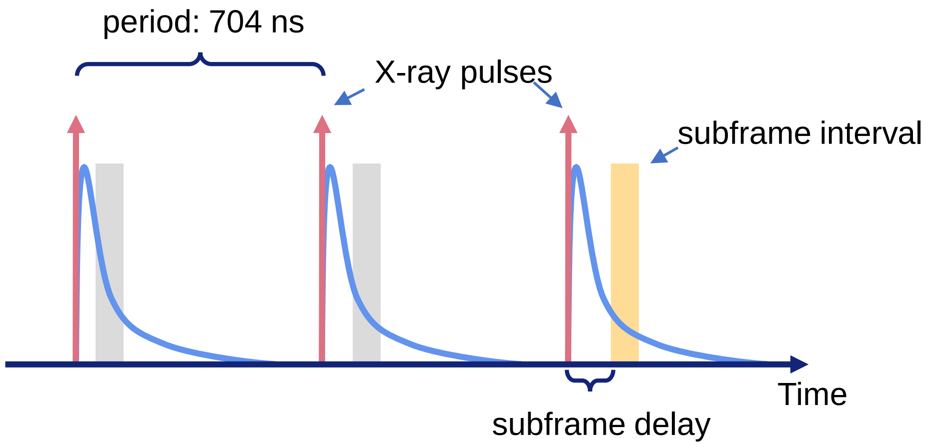


- Internal injection circuit
- Coarse stage counts in packet of 8 photons
- Fine stage in packets of 1 photon
- Mid-tread response
- Electronic noise: 350 e^- rms

- External injection circuit
- Dynamic range can be extended with charge pump frequency
- Dynamic range already approaching 0.7×10^9 ph/s/pixel

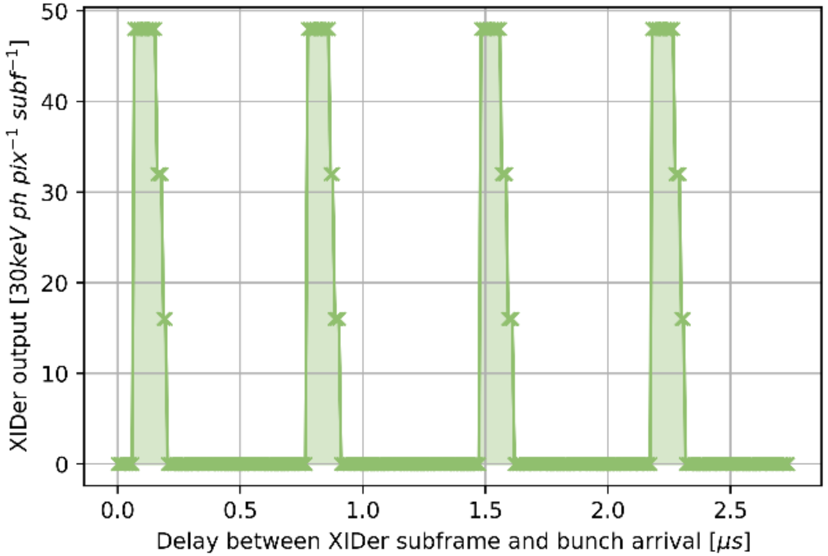
Time-resolved capabilities

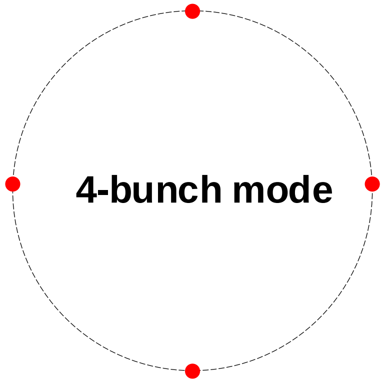
Concept



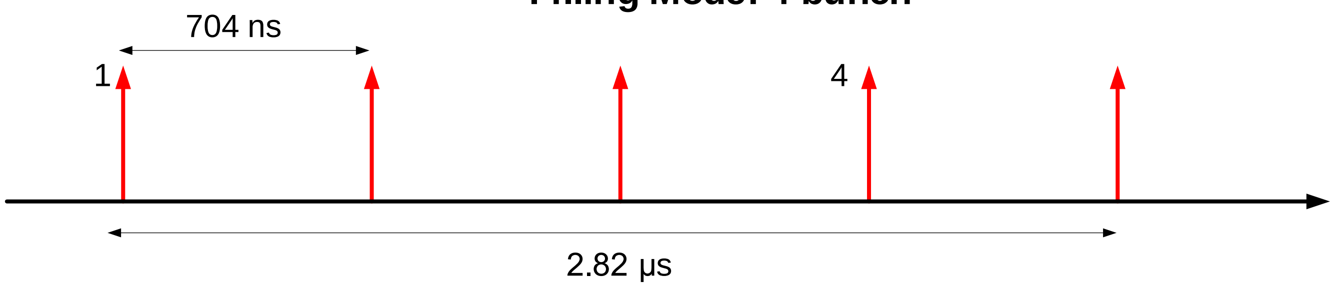
- XIDER active subframe of ~100 ns
- 4-bunch filling mode: 100 ps X-ray pulses every 704 ns
- Photon induced signal

Example of 4-bunch full orbit scan



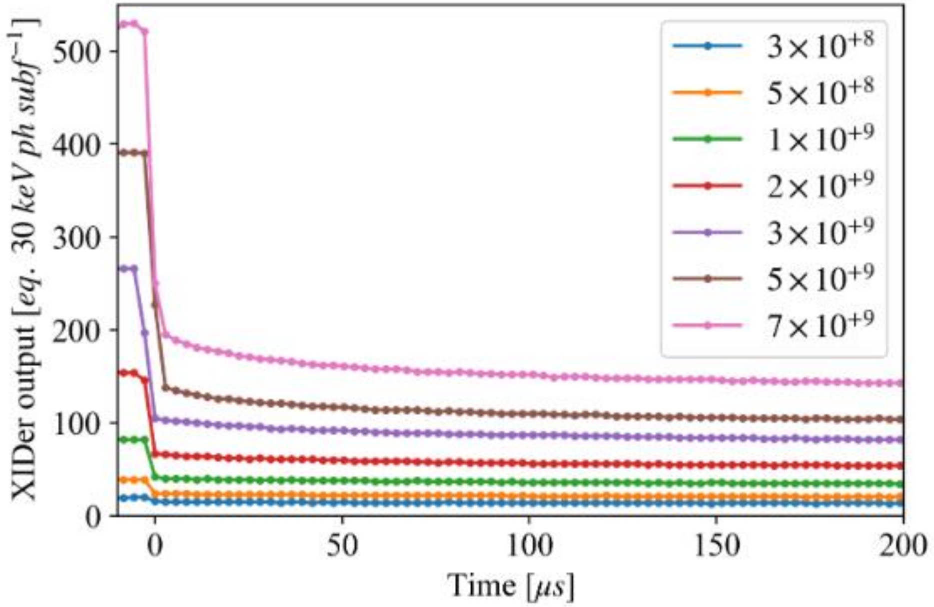


Filling Mode: 4 bunch

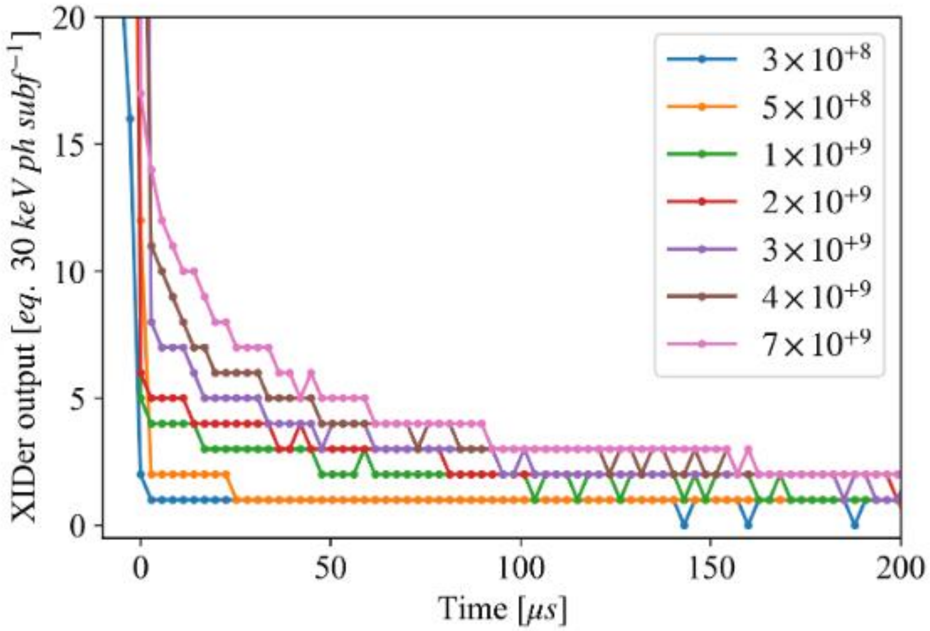


High-flux CZT

XIDER T4 - CdTe sample



XIDER T4 – HF-CZT sample



* Fluxes in ph/s/px

Afterglow/aftersignal

- Extra-charge delivered by the sensor after end of irradiation
  - CdTe performs much worse than CZT
  - Residual still present in HF-CZT
- For XFEL pulsed operation → effect mitigated

High-flux CZT

“High-flux” CZT

- Better charge transport properties than CdTe
- High-flux version improves hole transport properties

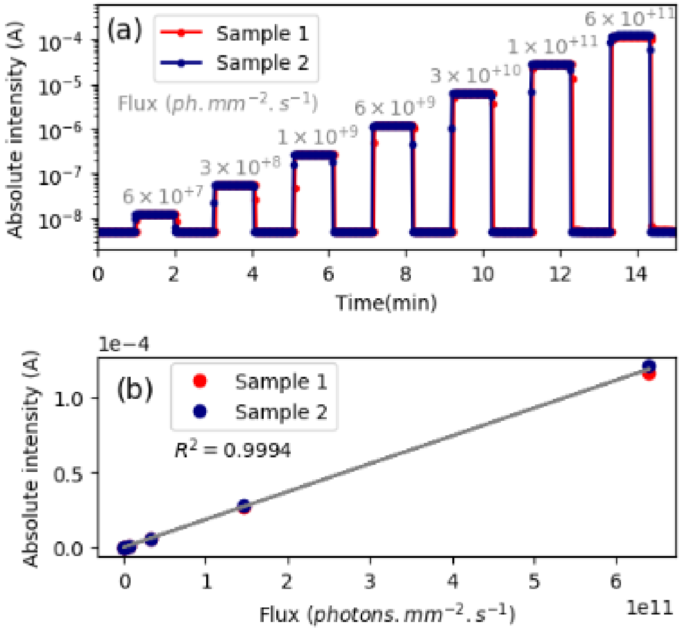
Redlen Technologies

- Redlen does not supply prototypes, slowly opening to the synchrotron market
- Their sensor processing technology (e.g. pixelation) is still somewhat “rudimentary”

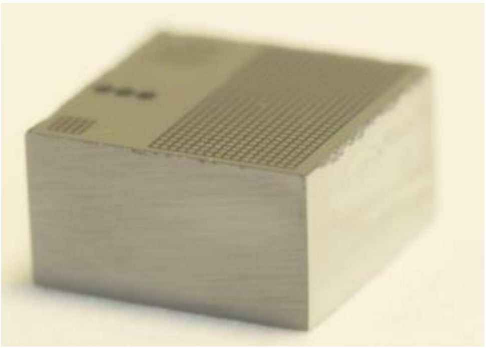
Collaborating with IMEM-CNR-Due2Lab (Parma):

- IMEM reprocesses “high-flux” CZT sensors from Redlen
- Developed a suitable platinum contact technology
    - First devices by the end of 2022 with very promising results:
    - Low leakage current (significantly lower than CdTe)
    - In terms of time stability (reduced polarization effects)
    - Good linearity up to high X-ray flux densities

HF-CZT linearity



Linearity up to
6×10^{9} 20 keV ph / sec / 100µm pixel



Outline

1. Introduction

- Motivation
- DynamiX and XIDER projects
- XIDyn collaboration

2. Front-end architecture

- Readout concept
- Continuous and pulsed illumination
- Data handling and telegram protocol

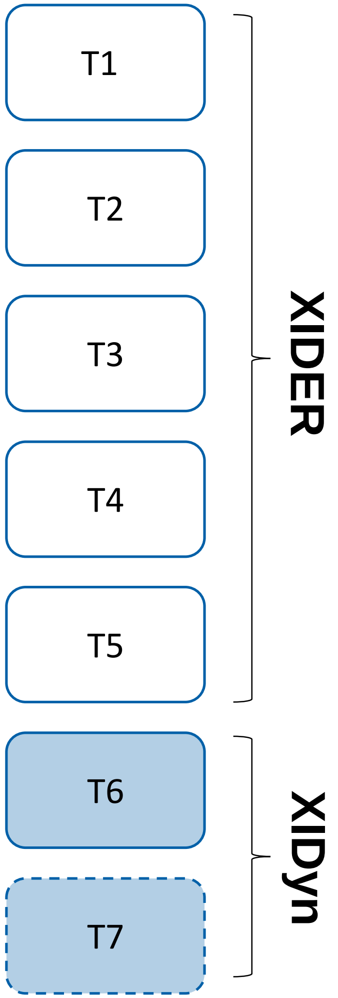
3. Experimental results

- Prototypes and characterisation
- High-flux CZT

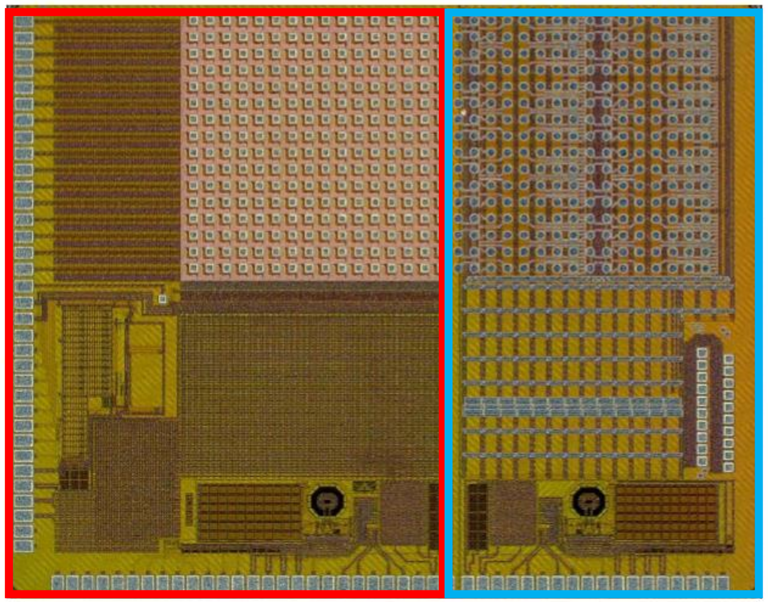
4. XIDyn collaboration

- Common MPW design
- Scale-up plans

Common MPW design



MWP ASIC: 2×16×16 pixels



DynamiX **XIDER T6 + STFC ser.**

MPW ASIC

- DynamiX: 16×16 pixel
- XIDER: 16×16 + STFC serialiser
- 14 Gbps high-speed data serializers
- Pitch is continuous (110 µm)
- One piece of CZT over the device

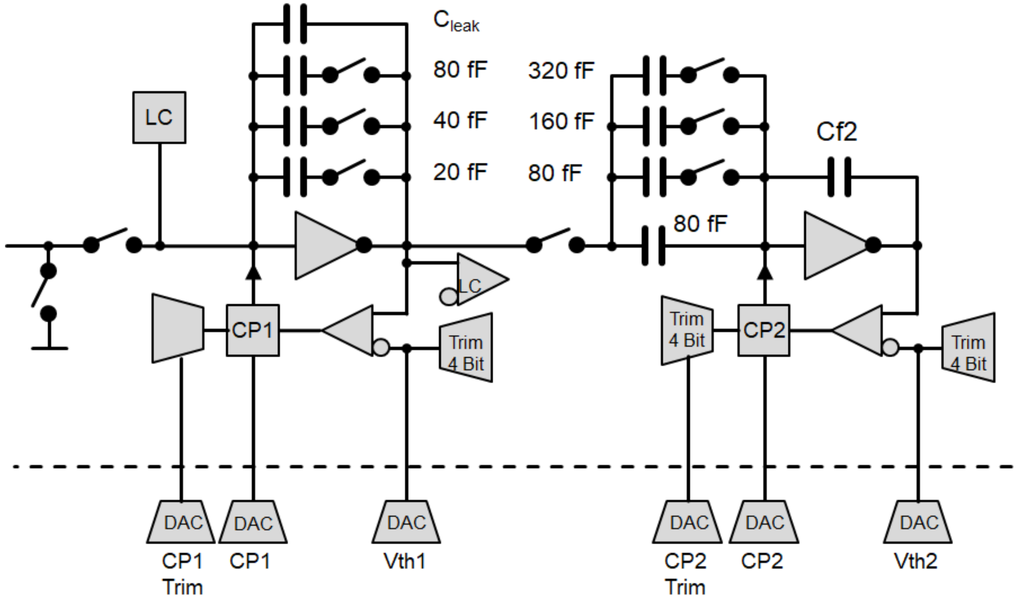
Chip is alive

New ASIC/sensor prototypes under assembly

Full reticle scale-up plans

- "**STFC Detector Hub**" funding scale up to **full reticle** over next 18 months
- **Merging design:** add adjustable gains/cancellations to match ESRF and Diamond needs
- Performance optimisation
  - Power, timing distribution
- Aim for **adjustable number of serialisers**. For example
  - 8 for high rate → 100kHz readout $$$
  - 1 for low rate → 10kHz readout $
- Use RAM to sum and keep flux capability or sum sequence of frames, rolling buffer, veto, compare…
- Interested in other collaborators, requirements… this version and future ones

Possible merged XIDyn design

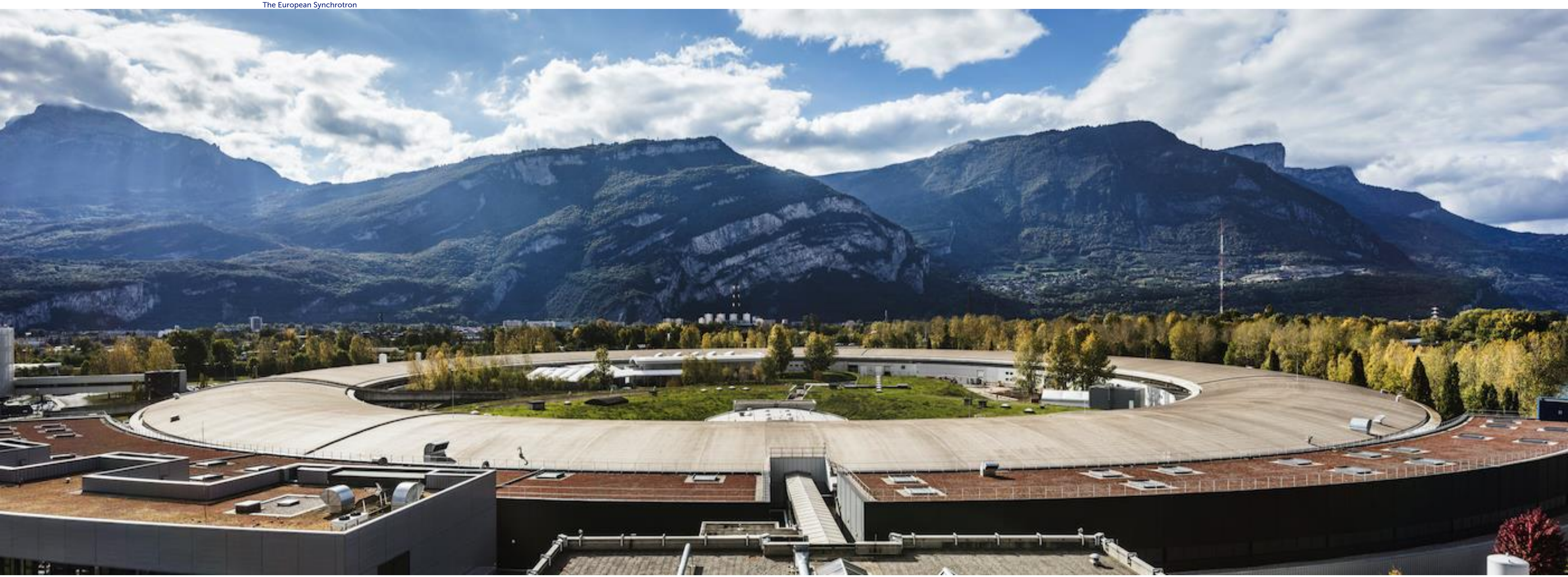


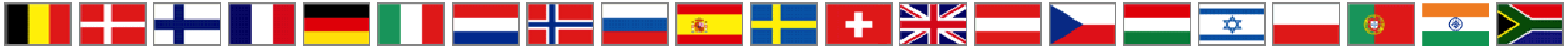
ESRF The European Synchrotron

UNIVERSITÄT HEIDELBERG ZUKUNFT SEIT 1386

diamond

UKRI Science and Technology Facilities Council





Thank you for your attention