Front-End Electronics and IP Blocks in 65 nm CMOS Technology for Pixel Detectors in X-ray Imaging Applications

Luigi Gaioni for the BG/PV group

Future Detectors for the European XFEL

18-19 Sept 2023

R&D activities in 65 nm CMOS technologies

Front-end Electronics for imaging applications

- PixFEL Project (INFN Pavia/Bergamo, Pisa, Trento): developing front-end electronics for diffraction imaging applications at FELs
- FALCON Project (UniBG, UniPV, ANL): development of a top tier detector for X-ray ptychography

IP Blocks in ASICs for High Energy Physics Applications

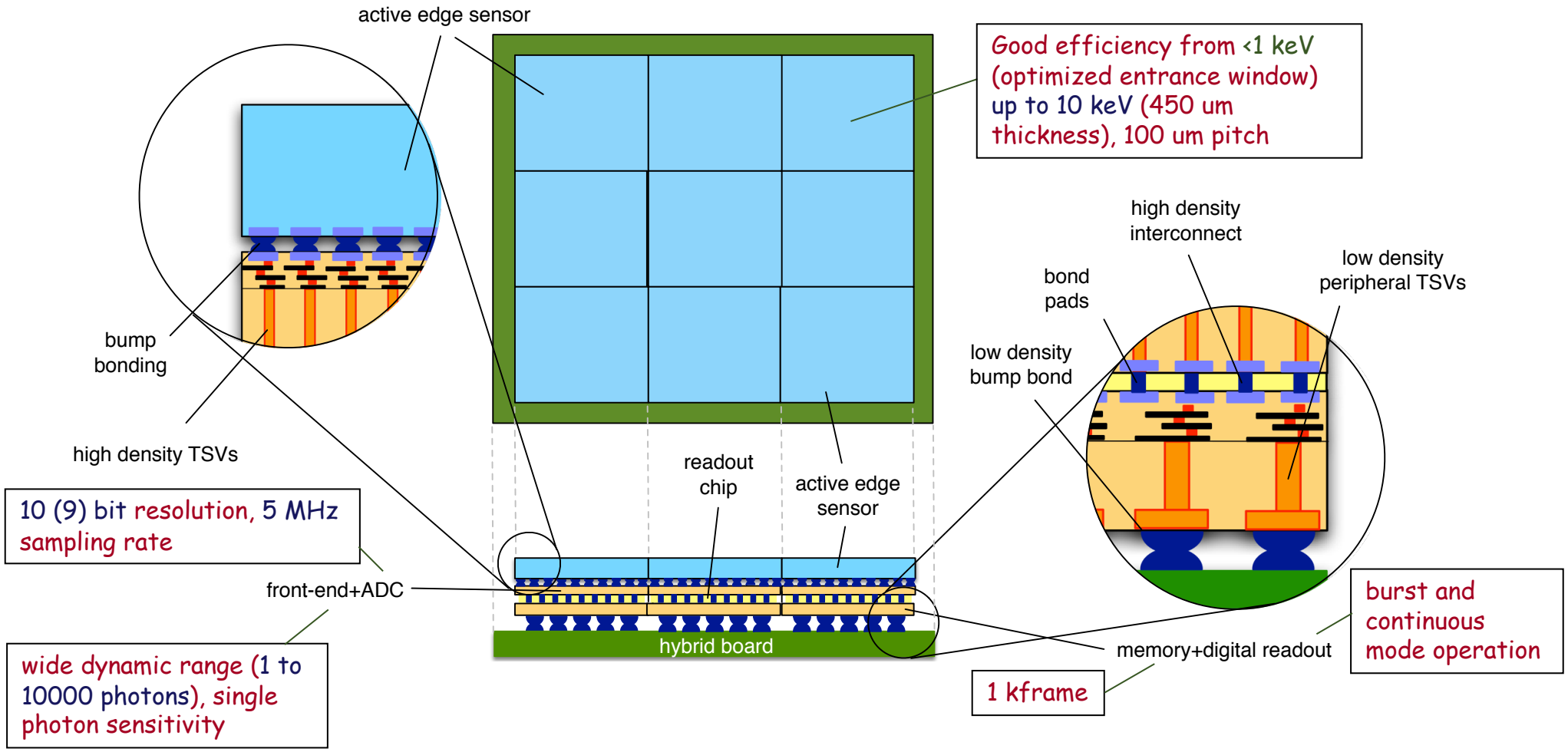
- CERN RD53 Collaboration
- Analog and M/S blocks

Research Groups

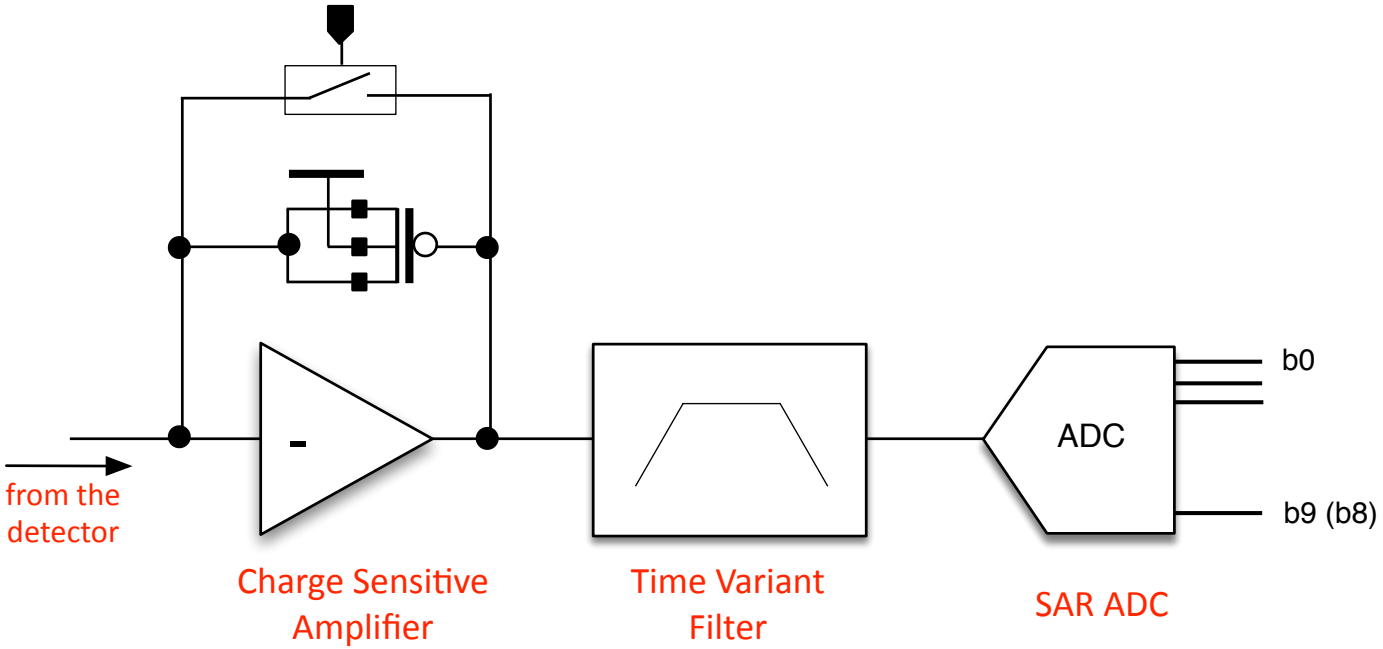
- University of Pavia: L. Ratti, G. Torilla, S. Giroletti, C. Vacchi, F. Shojaei
- University of Bergamo: V. Re, L. Gaioni, M. Manghisoni, G. Traversi, E. Riceputi, P. Lazzaroni, A. Galliani, L. Ghislotti

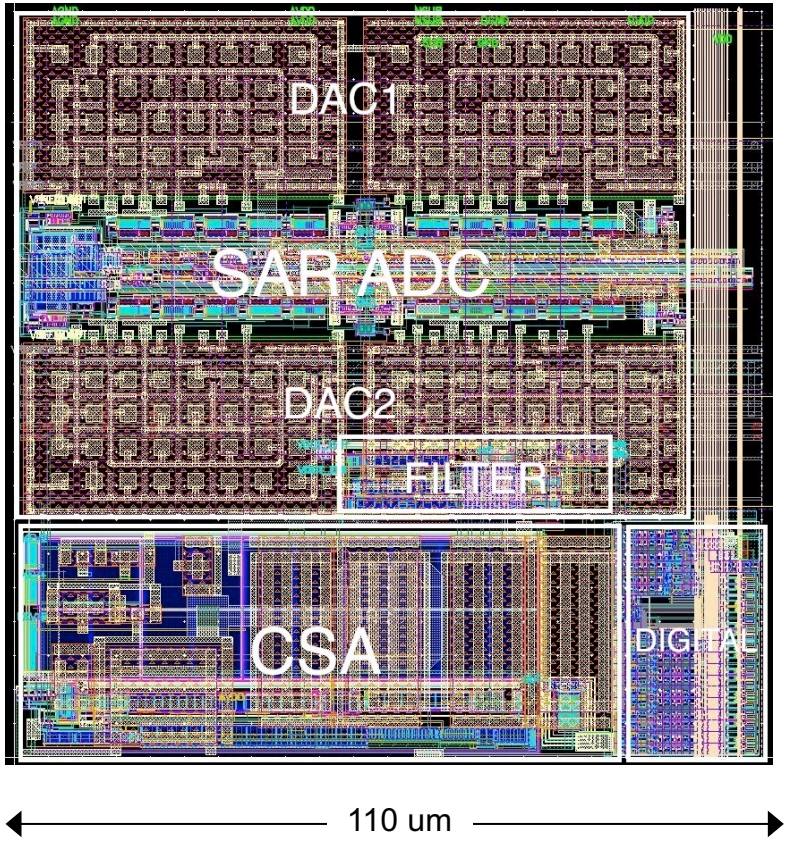
The PixFEL detector

Develop a four-side buttable, multi-layer module for the assembly of large area detectors with minimum dead area



Front-end Channel



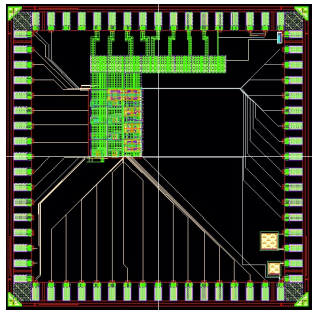


- Charge sensitive amplifier - dynamic signal compression and programmable gain
- Time variant filter – two different versions, transconductor+FCF and DGI
- Analog-to-digital conversion – 10/9 bit SAR ADC

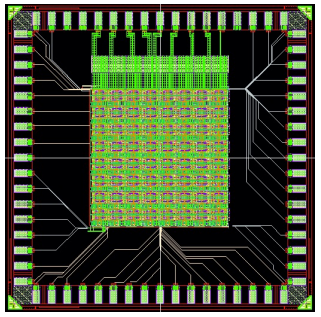
- 65 nm CMOS technology (1 poly 9 metal stack)
- Power dissipation: 230 uW/350 uW (depending on the filter solution)
- Cell area: 110 um x 110 um

Prototypes and test chips

PFT1

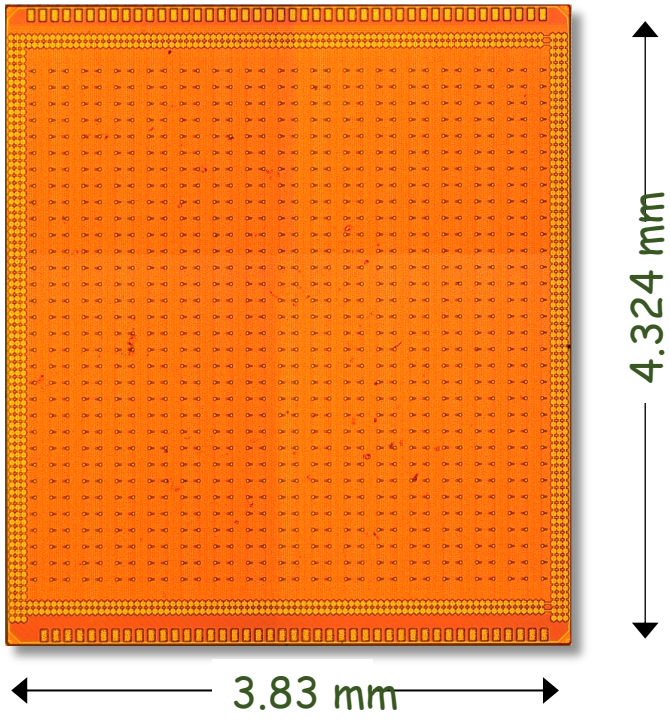


PFM1



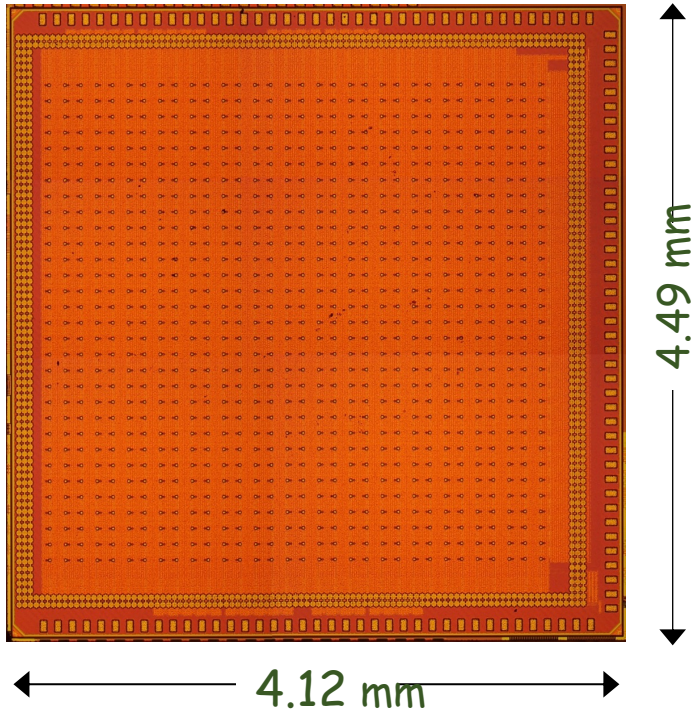
mini@sic chips,
~2 mm x 2 mm,
TSMC 65 nm technology

PFM2



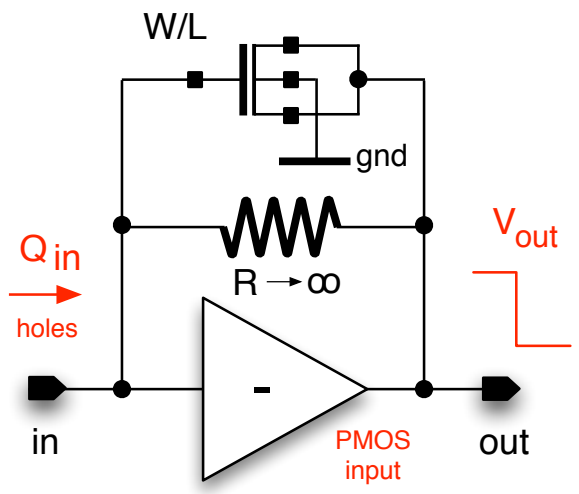
32x32, 110 um pitch channels
multi-project wafer (MPW) run
half array DGI-based, half FCF-based
10 bit with MIM capacitors in PFM2

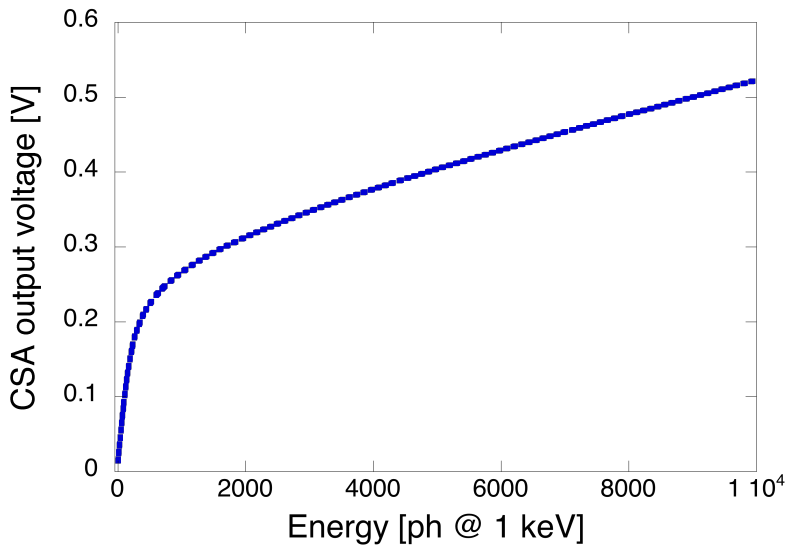
PFM3

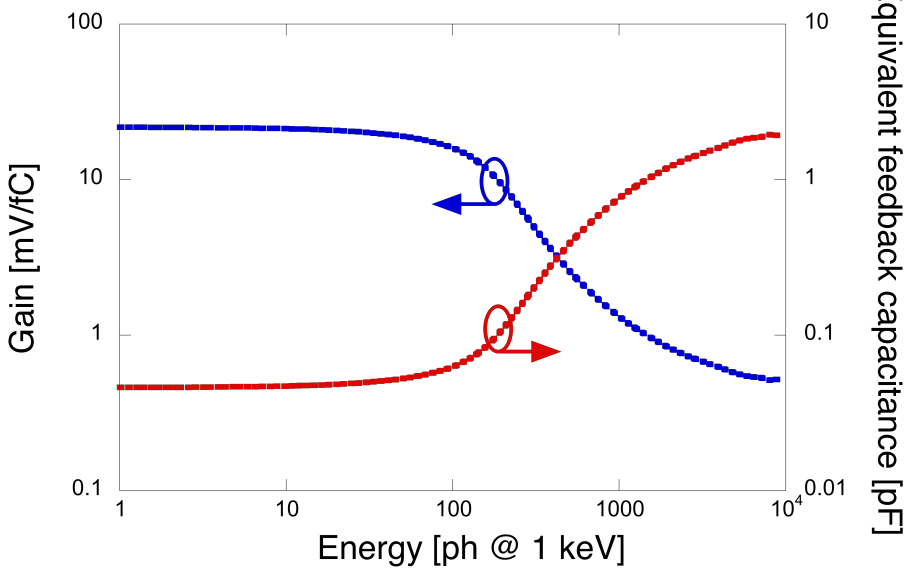


32x32, 110 um pitch channels
engineering run
DGI-based shaper only
1, 2, 3 keV gain configurations
9 bit SAR ADC with MOM capacitors
Designed for peripheral TSV implementation

CSA with dynamic signal compression



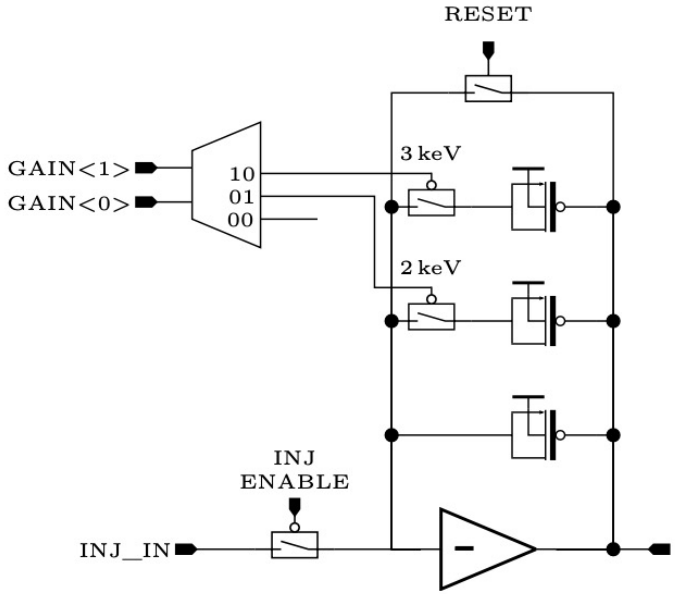




Based on the non-linear feature of a MOSFET operated in inversion mode

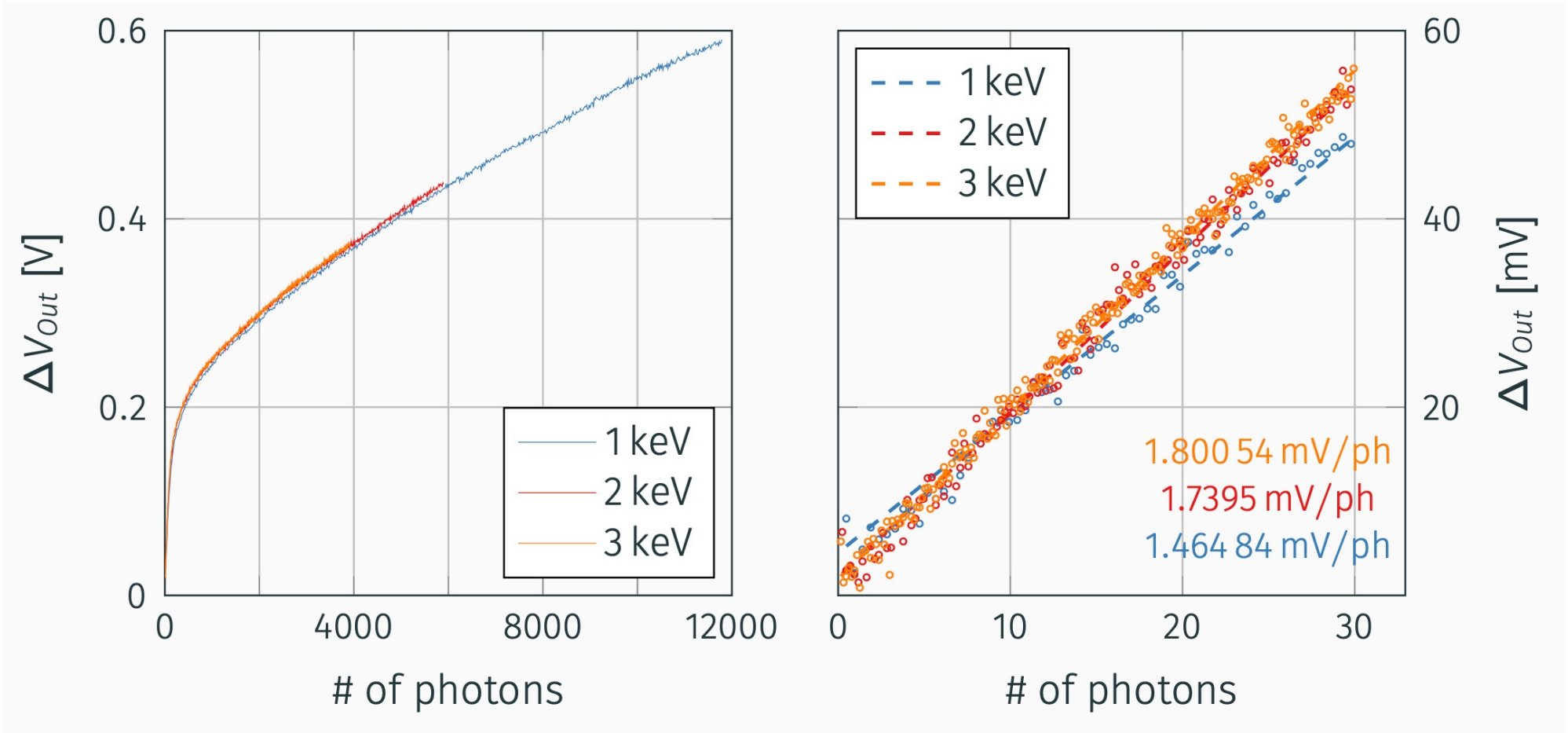
- $|\Delta v_{out}| \ll V_{Th}$ ➔ $C_f = C_{min}$, $Gain = G_{he}$
- $|\Delta v_{out}| \gg V_{Th}$ ➔ $C_f = C_{max}$, $Gain = G_{le}$

Appropriate choice of W and L to configure the gain in the low and high energy regime, under the constraint set by the preamplifier output range

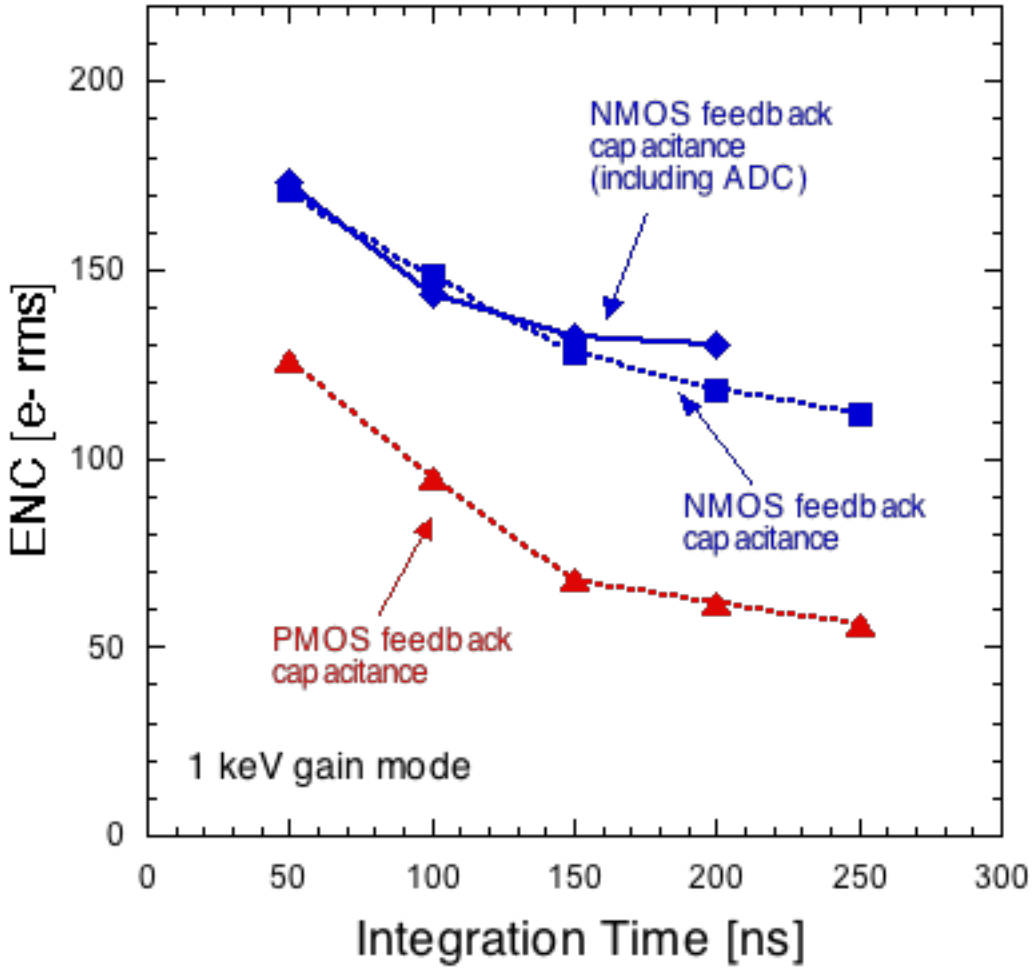


Gain Setting

Dynamic range



ENC measurements (channel V-to-I + FCF)

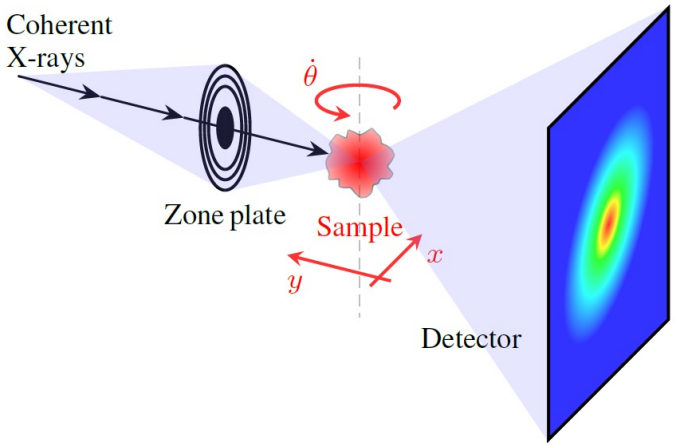


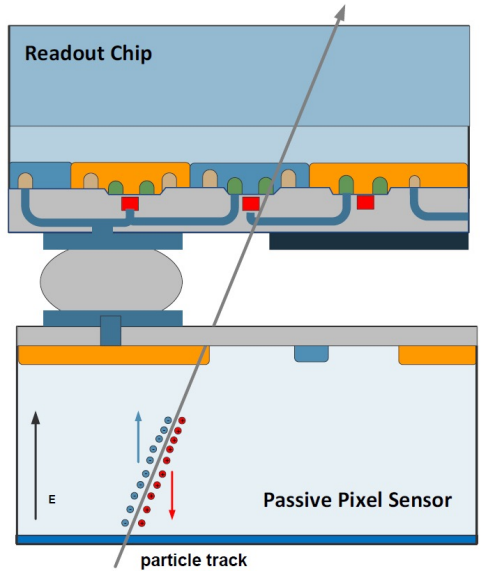
Larger ENC in the case of NMOS feedback capacitor

- larger stray capacitance at the preamplifier input
- the PMOS capacitance, being integrated in an N-well, is less sensitive to noise propagating through the substrate

FALCON Project for Ptychography applications

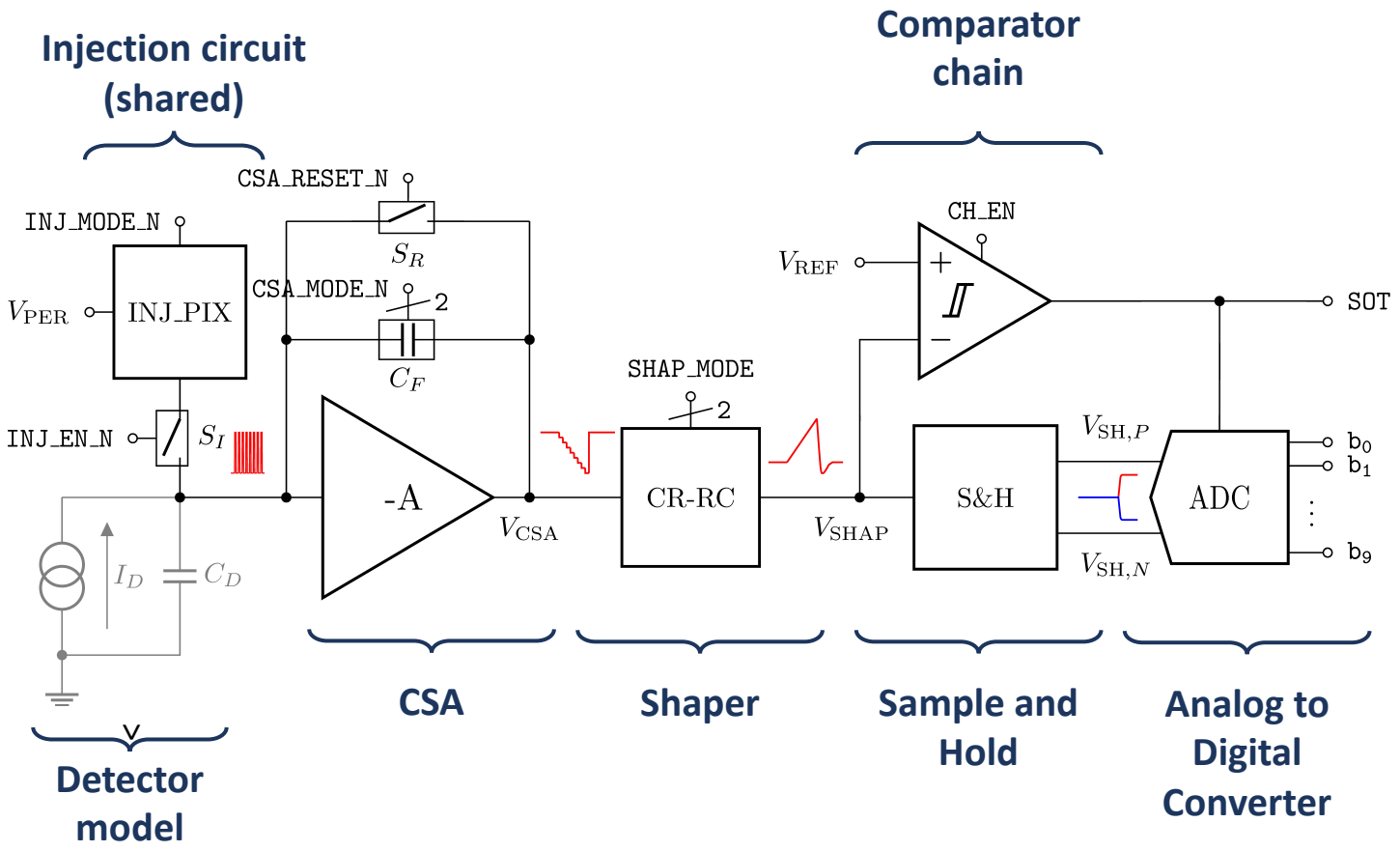
- **International collaboration** between ANL (Chicago, USA), UniBG and UniPV (Italy).
- Development of a **top tier detector for X-ray ptychography**.
- The **pixelated** detector will operate at frequency up to **1 MHz** and a **128-by-128 matrix** is envisioned.
- **Moderate dynamic range at the input**: 256 photons @ 5 keV, 9 keV, 25 keV.

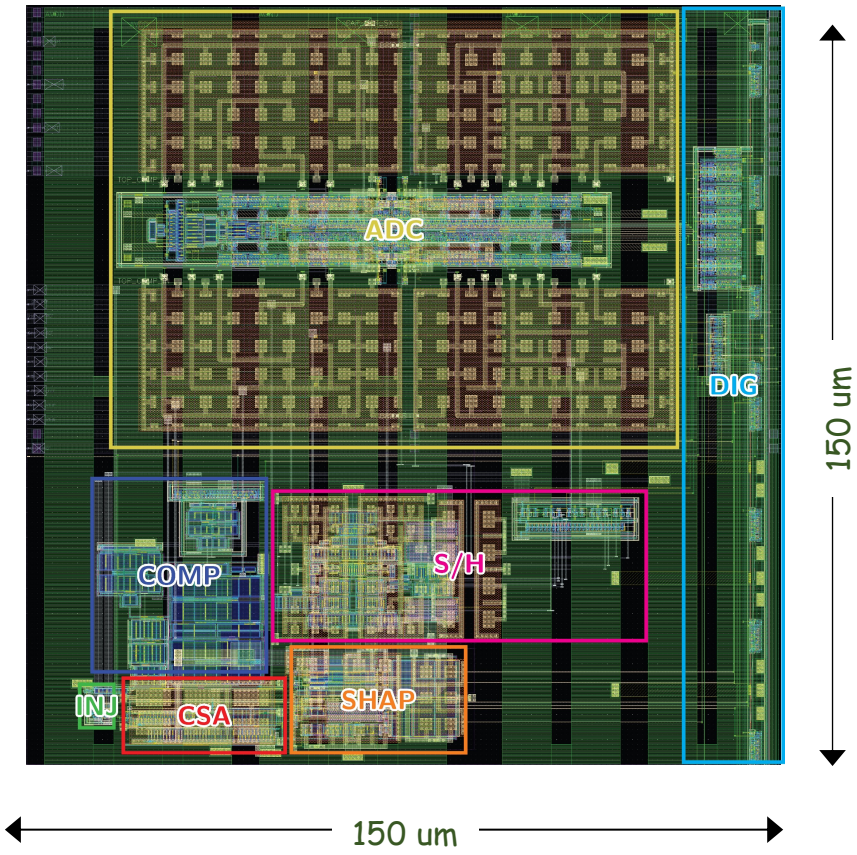




Hemperek T. (2021). Advances in Pixel Detectors.

Readout Channel



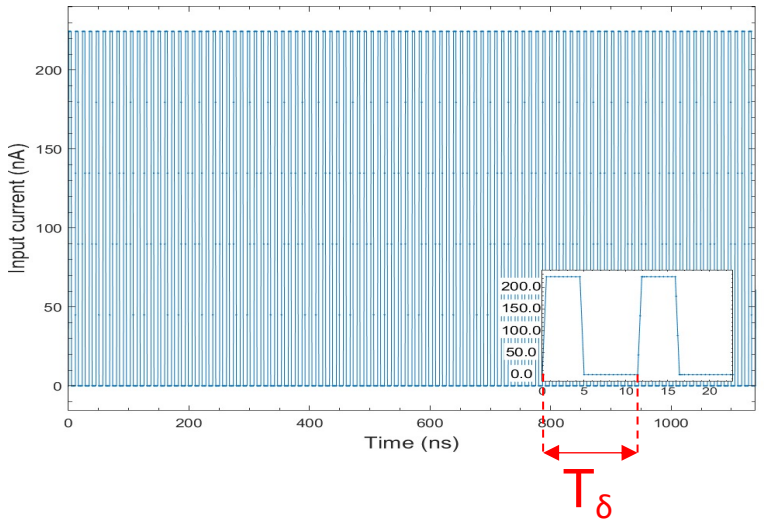


- Prototype Fast Readout for ptYchography Applications w/ 16 pixels.
- **Commercial 65 nm CMOS technology.**
- **Single photon detection**, with an **ENC of ~250 e⁻ rms** @ C_D = 100 fF.

- Adapts to **3 input photon energies**: 5 keV, 9 keV and 25 keV.
- **Input dynamic range up to 256 photons** in each mode.
- **RC-CR shaper** with 4 selectable peaking times (230 ns ÷ 530 ns).

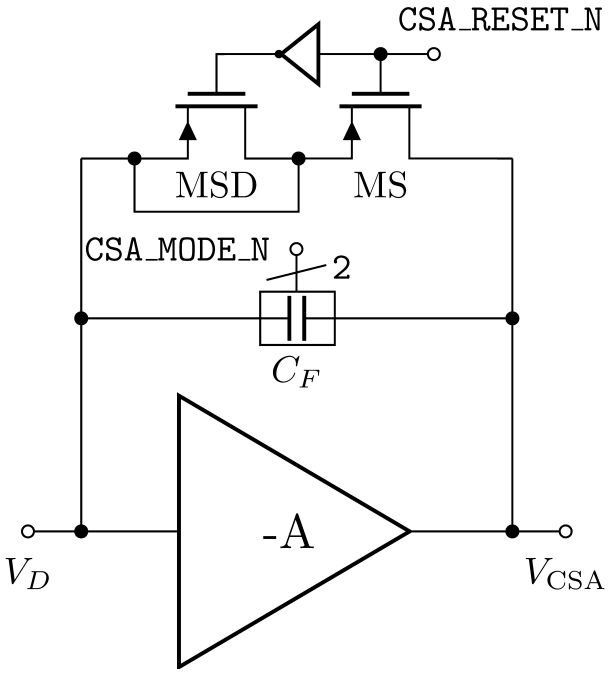
- **SOT comparator chain** to reject <1 input photon signals.
- **10-bit SAR ADC.**
- Power consumption: **~220 µW/px.**
- Area: **150 µm x 150 µm.**

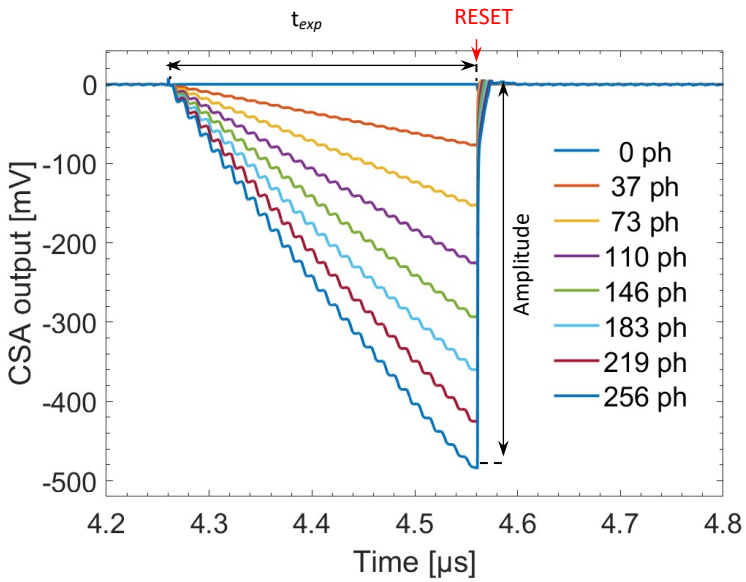
Charge Sensitive Amplifier



- Detector output modelled as in figure (T_δ = 11.4 ns), with C_D = 100 fF.
- **Too short of a time for a complete readout** (CSA integration, shaping and A/D conversion).

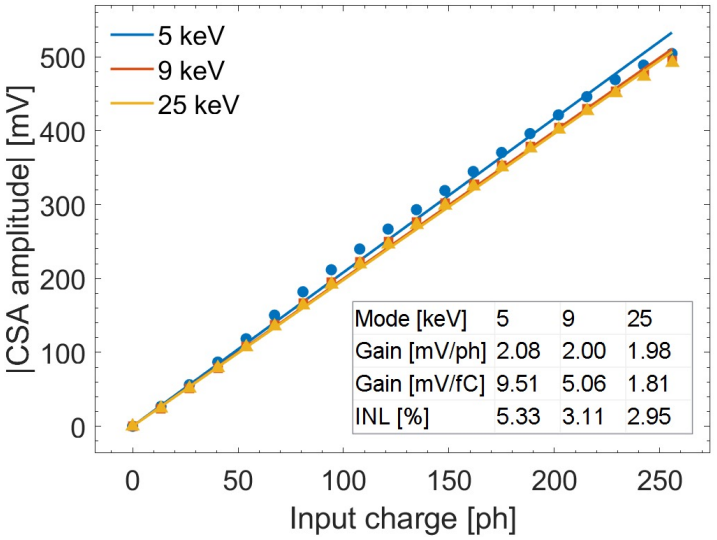
- CSA integration is performed in a tunable **exposure time** (t_{exp}) and for **t > t_{exp} the readout is forced to idle state** by a discharging switch on the CSA.
- **Signal at the switching is proportional to integrated charge**.



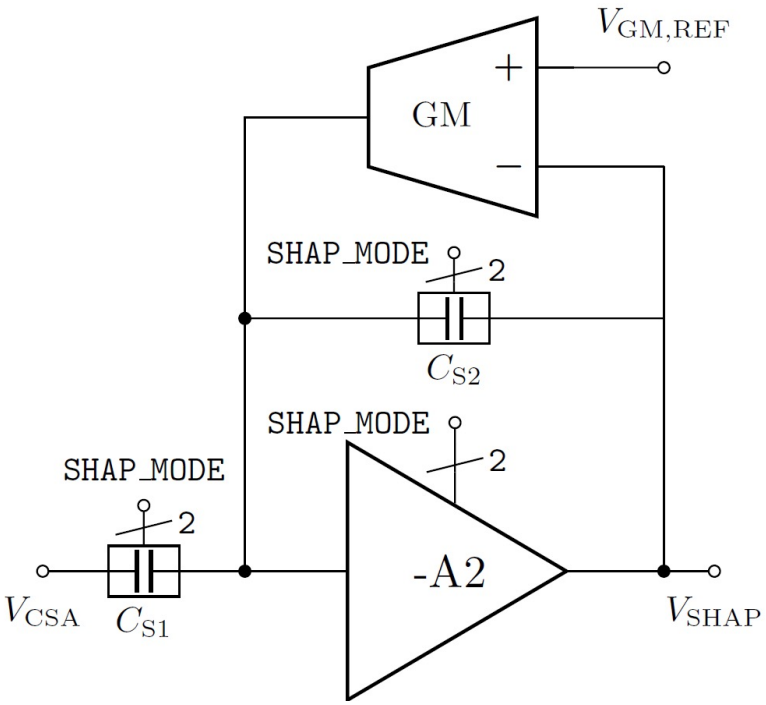


$$V_{\mathrm{CSA}}(t = t_{\mathrm{exp}}) \approx \frac{Q_D}{C_F} = \frac{1}{C_F}\int_0^{t_{exp}} I_D(t)dt \approx \frac{1}{C_F}\sum_{i=0}^{N} Q_{D,i}$$

Where $Q_{D,i}$ is the charge integrated at each pulse.



Shaper



$$V_{SHAP}(s) = -\frac{C_{S1}A_{02}}{(C_{S1}+C_{S2})\tau_{02}}\frac{s\tau_p}{(1+s\tau_p)^2}V_{CSA}(s)$$

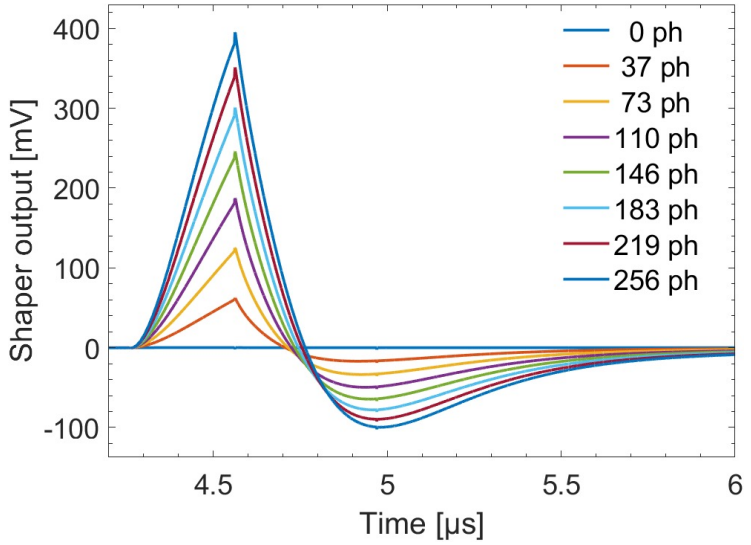
$$\tau_p = 2\frac{\tau_{02}}{A_{02}}\left(1+\frac{C_{S1}}{C_{S2}}\right) = t_p$$

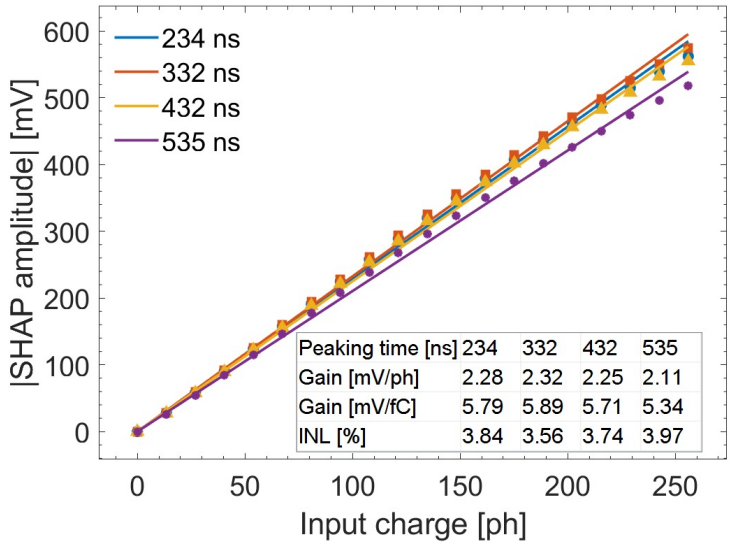
$$G_M = \frac{2C_2}{t_p}$$

$$\tau_{02} = \tau_{02}(\text{SHAP\_MODE})$$

$$C_{S1} = C_{S1}(\text{SHAP\_MODE})$$

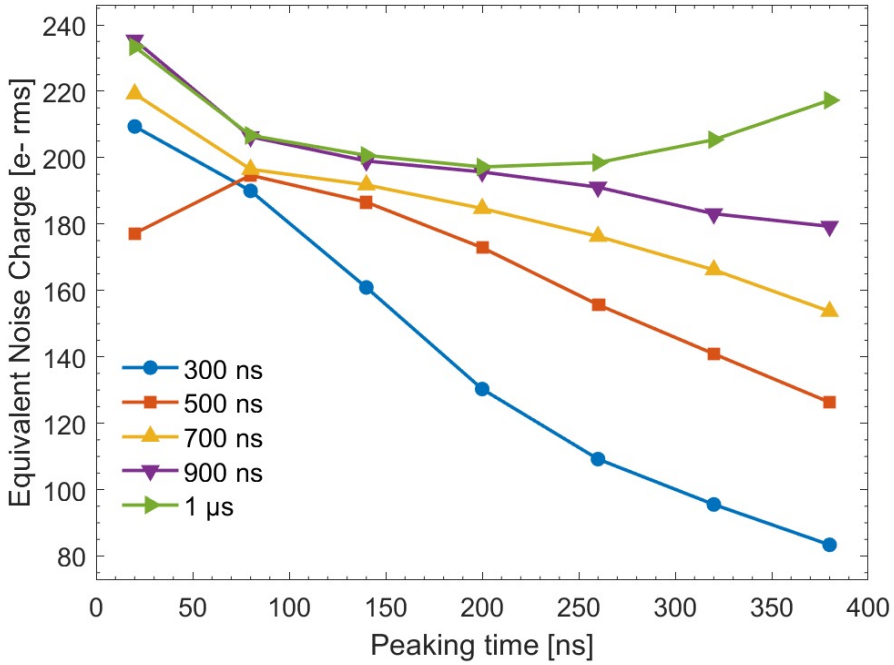
$$C_{S2} = C_{S2}(\text{SHAP\_MODE})$$





Architecture	CR-RC + TIA + SF
Peaking times	230 ÷ 530 ns

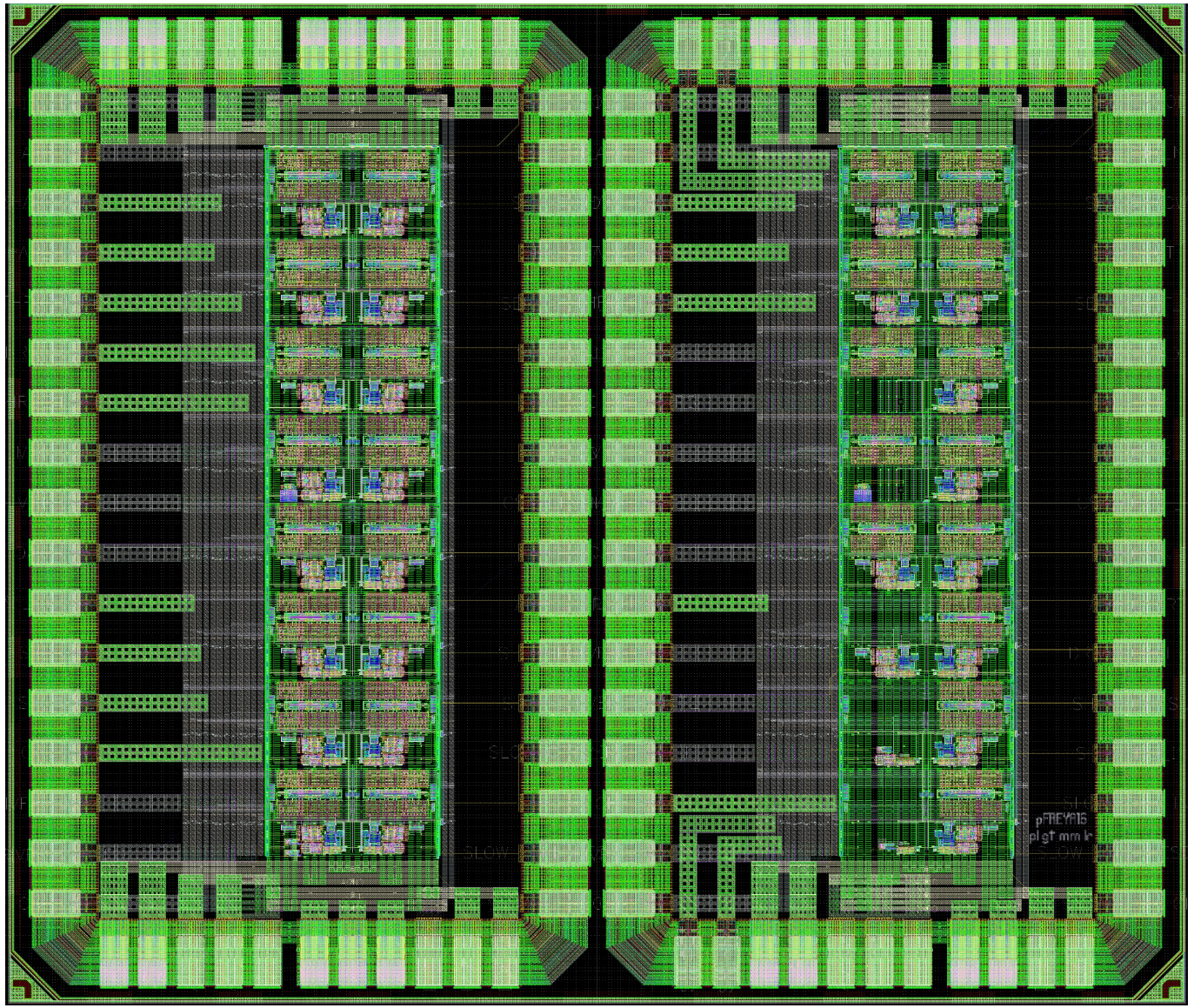
Equivalent Noise Charge



- **Noise in terms of equivalent charge at the input** (e^- rms).
- Only schematic-implementation of CSA was considered (should be the main contributor to noise).
- The rest of the circuit is ideal.
- 500 transient noise simulations for each point.

- **Shorter t_{exp} shows better noise performance.**
- **Longer t_p enable lower noise.**
- Combinations of **(t_{exp}, t_p) for which ENC < 200 e^- rms exist.**

pY16 and pYTS ASICs

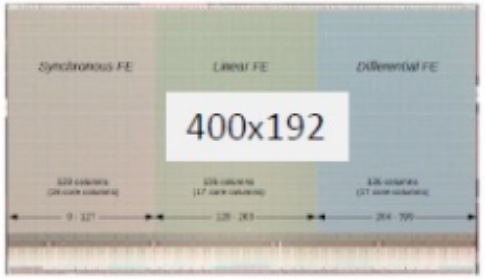


- Area of 1.7 mm x 2 mm.
- CLCC68 package.
- Elementary cells are mirrored about the vertical axis to isolate analog from digital.
- On the left, **pFREYA16 (pY16)**, composed by a **8-by-2 matrix of elementary cells and peripheral circuitry**.
- On the right, **pYTS**, a series of **test structures arranged in the same 8-by-2 matrix** fashion:
  - CSA only.
  - SHAP only.
  - ANALOG only.
  - ADC only (different versions)
- **Prototype chips** have been received last week, test setup is being developed

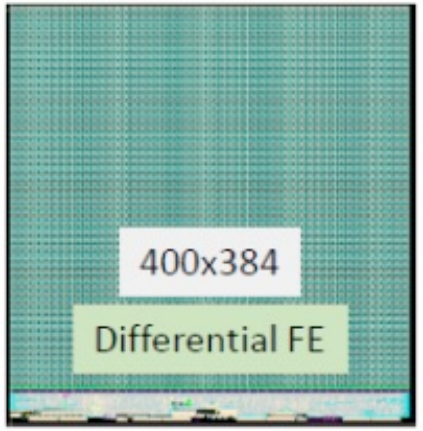
RD53 IP blocks in 65 nm CMOS

RD53 collaboration

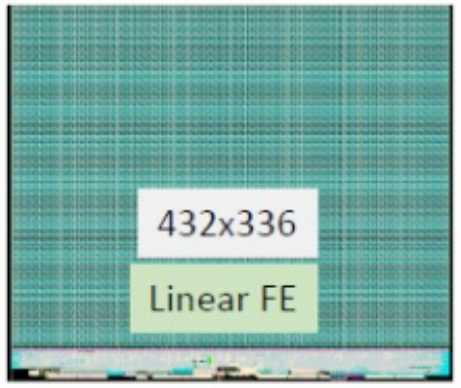
- **RD53 collaboration** was established to design and develop pixel chips for **ATLAS/CMS phase 2 upgrades**
- The RD53 project includes 24 institutes, ~20 designers
- Extremely challenging requirements for HL-LHC
  - Hit rates: 3 GHz/cm², small pixels: 50 x 50 µm²
  - Radiation: **500 Mrad** - 10^{16} neq/cm² over 5 years
- Technology: **65nm CMOS**
- **Characterization** of the 65 nm CMOS technology in harsh radiation environment
- Design of a **rad-hard IP library** (Analog front-ends, DACs, ADCs, CDR/PLL, high-speed serializers, RX/TX, ShuntLDO, …) qualified through a series of test chips



RD53A
Size: 20 x 11.5 mm^2 (Aug 2017)



RD53B-ATLAS (ITkPix-V1)
size: 20 x 21 mm^2 (Mar 2020)



RD53B-CMS (CROC-V1)
size: 21.6 x 18.6 mm^2 (May 2021)

Production chips

- RD53C-ATLAS (ITkPix-V2) submitted in March 2023
- RD53C-CMS (CROC-V2) to be submitted in Sept 2023

RD53 chip floorplan

- **Analog Chip Bottom (ACB)**

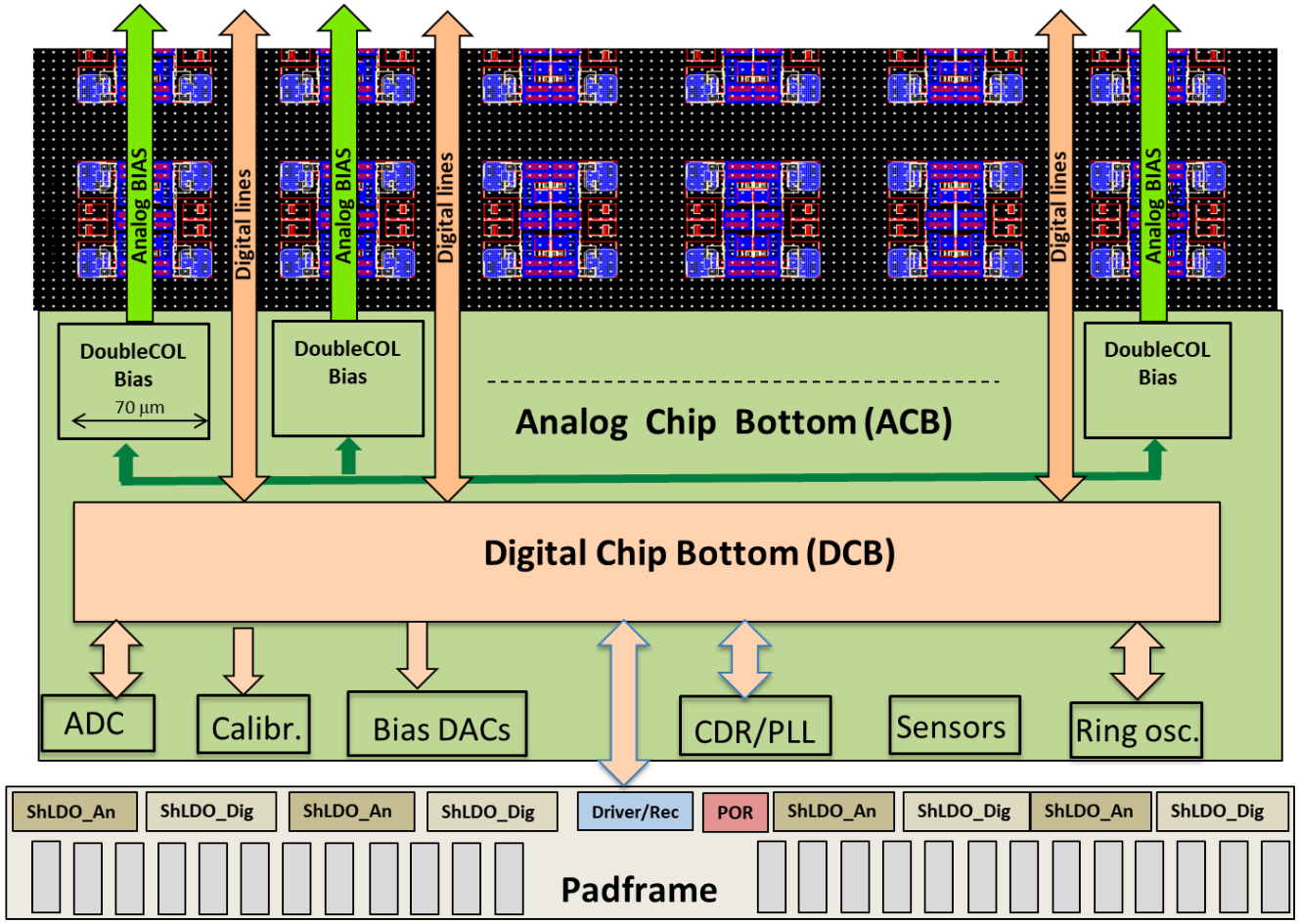
  includes building block for Calibration, Bias, Monitoring and Clock/Data recovery

- **Digital Chip Bottom (DCB)**

  synthesized logic for communication to/from chip, readout and configuration

- **Padframe (common to ATLAS/CMS)**

  includes I/O blocks with ESD protections and distributed ShuntLDO regulator for serial powering

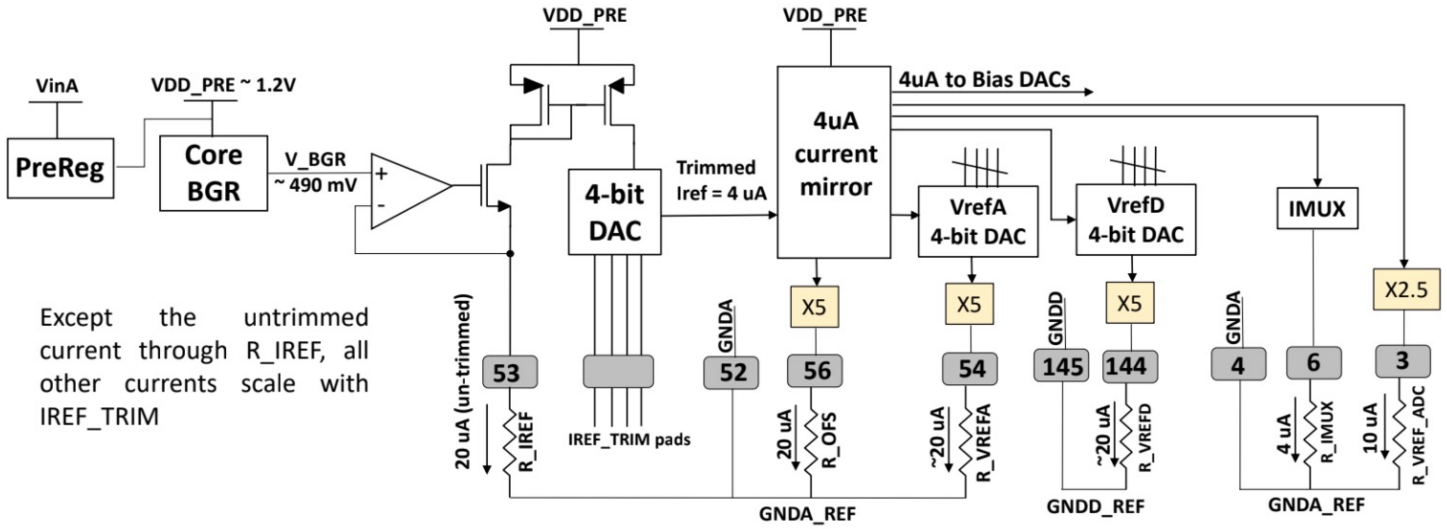


Analog and M/S blocks summary

Block	Description
Analogue front end	The ATLAS chip versions use a differential front end. The CMS chip versions use a linear front end.
Shunt LDO	Enables start-up and serial powering. Constant input current shared between chips, modules on serial chains. 1 LDO for digital power, 1 LDO for analogue power.
Clock & Data Recovery (CDR)/PLL	Recovers a 160MHz clock and command/trigger stream. The PLL generates internal clocks: 160 MHz, 64 MHz, 640 MHz and 1.28 GHz.
Bias circuit	Provides biases to the pixel array. Based on bandgap references.
Calibration circuit	Injects hits into the pixel array, to calibrate its response.
Monitoring block	Digitises analogue quantities using a voltage mux, current mux and 12-bit ADC
Temperature and Radiation sensors	Temperature sensors: polysilicon resistors. Radiation sensors: based on PMOS devices with a linear variation in voltage in the dose range 10 - 1000 Mrad.
LVDS pads/drivers	Pads and drivers for differential inputs/outputs

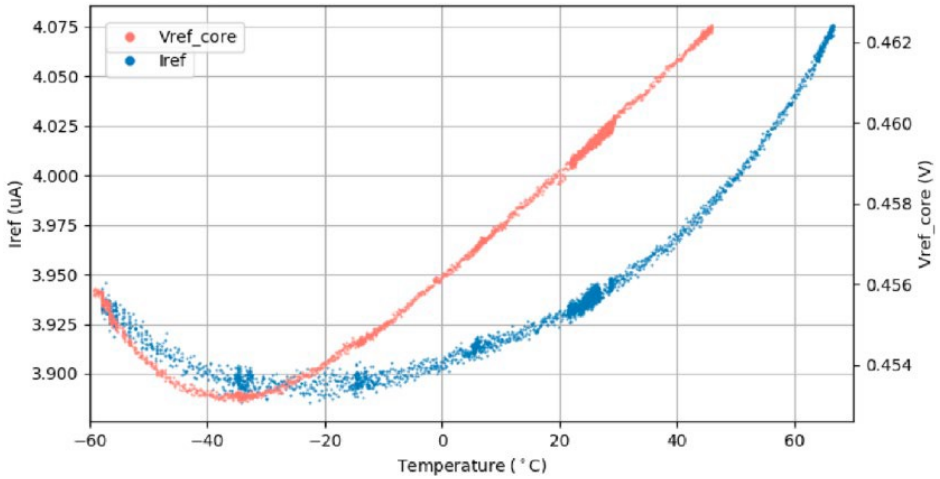
Bias circuit

- Based on Bandgap reference circuits (low sensitivity for V/I to temperature variations)
- Tuning by means of 4 wire-bond trimming pads (no risk of SEU bit flips) → optimal value is found during wafer probing
- Tuned current Iref is mirrored and used by DACS for the bias of analog front-ends, CDR and other IPs

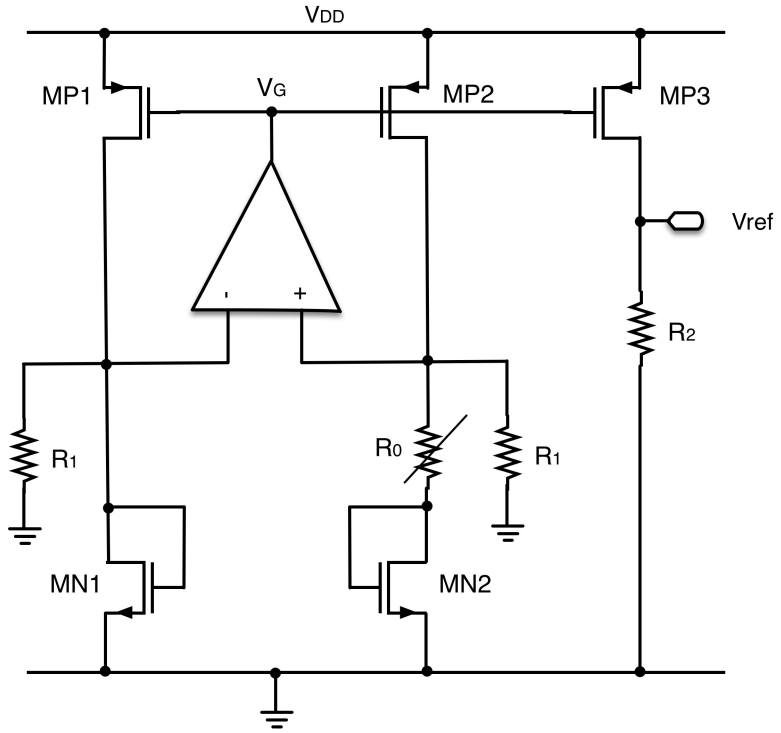


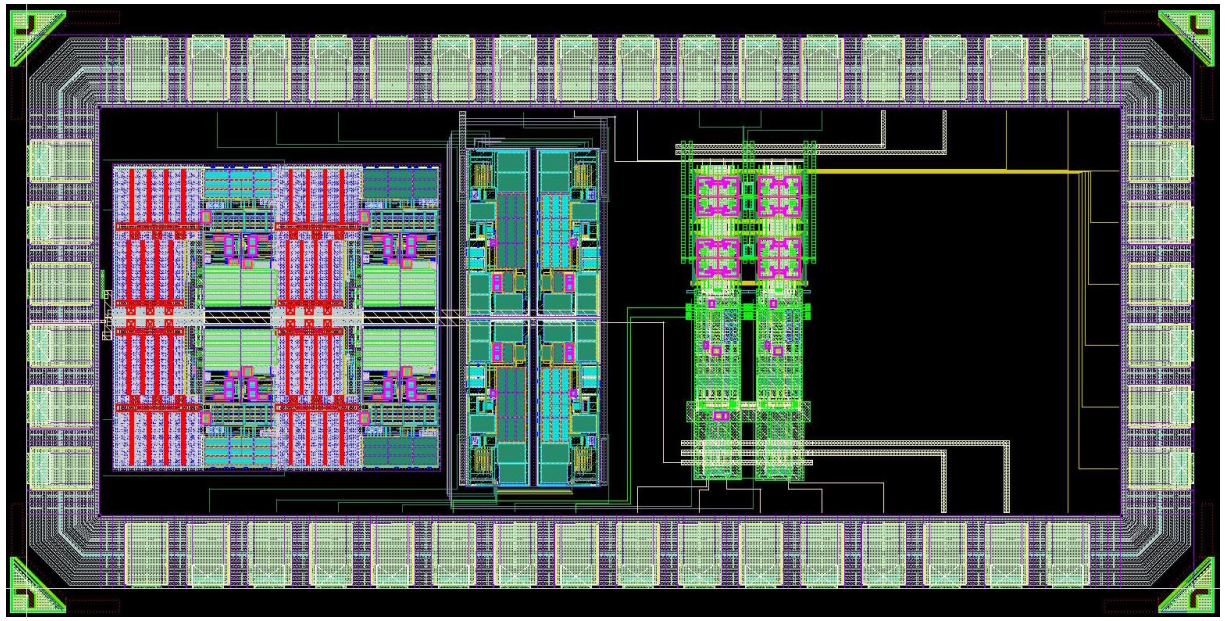
Except the untrimmed current through R_IREF, all other currents scale with IREF_TRIM

4% difference over 120°C temp. range



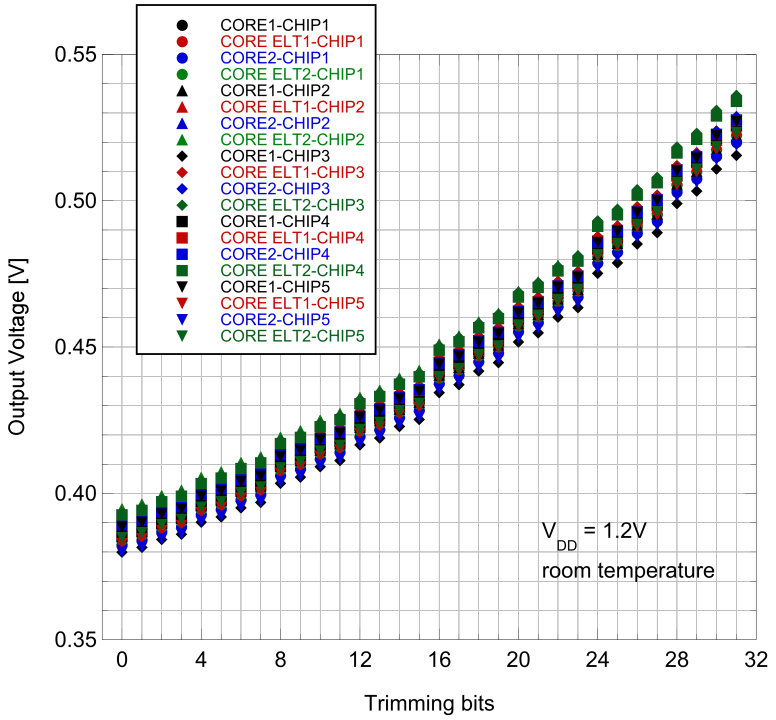
Bandgap reference

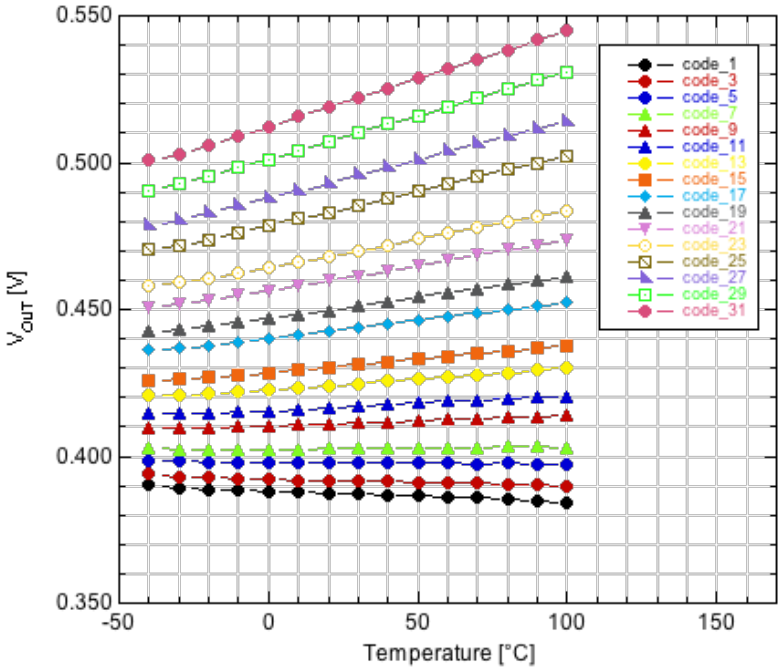


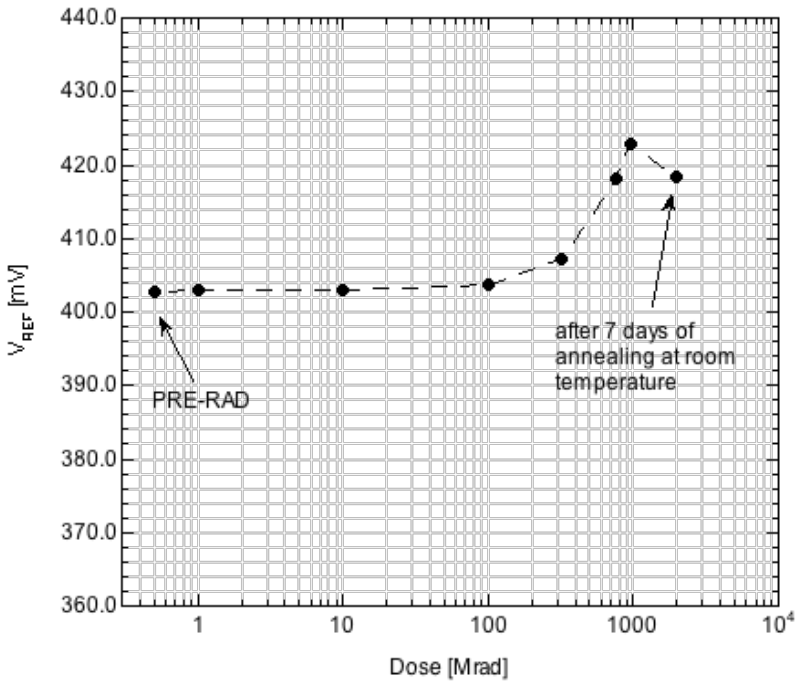


- Current in R0 ∝ difference of two VGS → **PTAT**, current in R1 ∝ to VGS → **CTAT**
- Current sum is mirrored onto R2, output is **T-independent**
- **5 bit** trimming
- Integrated in a **mini@sic prototype** before pre-production RD53 submission

Bandgap reference – test results







10 BGRs characterized (5 ASICs)

Vref ≈ 440mV ± 10mV (conf. 16)

2 ASICs have been characterized in the climatic chamber at the INFN Pavia between **-40°C and +100°C**

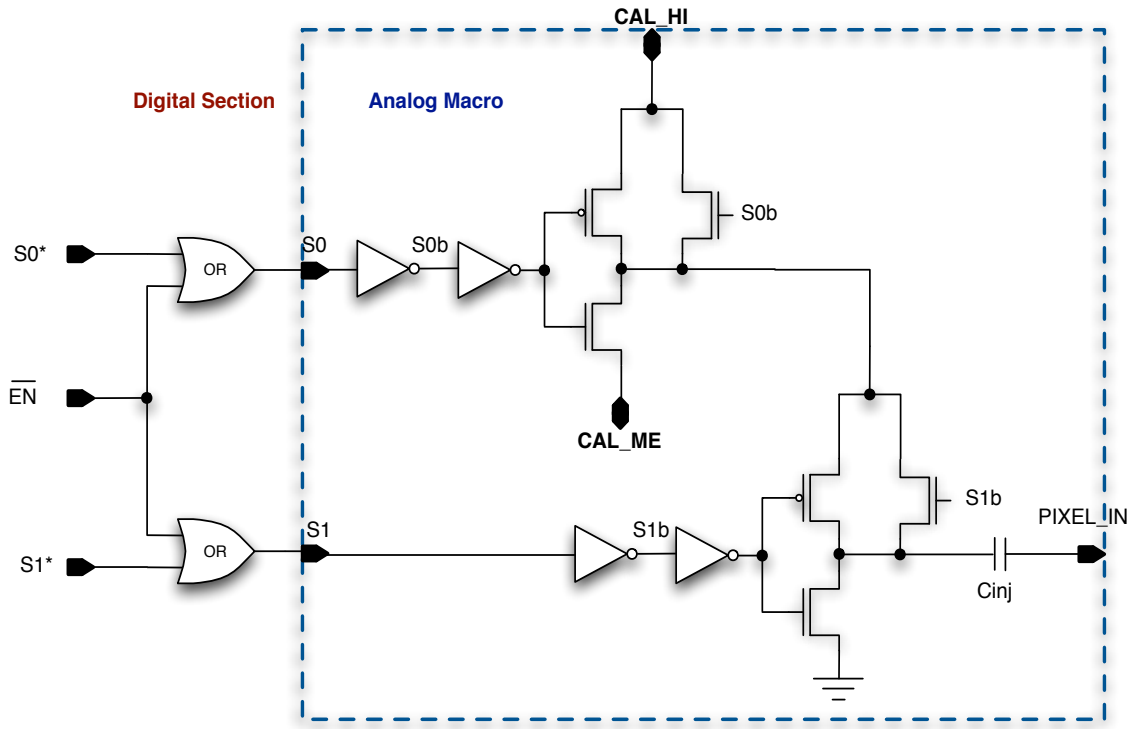
One chip irradiated (room T) up to **1 Grad(SiO_2) TID** of 10-keV X-rays.

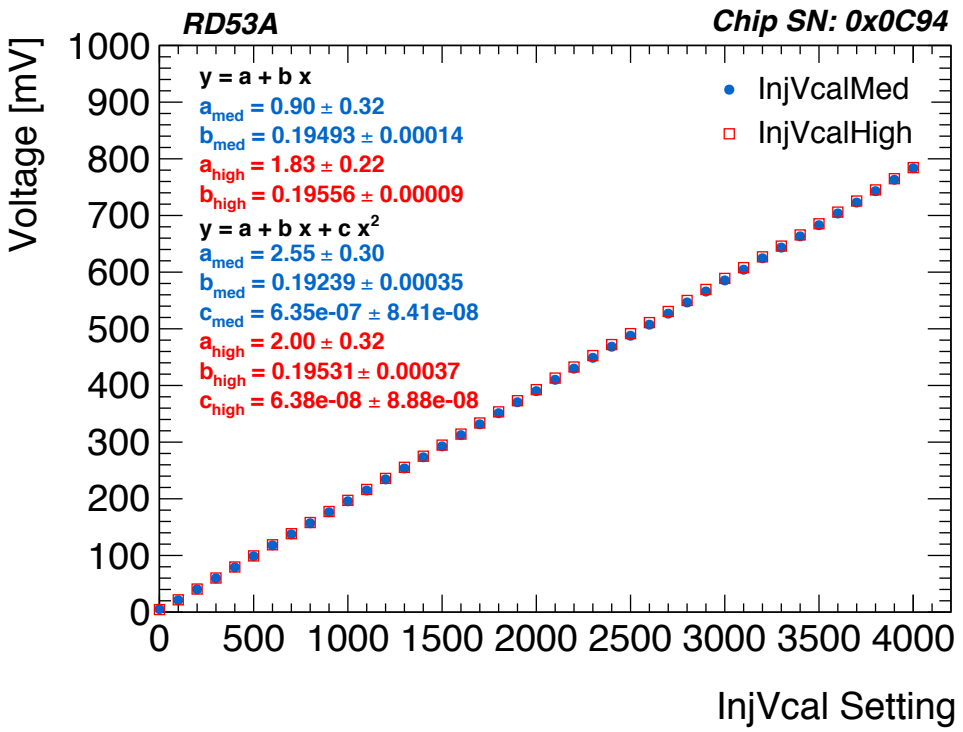
Dose rate of about 1 krad(SiO_2)/s.

During irradiation the bandgaps were biased as in the real application

Radiation induced $\Delta V_{REF} \approx 5\%$ @ 1 Grad

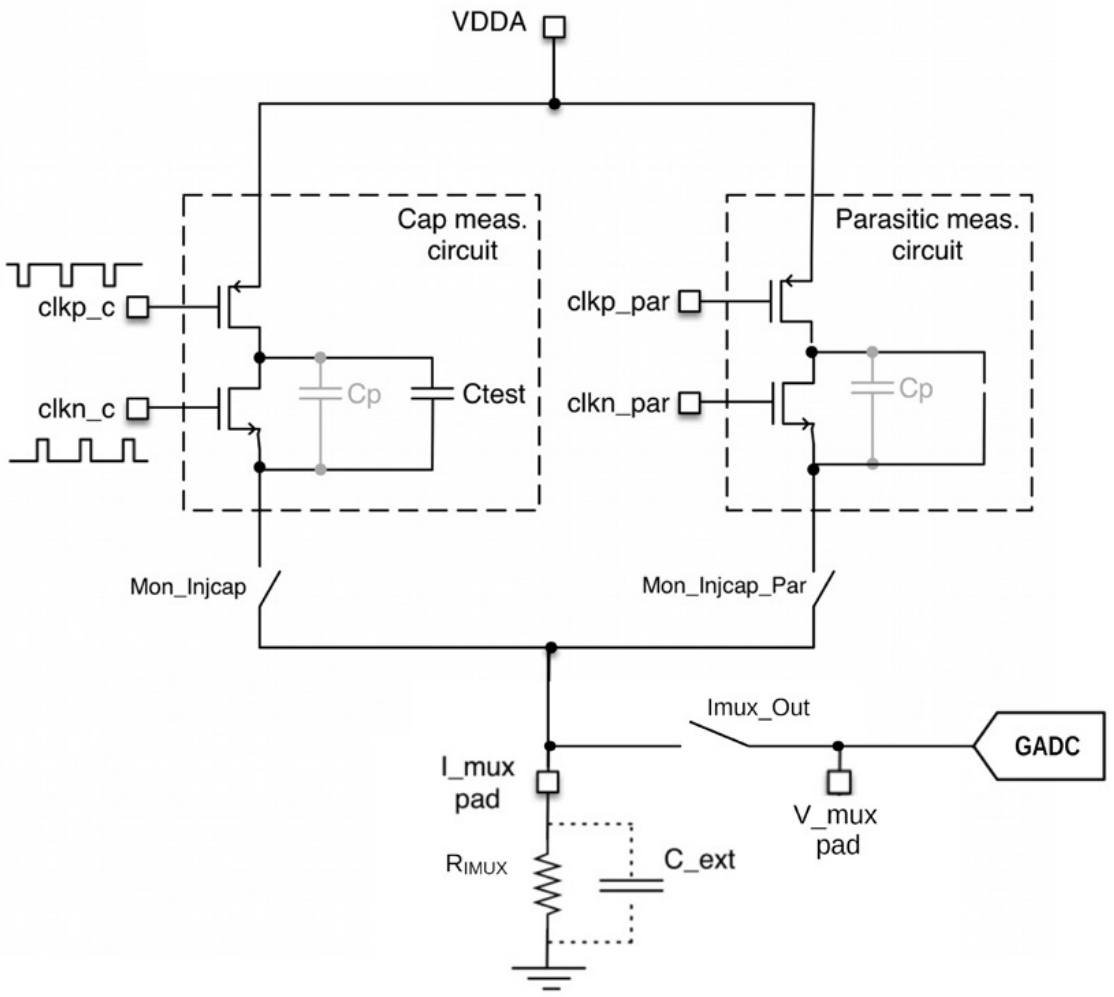
Injection circuit





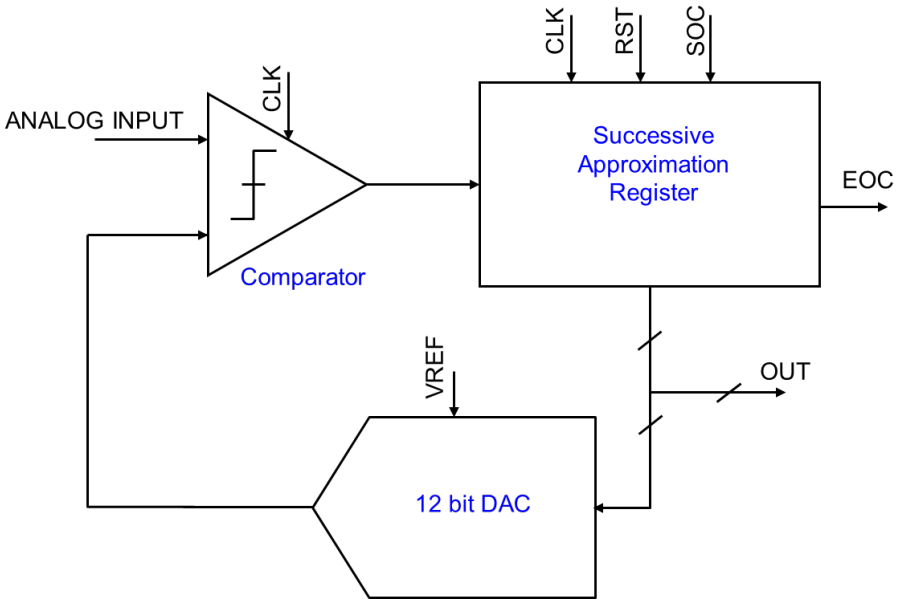
- **Each pixel** in the chip matrix is equipped with an injection circuit for test/calibration
- **Local generation** of the analog test pulse starting from **2 defined DC voltages** (CAL_HI and CAL_ME) distributed to all pixels and a 3rd level (**local GND**)
- Two operation modes which allow to generate **two consecutive signals** of the same polarity or to inject **different charges in neighboring pixels** at the same time

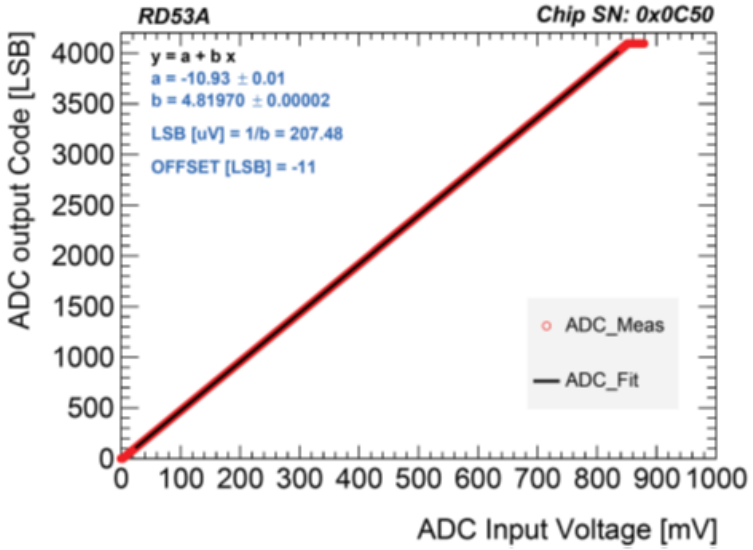
Injection cap measure

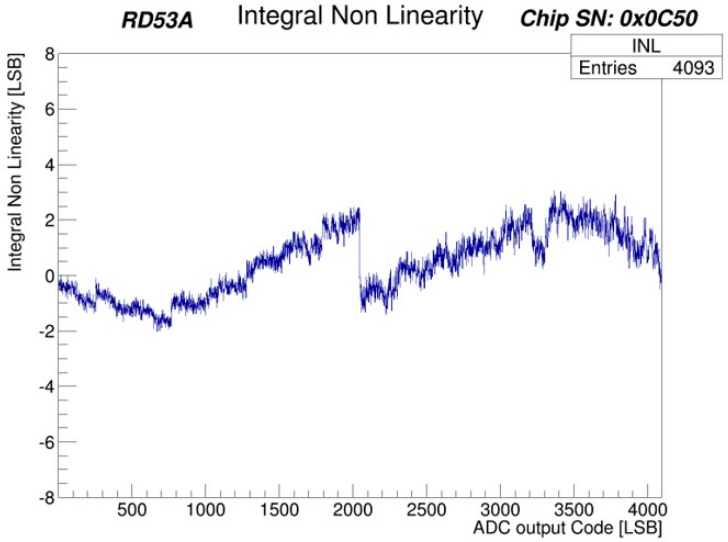


- Possibility to **measure the value of injection capacitor** using a dedicated circuit to define accurately the injected charge at the preamplifier input
- Integrated in the **Analog Chip Bottom**
- Two sections: the **cap measure** and **parasitic cap measure**. The first one consists of an array of 100 capacitors, each identical to the injection cap → routing metal is needed, which adds parasitic capacitance. An identical array with the capacitors removed is therefore integrated to evaluate the parasitic capacitance.
- The circuit is based on a **charge pump** with NMOS and PMOS transistors controlled by non-overlapping clocks → current in R_{IMUX} proportional to the capacitance

General purpose ADC

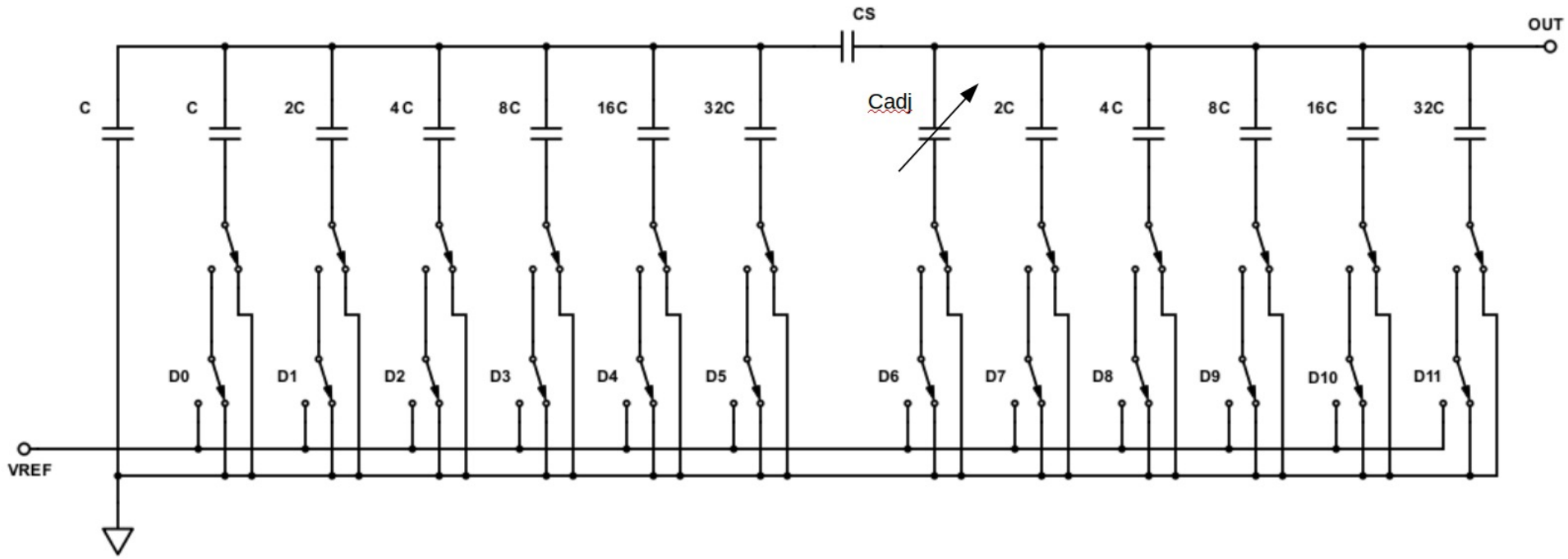






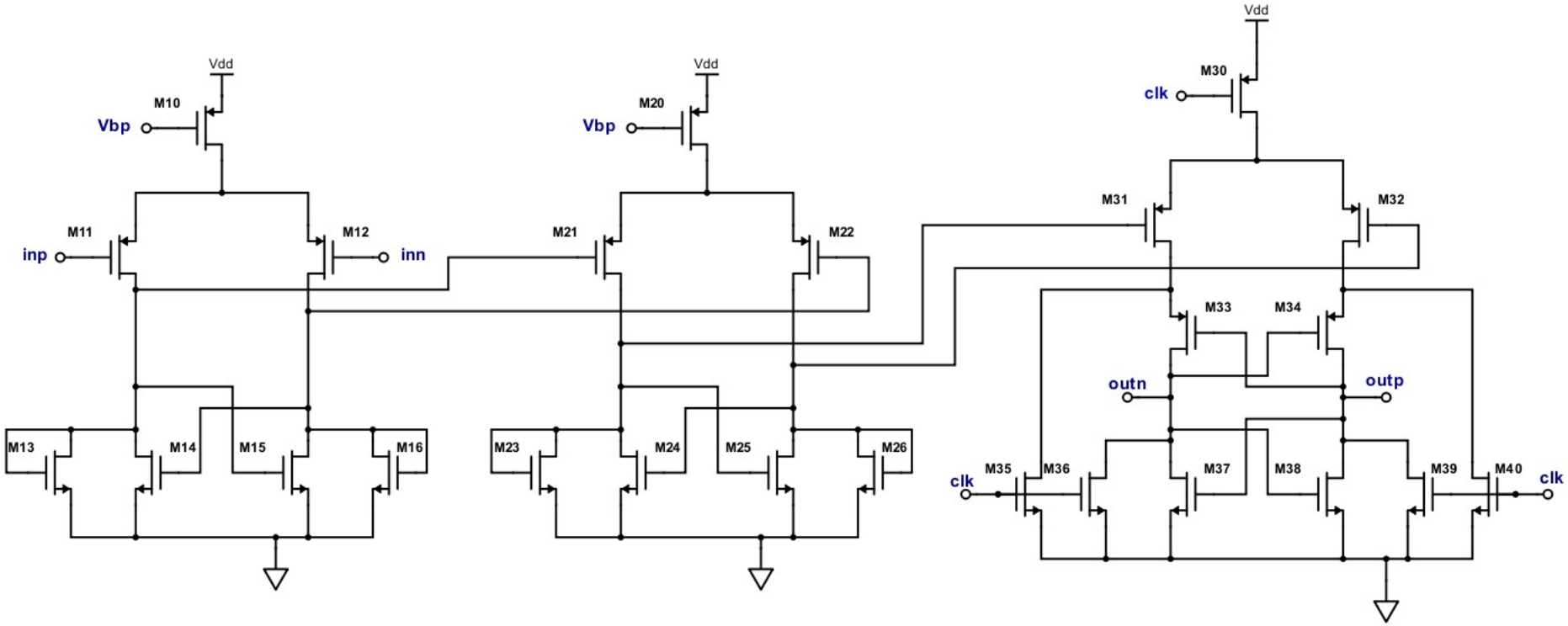
- Based on a **Successive-Approximation Register (SAR) architecture**
- In RD53 chips, the ADC is fed with the bunch crossing clock (40MHz). A 1024:1 frequency divider generates the **39 kHz internal clock** driving the ADC
- The SAR ADC consists of three main circuits:
  - a **12-bit DAC** based on a capacitance network supplied through the reference voltage (VREF)
  - a high sensitivity **comparator**
  - a **SAR logic** block including the frequency divider

12-bit DAC



- Capacitive DAC based on a **bridge structure** → larger unit capacitance → better element matching
- **Nonlinearity** due by mismatch of the bridge capacitance and by parasitic capacitance in the DAC array
- **6 trimming bits** allows to adjust Cadj to compensate the non-linearity

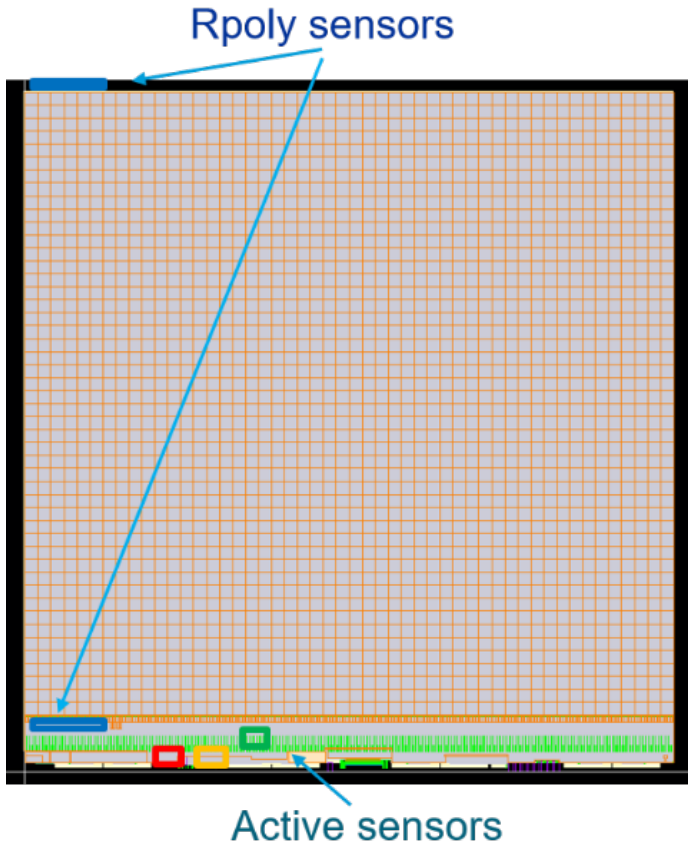
ADC comparator



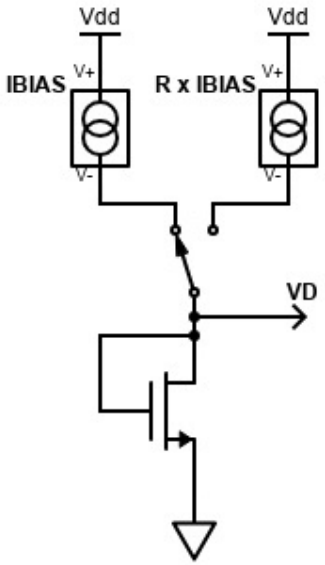
- **3-stage comparator** with two differential operational transconductance amplifiers with diode and current source loads followed by a dynamic latch comparator
- The first stage **input transistors** are critical for **linearity** and **accuracy**
- Large transistors → improved offset and less sensitive to radiation **but** large G-S capacitance (dependent on the input voltage!) →increased non-linearity
- A **compromise** has been found to keep low non-linearity with good tolerance to radiation

Temperature sensors

- Different temperature sensors are implemented in the RD53B chip :
  - **Three active sensors** are implemented in the chip bottom close to the shunt LDO circuit, considered the hottest part of the chip
    - Based on **NMOS diode-connected** transistor
    - Large area devices -> **very tolerant to the TID effect**
  - **Two sensors based on r-poly** resistances are placed on the top and the bottom of the chip
    - Monitor the **temperature difference** between the top and the bottom of the pixel array
  - **NTC device** implemented outside the chip with bias current provided from the chip



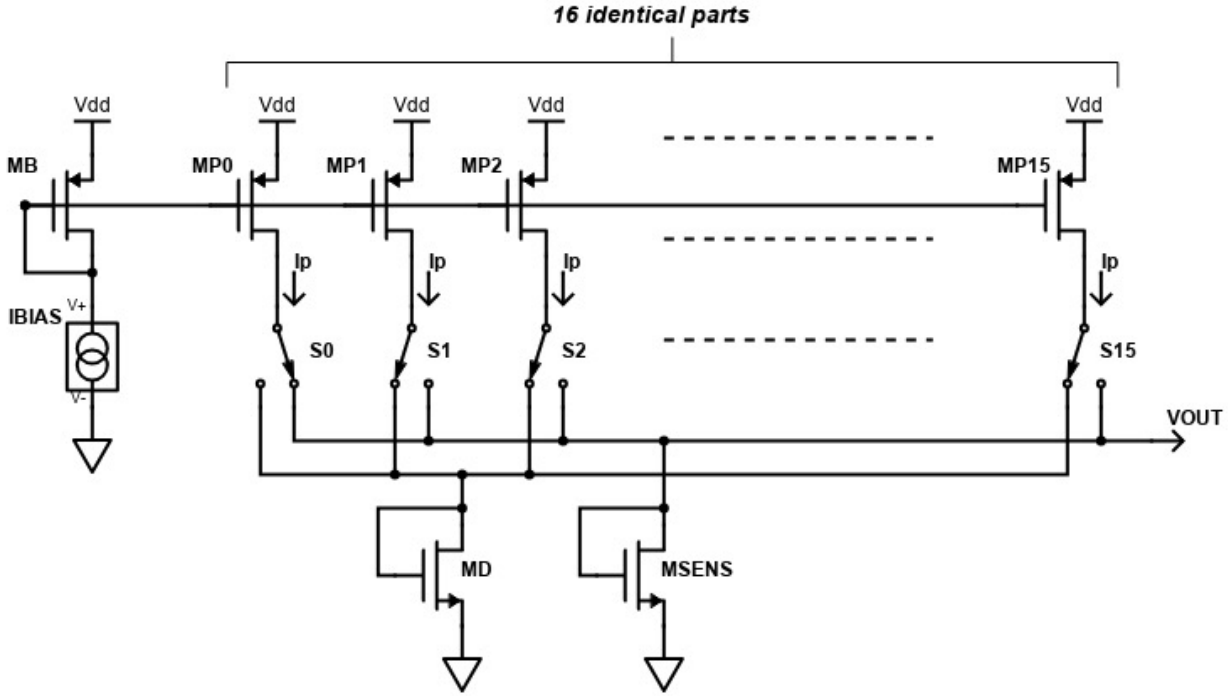
Basic sensor structure



- I_{BIAS} and $R \times I_{BIAS}$ are applied consecutively to the sensor
- The temperature is calculated off-line based on the **difference ΔVD**

$$T_{ab} = \frac{q}{n_f \times k_B \times \ln R} \times \Delta V_D$$

- Potential sources of **temperature measurement error** include the **ratio R** of the two sensor bias currents → **Dynamic Element Matching** is used to mitigate this effect

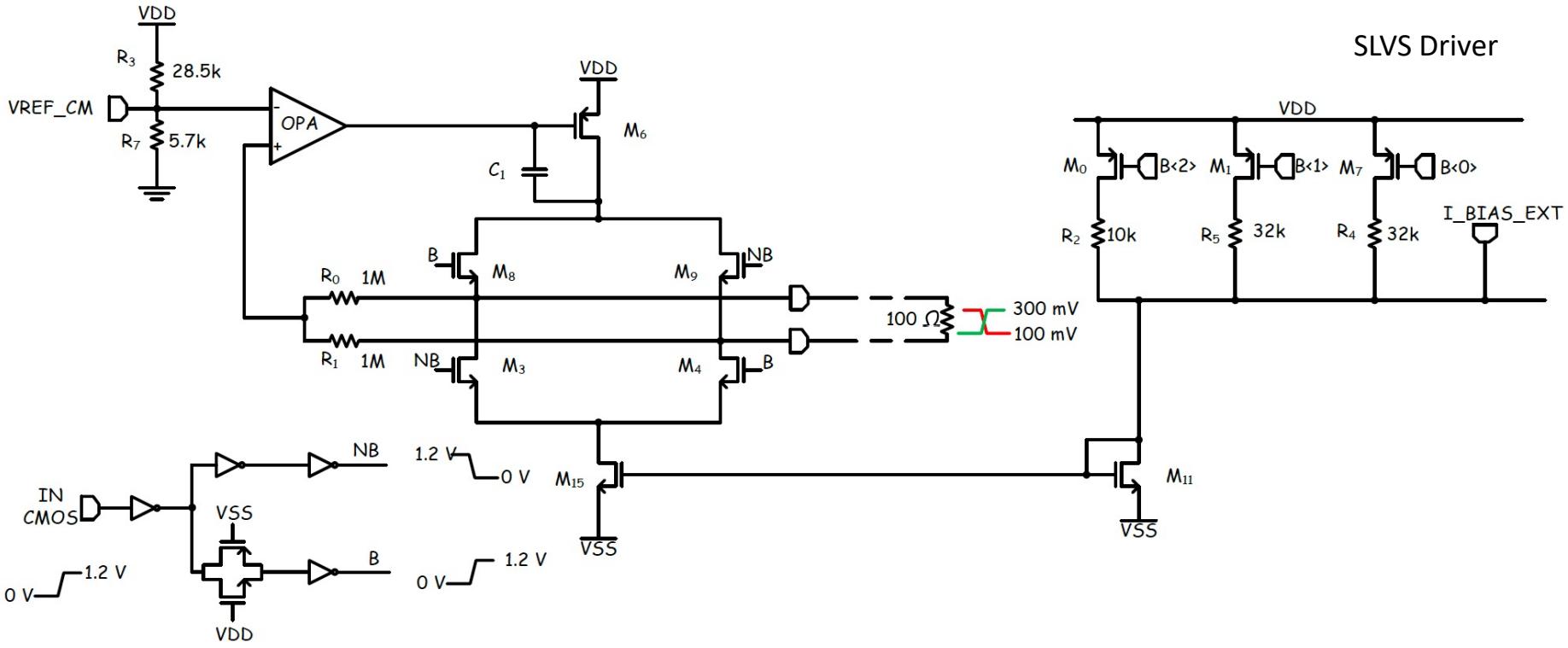


$$\Delta V_D = \frac{\sum \Delta V_{Di}}{16}$$

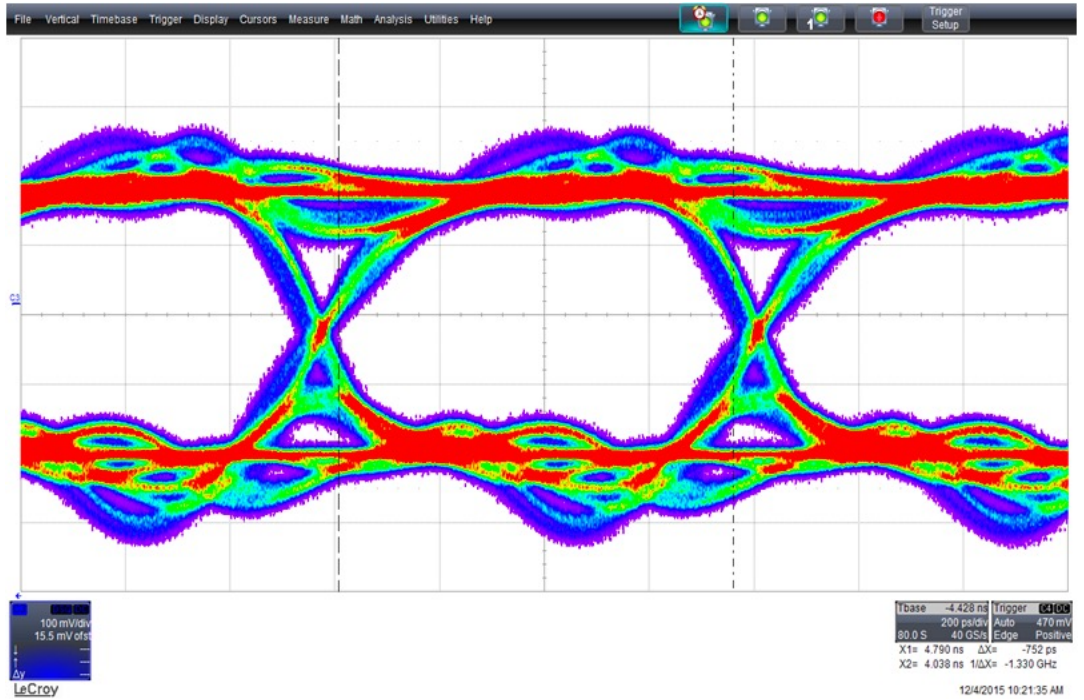
C-SLVS Driver

- The developed **C-SLVS features** a differential current-steering architecture with a voltage swing of 200 mV (programmable) on a 100 Ω termination resistance and a common mode of 600 mV.
- The **driver** architecture is based on a Bridged-Switch Current Source scheme. The **2 mA biasing current** is switched through a 100 Ω termination resistance, according to the input data stream. The output current of the transmitter can be trimmed, by means of three configuration bits, in a range from 500 µA to 2.5 mA.
- To achieve insensitivity to PVT variations, a simple **low power common-mode feedback** has also been included. The common mode voltage is sensed by two resistors, which are connected to the output node and compared with a reference voltage.

Power dissipation: 2.8 mW
Area: 150 µm x 200 µm



C-SLVS Driver – test results



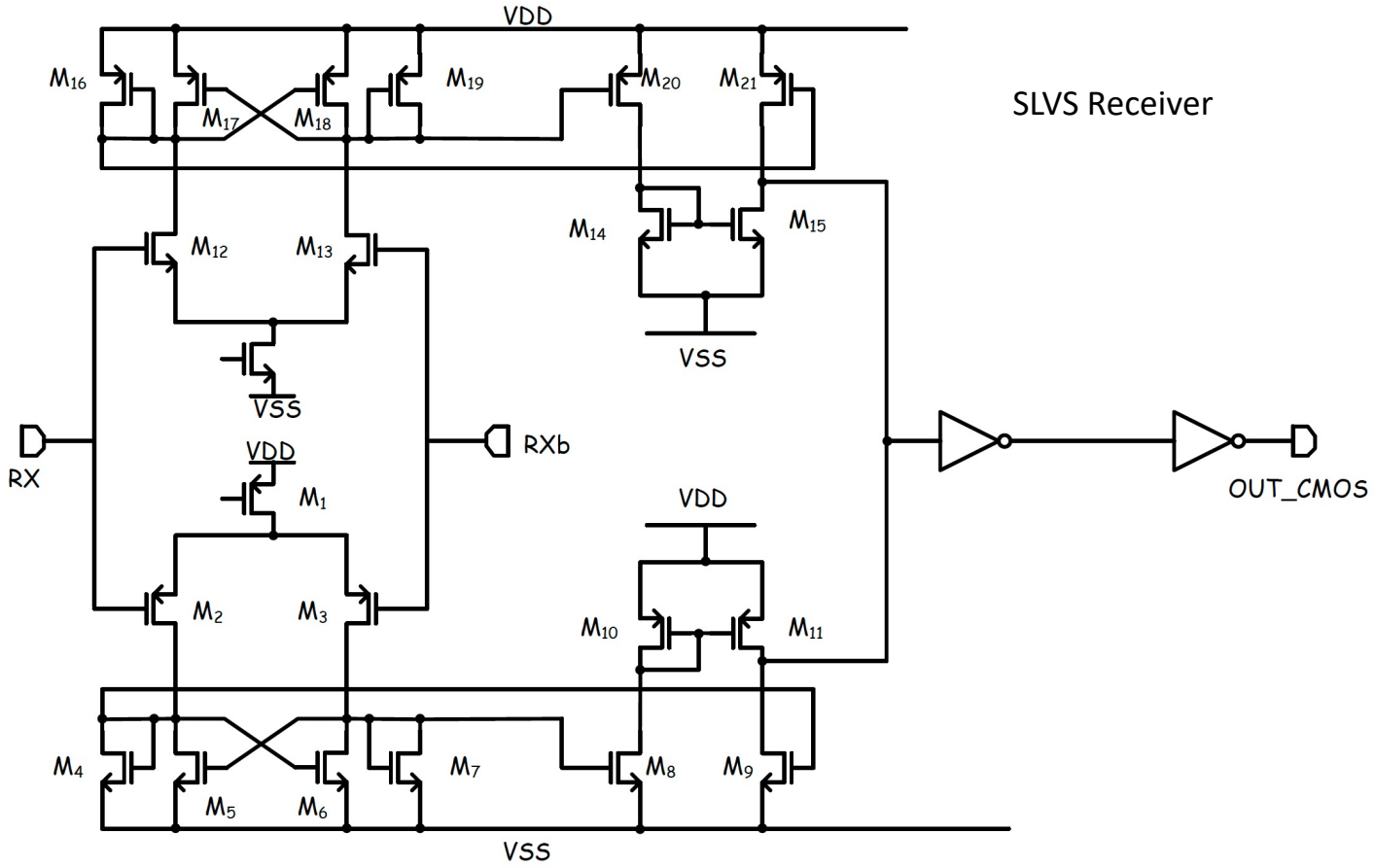
Eye Amplitude	376.7 ± 11.7 mV
Eye Height	365 mV
Eye Width	752 ps (0.9 UI)
rms Jitter	11 ps
Eye Rise Time	309 ps
Eye Fall Time	220 ps

- Two ASICs are bonded directly on the PCB
- The termination resistance is connected to the driver through a 5.5 cm microstrip differential pair
- 1.2 Gbit/s CMOS PRBS signal applied to the driver input
- Transmitter output signal via Differential Probe on termination resistance

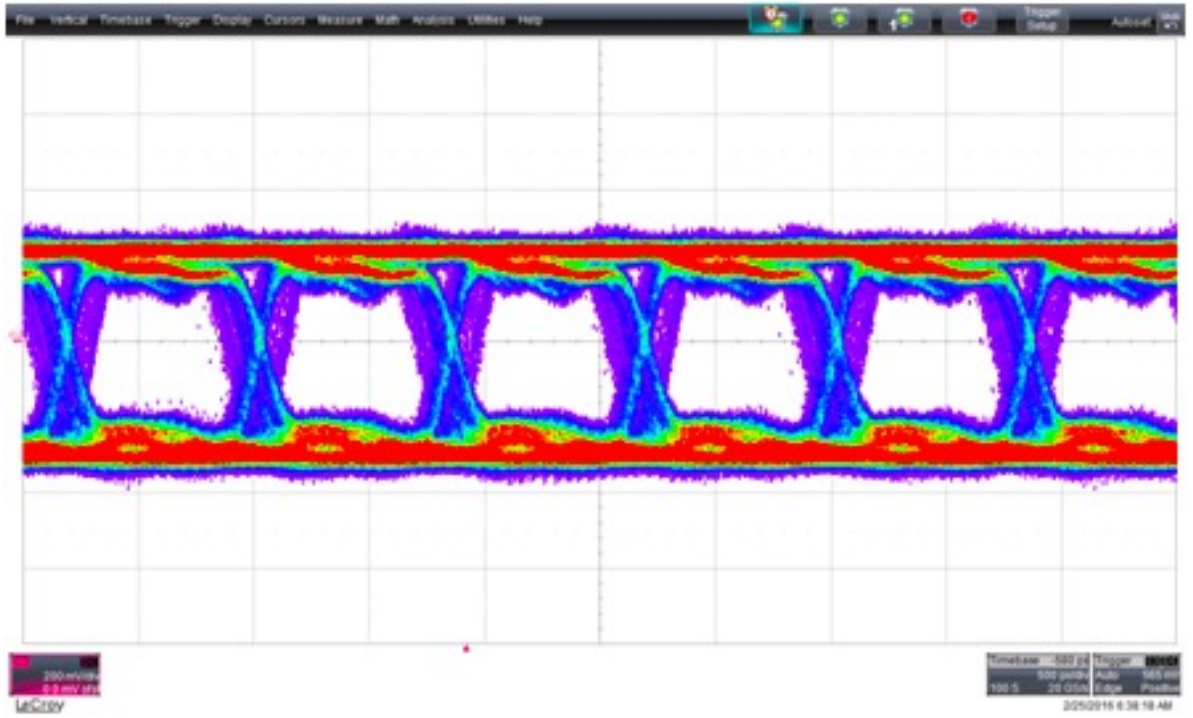
C-SLVS Receiver

- The **receiver** is a rail-to-rail stage, able to detect differential signals with a common mode from 100 mV to 1 V.
- Based on three stages
  - a **fully differential amplifier** with a cross-coupled load and with a bandwidth close to 1.2 GHz
  - a **differential-to-single ended amplifier** with a full swing CMOS output chip voltage
  - a chain of **inverters**

Power dissipation: 2.5 mW
Area: 90 µm x 115 µm



C-SLVS Receiver – test results



- The receiver has been stimulated with a 1.2 Gbit/s differential PRBS signal
- 100 Ω internal termination resistance
- The receiver is followed by CML driver provided by the microelectronics group of CERN
- The minimum detectable signal at 1.2 Gbit/s is an input differential voltage of 150 mV
- The eye diagram is measured at CML output at 1.2 Gbit/s, when at the input VID = 200 mV - VCM = 200 mV is applied

Conclusions

- In the framework of the **PixFEL project**, funded by INFN, a front-end chip has been designed in a commercial 65 nm CMOS technology
  - The front-end circuit includes a charge sensitive amplifier with dynamic compression of the signal, able to cope with a dynamic range from 1 to 10000 photons

- The **FALCON project** aims at the development of a **top tier detector for X-ray ptychography**
  - a front-end able to cope with moderate dynamic range is under development. The front-end is designed to be low power (≤ 150 µW), while an ENC ≤ 200 e^- rms can be achieved in a small pixel area(150 µm x 150 µm).

- A number of analog and M/S **IP blocks in 65 nm CMOS** has been designed by the **RD53 Collaboration**, aiming at the development of pixel readout chips for **ATLAS/CMS phase 2 upgrades**

References

PixFEL Project

- G. Rizzo et al., “The PixFEL project: development of advanced X- ray pixel detectors for application at future FEL facilities”, *Journal of Instrumentation*, 2015 JINST 10 C02024. doi: 10.1088/1748-0221/10/02/C02024
- M. Manghisoni, et al., “Dynamic Compression of the Signal in a Charge Sensitive Amplifier: Experimental Results”, *IEEE Trans. Nucl. Sci.*, vol. 65, no. 1, 2018. doi: 10.1109/TNS.2017.2784095
- L. Lodola, “Interleaved SAR ADC for in-pixel conversion in future X-ray FEL applications”, 2015 PRIME Conference, DOI: 10.1109/PRIME.2015.7251339
- M. Pezzoli et al “Characterization of PFM3, a 32x32 readout chip for PixFEL X-ray imagers ” 2019 IEEE NSS, doi: 10.1109/NSS/MIC42101.2019.9059651

FALCON Project

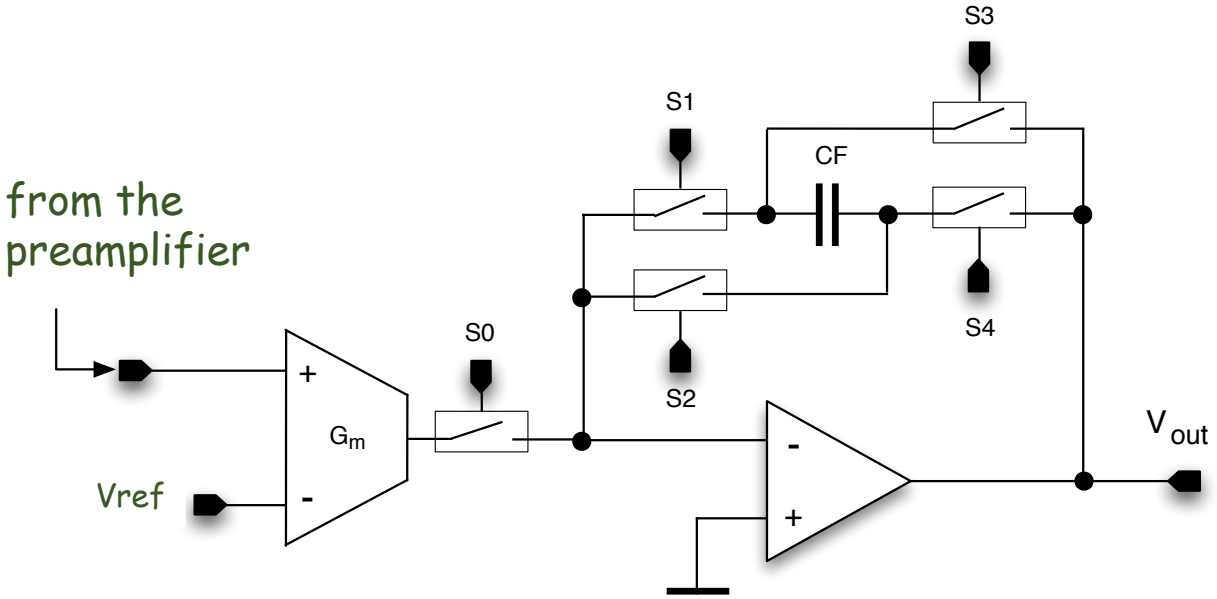
- P. Lazzaroni, et al., “FALCON readout channel for X-ray ptychography applications”, 17th Conference on Ph.D Research in Microelectronics and Electronics (PRIME), 2022. doi: 10.1109/PRIME55000.2022.9816837
- P. Lazzaroni, et al., “A low-noise readout channel for X-ray ptychography applications”, presented at 2022 IEEE NSS

RD53

- M. Garcia-Sciveres, F. Loddo, J. Christiansen, “RD53B Manual”, CERN-RD53-PUB-19-002

Backup slides

Time variant filter: transconductor + FCF

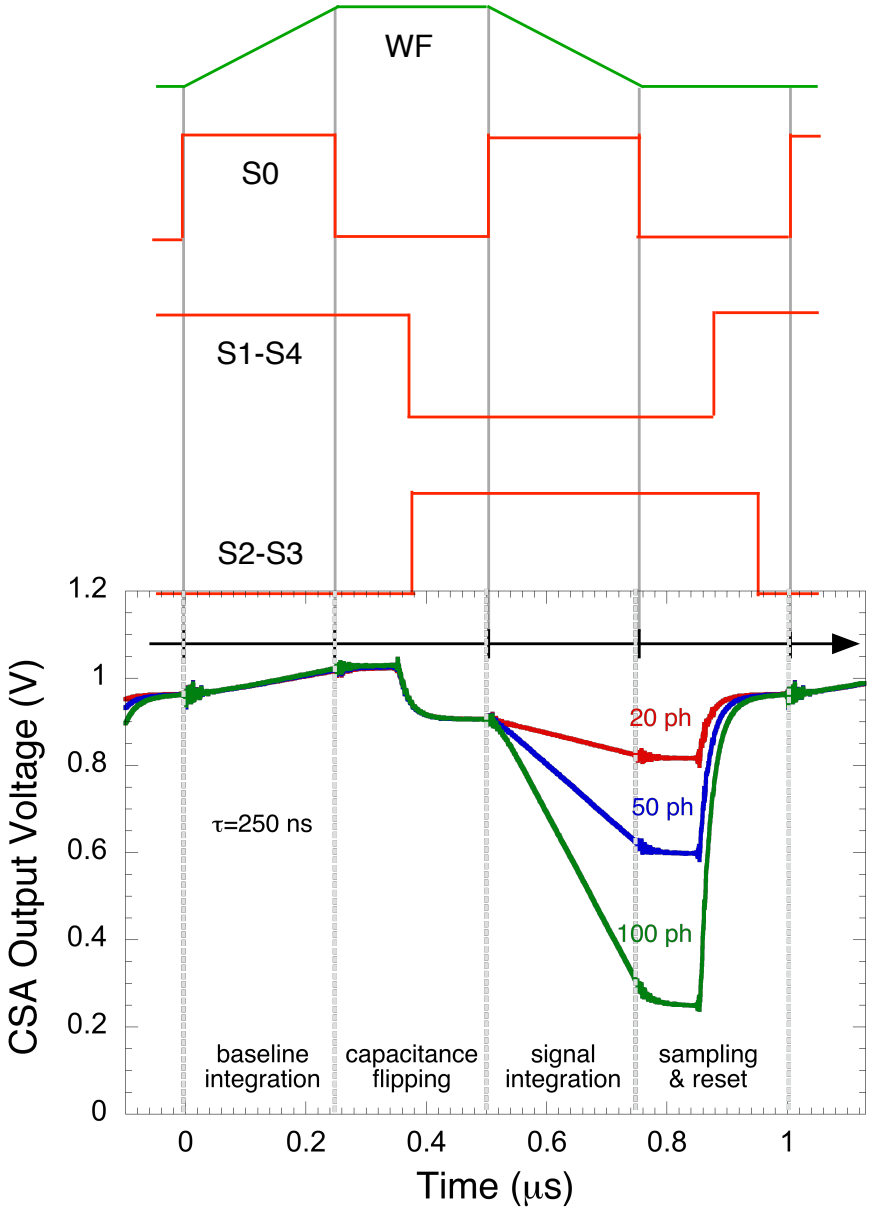


Flip capacitor filter (*)

- events with a known repetition rate → time-variant shaping
- trapezoidal weighting function by feedback capacitor flipping
- performs correlated double sampling (CDS)

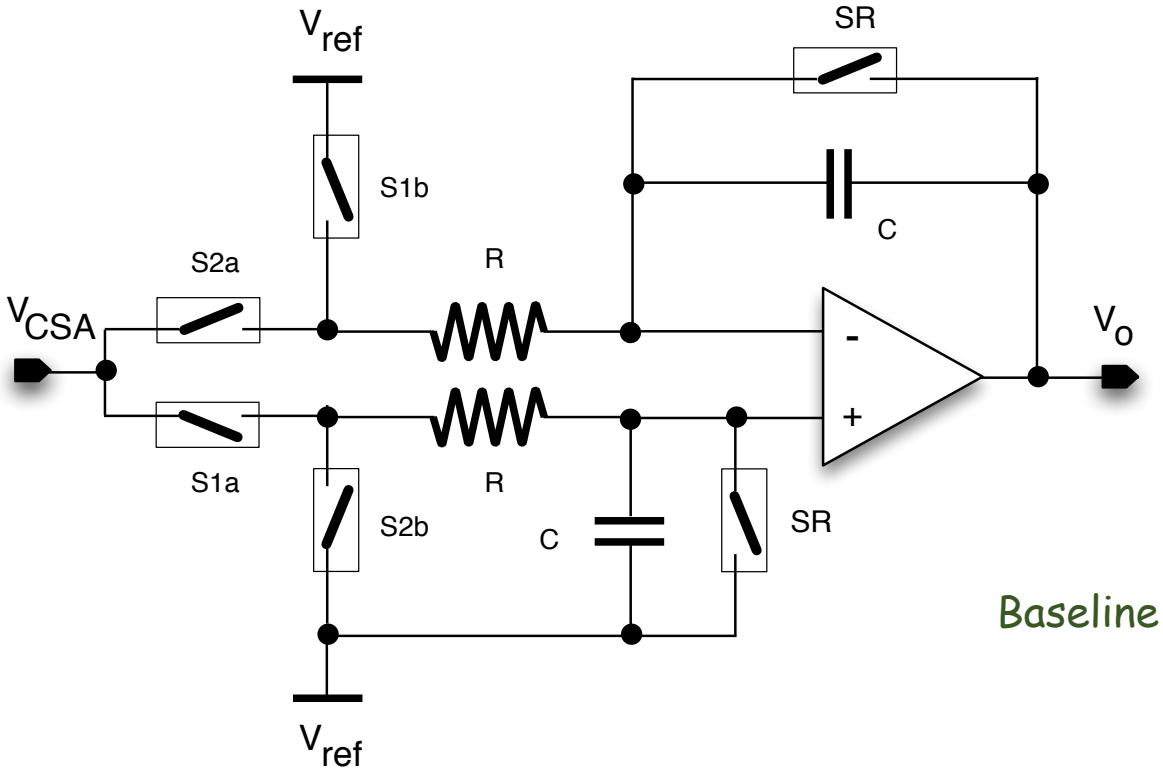
Charge sensitivity

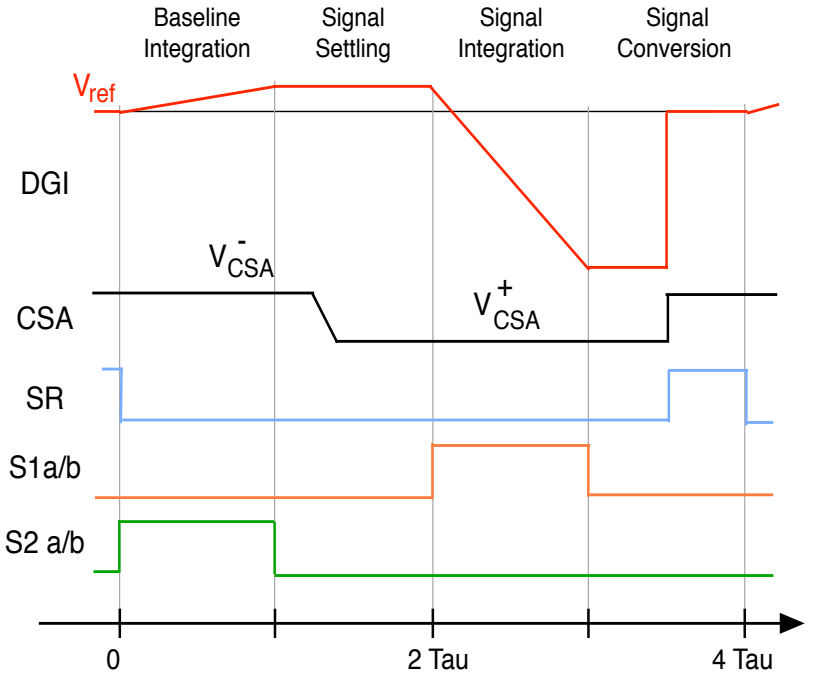
$$G_Q = \frac{V_{out}}{Q} = \frac{G_m \tau}{C_f C_F}$$



(*) L. Bombelli et al., "A fast current readout strategy for the XFEL DePFET detector", Nucl. Instr. and Methods, vol. A624, pp. 360-366, 2010

Differential gated integrator (DGI)





Baseline integration

$$V_o(t) = -\frac{t}{RC} V_A^- \Rightarrow V_o(\tau) = -\frac{\tau}{RC} V_A^-$$

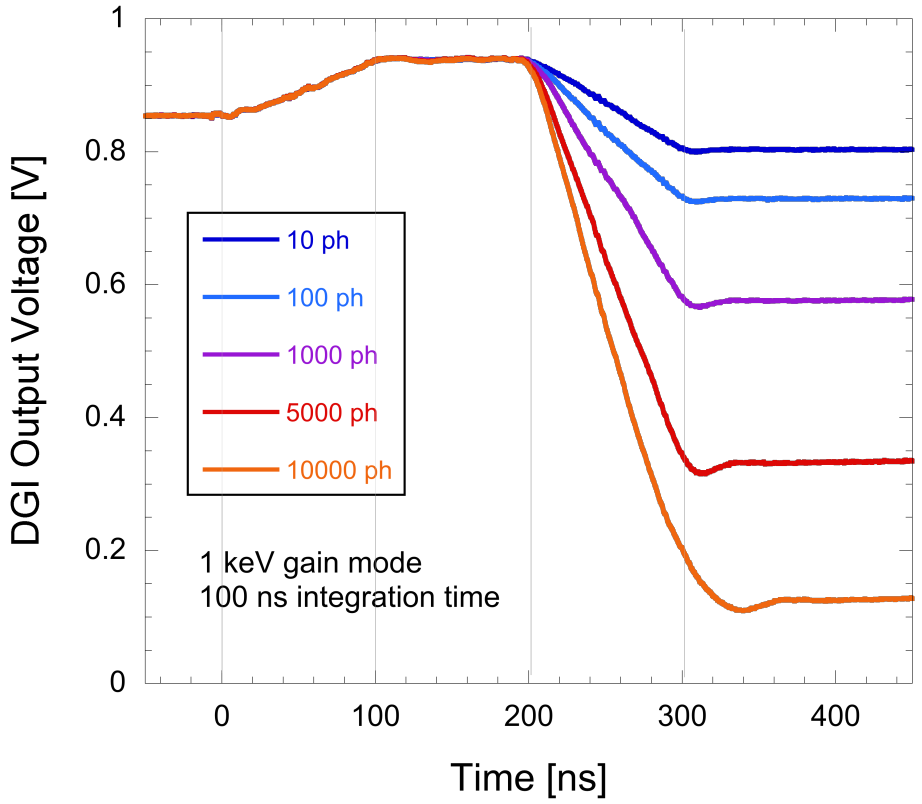
Signal integration

$$V_o(t) = V_o(2\tau) + \frac{t}{RC} V_A^+ \Rightarrow V_o(3\tau) = \frac{\tau}{RC}\left(V_A^+ - V_A^-\right)$$

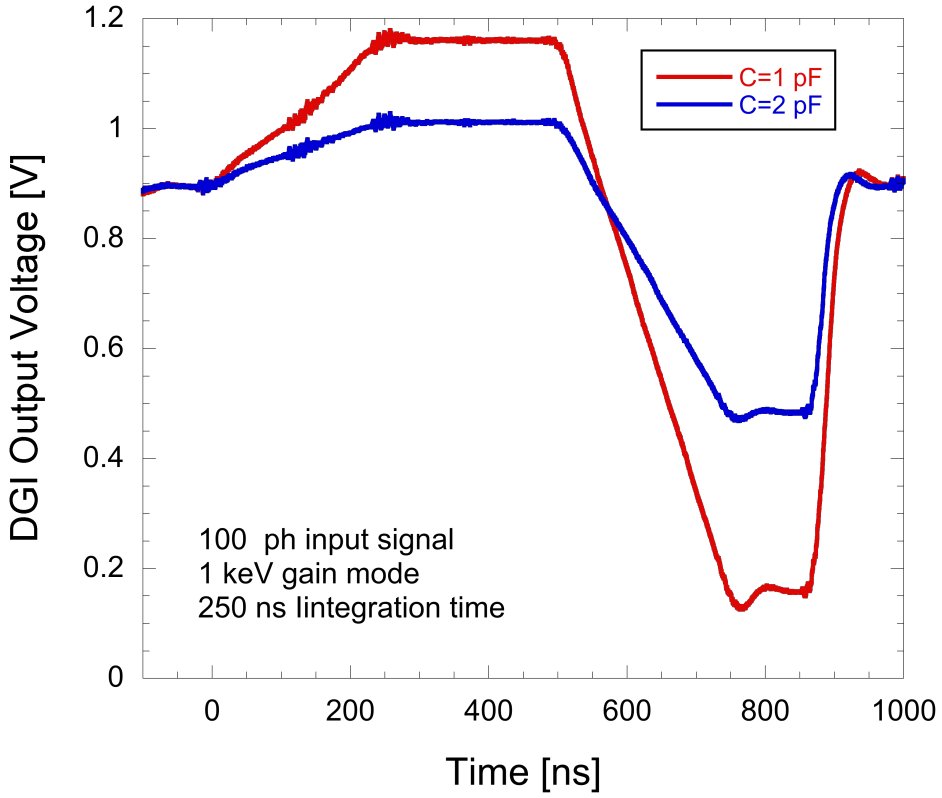
Charge sensitivity

$$G_Q = \frac{V_{out}}{Q} = \frac{\tau}{C_f RC}$$

DGI transient response



Response to a signal from 10 to 10000 photons at a 100 ns integration time



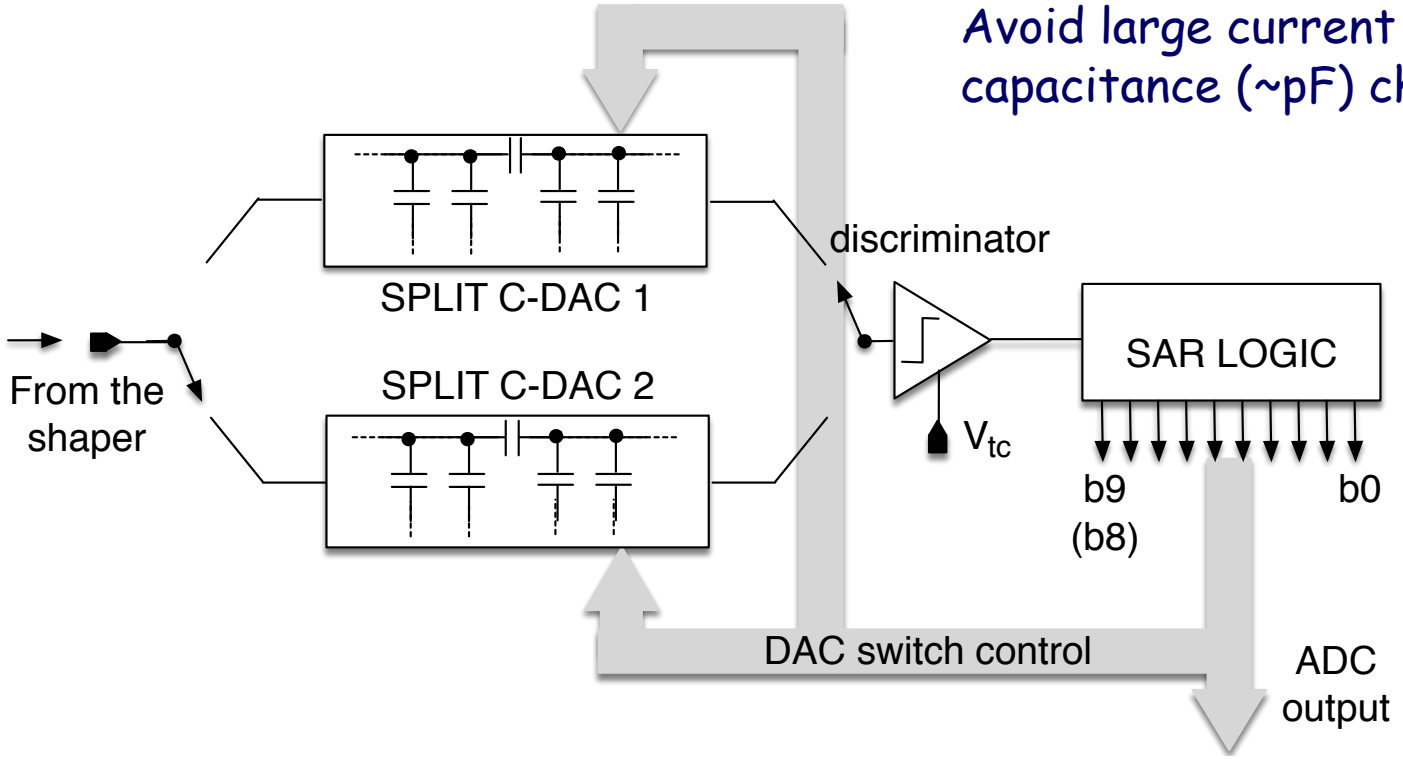
Response to a 100 photon input signal for different gain configurations at a 250 ns integration time

Time interleaved SAR ADC

Two split capacitive DACs in a time-interleaved structure; for each DAC

- pre-charge during one sampling period
- conversion during the subsequent period

No need for a dedicated stage for fast DAC charging

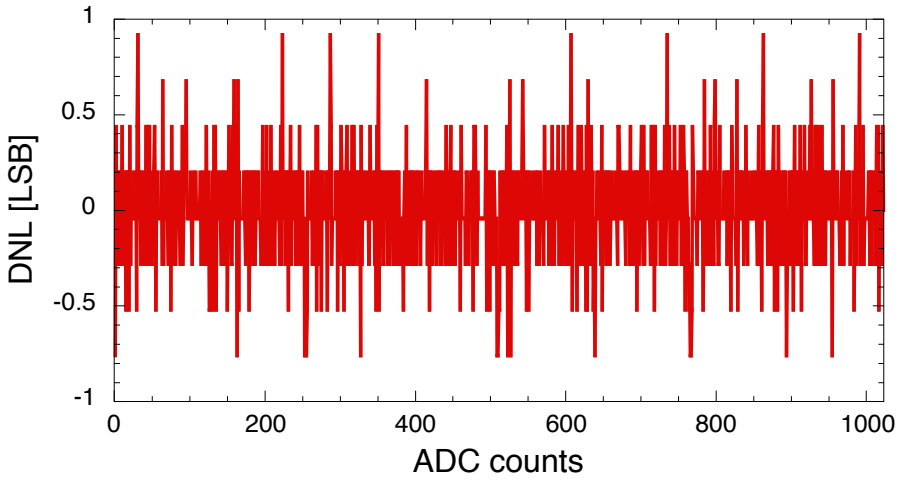


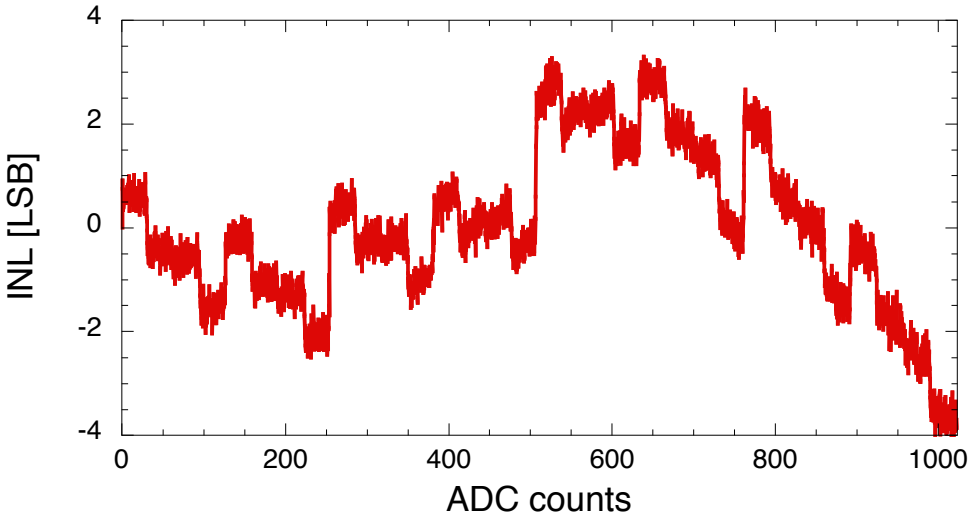
Avoid large current peaks due to fast capacitance (~pF) charge

Comparator based on a pre-amplification stage (to avoid kickback noise), a second gain stage and a latch

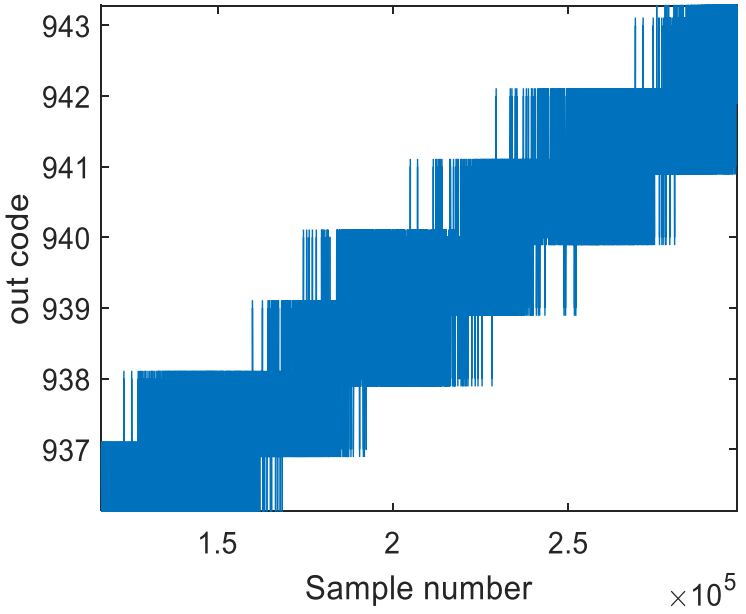
Time interleaved SAR ADC

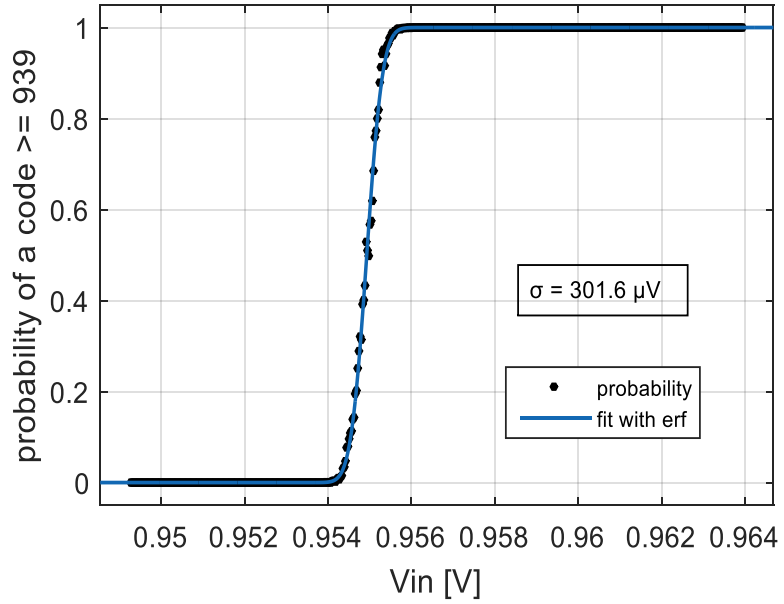
- Sample rate: 5 MHz → Clock frequency = 5 MHz × 11 = 55 MHz
- Resolution: 2 ADC bins attributed to 1 ph in the linear region (first 10 ph)



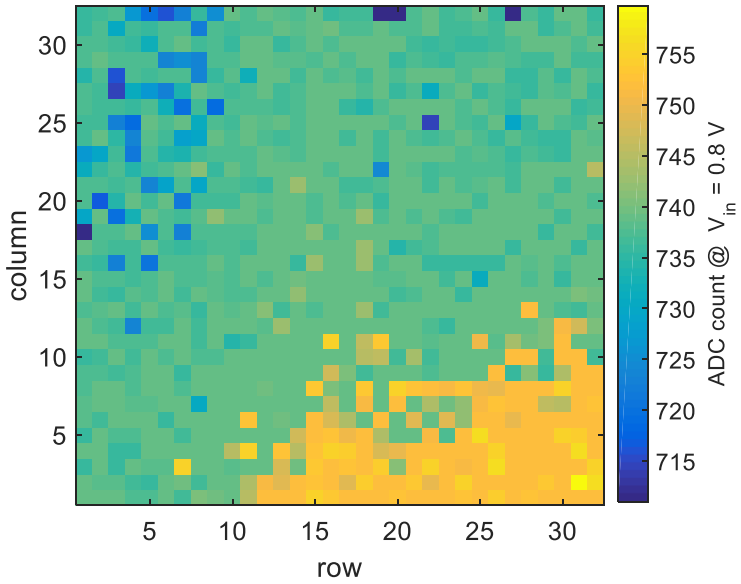


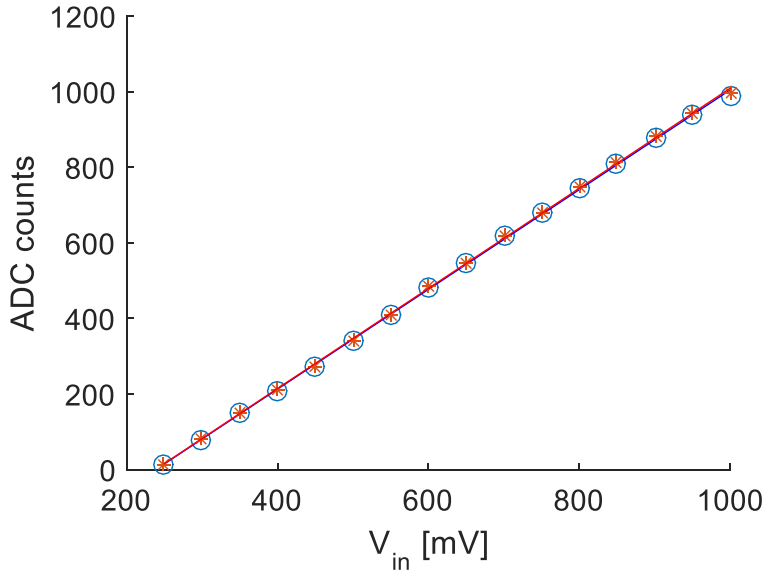
- 1.82 MHz sampling operation achieved, 10-bit conversion in 11 clock periods (TCLK =50 ns). Limitations due to the comparator cured in the PFM2 chip
- |DNL| < 1 LSB → no missing codes
- SNR = 55.84 dB compatible with 300 uV rms noise referred to the ADC input
- ENOB = 9





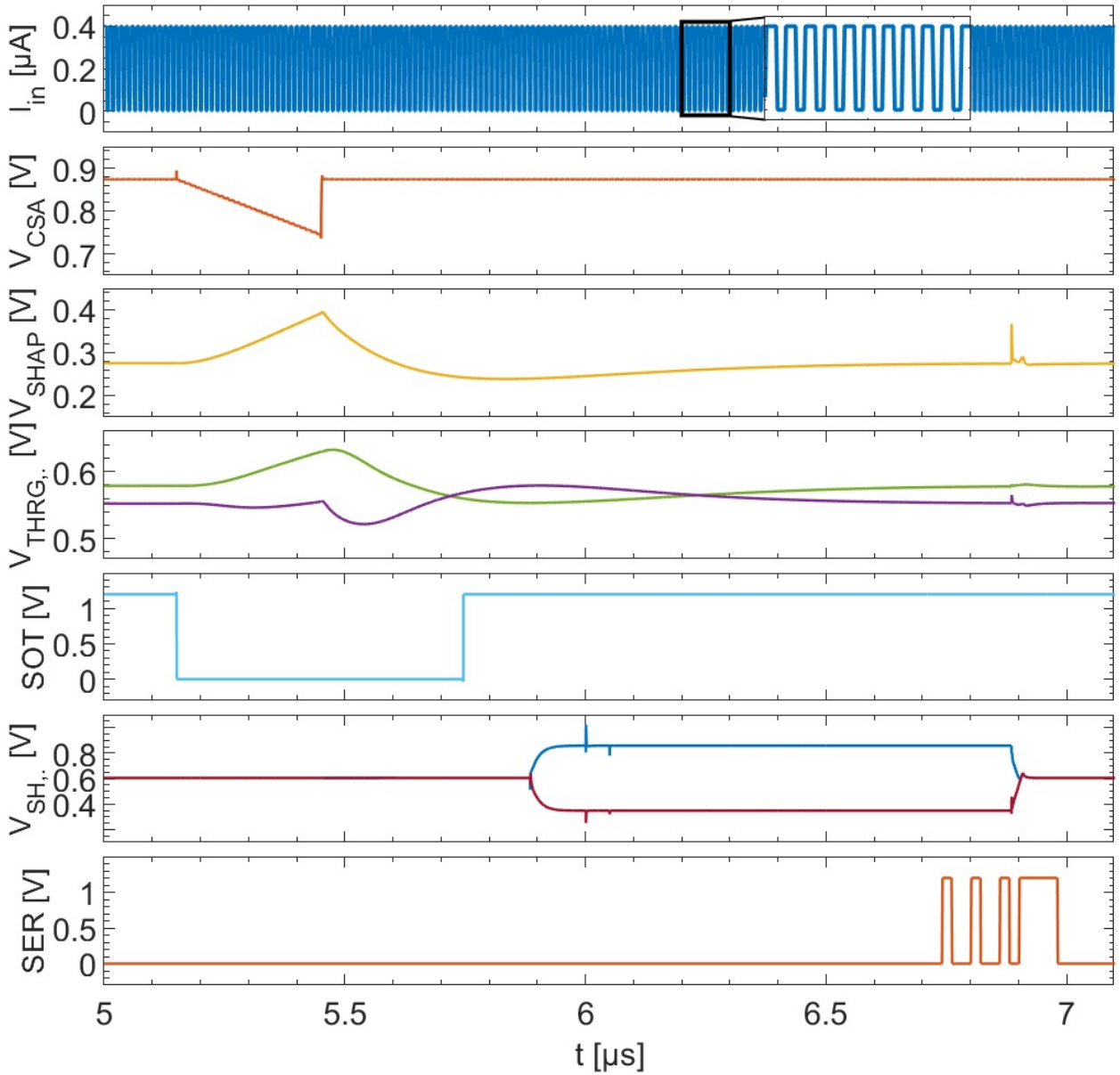
Time interleaved SAR ADC



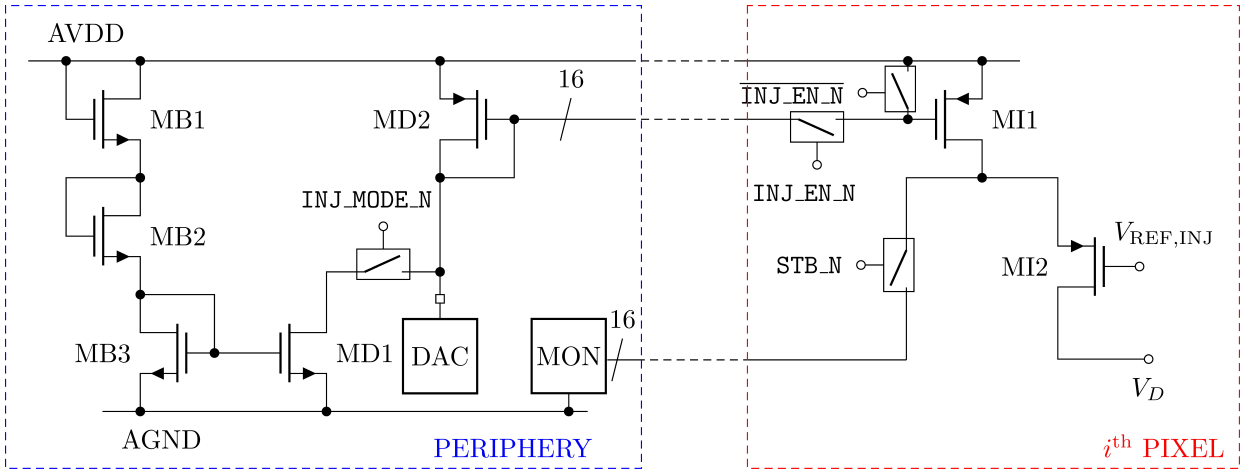


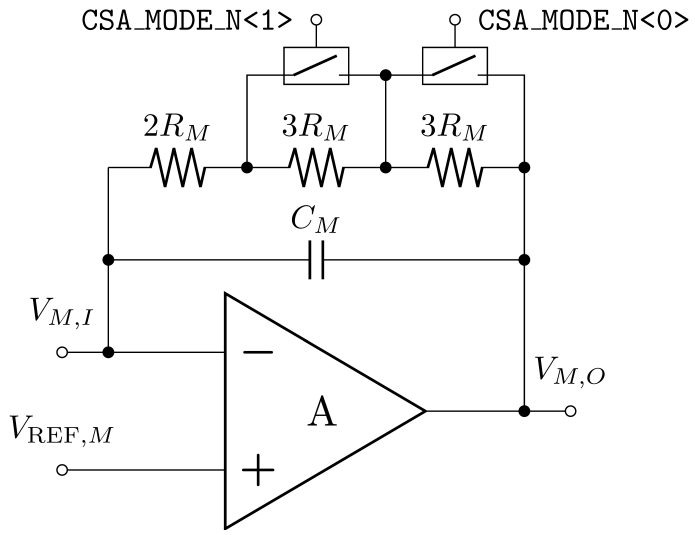
f_s = 4.5 MHz

FALCON - Full channel transient



Injection circuit & monitor

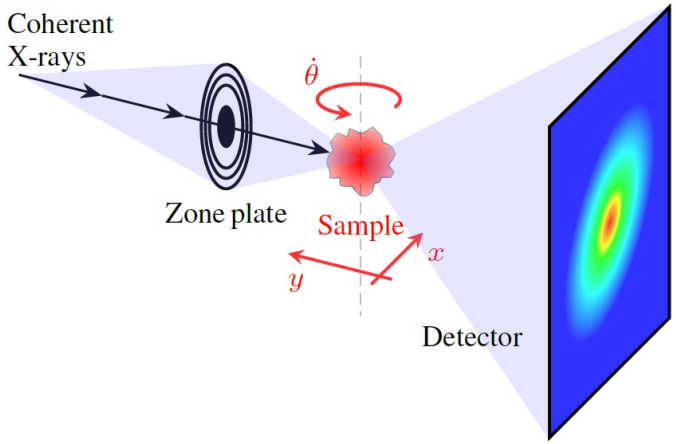




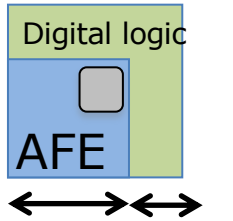
- A **DAC sets the amplitude** of the pulses.
- The **shape of the pulse train is set by the strobe** (STB) signal, which steers the injected charge from a **monitor (MON) branch** to the CSA and back.
- The switch on the CSA input branch is set to a **fixed voltage to avoid clock feedthrough** on the CSA.
- A **constant bias branch is added to improve linearity** for low DAC currents in continuous train mode.
- The circuit is **split between periphery and pixel** to minimise power consumption on pixel and maximise DAC and monitor performance, but only a single pixel of those connected can be injected at a time.
- The **MON is realized through a TIA** and keeps the steering circuit balanced.
- The MON has **multiple modes to adapt to the input charge injected**, accordingly to the CSA mode.

FALCON Project for Ptychography applications

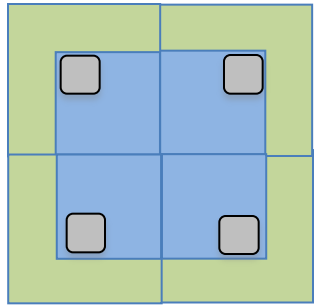
- Micro-Computed Tomography (µCT) is limited to micrometre-resolution.
- New techniques, such as **X-ray ptychography**, can achieve nanometre-resolution:
  - A **coherent X-ray beam is scanned across a specimen** of interest, point by point:
    - Step-scan ptychography.
    - **Fly-scan ptychography.**
  - At each position a **diffraction pattern is generated and a modest-sized frame is acquired at very high rate**.
  - **Iterative phasing techniques** are applied to the obtained diffraction patterns to achieve a **super-resolution beyond lens limits**.



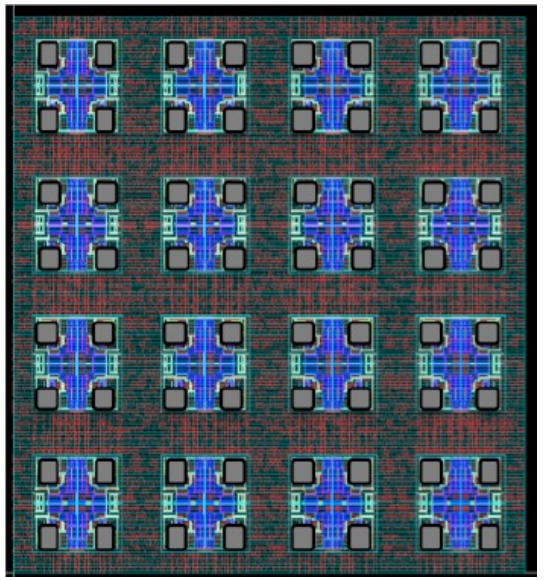
RD53 chip floorplan



Pixel

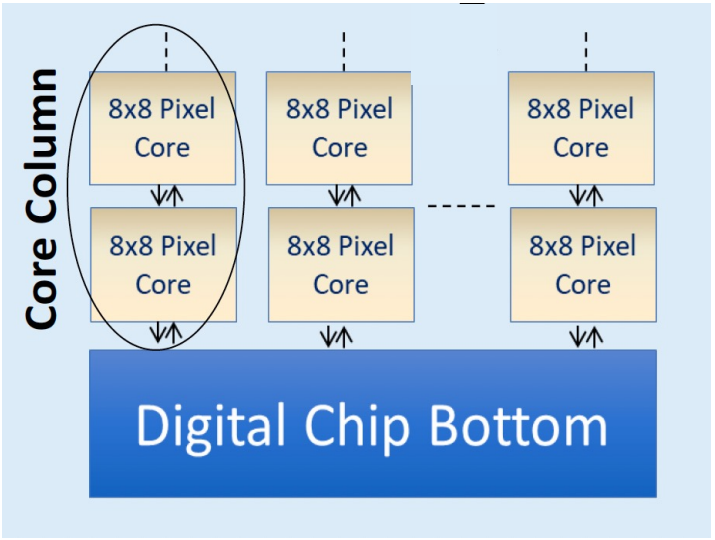


Quad

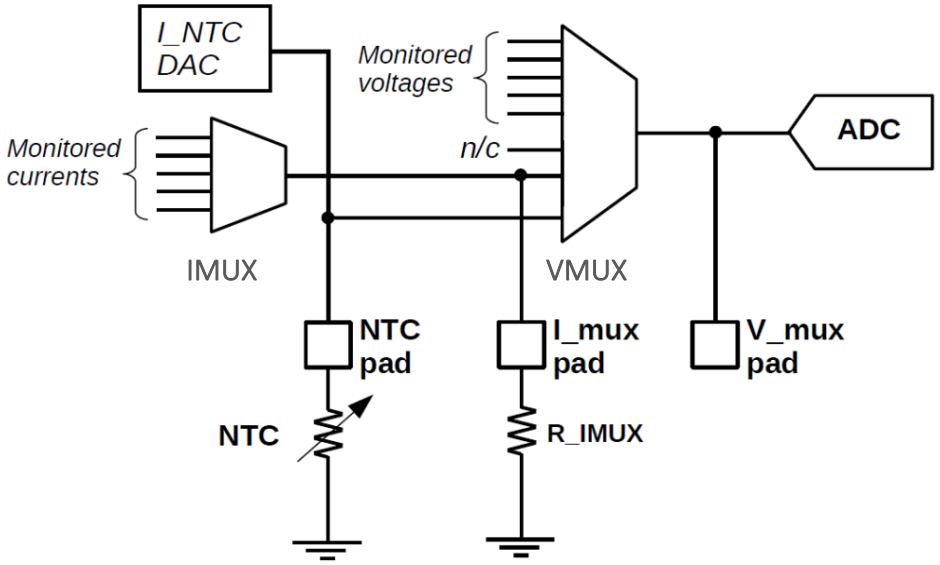


Core

- **Isolation strategy**: two different DNWs for analog and digital
- DNW-isolated **analog 'islands'**:
  - Occasional PFETs using body NW for sub isolation
  - DNW shorted to VDDA
- DNW-isolated **digital 'sea'**:
  - DNW biased at VDDD
- **Global substrate** not used by supply or device bodies
- **Digital logic** synthesized for 8 x 8 pixels to form a pixel Core



Monitoring block



This blocks is exploited for the digitization of several sensitive parameters in the chip:

- Voltages or currents in different sections of the chip
- Temperature
- Total ionizing dose

The monitoring block includes:

- an analog **current multiplexer (IMUX)** followed by an analog **voltage multiplexer (VMUX)**
- a **12-bit ADC**