# Development of Front-End Electronics in 28 nm CMOS Technology

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Future Detectors for the European XFEL

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# Outline



- Introduction
- 28 nm CMOS technology (with a comparison with the 65 nm)
- Analog front-end building blocks
    - Charge sensitive amplifier gain stages
    - Feedback topologies
    - Threshold discriminators
- Flash-ADC based front-end
- Time-over-Threshold based front-end

# Bergamo/Pavia 28 nm activities in INFN projects



## Falaphel

- Development and integration of **Silicon Photonics** modulators with high speed, rad-hard **electronics in 28 nm**
  - INFN Padova, Pavia, Pisa, Scuola Superiore S. Anna di Pisa, UniPisa, UniMilano. (P.I. Fabrizio Palla)

## IGNITE

INFN Ground-up iNITiative for μElectronics developments

- Develop a **detector-grade ASIC** (≈1-2 $cm^2$) in CMOS 28 nm technology, coupled to a Silicon Photonics integrated device for high-bandwidth data communications (4D tracking, rad-hard, low threshold operation,…)
- Establish an operative and coordinated network for the **exchange of competences** at a national level and for a **common R&D strategy** in microelectronics
  - INFN Bari, Bologna; Cagliari, Firenze, Genova, LNF, Milano, Milano Bicocca, Padova, Perugia, Pavia, Pisa, Trento, Torino (P.I. Adriano Lai)

## PiHEX Project

- Starting at the end of Sept 2023, and funded by the Italian Ministry of University and Research, focused on the design and radiation hardness qualification of **analog front-end channels** for **pixel sensors** (both for high energy physics and photon science applications) **in a 28 nm CMOS technology**

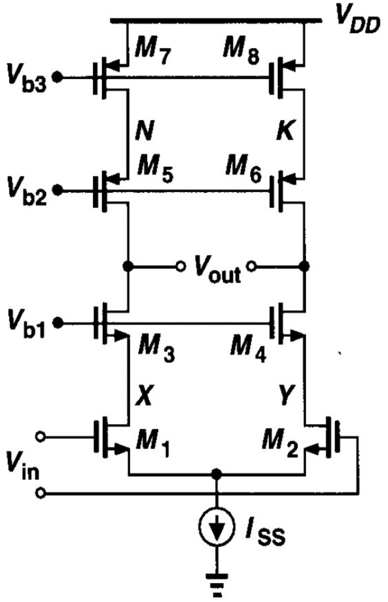
# The 28 nm CMOS technology



- The 28 nm is the major commercial successor of the 65 nm node (used for the design of RD53 chips). It is interesting to study and compare the main **static/noise performance** parameters

- **The 28 nm process**
  - Minimum nominal gate length 30 nm
  - Minimum nominal gate pitch 130 nm
  - Different technology flavours
    - Low power versions, featuring low gate capacitance, low on-current, low leakage (for portable devices)
    - High performance versions, with high-k metal gate, high on-current , high leakage (higher speed, higher power consumption)
    - Building blocks described here are relevant to a *high performance* flavour

- **From 65 nm to 28 nm**
  - Reduced core supply voltage (from 1.2 V to 0.9 V)
  - Limited number of architectures that can be exploited in the design of gain stages
  - More dense digital functionalities
  - More (and complex) design rules (e.g. density requirements and physical design limits)

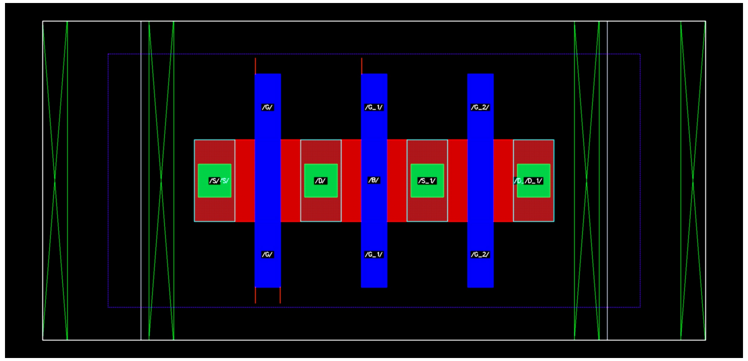



Razavi, Design of Analog CMOS Integrated Circuits

# Layout in 28 nm CMOS



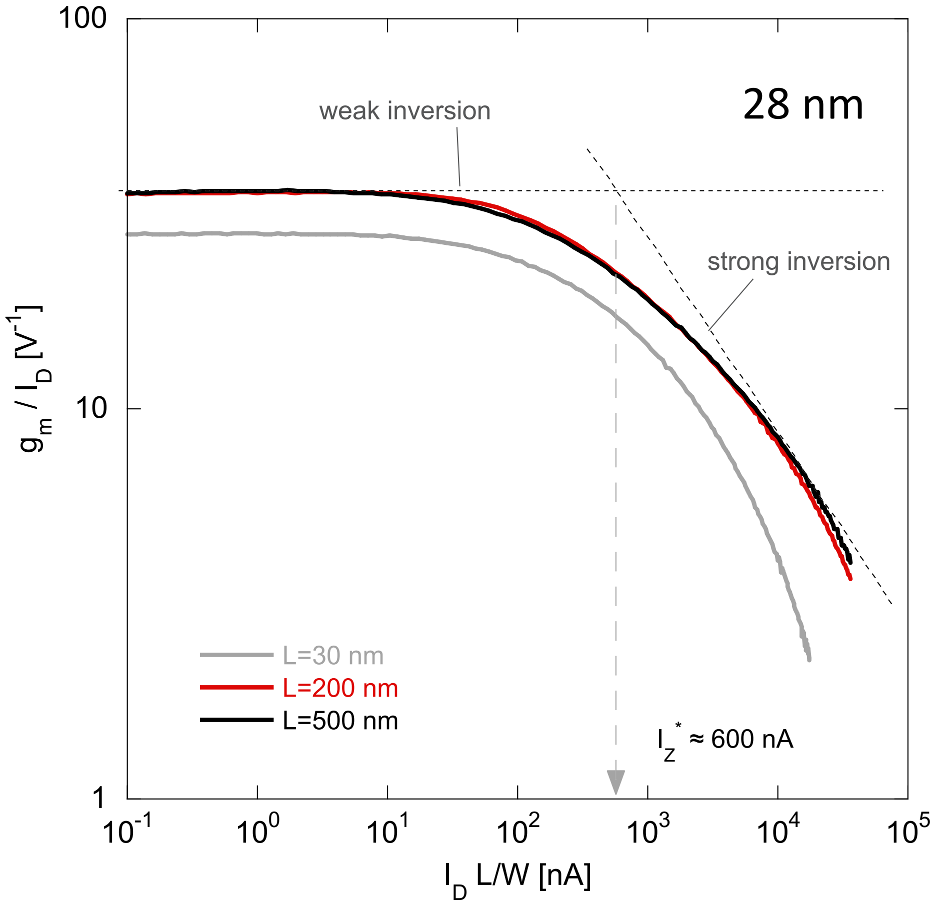
- Uniform **gate orientation** across the whole wafer
- Devices/circuits **rotation** is strictly prohibited
- Two **dummy gates** per side
- **Main restrictions**:
  - maximum transistor width (3 μm)
  - maximum transistor length (1 μm)
  - straight vertical gates (no *L-shaped* gates)

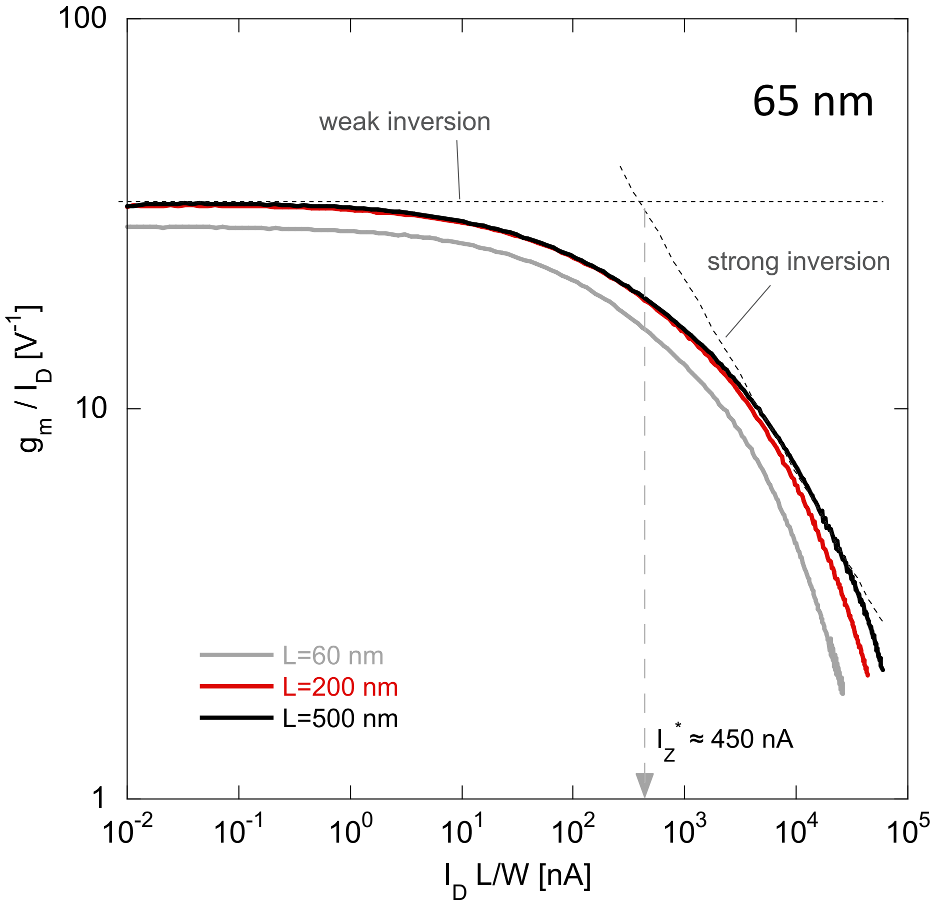


A comprehensive introduction to the 28 nm technology from V. Liberali (UniMI) can be found at https://agenda.infn.it/event/14974/contributions/27694/attachments/19786/22424/TimeSPOT_28nm_intro.pdf

# Transconductance efficiency






- Simulation results for regular threshold NMOS (W = 3 µm)
- $I_Z^*$ sets the boundary between weak and strong inversion
- Moderate increase in $I_Z^*$ for the 28 nm process

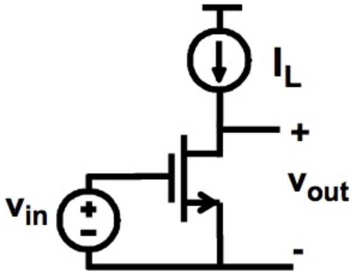
Inversion coefficient

$$I_{C0} = \frac{I_D}{I_Z^*} \frac{L}{W}$$

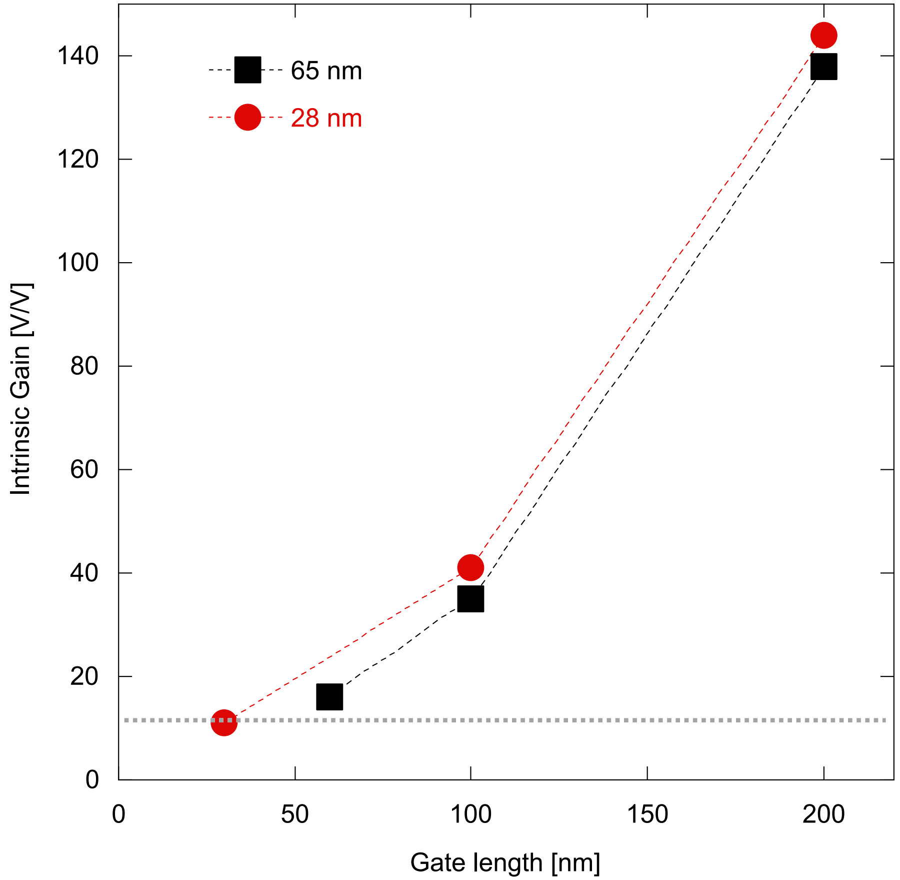
$I_{C0} > 10$ → strong inversion
$I_{C0} < 0.1$ → weak inversion

# Intrinsic gain






max gain achievable by one transistor




- Simulated **intrinsic gain** (gm/gds) as a function of channel length, for the 65 nm and 28 nm processes
- Data reported has been taken from **devices biased at $IC_0$ = 0.1**, where the device lies between the weak and moderate inversion
- **Limited variation** of the IG at the shortest channel length

# Mismatch



$$\sigma_{\Delta V_{TH}} = A_{\Delta V_{TH}} \cdot \frac{1}{\sqrt{WL}} = k \cdot \frac{t_{OX}}{\varepsilon_{OX}} \sqrt[4]{N} \cdot \frac{1}{\sqrt{WL}}$$

k is a scaling-independent constant

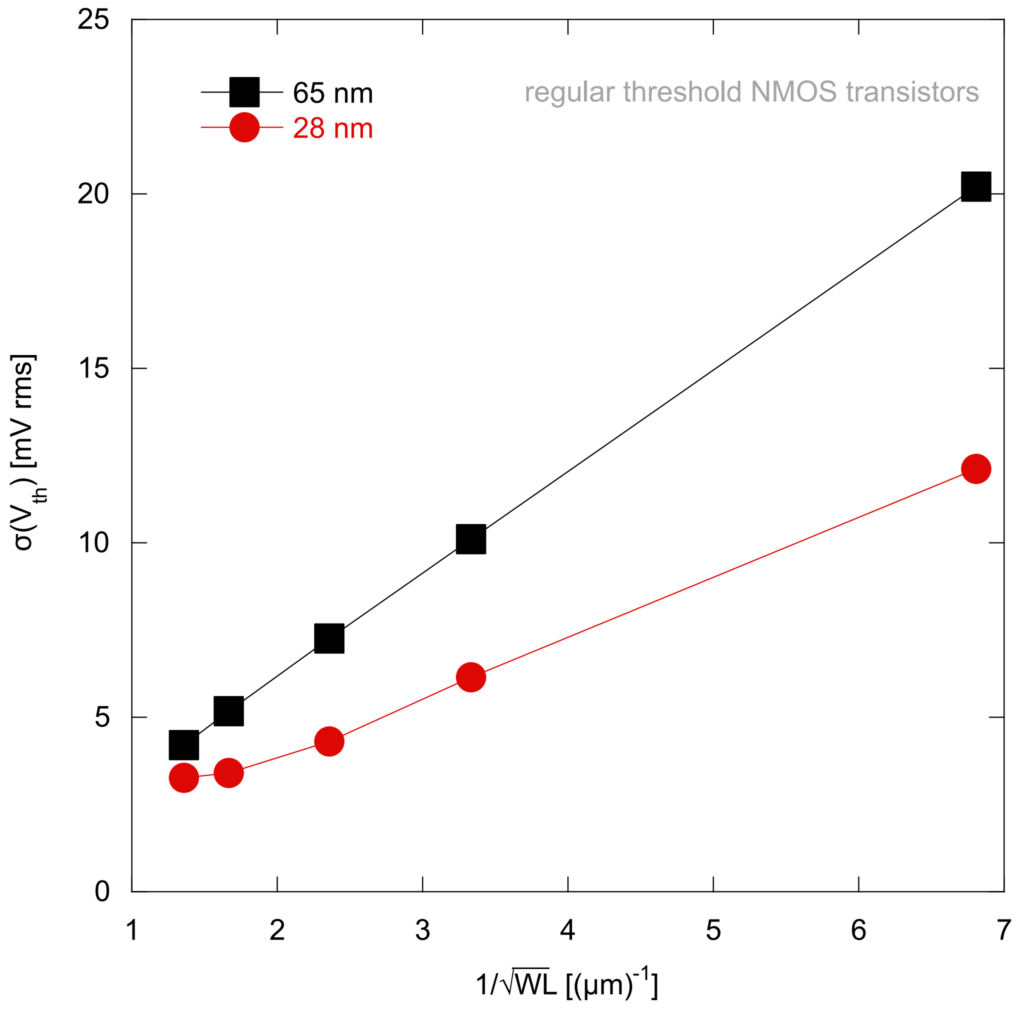
$t_{ox}$ is the gate oxide thickness

$\varepsilon_{ox}$ is the oxide dielectric constant

N is the dopant density in the transistor channel

- With scaling, $t_{ox}/\varepsilon_{ox}$ decreases and N increases (slower rate) → $A_{\Delta Vth}$ decreases

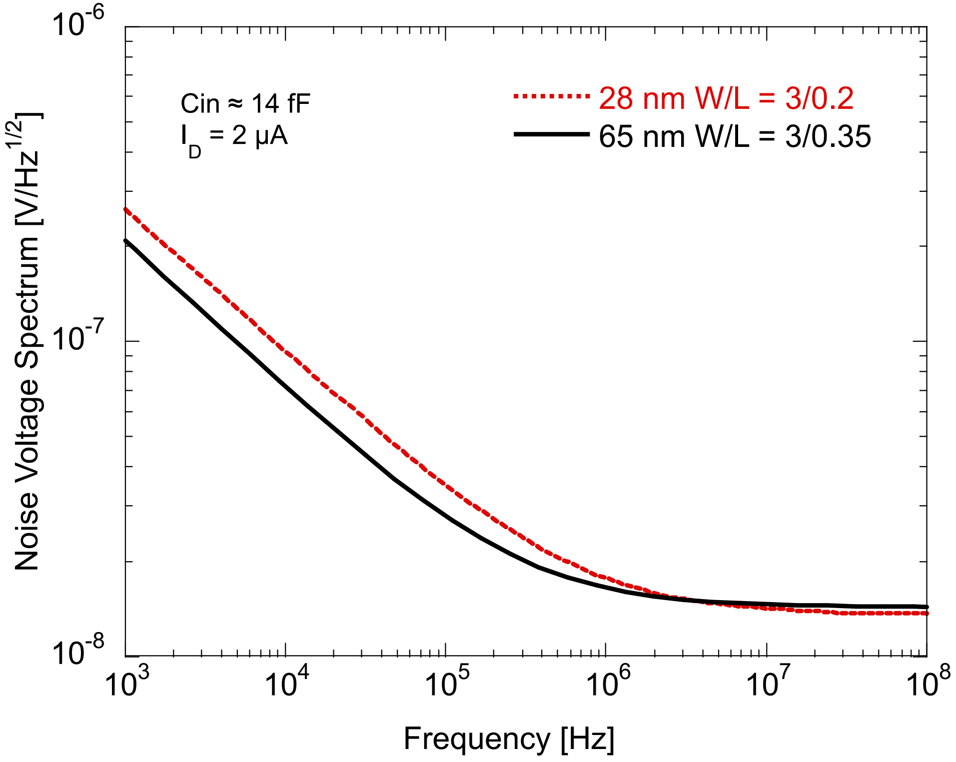
- This means that, for the **same device dimensions, scaling has (in principle) a beneficial impact** on transistor threshold voltage matching

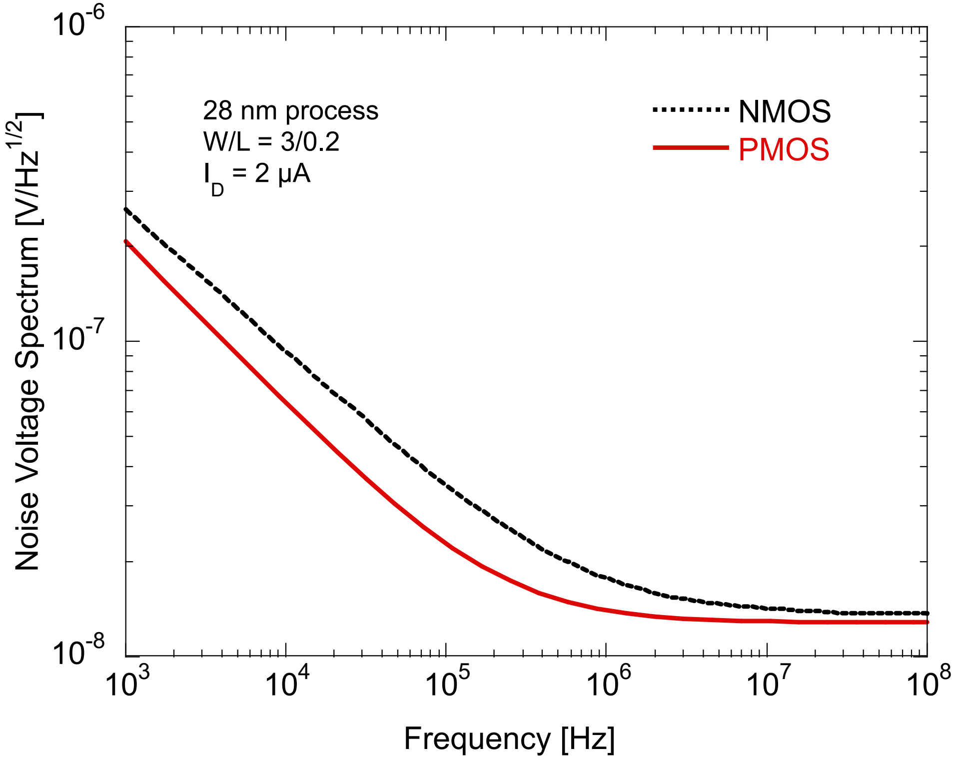



- This seems to be confirmed in the 65nm / 28nm comparison where the simulated **threshold voltage mismatch** is plotted for different gate areas (NMOS)

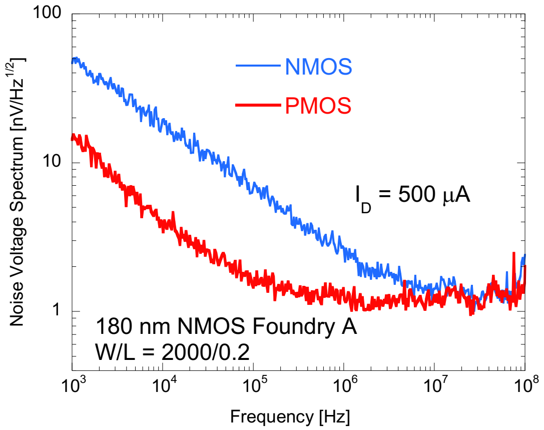
# Noise





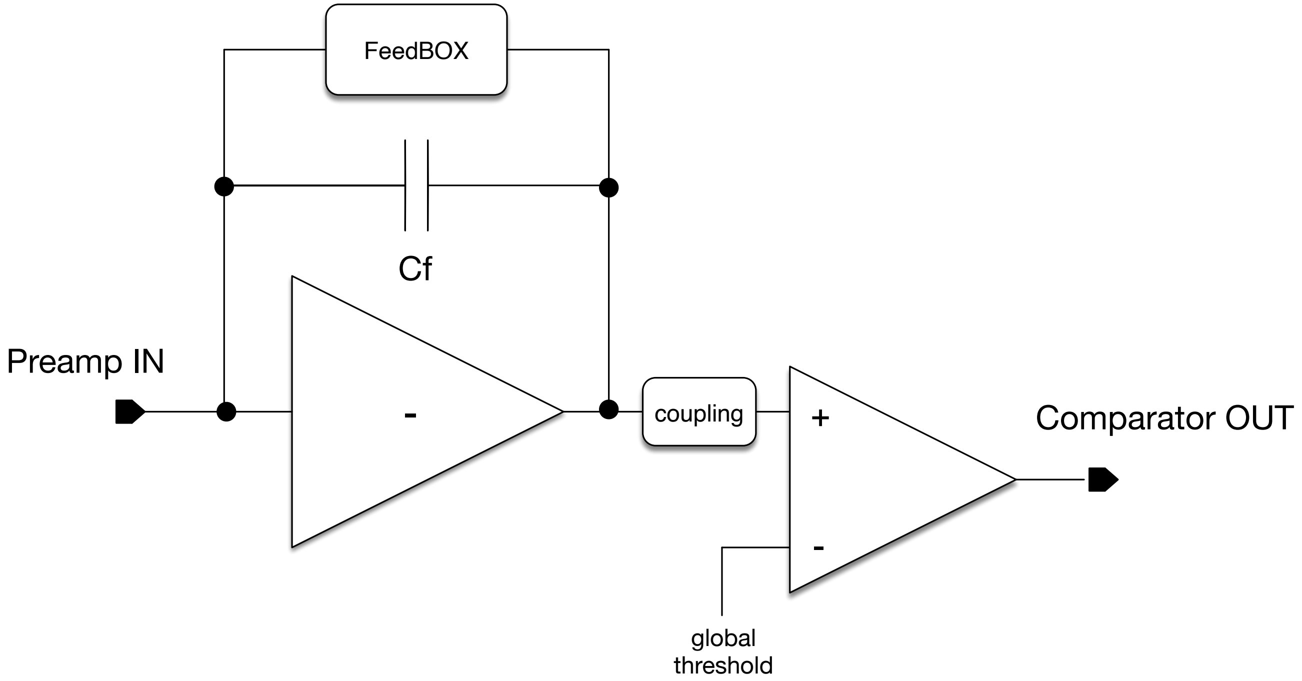




- Noise voltage spectrum for NMOS transistors in 65nm and 28 nm featuring (approximately) **the same $C_{OX}$WL** (~14 fF) → **similar noise performance** (slightly higher 1/f in the 28 nm)
- As for the 65 nm, also in the 28 nm process NMOS and PMOS devices feature similar 1/f noise behavior (in less scaled technologies PMOS has a lower 1/f noise than the NMOS), with a higher slope per P-channel devices



# Front-end design

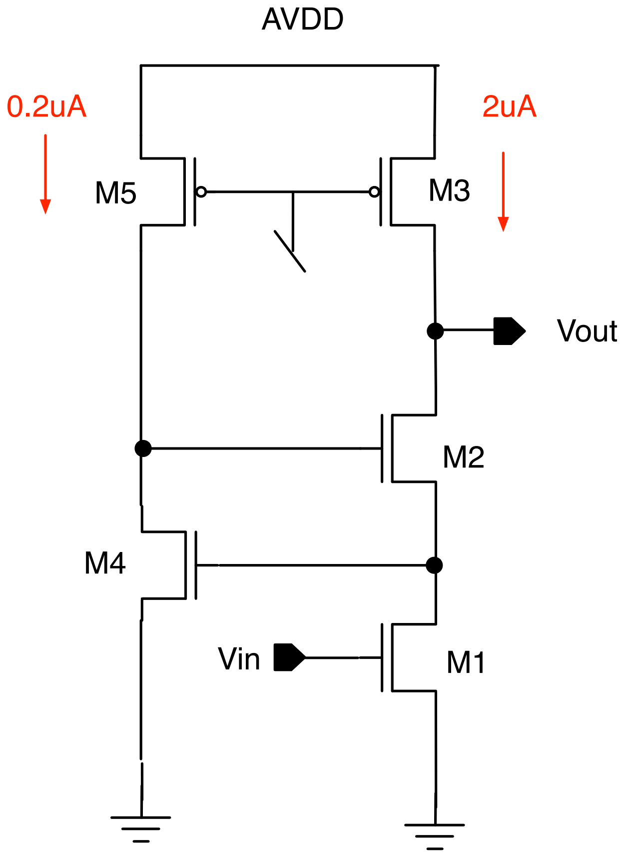


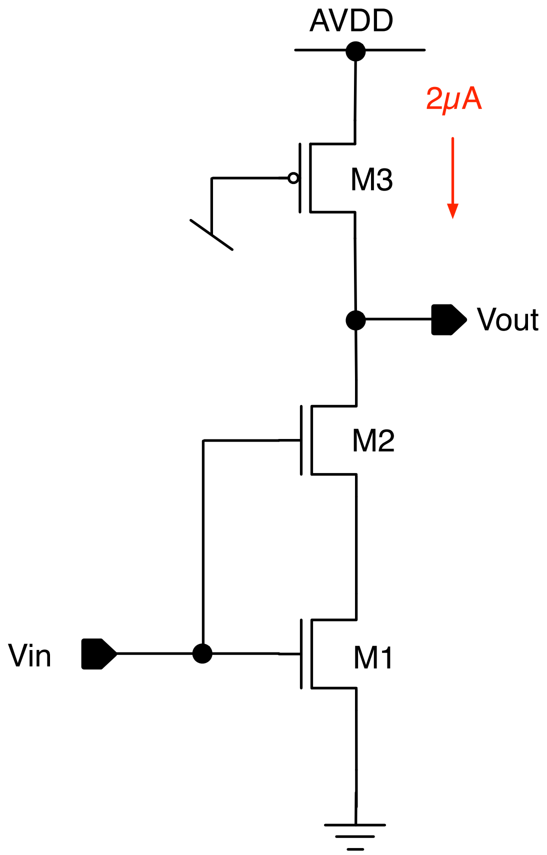



- The **basic building blocks** of a “classical” shaperless front-end for pixel detectors have been studied in 28 nm
  - Preamp gain stage
  - Preamp feedback network
  - Threshold discriminator

# Preamp gain stage





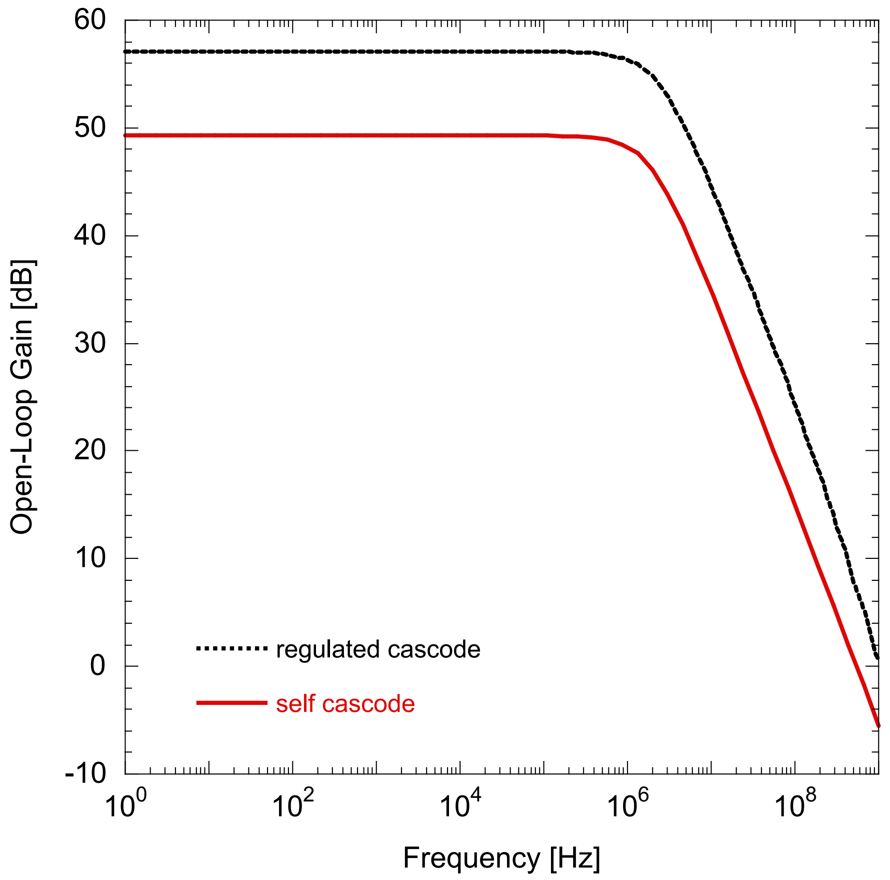



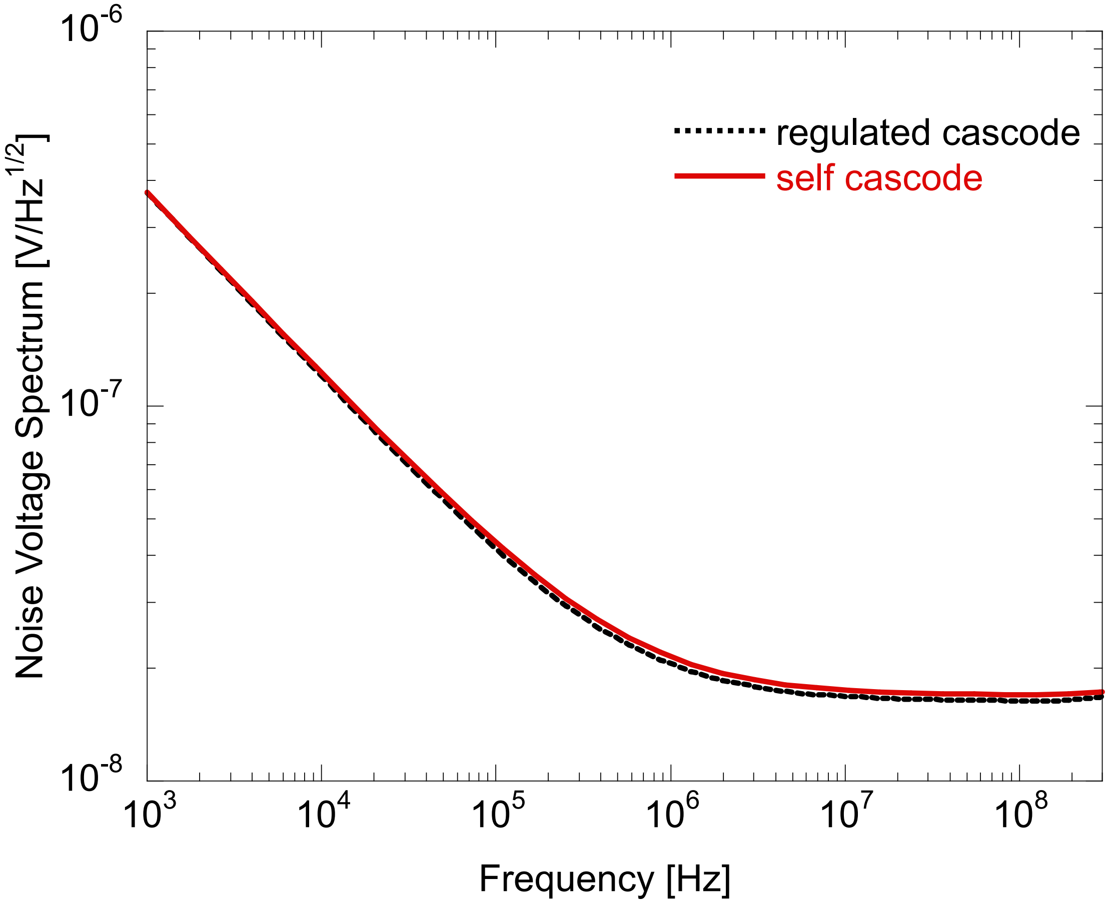

Regulated cascode

Self cascode

# Preamp gain stage: open loop gain and noise



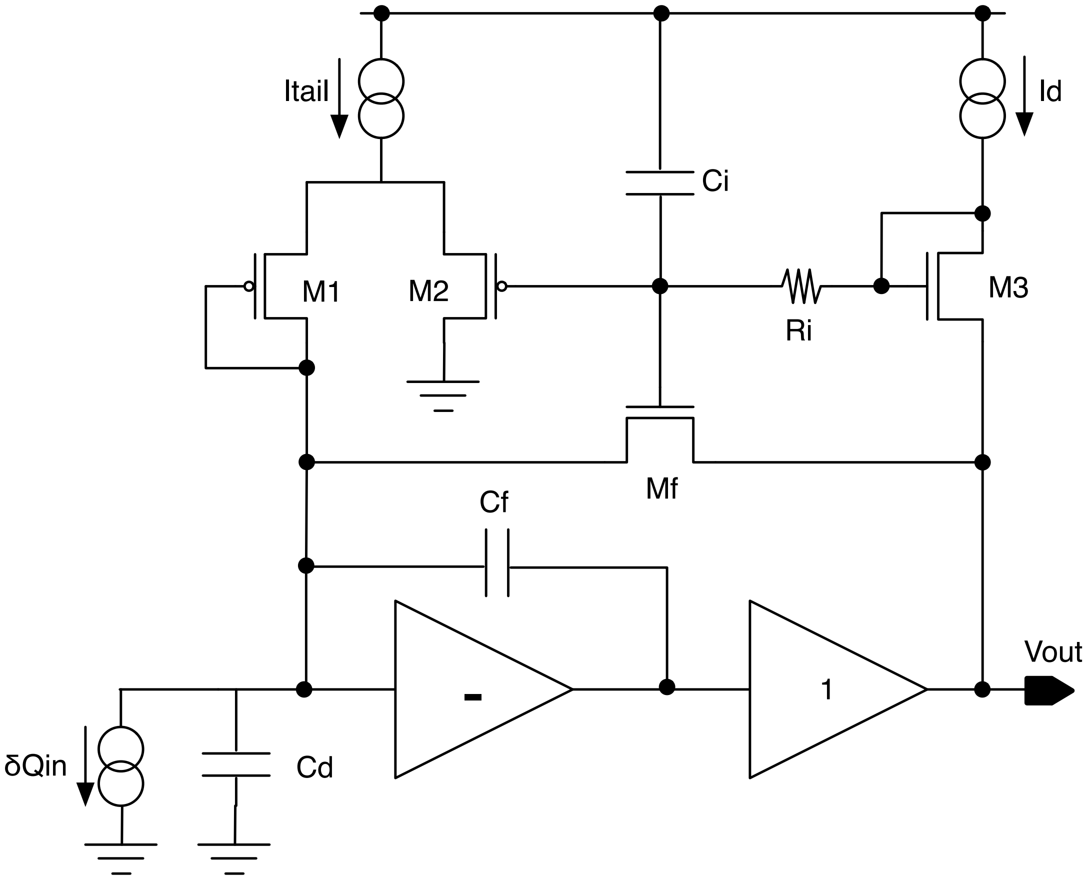



- Larger **low-frequency gain** (57 dB vs 50 dB) for the regulated cascode, thanks to the local feedback (M2-M4 transistors)
- Very **similar noise performance** (with channel thermal noise of M1 being the main contribution, followed by the contribution from the load transistor M3)

# Preamplifier feedback network (IFCP65-like version)

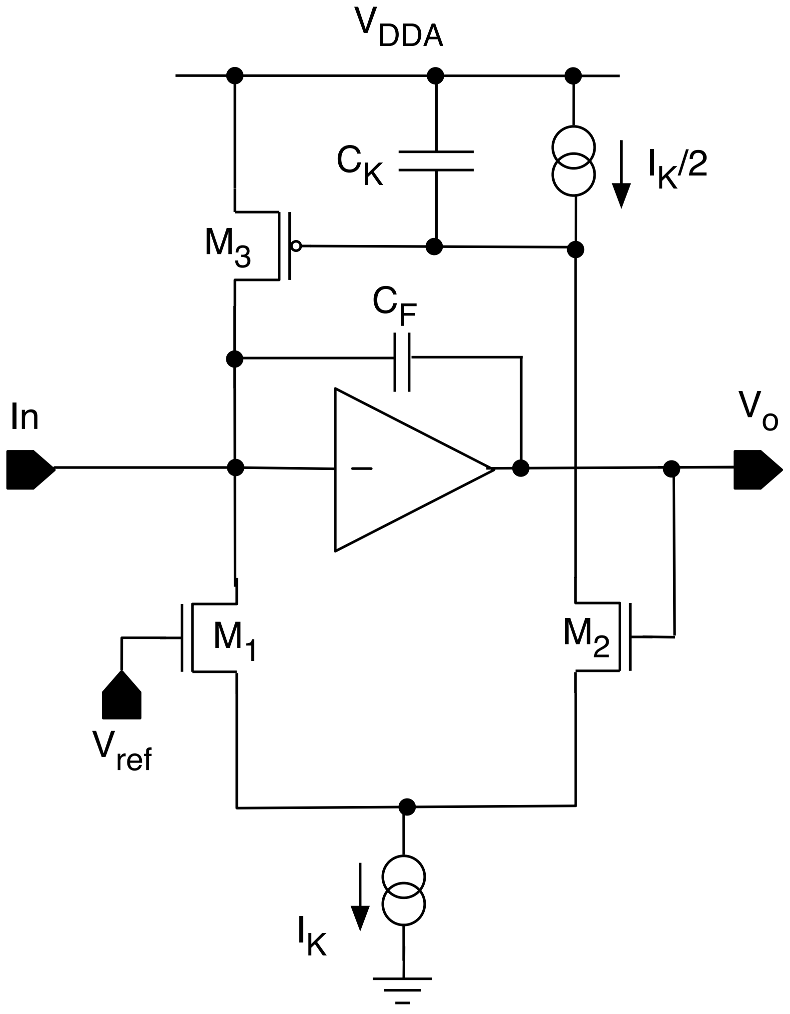





- Mf acts as a **1/gm resistor** for small signals
- **Constant current source** for large signals
- M1 provides a DC path for the detector **leakage current**
- Ri + Ci ensures **low frequency operation** of the leakage compensation circuit
- Suitable for **AC coupled** comparators (DC shift at the output due to detector leakage)

# Krummenacher feedback

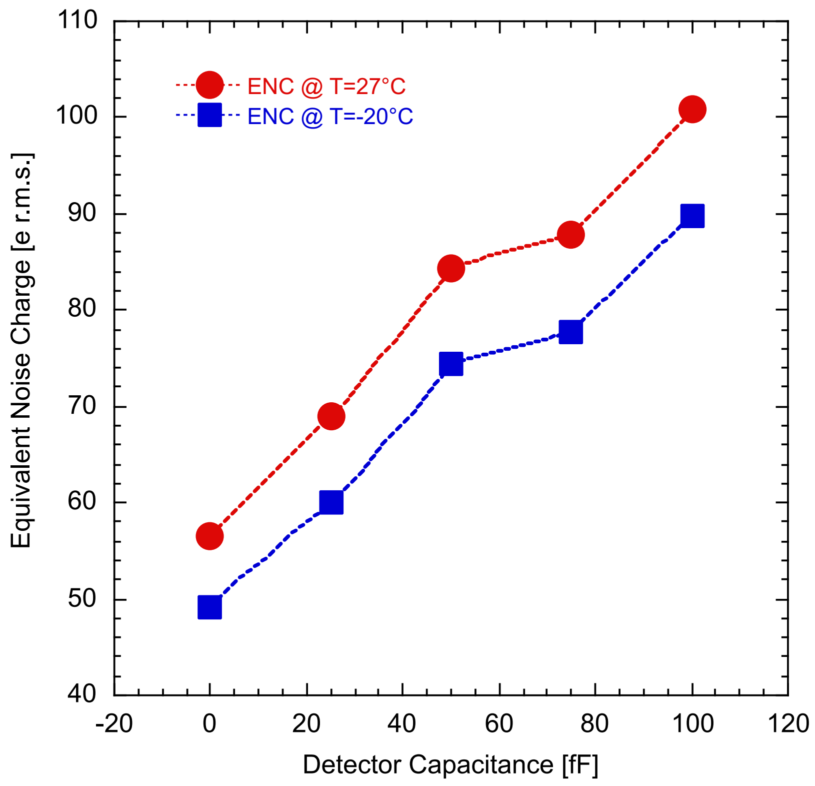


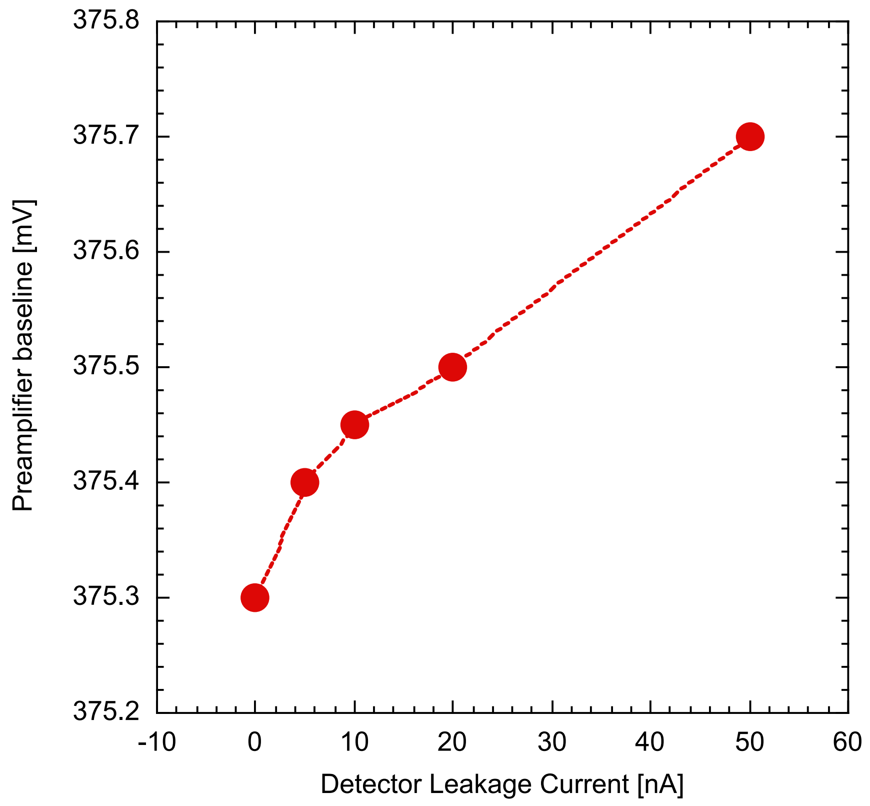



- Signal discharge
  - Equivalent **feedback resistor of 2/gm$_2$** for small signal
  - **Constant current discharge** ($I_K$/2) for large signals
- **Leakage current** through M3 transistor (slow feedback adjusts the potential at the gate of M3)
- Big $C_K$ is needed to ensure **stability**

# Krummenacher feedback



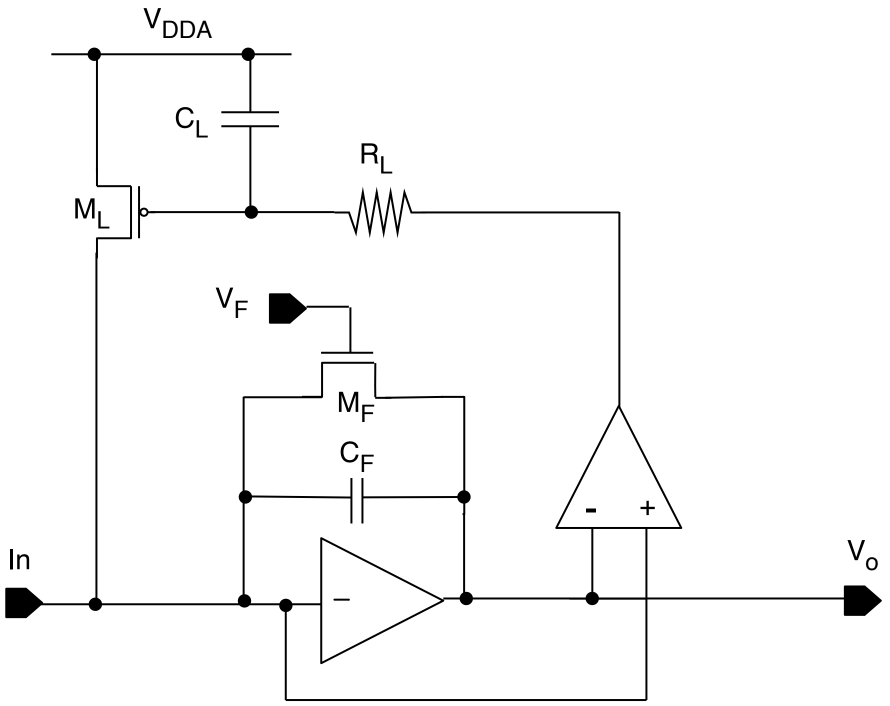


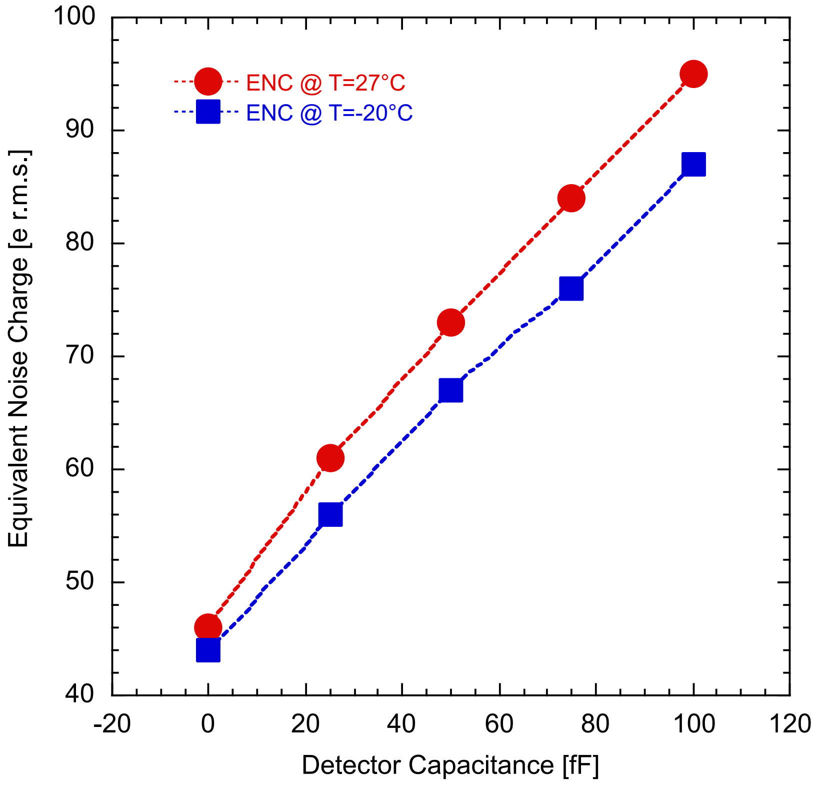




- **Equivalent noise charge** (ENC) smaller than 105 $e_{rms}$ for $C_{d,max}$ =100 fF
- **Leakage compensation** circuit works fine for detector current up to 50 nA (very stable DC output)

# Independent feedback networks



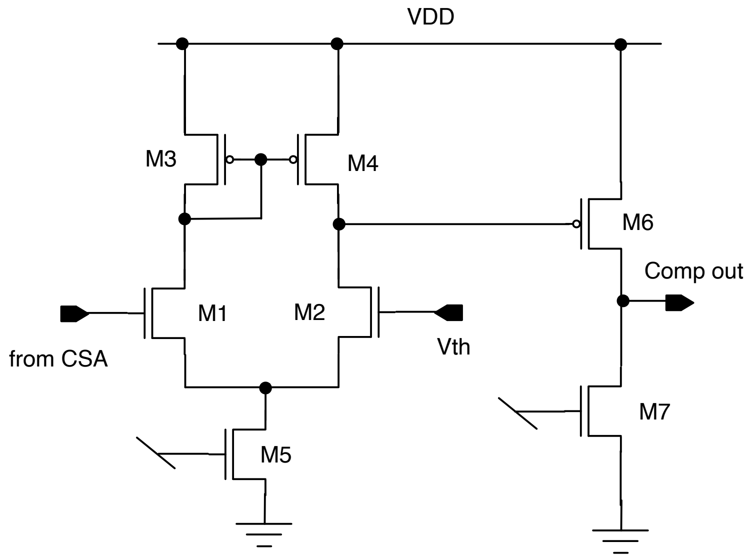


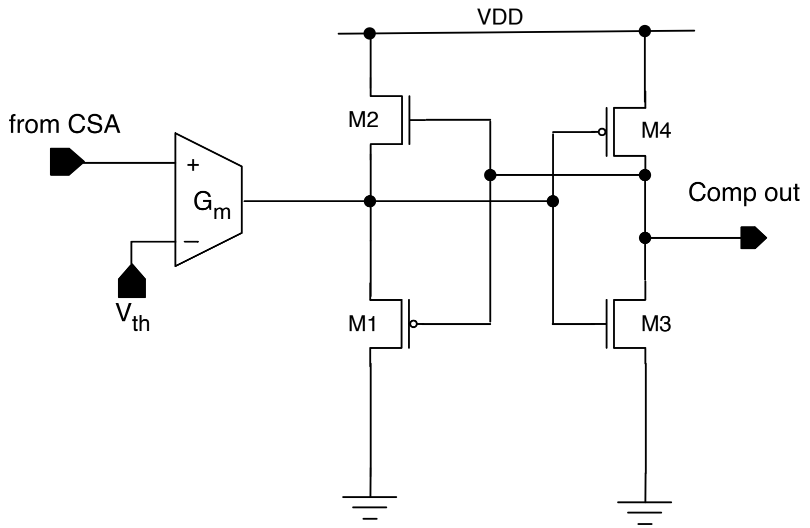




- Two independent feedbacks, one for the discharge of the feedback capacitor and the other for the detector leakage compensation.
- **Equivalent noise charge** smaller than 100 e rms for Cd,max =100 fF

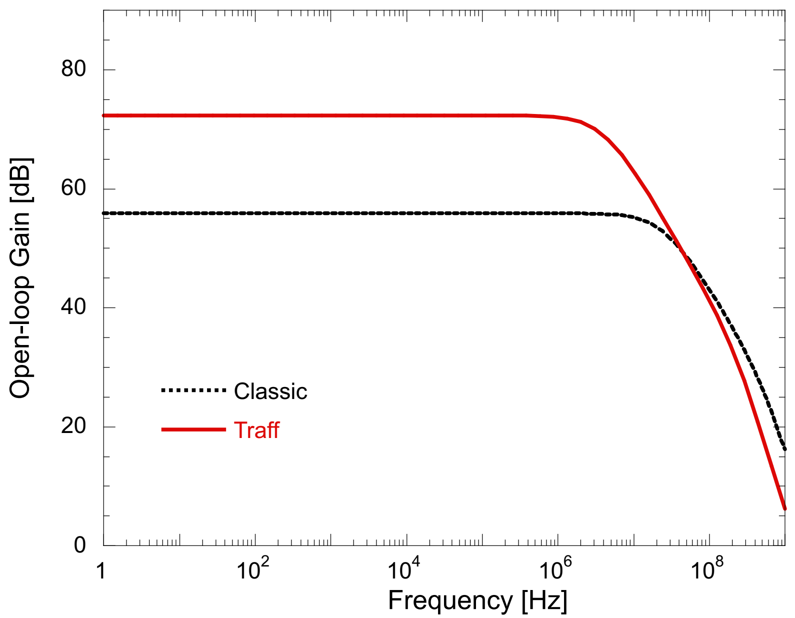
# Asynchronous comparators





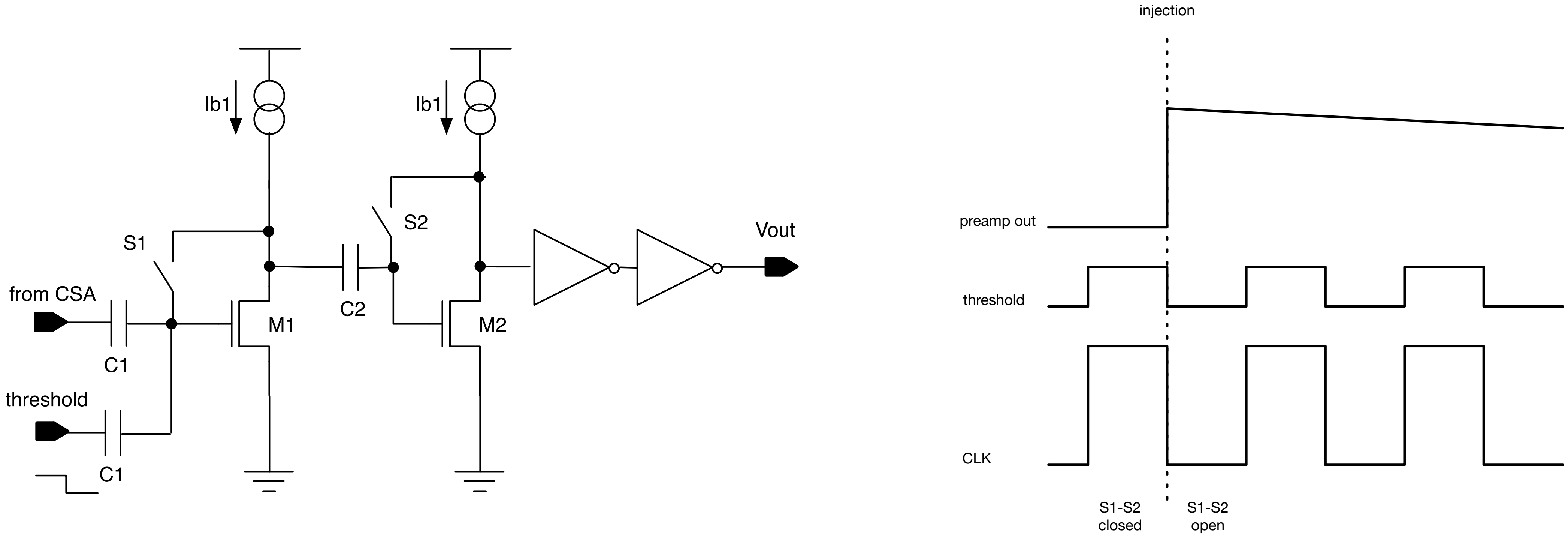




- Two **continuous-time comparator** architectures have been investigated
  - Classical differential pair with active load followed by a CS stage
  - Transconductane stage with transimpedance amplifier (Traff)
  - **Open-loop gain** and **time-walk** performance have been evaluated (slightly smaller time-walk from simulations for the Traff version)



# Clocked comparator






- Clocked, **auto-zeroed** comparator featuring low power consumption (700nW)
- Two phases operation: Reset phase (S1, S2 closed) and Comparison phase (S1, S2 open)
- Signal from CSA and threshold injected at the gate of the input transistor M1, **synchronous with CLK** (controlling S1 and S2)
- CSA signal larger than the threshold → positive going signal at M1 gate, amplified by two common source stages and fed to output inverters that consolidate the output logic
- Extremely **low threshold dispersion** (signal injected at the gate of one single transistor)

# Front-end specifications and design in 28 nm CMOS

- Developing **two analog front-end architectures**, to be integrated in a pixel readout cell
  - Analog cell area reduced with respect to current 65 nm designs, room for more complex pixel logic

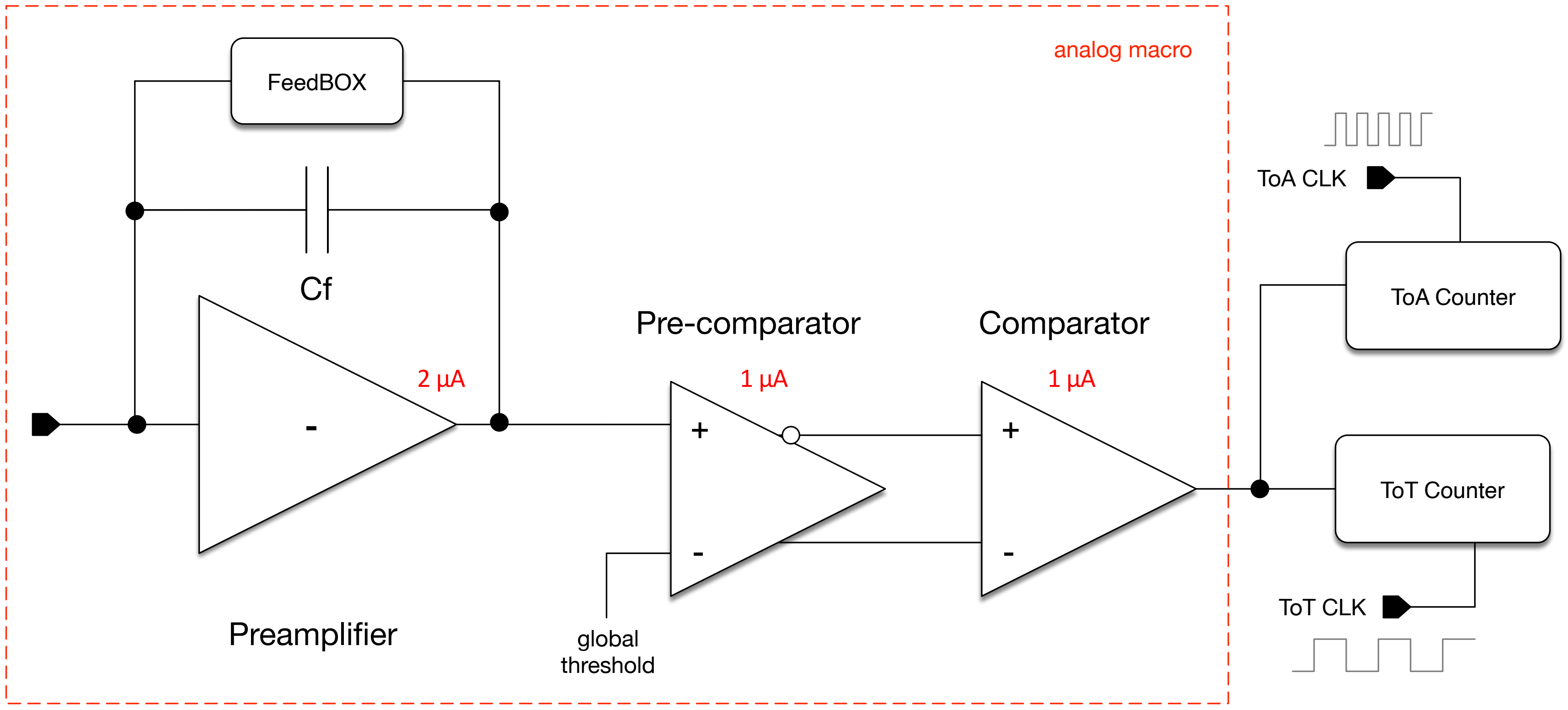
- **Time-over-Threshold (ToT)** based front-end → preamp + DC coupled comparator, with ToT A/D conversion of the signal + threshold tuning DAC
  - Specs mostly **derived from RD53, but targeting operation at a lower threshold (< 500 electrons)**

- **Flash ADC** based front-end → preamp + AC coupled bank of auto-zeroed comparators implementing a 2-bit flash A/D conversion
  - **Zero dead-time analog channel for high rate applications** (non negligible probability of having hits in adjacent bunch crossings)

# ToT-based front-end



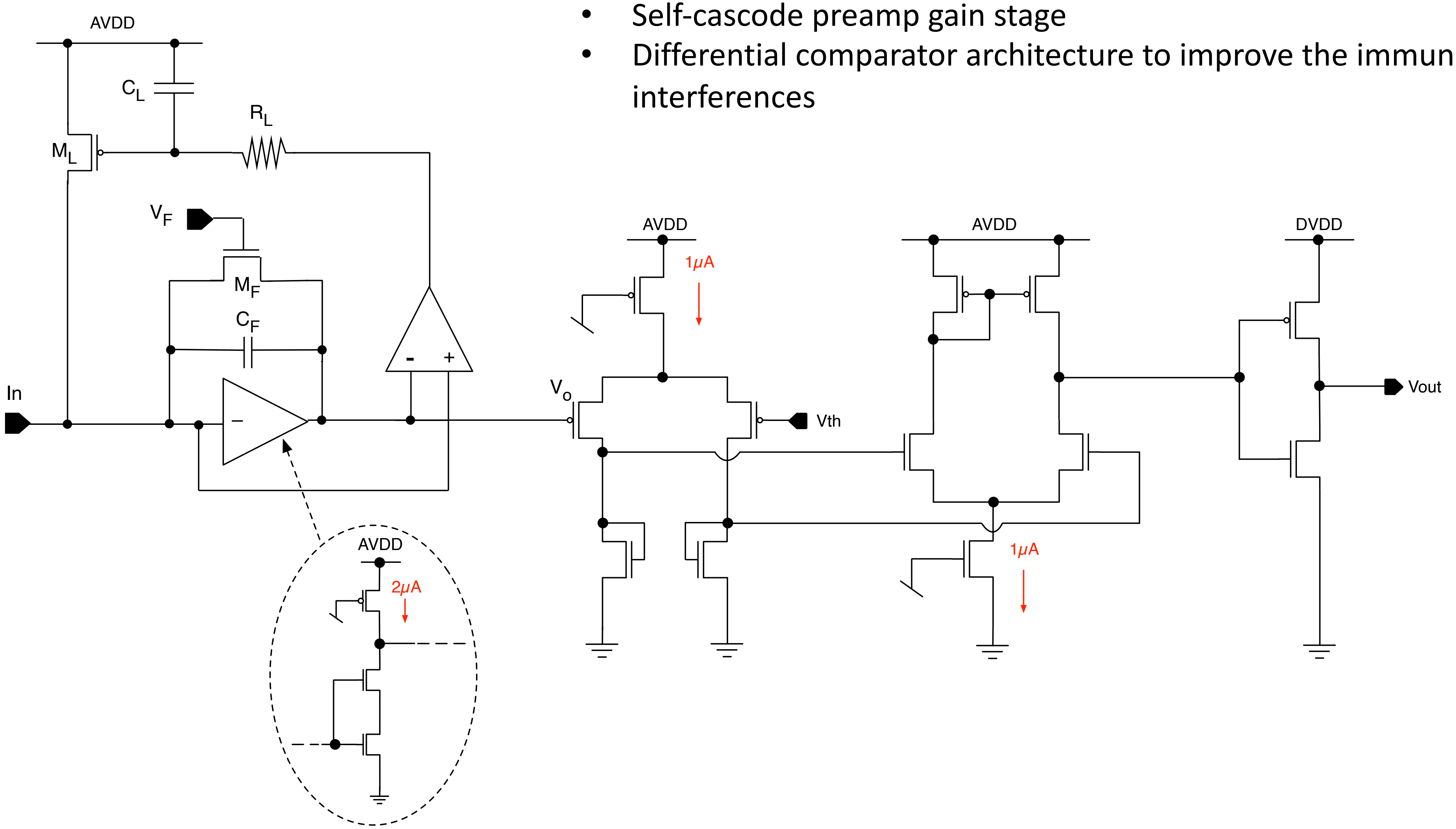
- **A front-end architecture (optimized for very low threshold)** is being investigated, based on **Time-over-Threshold (ToT)** → preamp + DC coupled comparator + **5/6-bits** threshold tuning DAC



# Analog processor

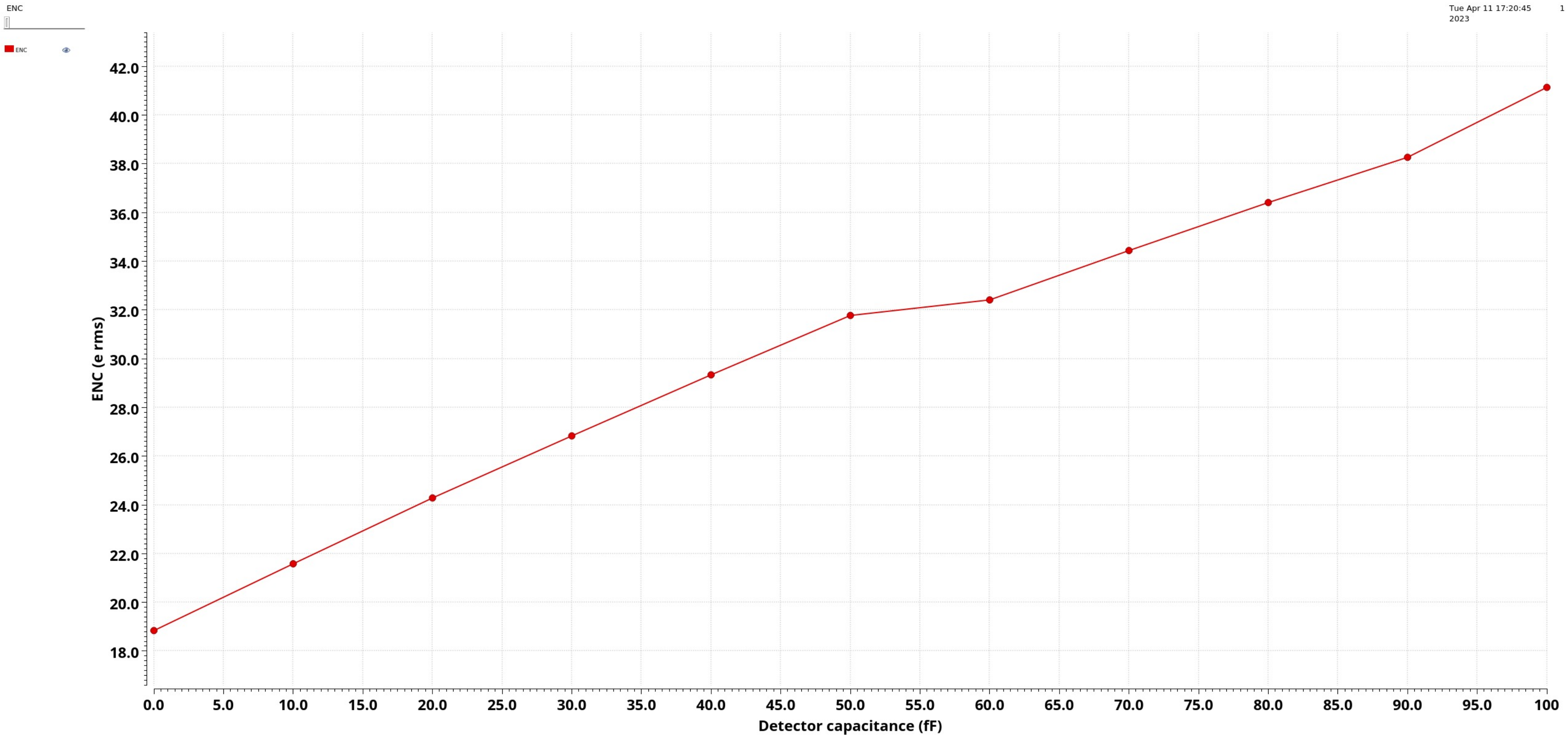


- Self-cascode preamp gain stage
- Differential comparator architecture to improve the immunity to interferences



# ENC vs detector capacitance

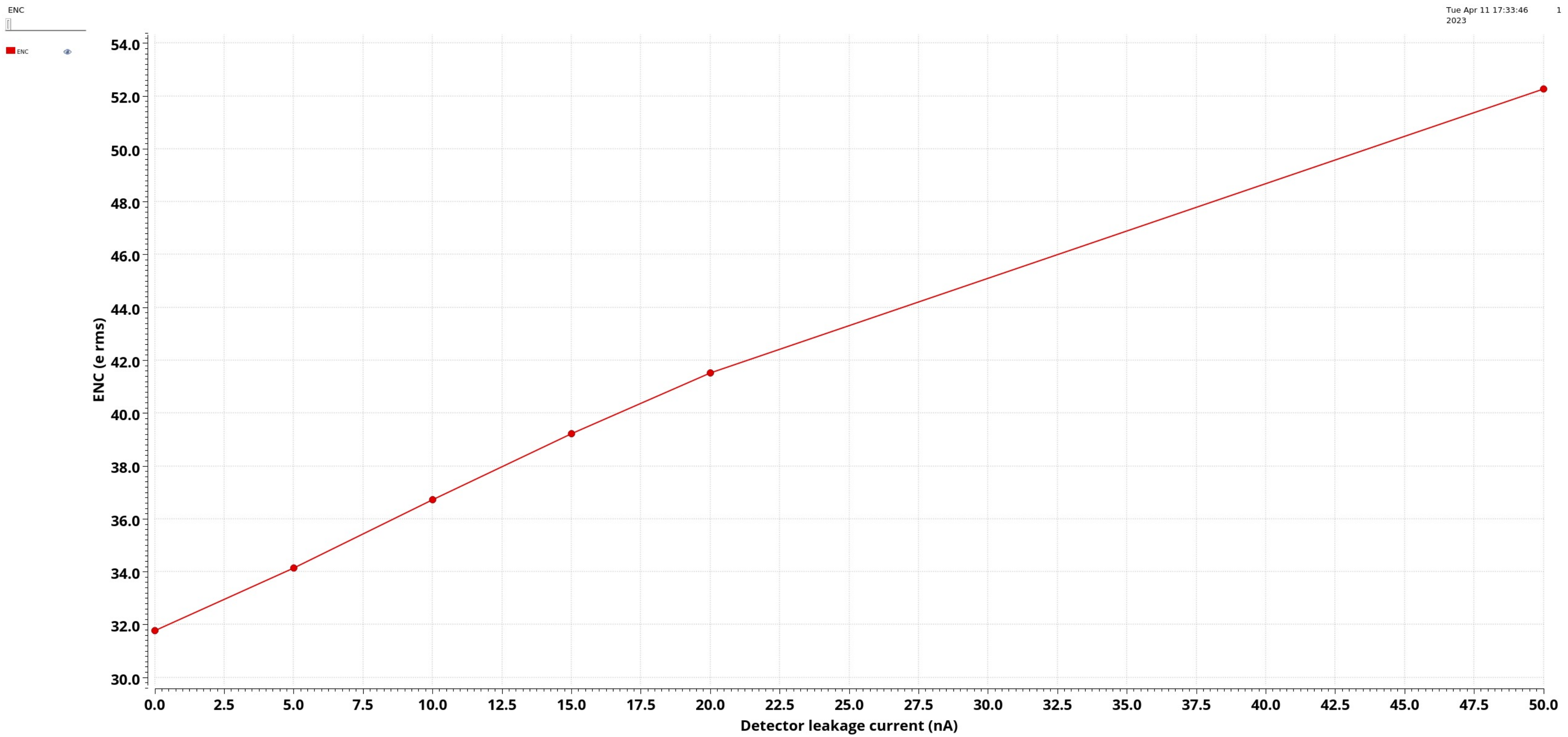





- Equivalent noise charge increases with detector cap
- ENC ~32 e rms @ CD = 50 fF (simulation for T=-20°C)

# ENC vs detector leakage



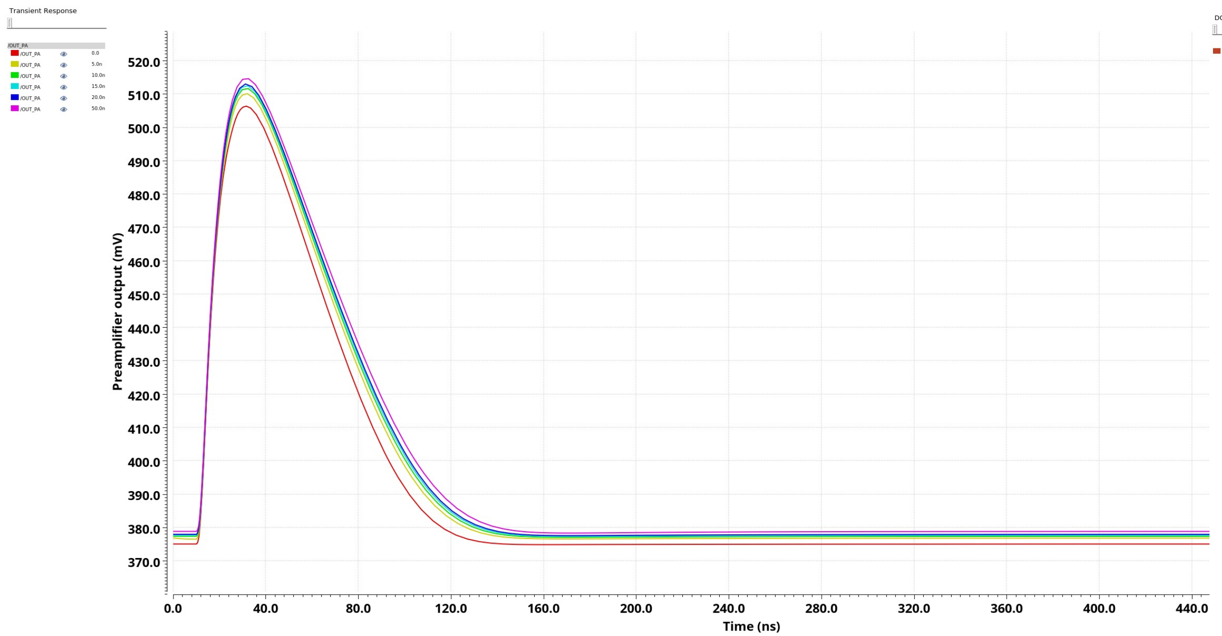



- Equivalent noise charge for detector leakage current up to 50 nA, for CD=50 fF
- Significant (~60%) increase in the ENC at 50 nA

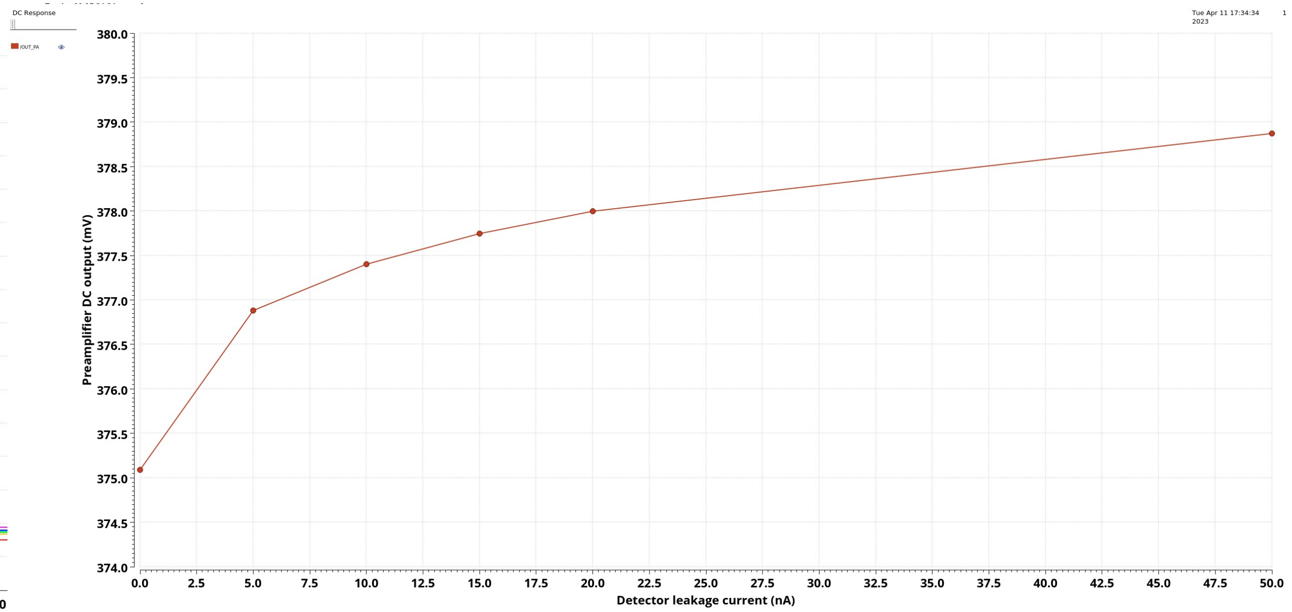
# Leakage compensation



Preamp out in response to Qin=6 ke



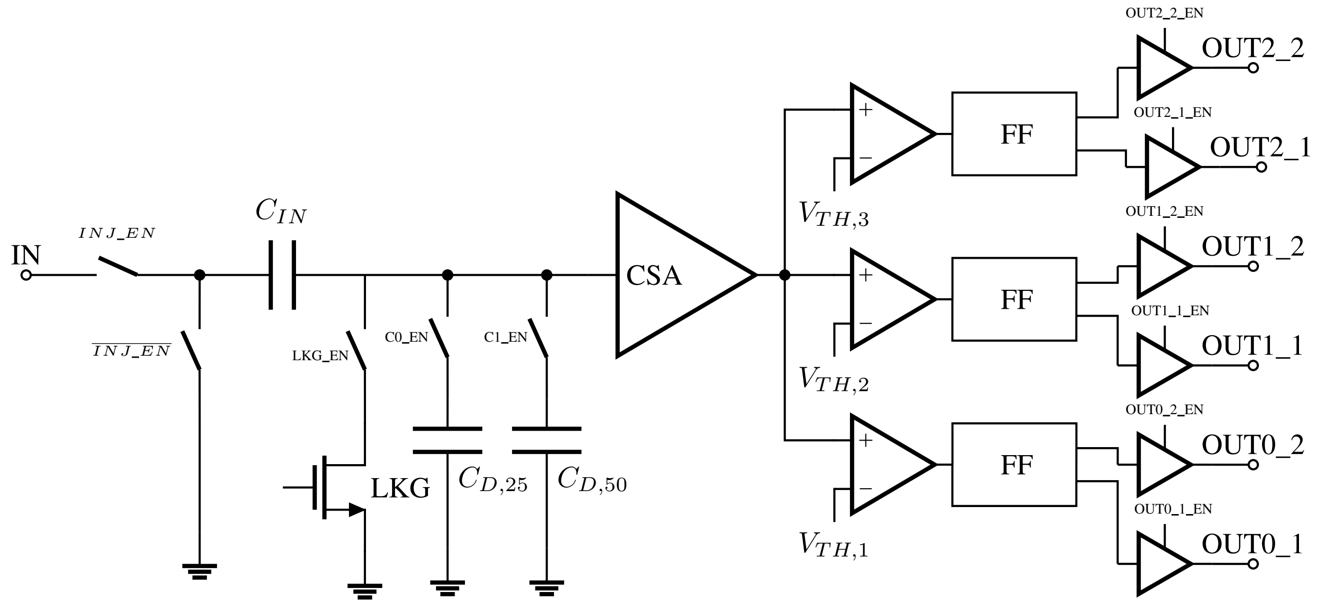

Preamp DC out vs detector leakage current



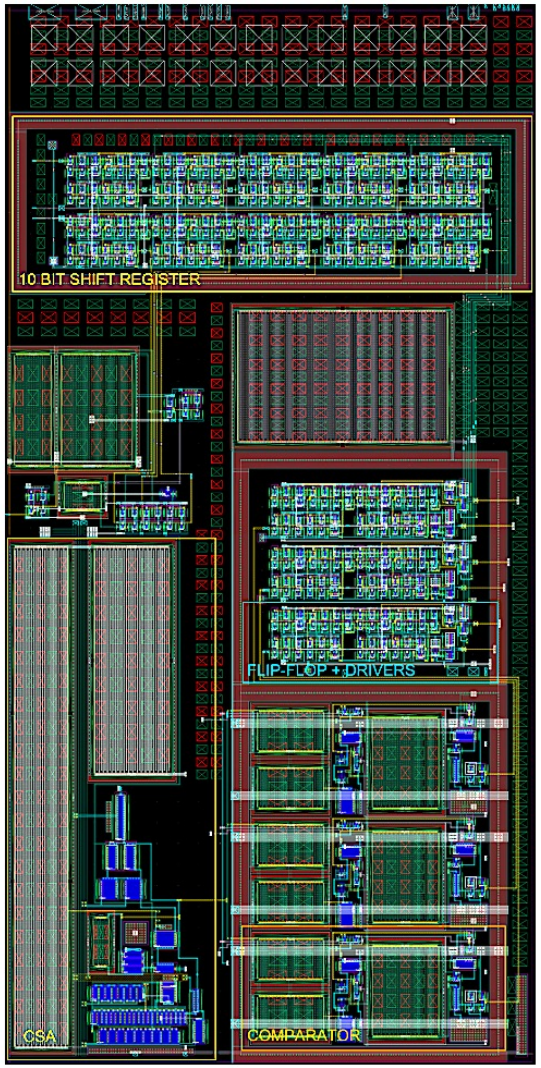

- Preamplifier output waveform not significantly affected by leakage
- Slight (~4 mV) increase in the preamp DC output

# Flash ADC based front-end





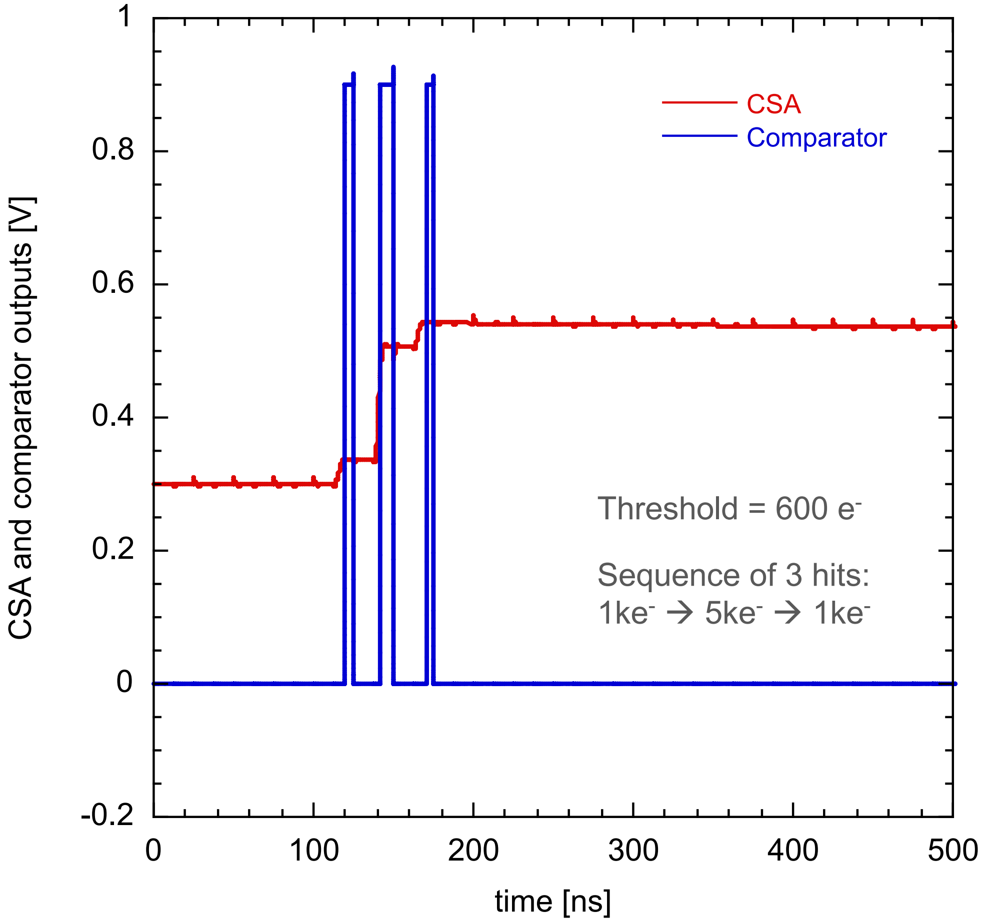

- Preamp (**regulated cascode**) two independent feedbacks
- Ancillary blocks for **detector emulation**

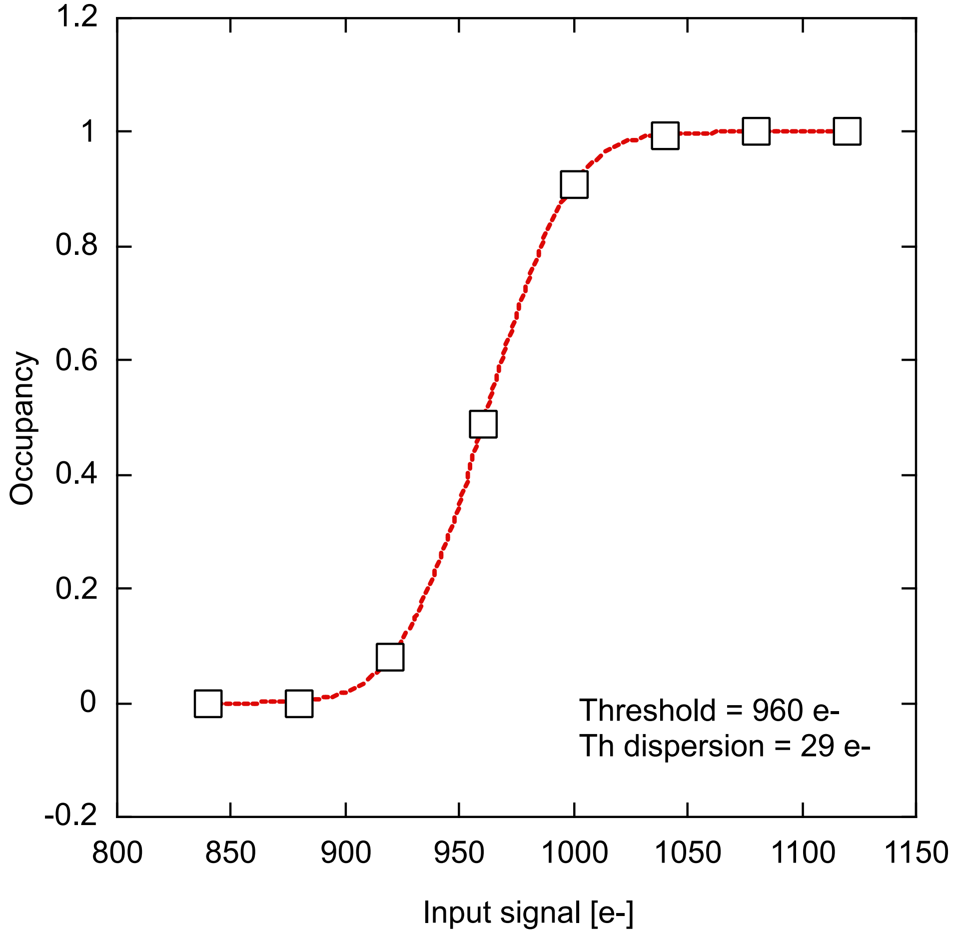



- **AC coupled, auto-zeroed comparators**, operated with 40 MHz clock, implementing a **2-bit flash ADC.** The design is ideally insensitive to device threshold voltage mismatch → threshold tuning DAC not required
- Overall **current consumption**: 5.4 uA → 4.9 µW **power consumption** @ $V_{DD}$=0.9 V
- Elementary cell size: 25 x 50 µm$^2$ (analog+digital)
- Minimum **in-time threshold**: 600 e-

# Flash ADC based front-end



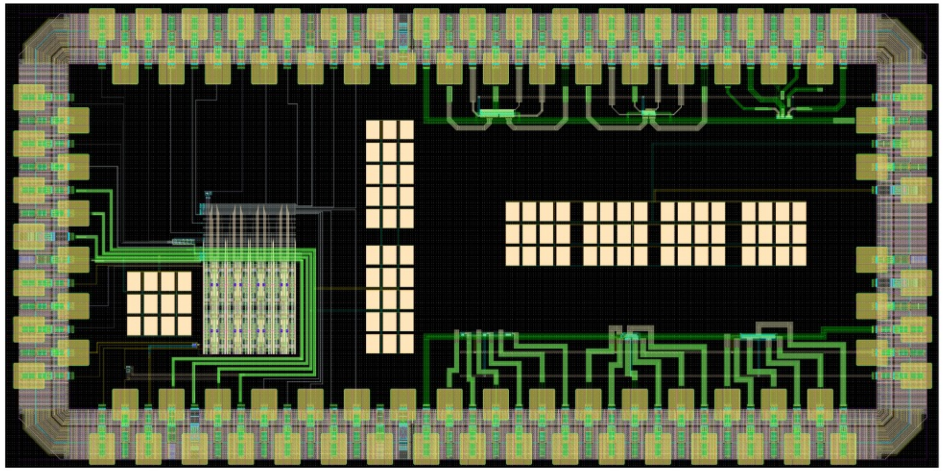


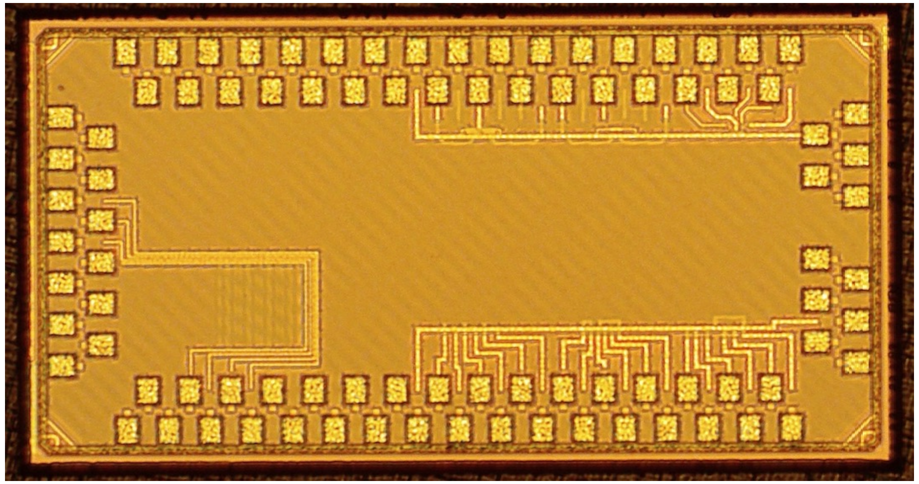




- Zero dead-time
- Low threshold dispersion (~30 e r.m.s.)

# Flash ADC based front-end



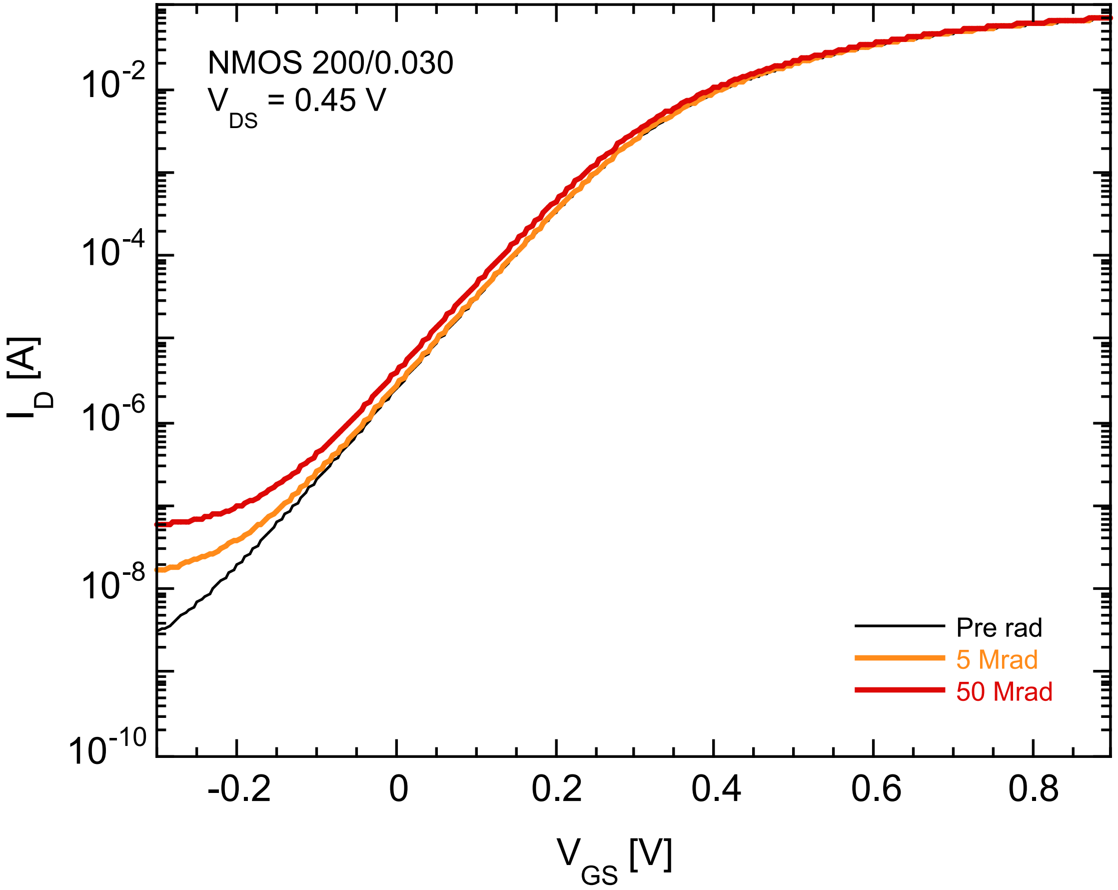


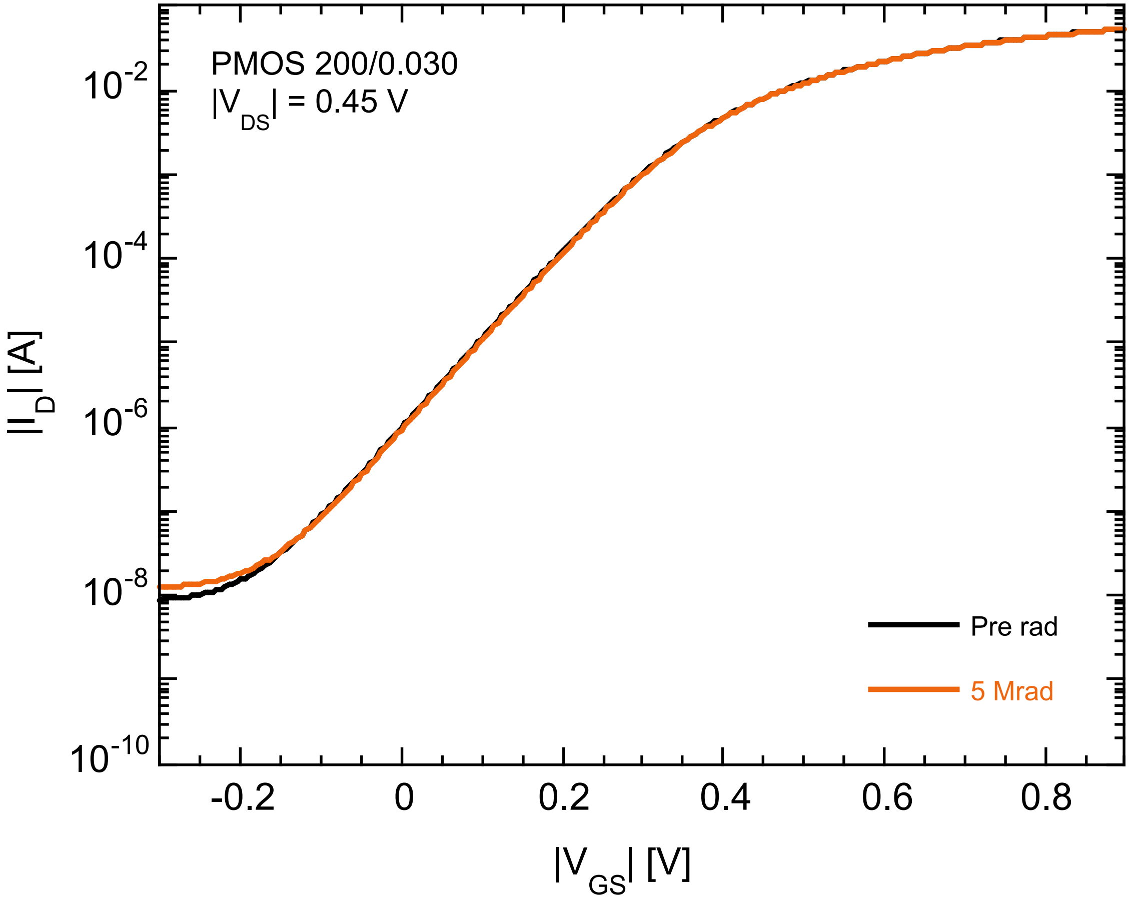


- **Prototype chip including a 4x8 readout matrix** has been submitted in a mini@sic run in October 2022
- Simple digital configuration and readout (shift registers)
- Prototype chip includes **standalone NMOS and PMOS** transistors for static and noise characterization
- We received **100 bare chips**, test on single devices and front-end channels started, irradiation campaign on-going

# Test results – single transistors



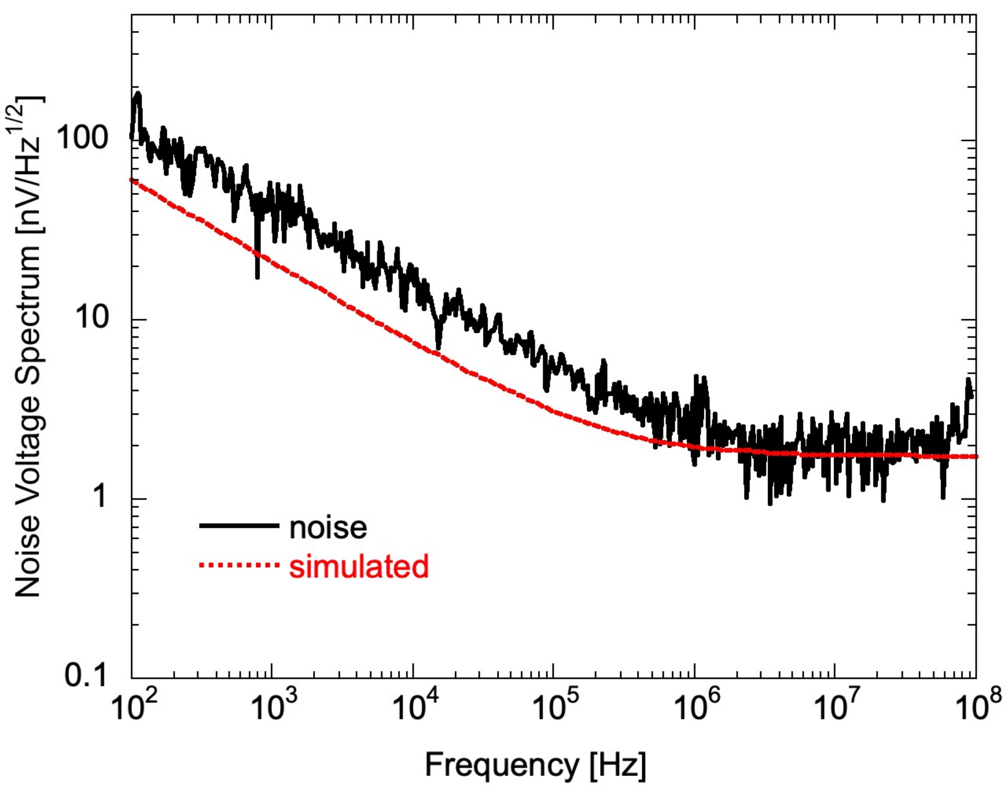


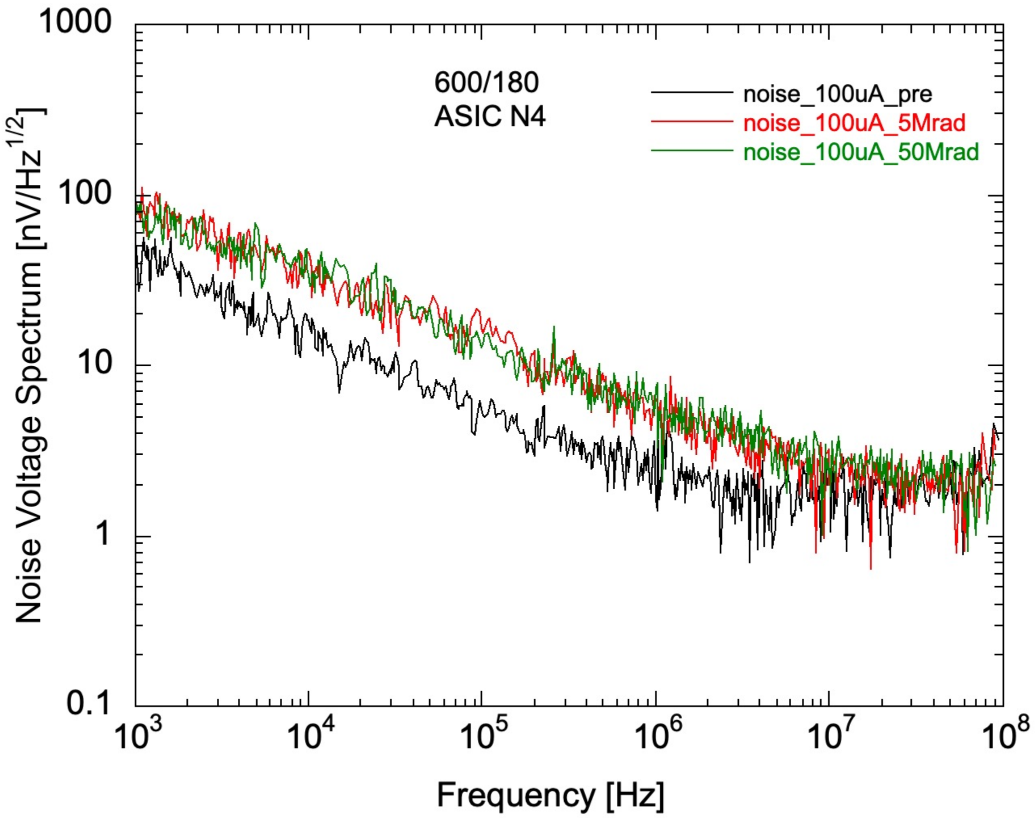




- **ID-VGS curves** for NMOS and PMOS transistors with W/L = 200/0.03, **before and after irradiation**
- **Radiation-induced changes** are apparent in NMOS devices operated in the subthreshold region
- Radiation campaign on-going (**target TID 1Grad**)

# Test results – single transistors



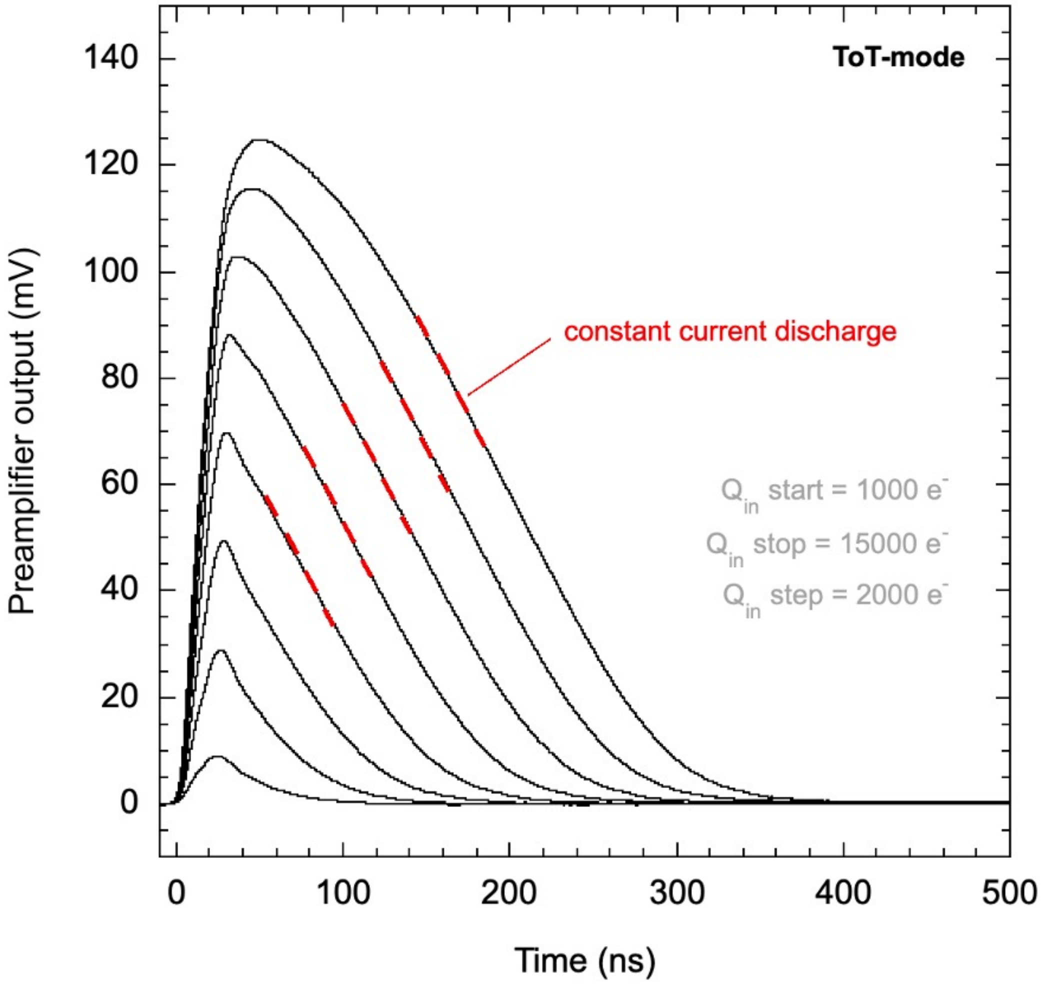


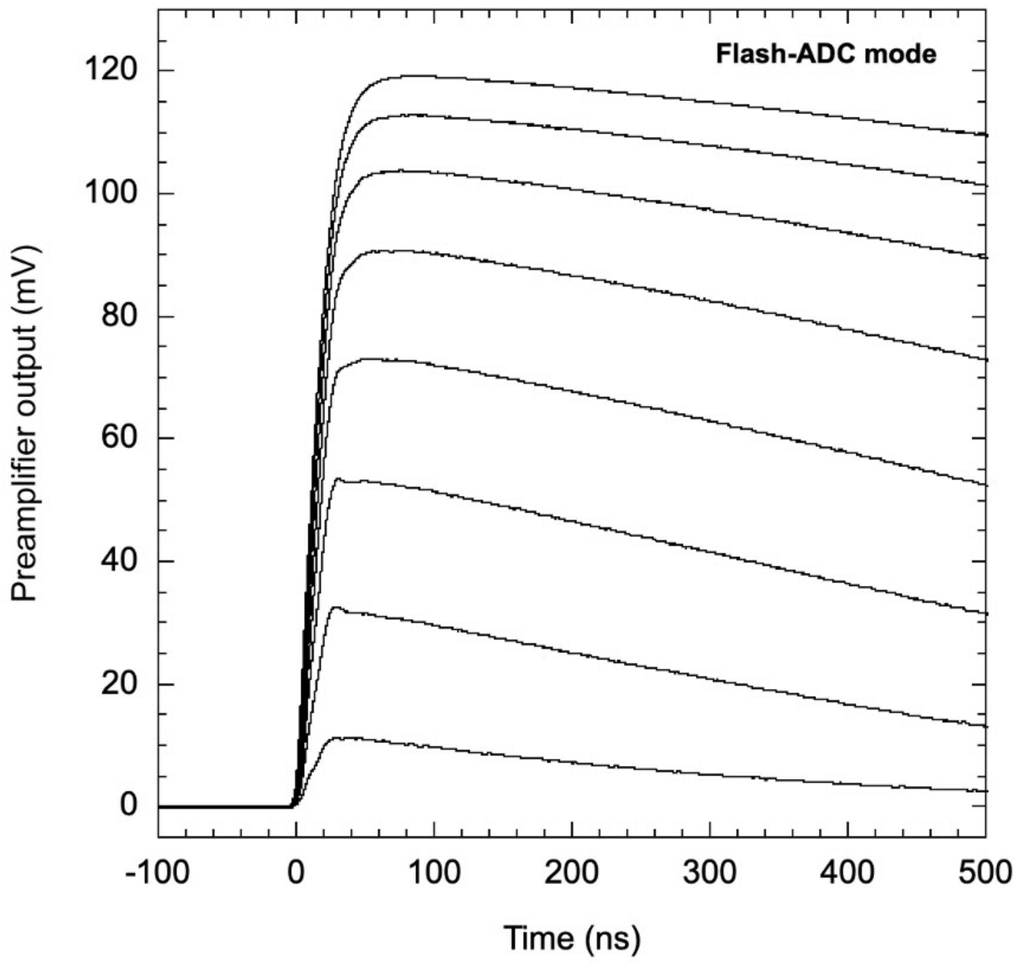




- **Noise voltage spectra** for an NMOS device (600/0.18) operated at a current density close to the one in the front-end input transistor
- Results for a chip irradiated at **5 and 50 Mrad**. Slight increase in the **1/f noise component** of the spectrum, detectable already at 5 Mrad, for low current densities, for devices with L >> Lmin

# Test results - preamplifier response



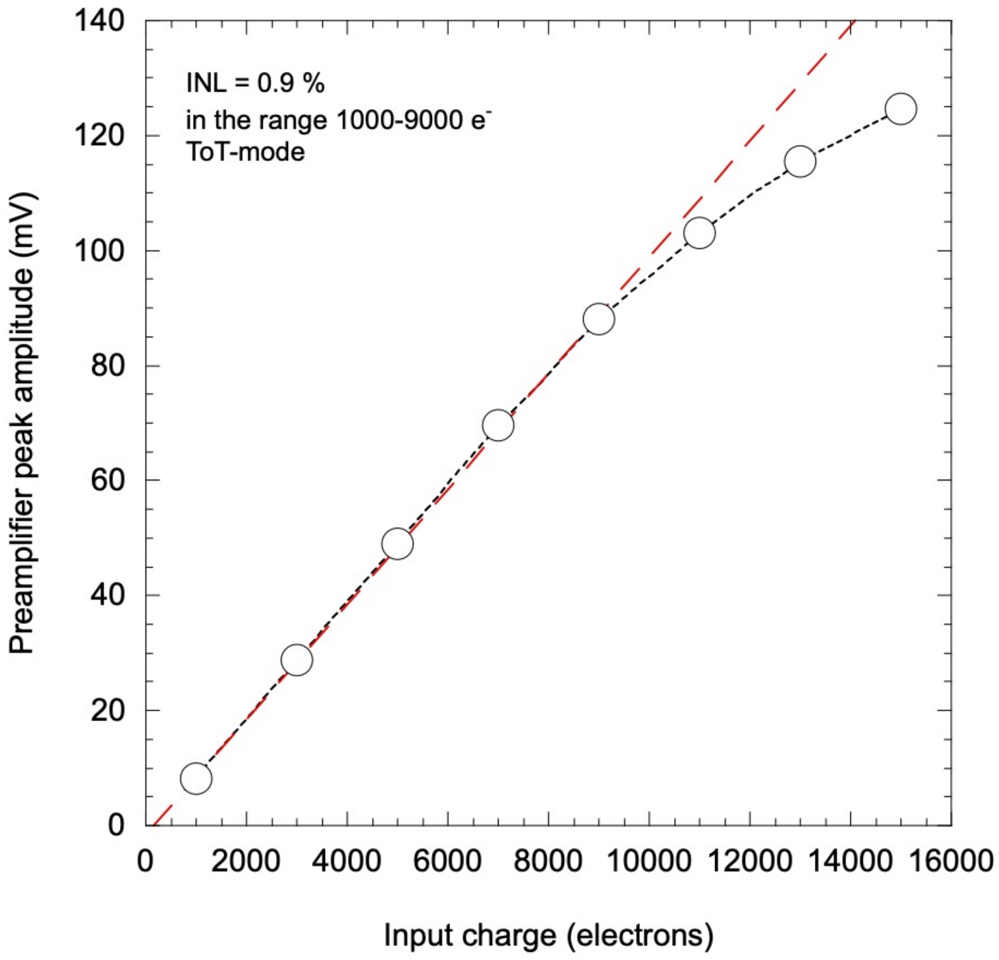


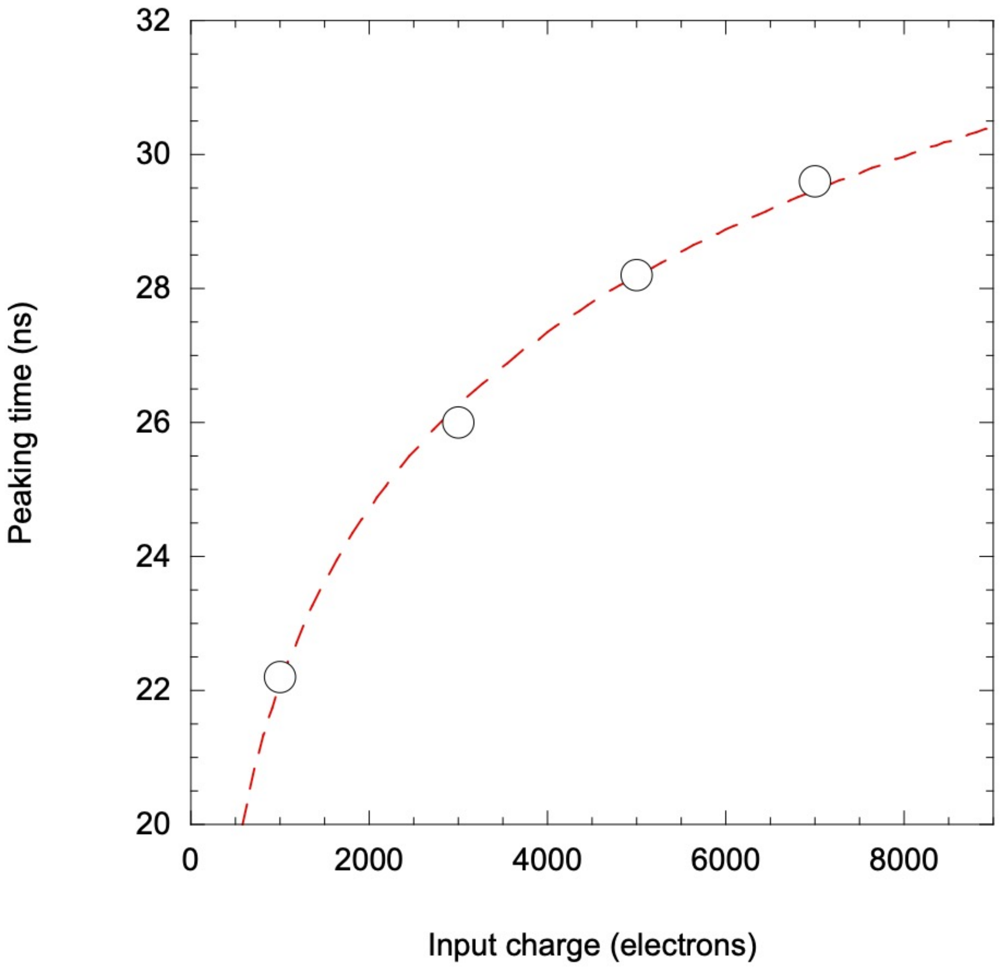




- **Preamplifier** have been characterized in **ToT-mode** (namely, with fast discharge) suitable for ToT conversion of the signal from the sensor, and in **Flash-ADC mode** (with slow discharge to enable A/D conversion through the in-pixel Flash ADC)
- **Noise close to 75 e rms** for the preamp not connected to the detector emulating capacitor

# Test results - preamplifier response






- **Good linearity up to ~10000 electrons**, with a peaking time found to be a monolithically increasing function of the input charge

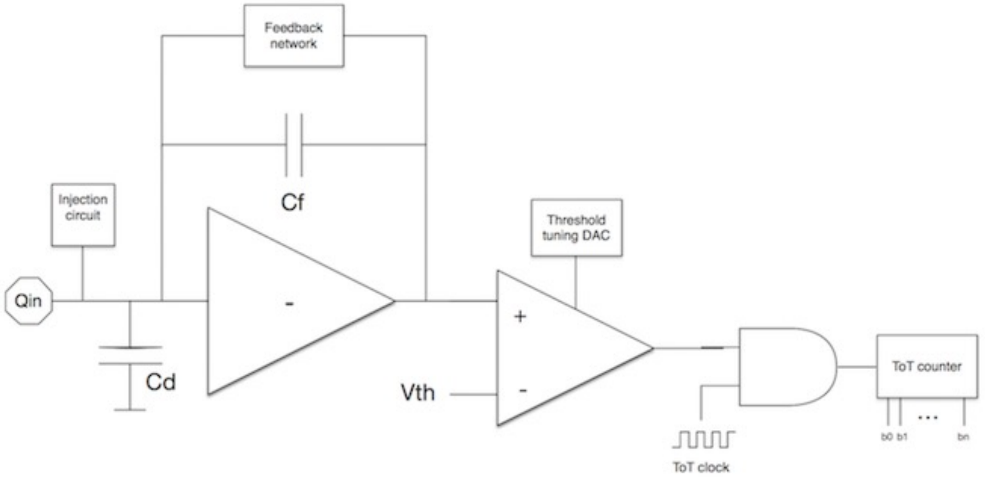
# PiHEX project



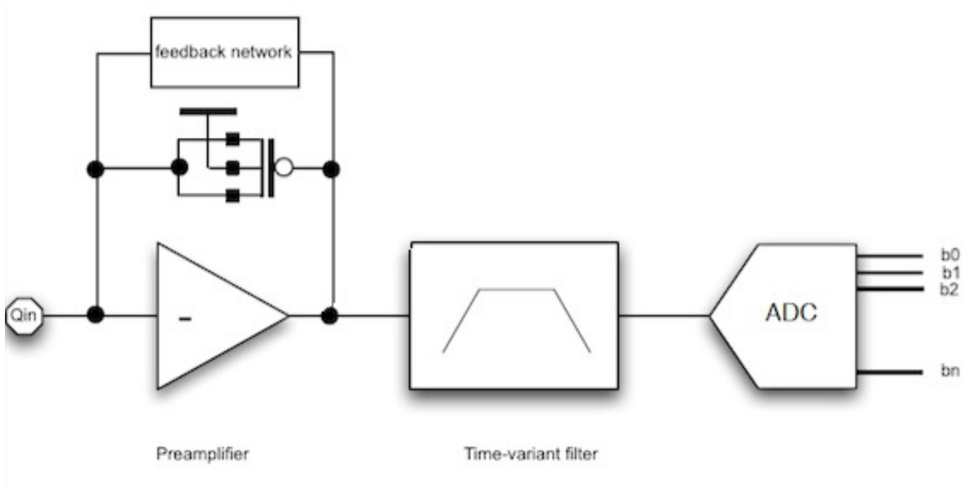
- Starting at the end of Sept 2023 will be focused on the design and radiation hardness qualification of **28 nm CMOS analog front-end channels** for **pixel sensors** for high energy physics and photon science applications

- **Two front-end channels** will be developed, optimized for HEP and FEL applications, meeting a set of challenging requirements, including extreme radiation tolerance, high spatial resolution and wide dynamic range

HEP front-end




FEL front-end



# Conclusions

- **Building analog blocks** in 28 nm CMOS have been investigated in the framework of Falaphel/Ignite INFN projects

- **Two different AFEs** are begin designed in a 28 nm CMOS technology:
  - **ToT** A/D conversion
  - **Flash** A/D conversion

- **Characterization** of the the Flash-ADC based front-end just started

- **Submission in January 2024 (mini@SIC):**
  - ToT-based front-end in a 32x16 matrix of 100x25 $\mu m^2$ pixels

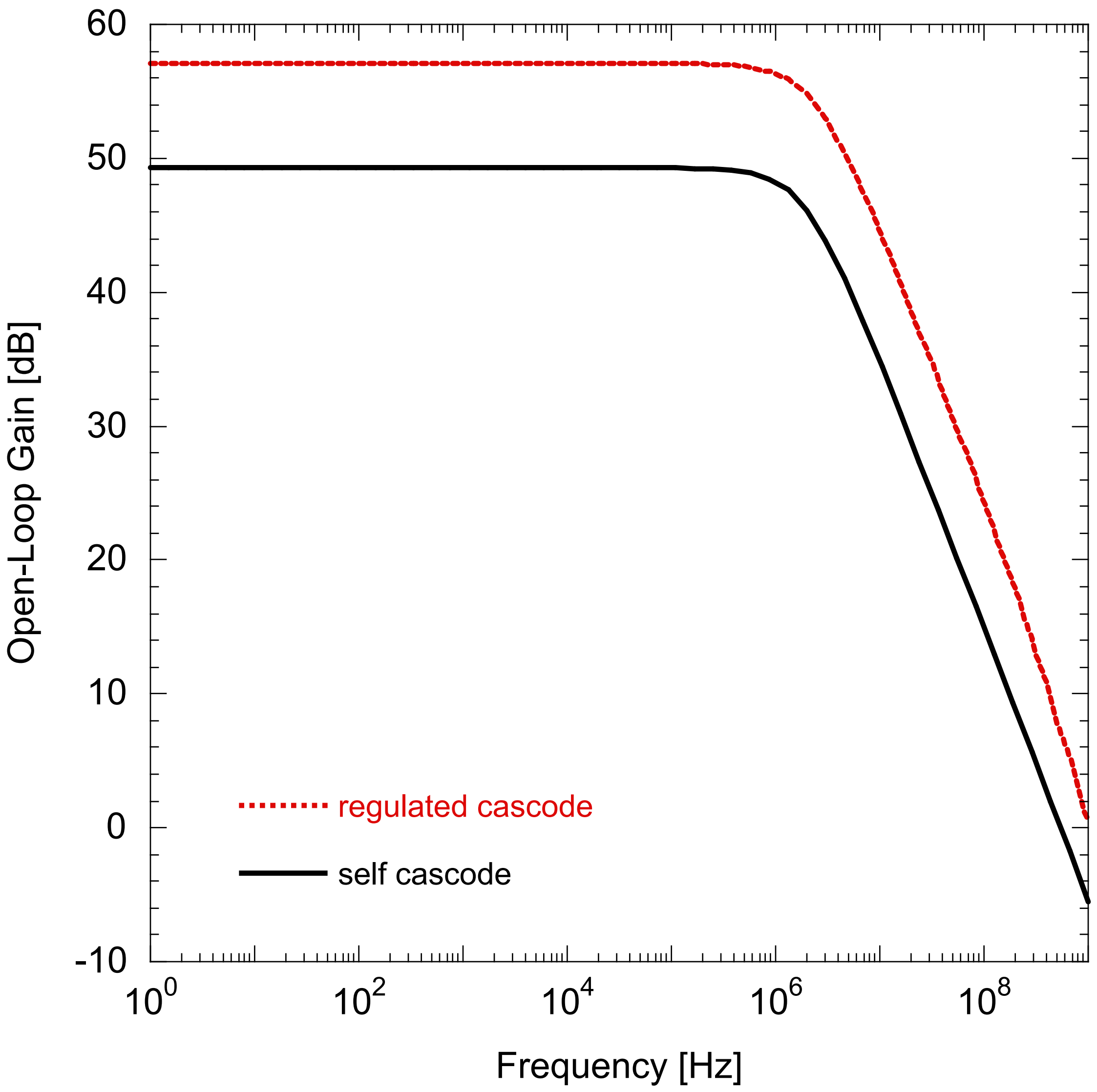
- **PiHEX project** will start at the end of September with the goal of developing, in a 28 nm CMOS technology, front-end channels for HEP and photon science applications

Thanks for your attention!

# Backup

# Preamp gain stage: open loop gain






Self cascode

$$A_0 \approx -\frac{g_{m1}}{\frac{g_{ds1} g_{ds2}}{g_{m2}} + g_{ds3}}$$

Regulated cascode

$$A_0 \approx -\frac{g_{m1}}{\frac{g_{ds1} g_{ds2}}{g_{m2}} \frac{g_{ds4}}{g_{m4}} + g_{ds3}}$$

extra-boost

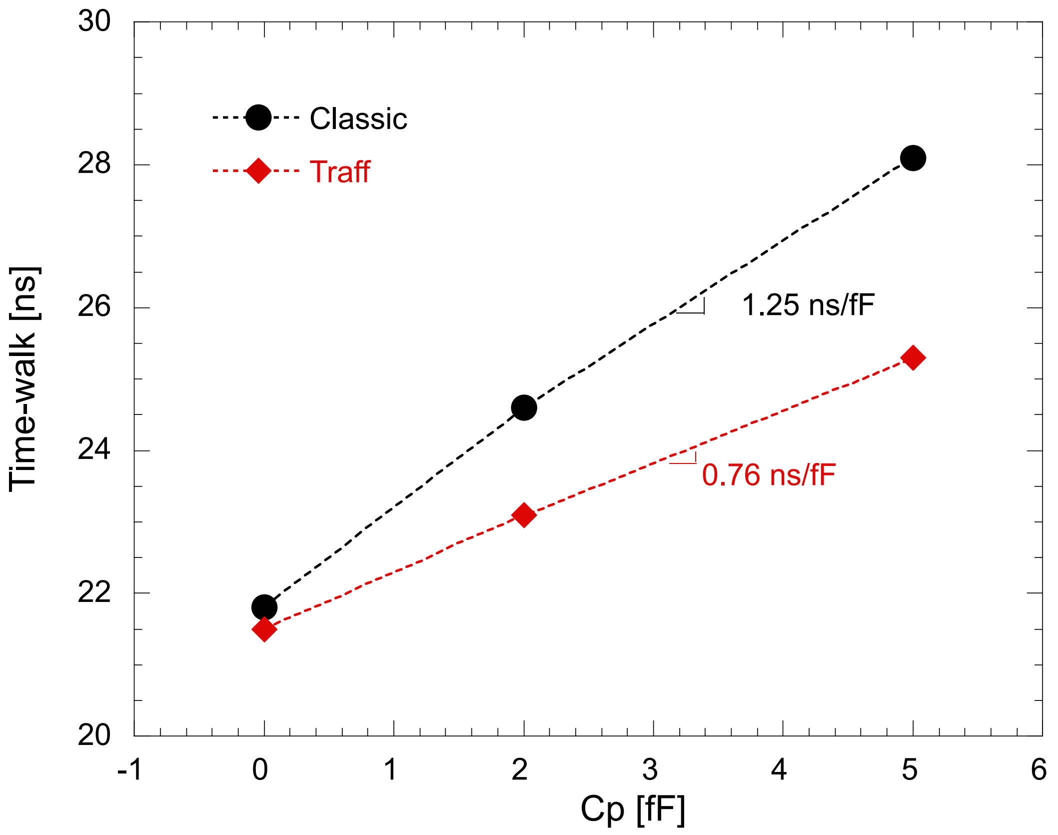
# Front-end specifications



- Elementary cell size: 25 x 100 $\mu m^2$ (analog+digital)
- Per-pixel analog current consumption < 5 µA
- Minimum threshold < 500 e-
- Radiation TID > 1 Grad
- *Analog island* layout arrangement as in RD53
- Isolation of analog circuits: Single DNW

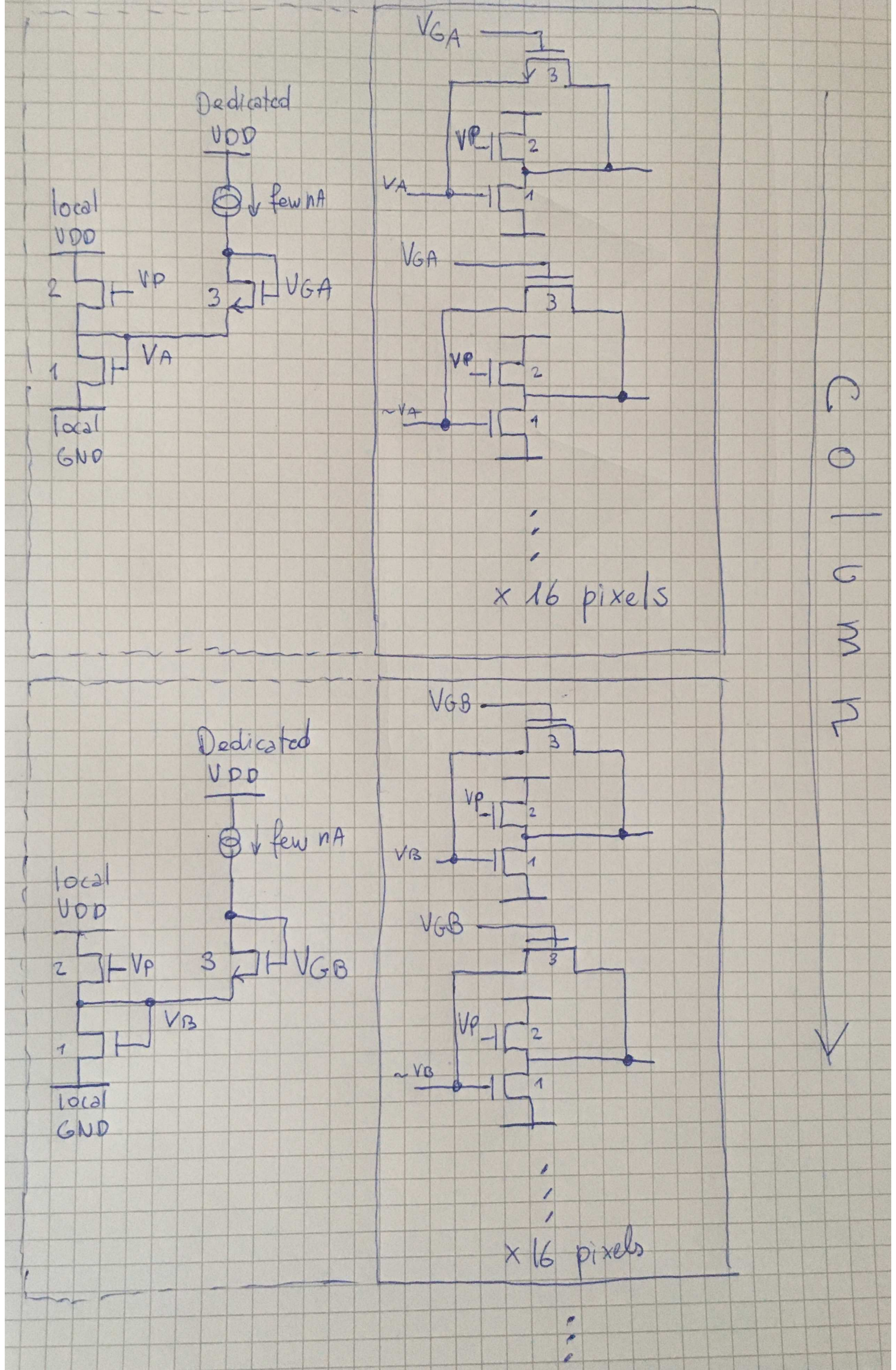
# Continuous-time comparators





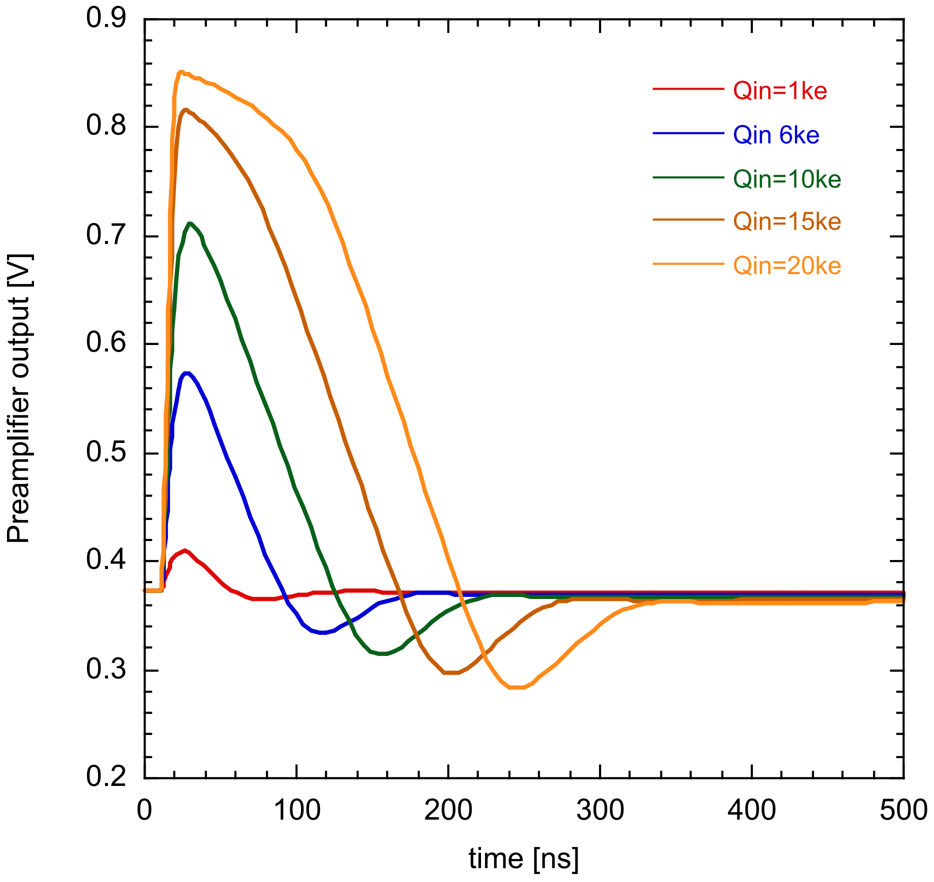

- **Time-walk** (contributed by comparator) for the two versions: schematic-level simulations with an ideal preamp with 20 ns peaking time
- **Parasitic capacitance** (Cp) added to the main nodes of the comparators

# Voltage drop compensation



# Krummenacher feedback

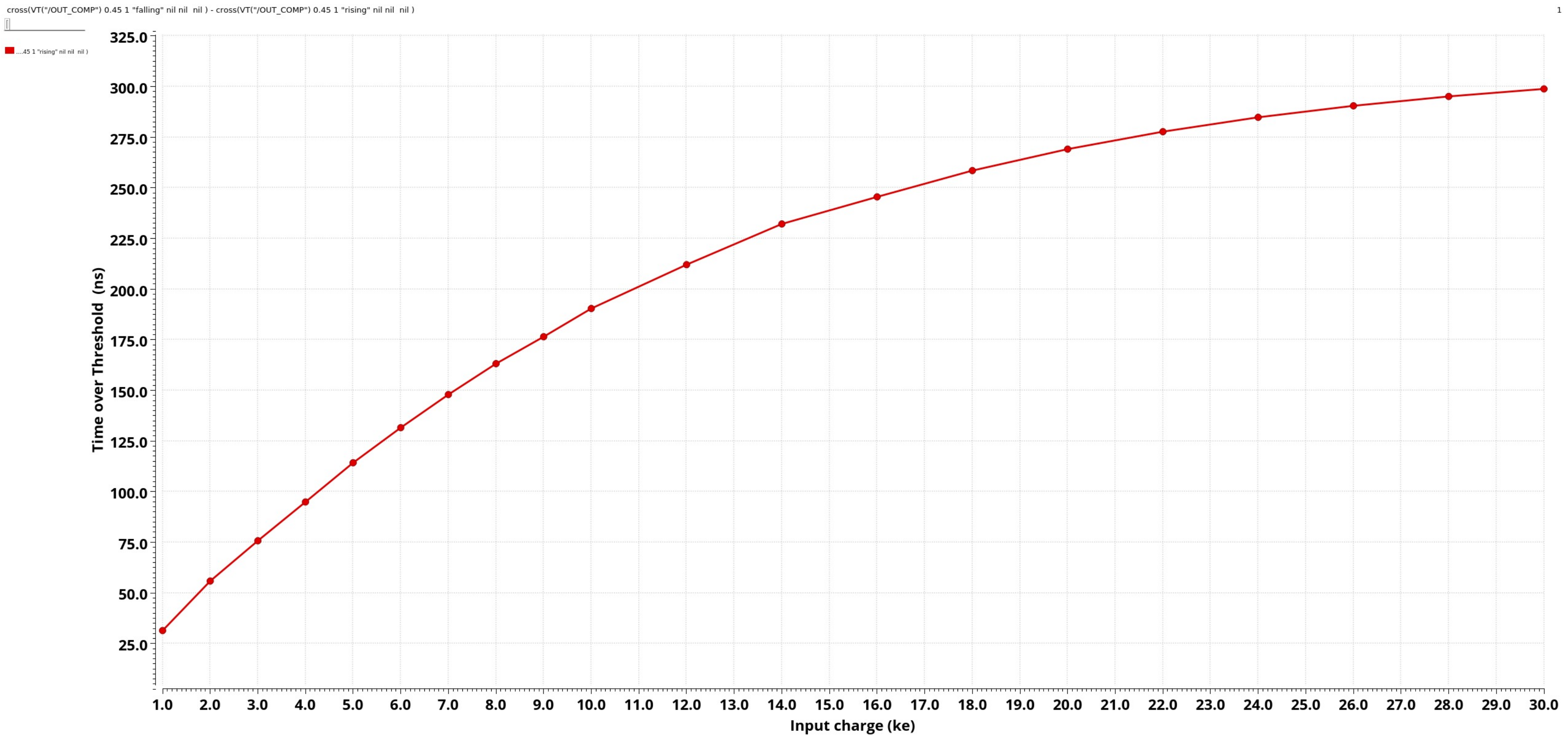





- Preamplifier output for different input charges

# Time-over-Threshold

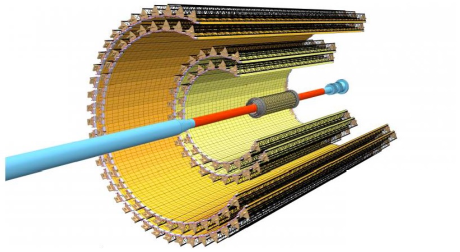


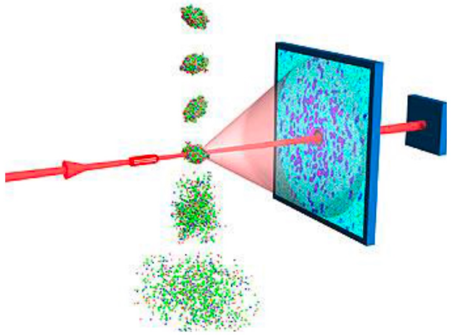



- Time-over-Threshold as a function of the input charge
- ~ linear behavior up to Qin=10 ke$^-$

# Pixel detectors for HEP and photon science







- Pixel detectors have become essential devices in crucial applications in **high energy physics** (HEP) and **photon science**
- Different applications with different requirements
- But also some **similarities**:
    - **Multichannel, large area readout chips** →inter-channel and intra-channel (analog-digital) cross-talk, chip integration issues, power distribution
    - **Complex circuits**: different IP blocks (voltage and current references, regulators, PLLs, ADCs and DACs, I/O pads), many different functions (data conversion and storage, sparsification, threshold adjustment, gain calibration)
    - **Fast analog processing** to comply with the machine and the experiment requirements
    - **Large amount of data** to transmit off-chip
    - **Unprecedented levels of radiation**: TIDs from several MGy up to 10 MGy
- **Front-end electronics** may benefit from **scaling** in terms of functional density (small pitch pixels) and digital performance - analog design remains a challenge (reduced supply voltage and dynamic range, statistical doping effects). HEP designers' community is now starting investing in the **28 nm CMOS for future developments**