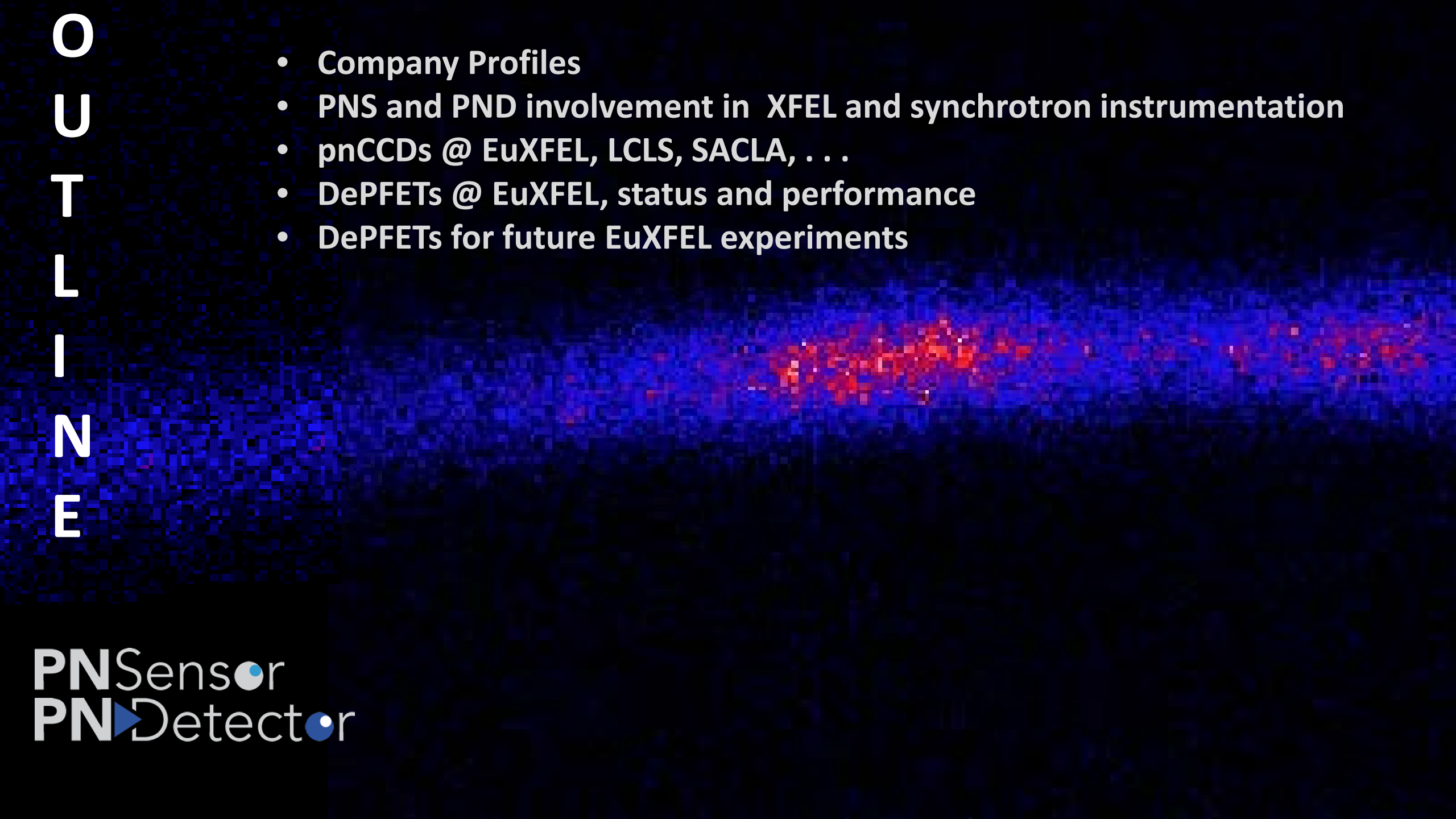
The Future of DePFETs (and other devices) for XFELs and Synchrotrons

PNSensor
PNDetector

OUTLINE

- Company Profiles
- PNS and PND involvement in XFEL and synchrotron instrumentation
- pnCCDs @ EuXFEL, LCLS, SACLA, . . .
- DePFETs @ EuXFEL, status and performance
- DePFETs for future EuXFEL experiments



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Silicon Sensor Fabrication

PNS	founded in 2002	10 employees	new CEO: Robert Hartmann
PND	founded in 2007	90 employees	

Fab, test, mounting, . . .	1400 m^2
Offices, meeting rooms, administration, storage, . . .	1500 m^2

Mission PND: Development and fabrication of modern silicon radiation detectors, detector modules and system of highest quality for high energy resolution and high speed material analysis and imaging applications with X-ray and electrons

Mission PNS: Development of state of the art instrumentation for applications in basic research and applied research

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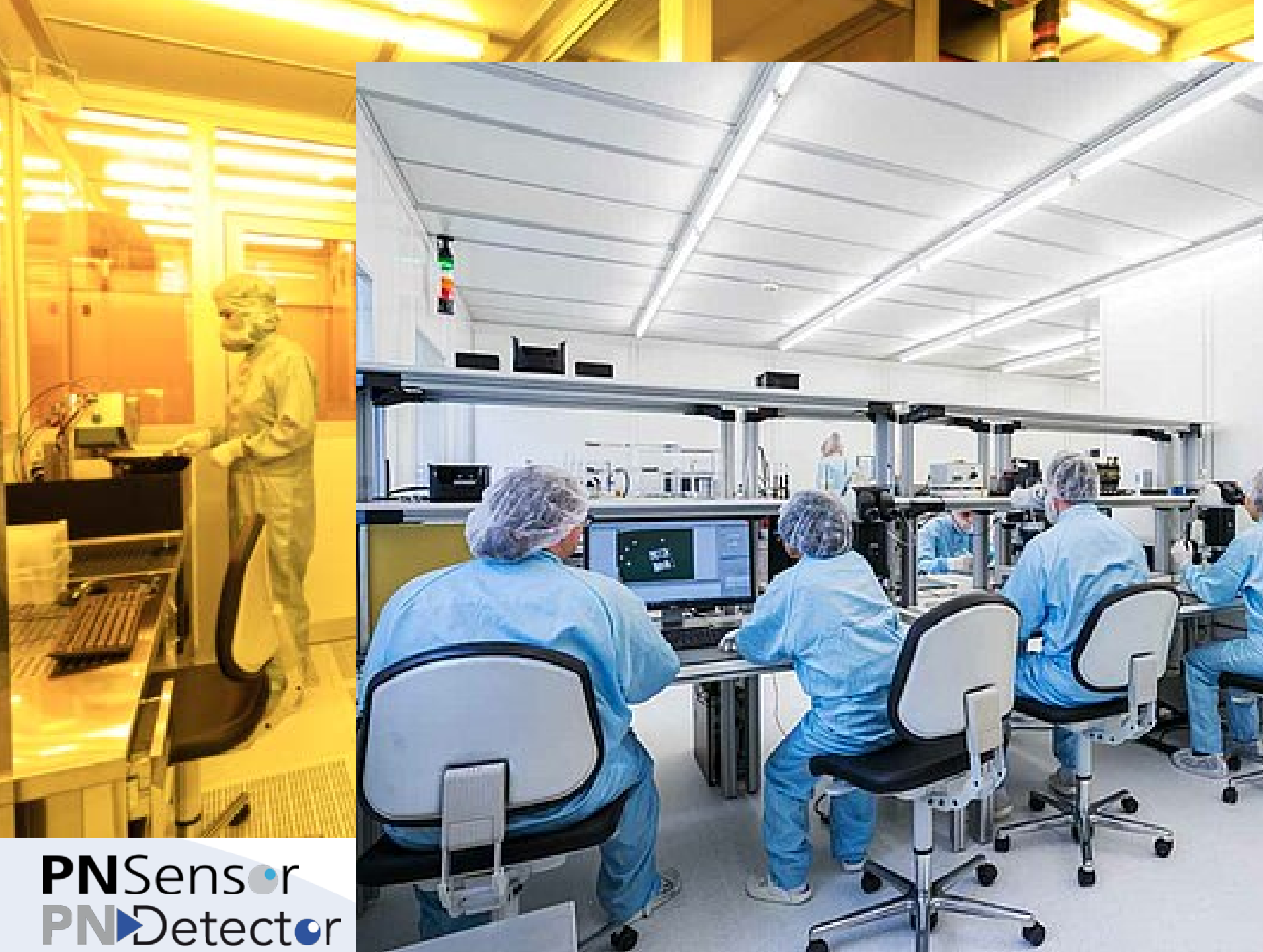

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PNS & PND involvement in XFELs and synchrotrons:

- FLASH
- LCLS
- SACLA
- EuXFEL
- NSLS 2
- ESRF
- BESSY
- PETRA III
- Shanghai
- SLRI
- . . . .
-

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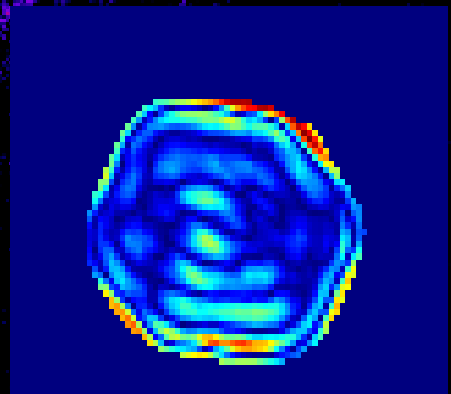
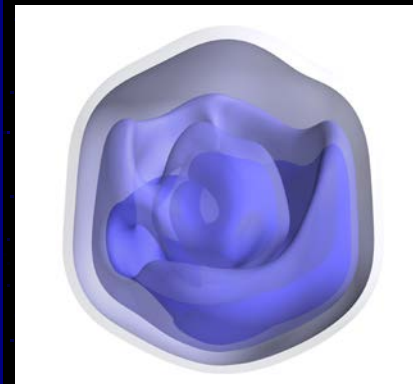
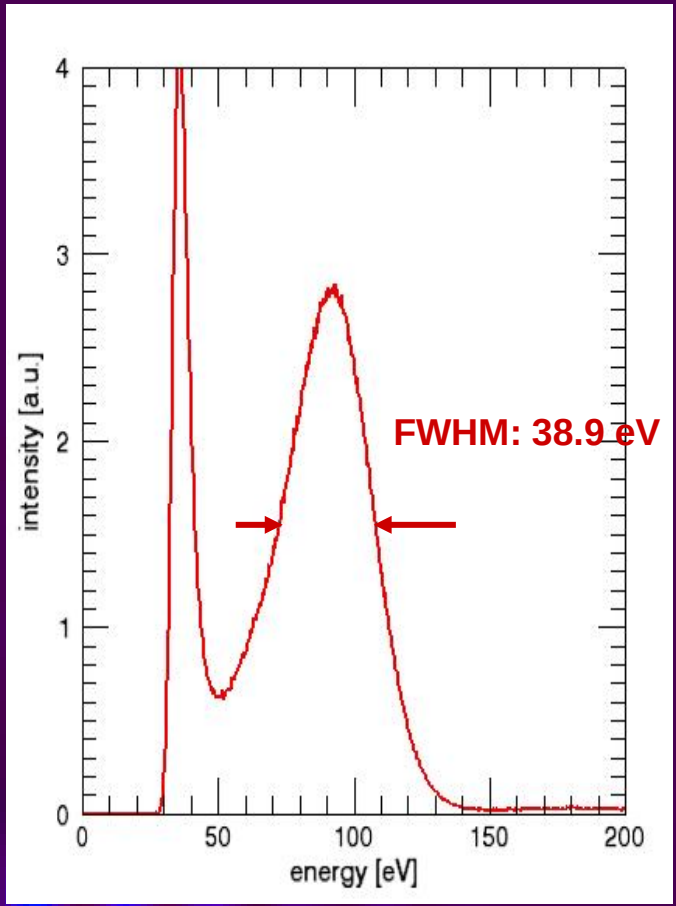




Double slit experiment with pnCCDs at FLASH

X-ray coherence measurements
at 90 eV at FLASH



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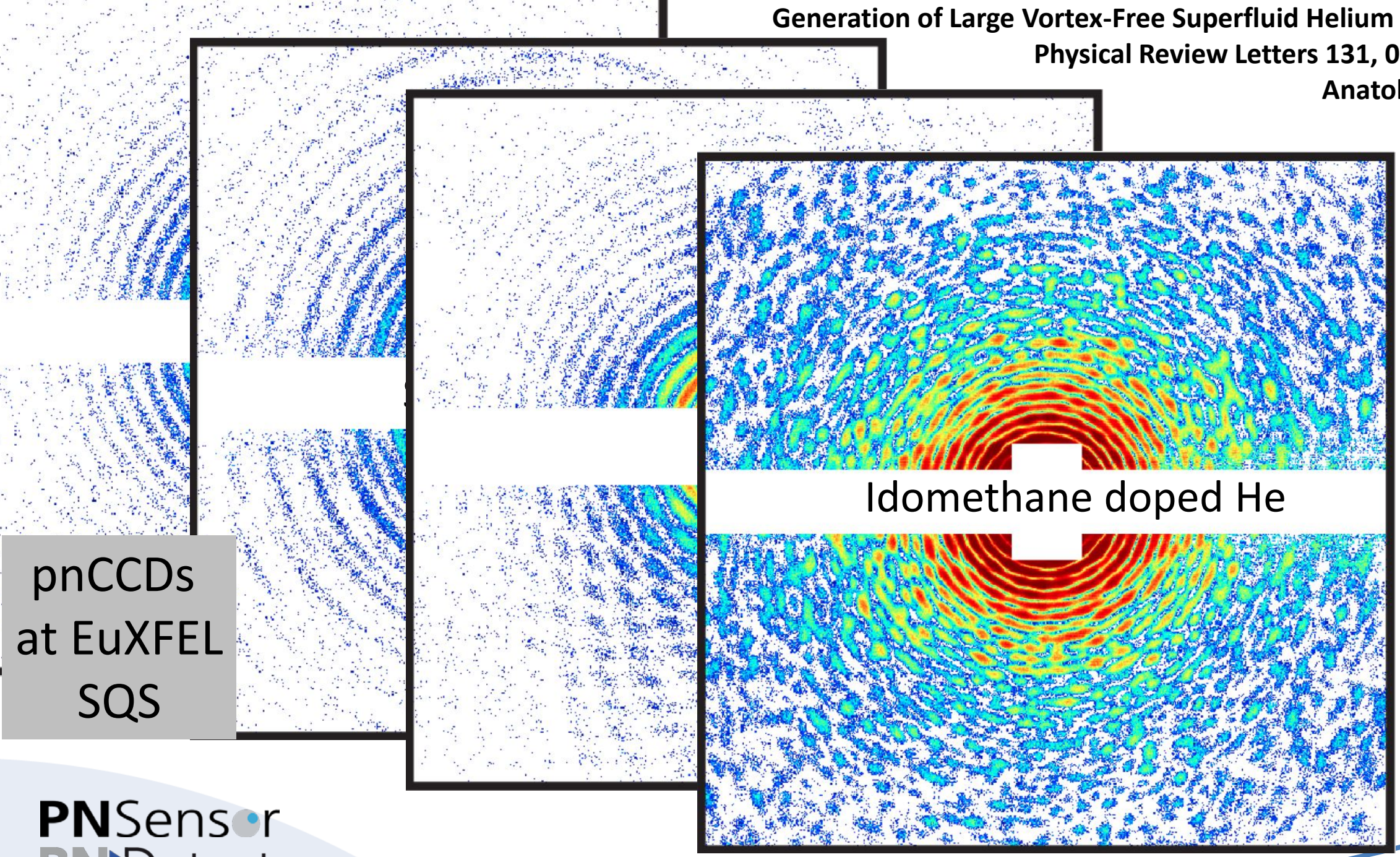
Generation of Large Vortex-Free Superfluid Helium Nanodroplets
Physical Review Letters 131, 076002, (2023)
Anatoli Ulmer et al.



pnCCDs
at EuXFEL
SQS

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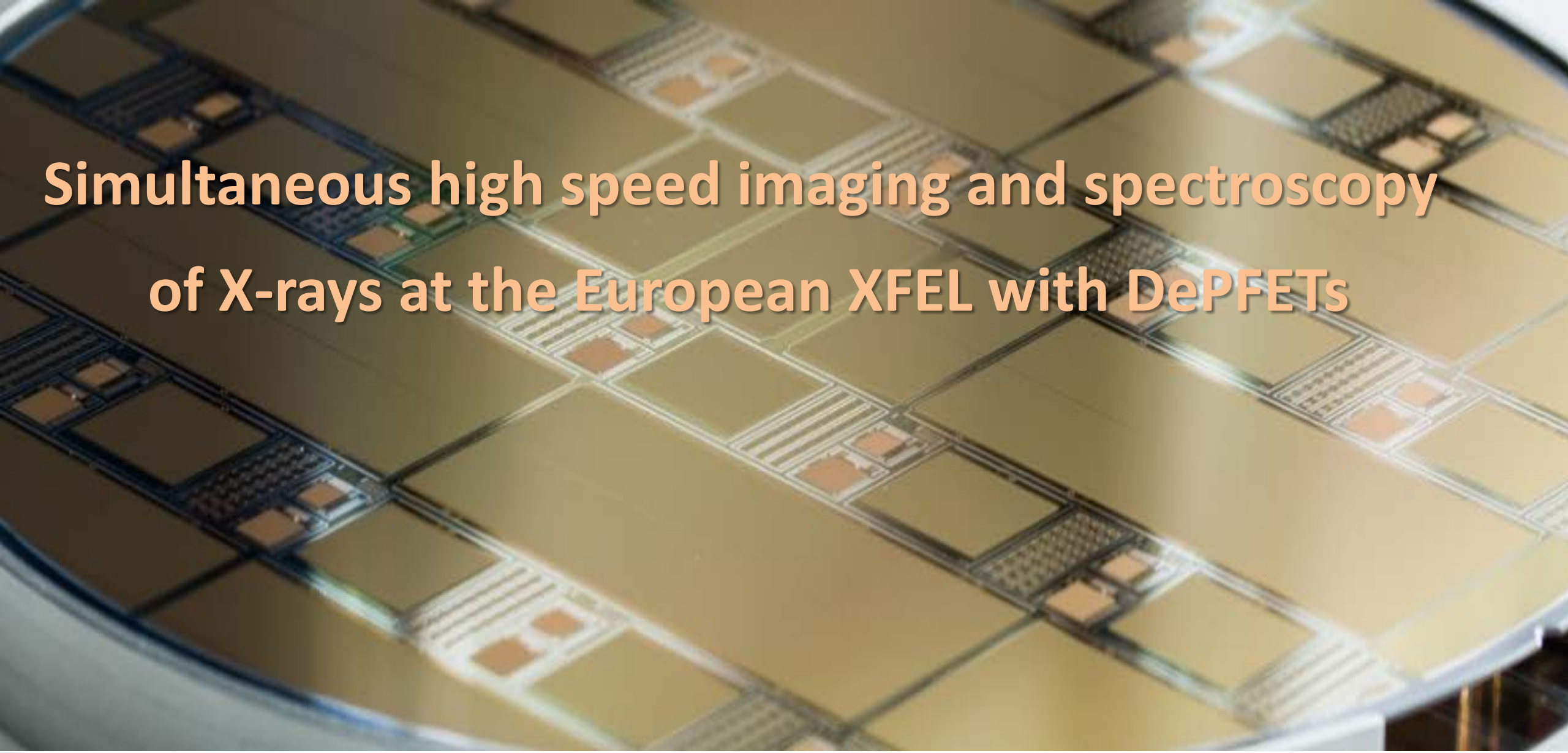

Simultaneous high speed imaging and spectroscopy of X-rays at the European XFEL with DePFETs

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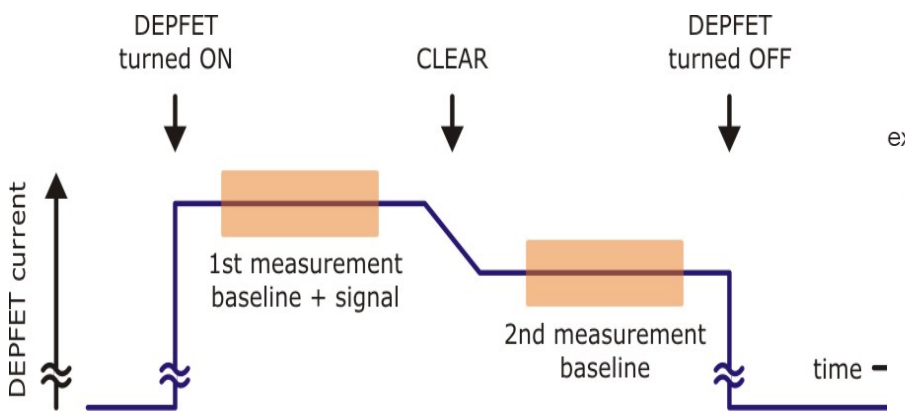
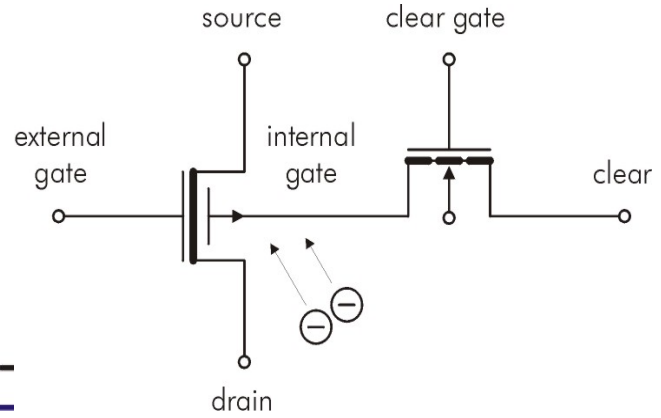
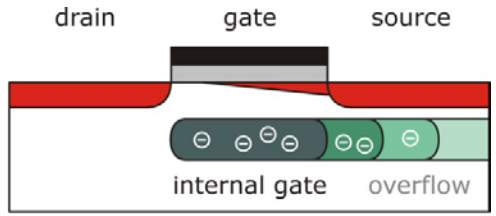
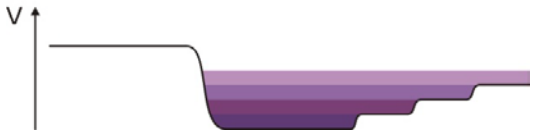
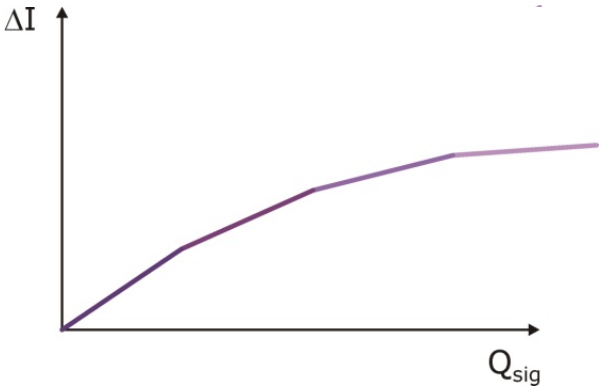
DePFET Active Pixel Sensor – basic principles





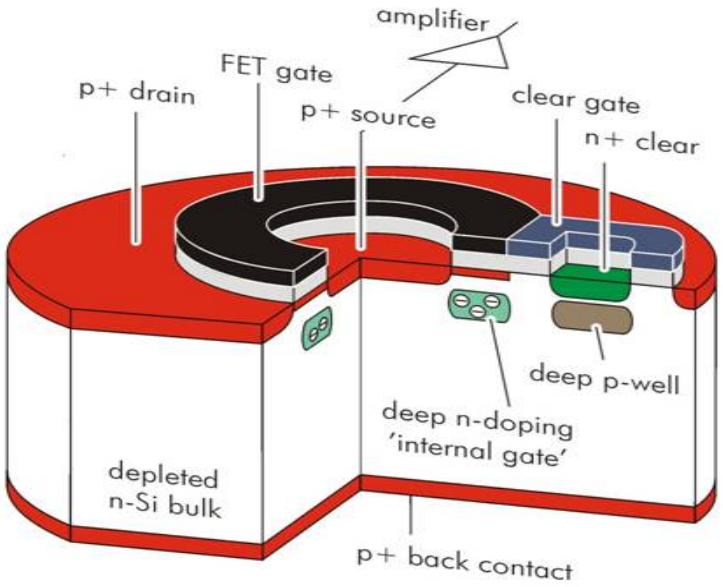






Advantages:

- very low input capacitance
- no reset noise
- high first amplification
- gatable within ns
- repetitive non-destructive readout
- homogeneous entrance window
- high quantum efficiency
- fexibility in pixel geometry
- high dynamic range



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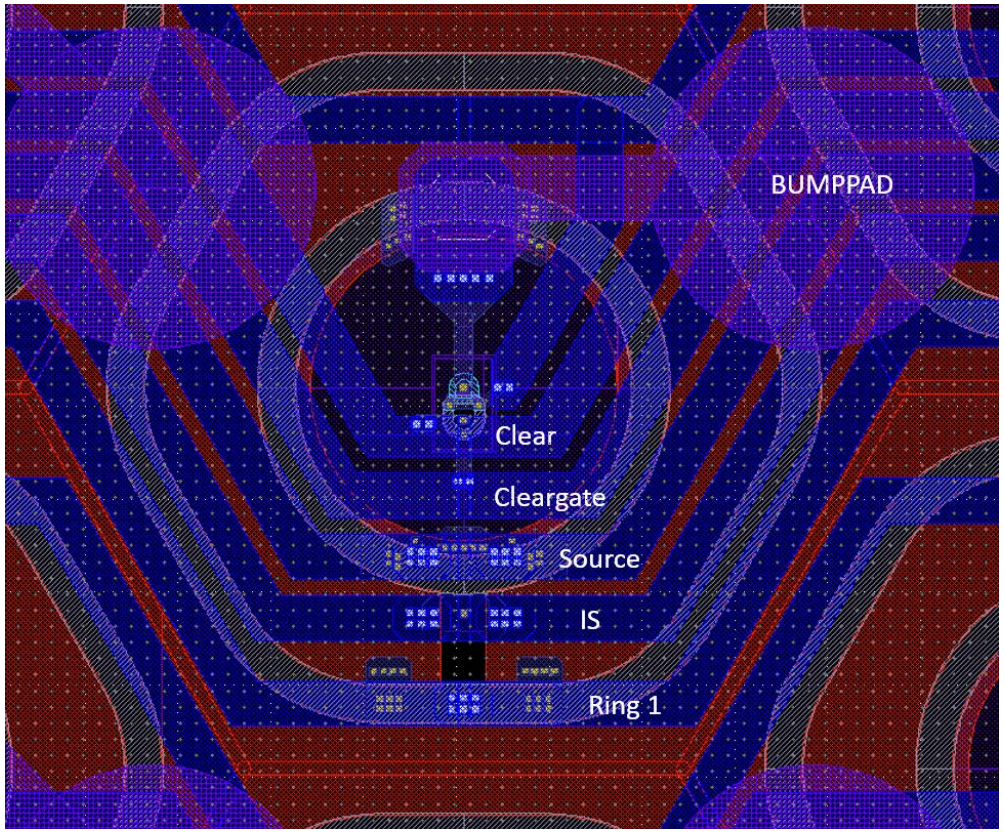
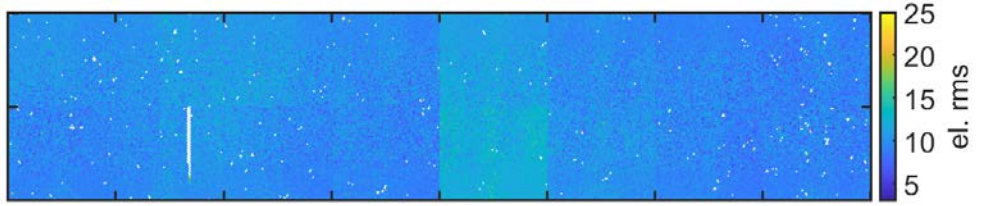
DePFET ladder operation

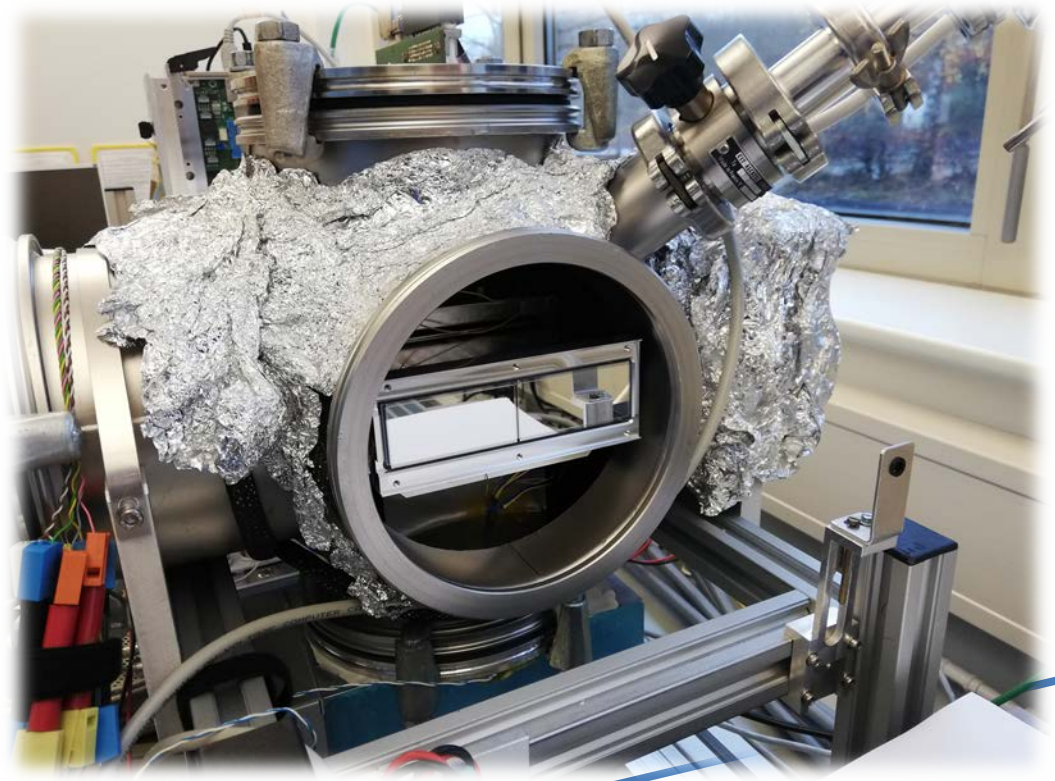


DEPFET Ladder: 128 x 512

ENC ~ 9.8 el. rms

T_{int} = 300 ns (1.125 MHz operation)





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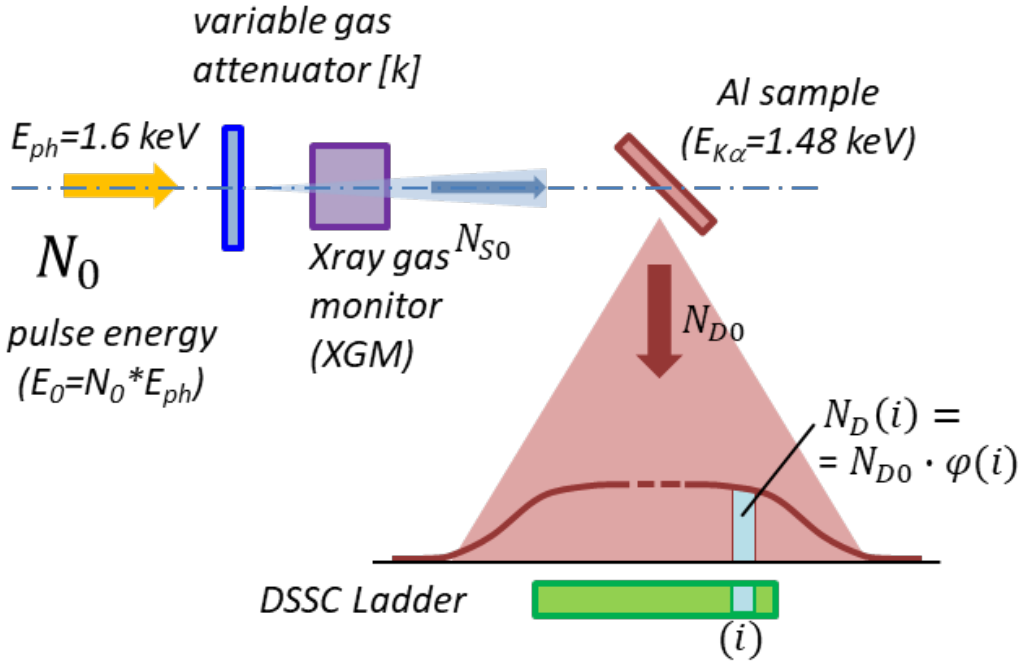
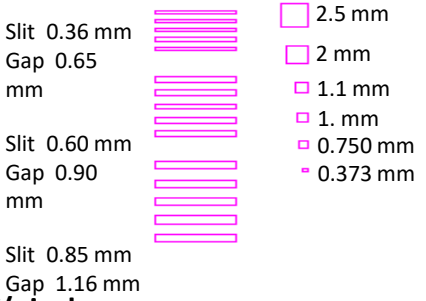
DEPFET-ladder prototype: *beamline tests*

1st prototype characterization at Small Quantum System (SQS) Instrument in two beamtimes @ EuXFEL

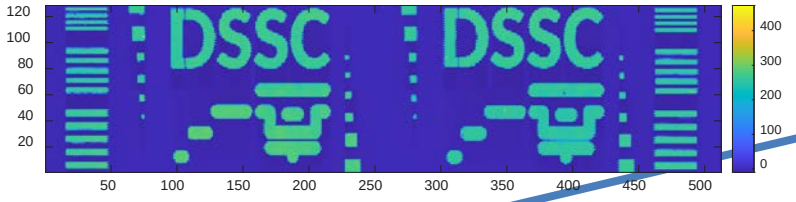
- XFEL beam on Al target
- DEPFET ladder mounted in Grifone vessel in a branch of the interaction chamber perpendicular to the XFEL beam in order to collect Al fluorescence photons (Al Kα 1.48 keV).
- Beam intensity on the Al target finely trimmed by a gas attenuator.



Steel, 0.5 mm



Run167, E~2 MeV/pixel



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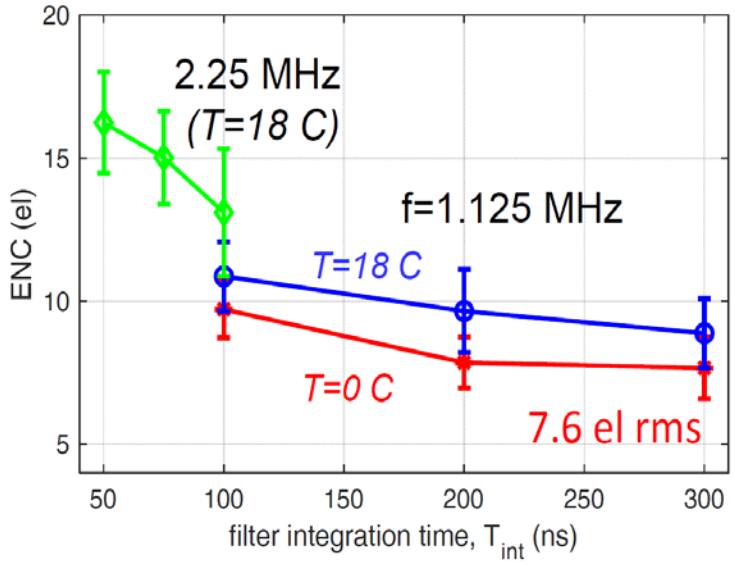
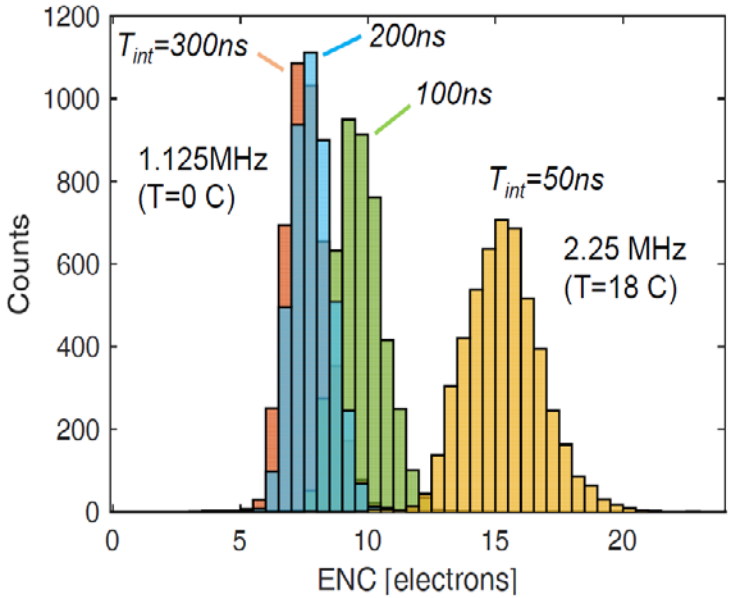
Results from Beamline Tests with Al $K_{\alpha K}$ radiation

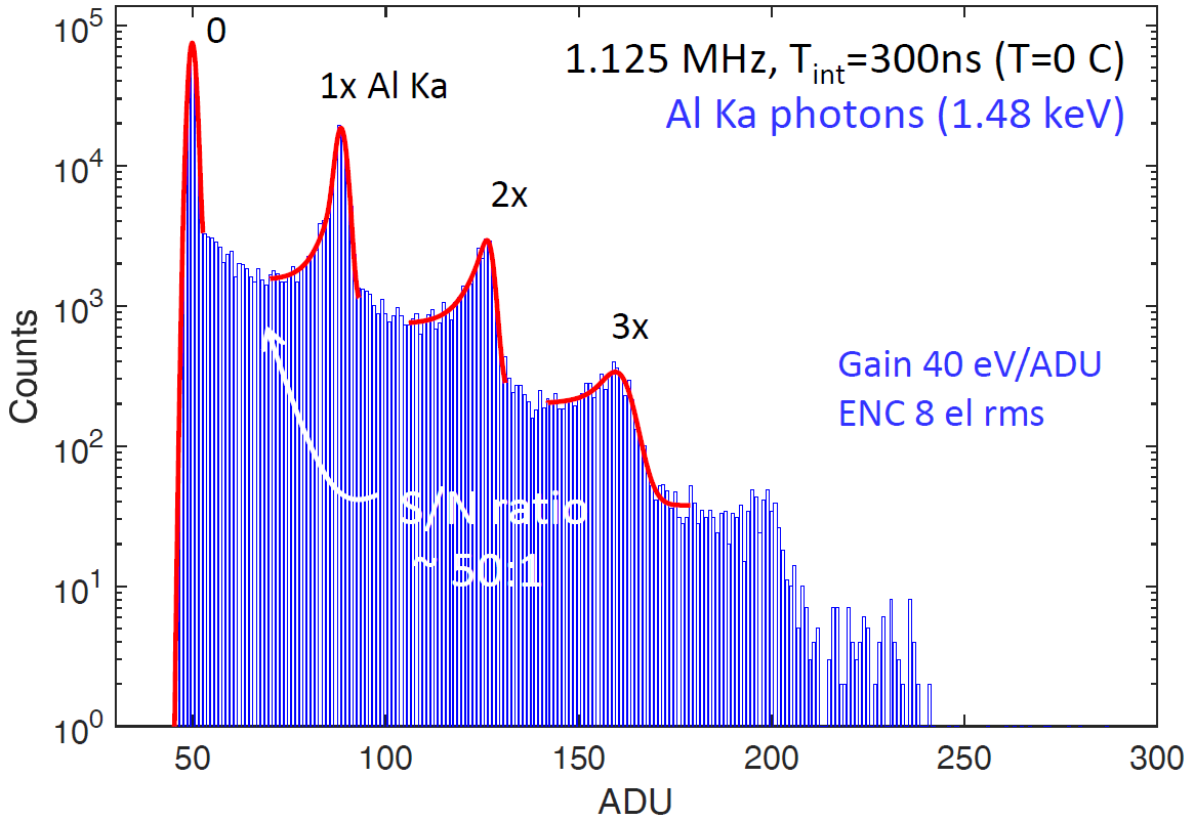
- ENC vs. integration time



Centroid and 1-sigma error bar of ENC vs. integration time



histograms of ENC (selected configurations)



- for readout freq. < 4.5 MHz, int. time can be increased to optimize noise
- Small further improvement by cooling to T=0 °C, best ENC < 8 el rms.
- Combination of high gain (40 eV/ADU) and low noise: single-photon resolution at Al Ka peak with Signal/Noise 50:1 (low intensity cases)

Boundary Conditions

- ASIC was designed to operate at 4.5 MHz in the XFEL burst mode
- The internal gate of the DePFET was designed to accommodate ≈ 10 MeV energy deposit (i.e. 10^4 X-rays of 1 keV)
- The pixel size was tailored to match the C4 bump bonding process conditions
- The 725 µm Si thickness guarantee safe operation up to 8 keV X-rays
- The radiation entrance window is covered with 150 nm Al as a shielding for the visible light

pixel size [µm²]	Format	active area [cm²]	ENC and fps	readout mode
300 x 300	64 x 64	3,6	4, 6600	rolling shutter
220 x 220	128 x 256	16	8, 14, 22, 1.1, 2.2 4.5 MHz	bump bonded
100 x 100	32 x 32	0.1	5, 12.000	RS
150 x 150	32 x 32	0,23	5, 12.000	RS
150 x 150	32 x 32	0,23	9, 20.000	RS

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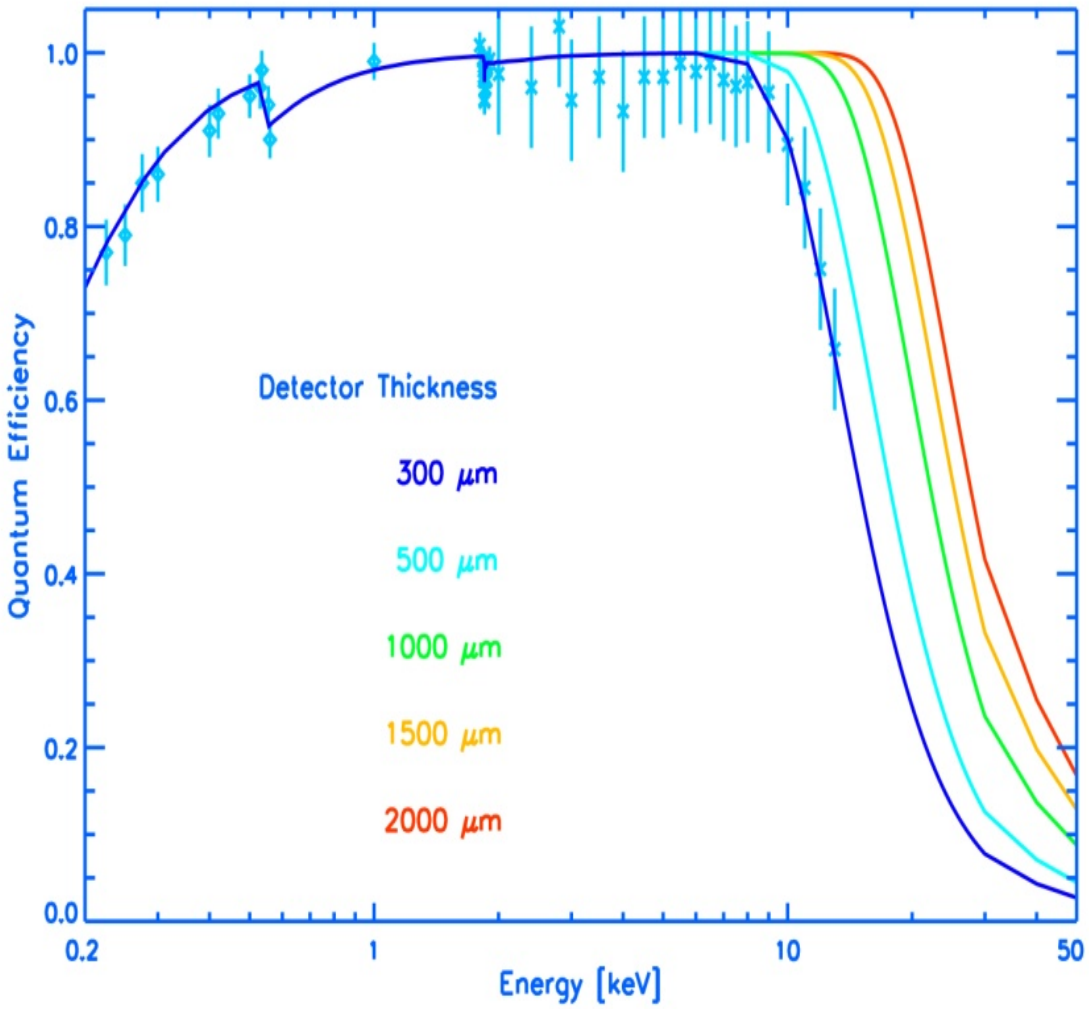

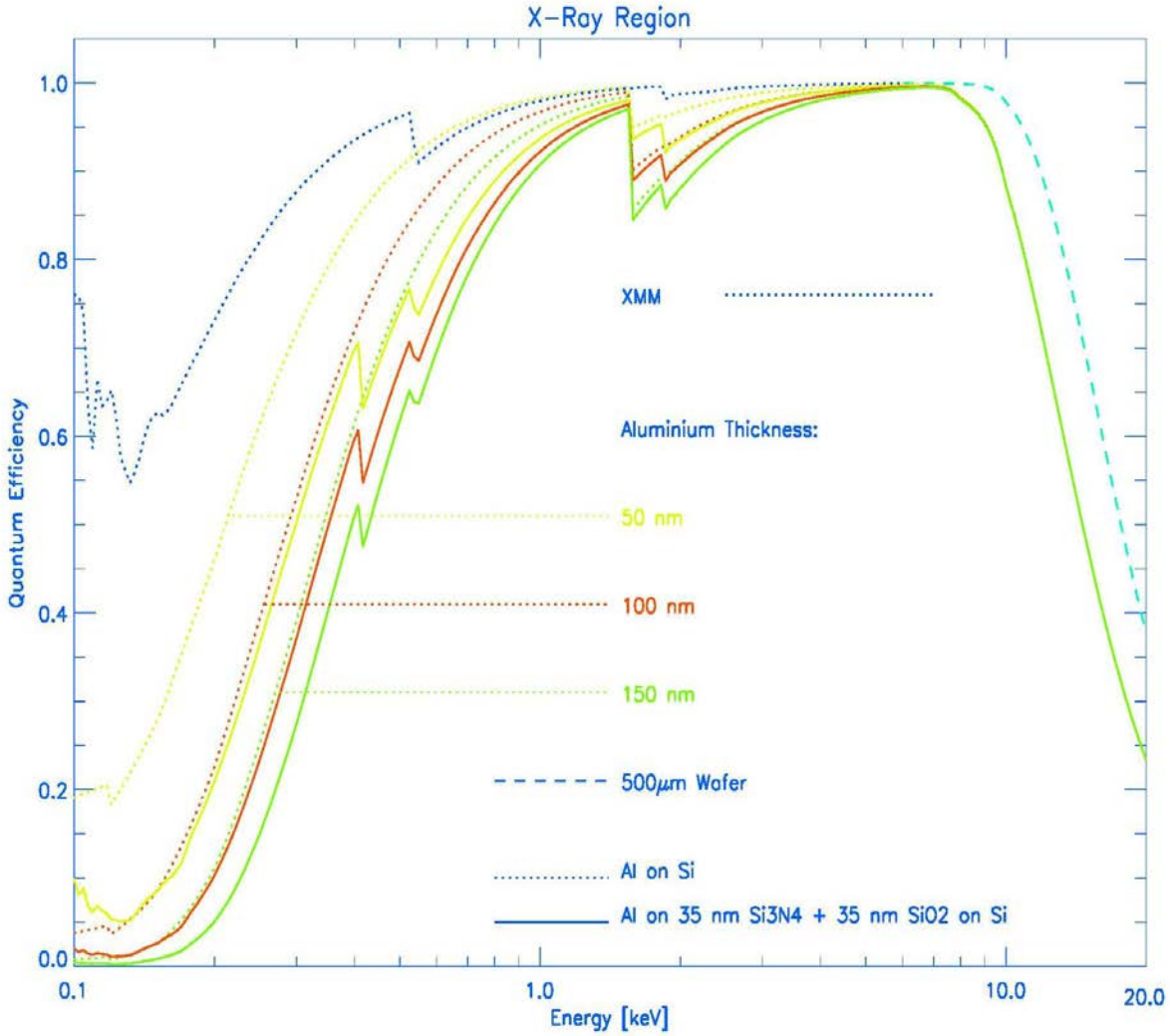

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EuXFEL parameters for soft X-ray instrument

	Target values	
Sensitive Energy Range	0.4 - 3 keV, possibly higher	
Dynamic range in photons	> 5 x 10^3 1 keV ph./px	500 - 1000 1 keV ph./px, one gain
Noise (ENC)	< 30 el. rms ~0.125 keV photon in Silicon	
Frame rate	Burst mode, 1.1 MHz	Burst mode, 1.1 - 4.5 MHz
Sensor type	2D pixelated	
Pixel size	80 - 100 µm pitch	
Pixel count	Move away from fixed large detectors, modular approach, max 4 Mpix	
Operating pressure range	< 10^{-6} mbar	

Why not cover the full water window ?

Okay with DePFETs

ENC < 15 el. possible with DePFETs @ 2.2 MHz

Okay with DePFETs

Okay with DePFETs

Okay with DePFETs

Okay with DePFETs

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Possible improvements for the next generation

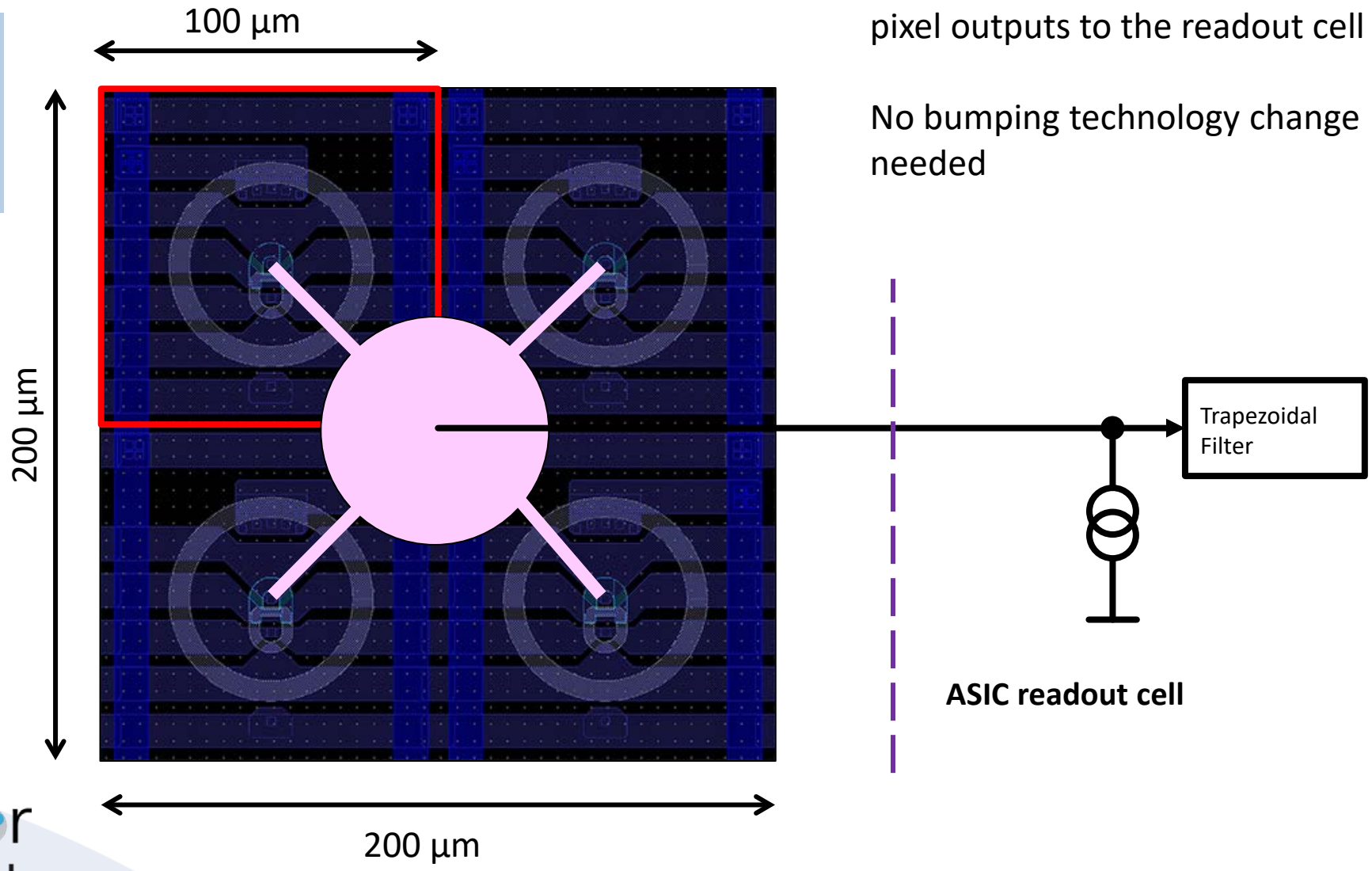
- reduce pixel size (possible from 50 µm to 150 µm)
- reduce switching voltages
- implement MOS switches on the CMOS sensor
- reduce power consumption
- implement shutter features, in-pixel-storage features
- consider back side treatment in collaboration with IMS
- consider thinning of the sensors
- optimize on-chip wiring
- reducing dead area at the sensor boundaries
- . . . .

Pixel size considerations

- One straightforward strategy is to reduce the pixel size of the DePFET to 75µm – 100µm through **pixel-by-pixel bump bonding**
  - No change in DePFET technology needed
  - In this case the ASIC has to include all required features on a smaller footprint
  - A choice for the ASIC has to be made whether cw or bunch mode operation is desired. Before starting the DePFET manufacturing a preliminary ASIC layout has to prove whether it can integrate all required features on the pixel footprint. The CMOS technology may need to shrink down to 28 nm. Power consumption issues must be studied
  - The DePFET layout can remain identical for both cases, cw or bunch mode
  - The bump bonding footprint may need to be reduced to approx. 20x20 μm^2
- Another strategy could be to share one output node with 4 neighboring pixels
  - This requires a different DePFET design, but no change in DePFET technology is needed
  - This concept may save space for the CMOS circuit
  - The bump bonding footprint can stay relaxed as it is now

Example of pixel clustering

This option was proposed by Matteo Porro in 2019 !



One single bump connects the 4 pixel outputs to the readout cell

No bumping technology change needed

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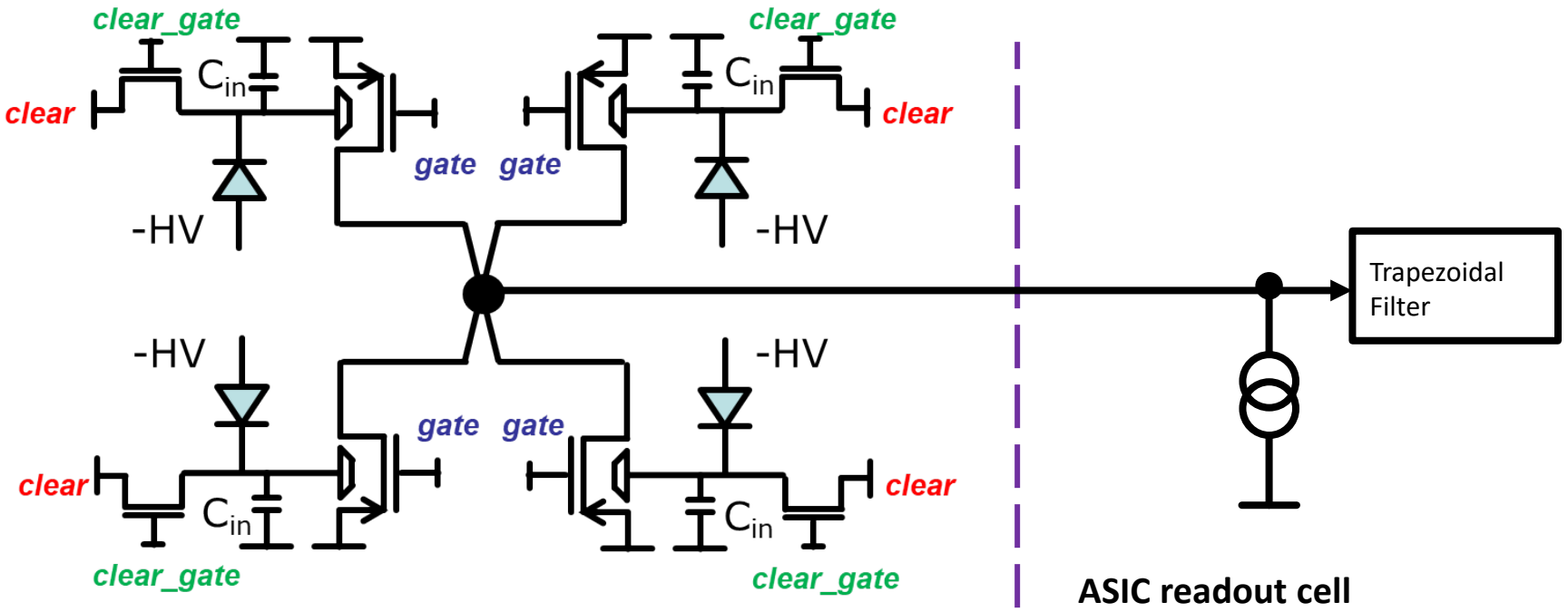
Example of pixel clustering

- Every DEPFET has 3 independent control signals: gate, clear, clear gate
- The 4 drains are connected
- The source is common to the whole matrix

One single bump connects the 4 pixel outputs to the readout cell

No bumping technology change needed



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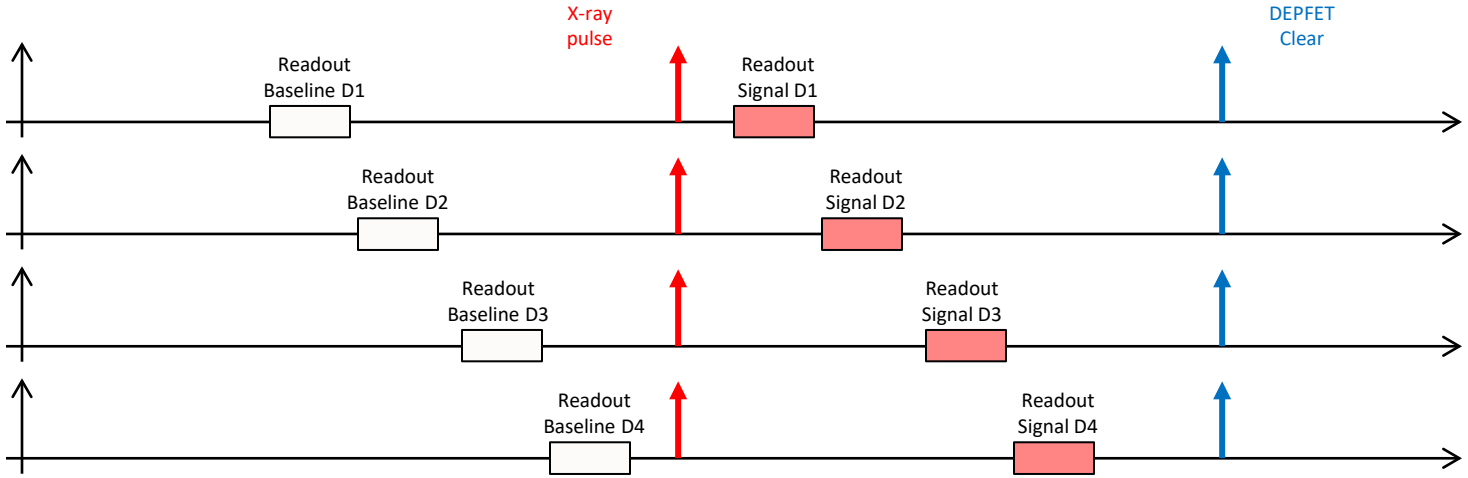
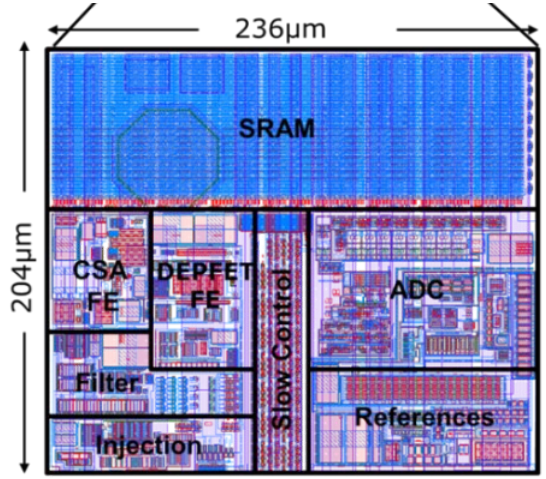
First Readout Strategy



- The baseline of all four pixels is read-out first
- The signal + baseline of all four pixels is read out in a second phase
- DEPFETs collect charge in OFF state
- 4 CSAs and 4 Filters in one cell (1 CSA with 4 independent caps maybe possible)
  - ➢ Area occupancy is critical: compromise in gain settings; SRAM to be reduced
  - ➢ Complex power management
- 1 shared ADC per cell (4 S&H caps)
- Clear and clear gate require only a single line



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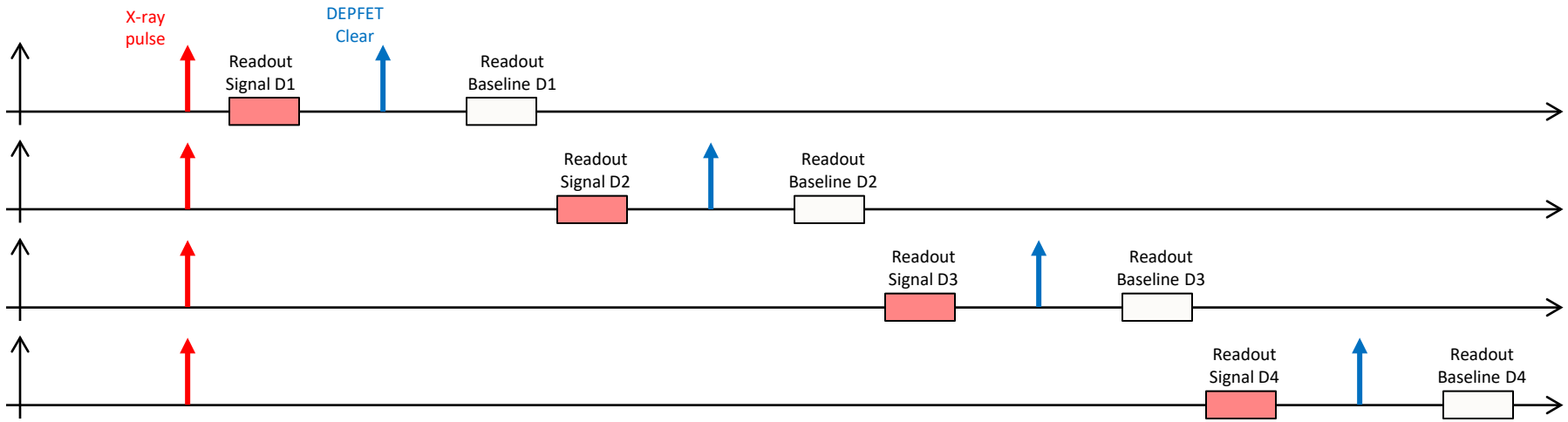
Second Readout Strategy



- The DEPFET pixels collect the charge in OFF state
- A complete readout cycle per pixel is performed. Pixels are read out sequentially.
- The current subtraction must be performed before every readout cycle or 4 current sources are needed
- The signal + baseline must be read out first
- **The entire readout channel is shared among 4 pixels**
- The **polarity of the analog readout has to be inverted** (new design needed!)

First steps towards a new generation of DePFETs

- basic properties of the new DePFETs can already be studied on existing 100 x 100 µm^2 and 150 x 150 µm^2 DePFETs on 32 x 32 matrices
- available experimental data should be analyzed on 75 µm pixel devices to study the impact of pixel size on scientific output
- a design study of the new DePFET sensors can be started with the implementation of new desired features
- ASIC design, layout and simulation should be considered in the two possible technologies: 65 nm and 28 nm to find out the footprint of the realistic minimum pixel size.

Start as early as possible !

Summary

Sensor

- Reduction of pixel size is possible
- Basically no technology change needed
- BUT: technological improvements could be studied
- Speed requirements can be implemented
- Before starting fabrication ASIC feasibility must be verified
- Noise performance, dynamic range, energy bandwidth, speed and formats have already been demonstrated.
- Ideas of the implementation of new features can be studied early on
- **PNS/PND is able to start new developments**

ASIC

- choice of technology must be made at an early stage
- depending on the required functionality the pixel footprint must be verified
- The development of a dedicated ASIC is th biggest challenge in this approach