Characteristics of ARCADIA Fully Depleted MAPS and Perspectives for X-ray Imaging at XFELs

"Future Detectors for the European XFEL" Workshop

18-19 September 2023

Lucio Pancheri[1]

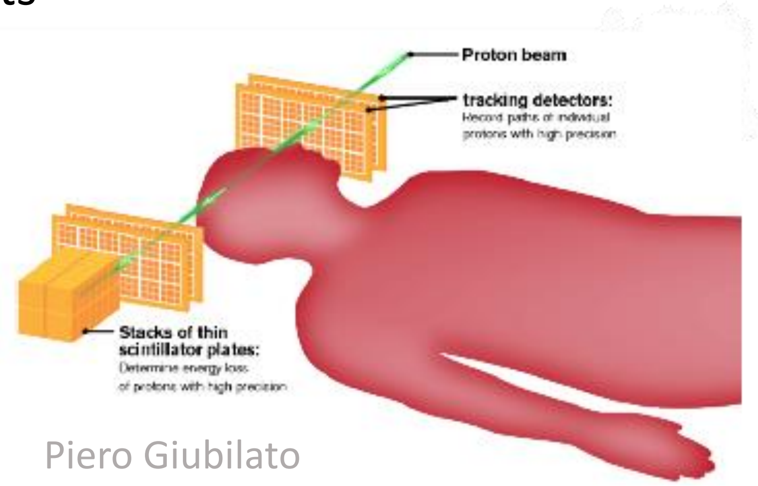
on behalf of the ARCADIA collaboration

[1]University of Trento and TIFPA-INFN

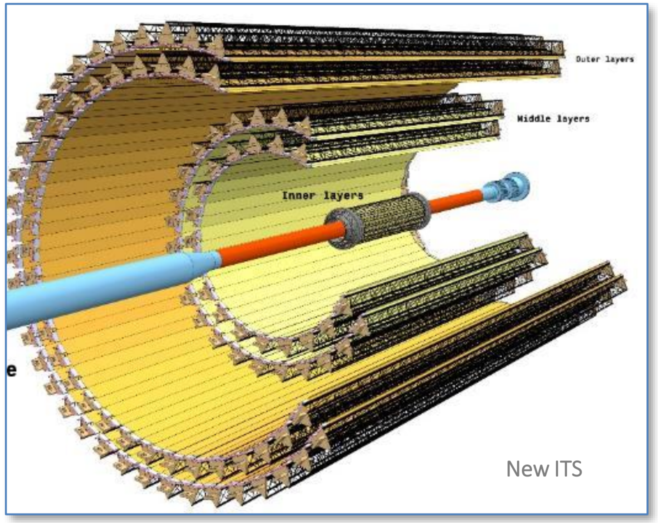
Motivation

- ARCADIA (Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays): INFN-funded R&D to develop a versatile monolithic process for large-area **monolithic pixel detectors**
- Based on **LFoundry 110nm CIS** process
- Target **applications**:
  - Medical imaging (e.g. Proton Computed Tomography)
  - Astro-particle detection on satellites
  - High Energy Physics experiments
  - X-ray detection

CSES-01



Piero Giubilato

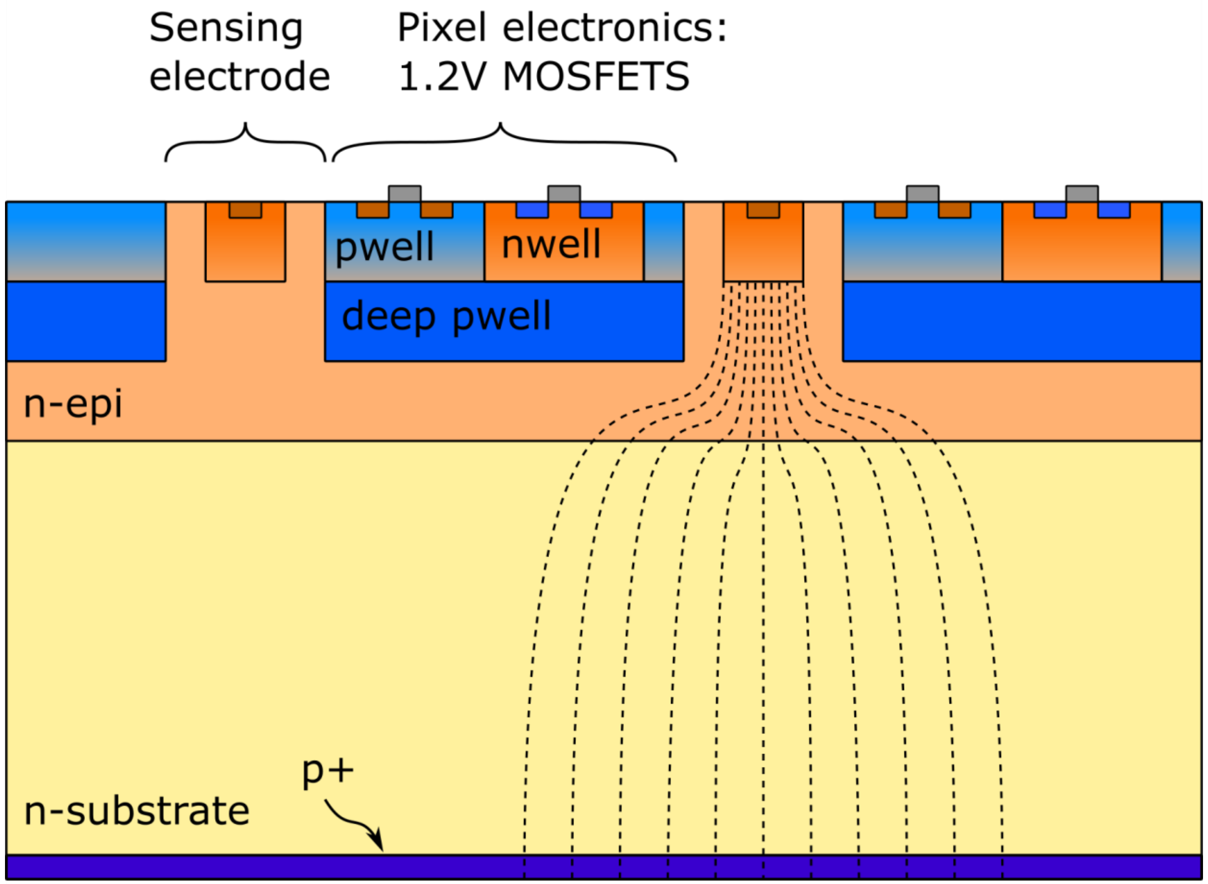


ALICE

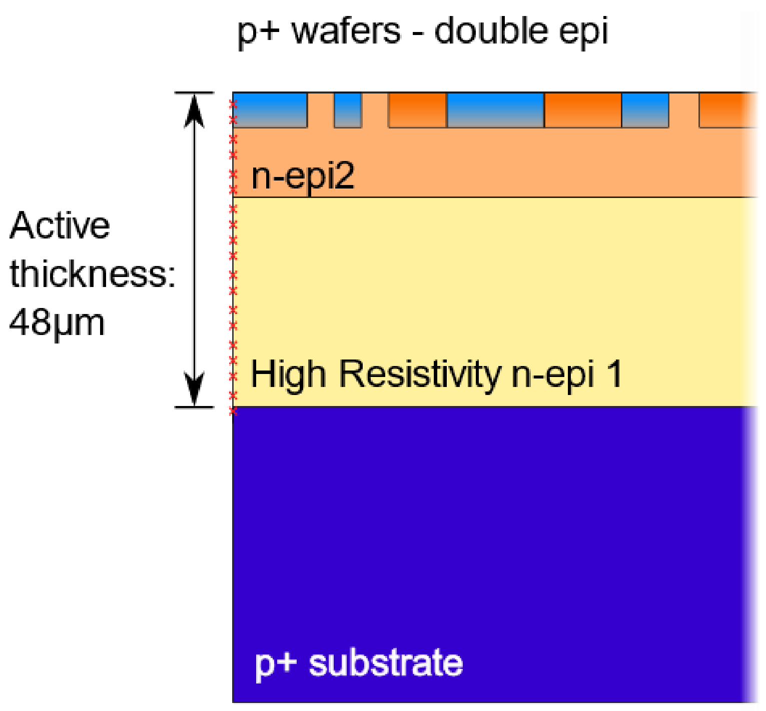
Joint patent INFN – LFoundry EP3701571B1 (priority 2017 – granted 2021)

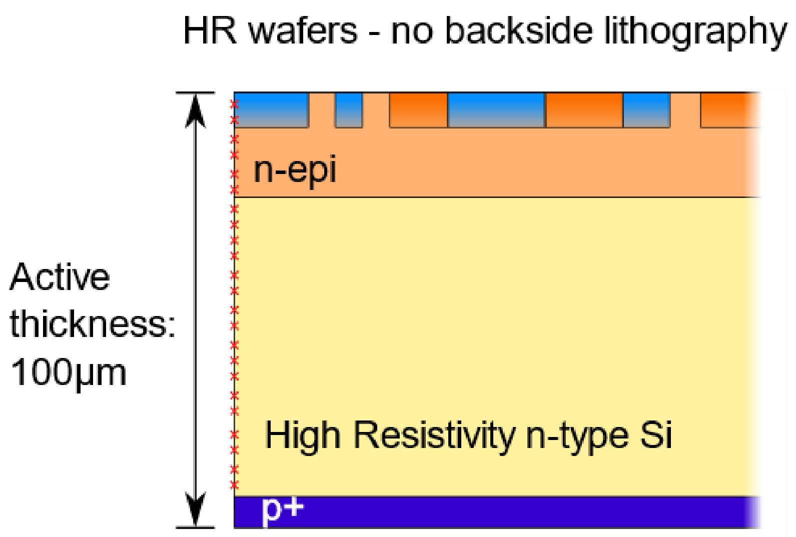
Sensor concept

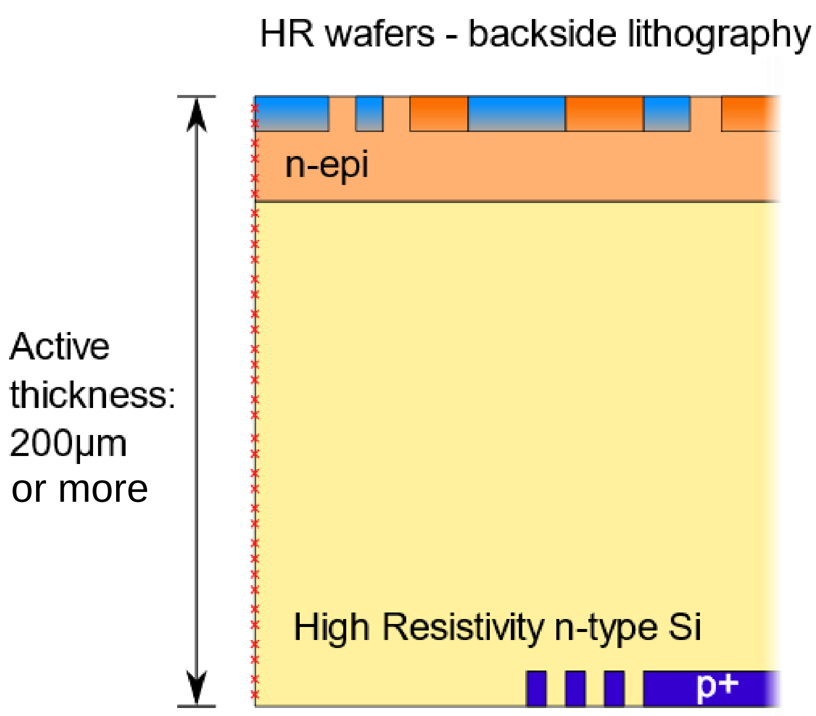
- Customized **110nm CMOS** process (LFoundry)
- n-type **high resistivity** active region
- Reverse-biased **junction at the bottom**: depletion grows from back to top
- **Sensing** electrodes can be biased at **low voltage** (< 1V)
- nwells with electronics shielded by **deep pwells**
- **n-epi** layer: reduce **punch-through** current between p+ and deep pwells



Wafer post-processing: starting material and backside process







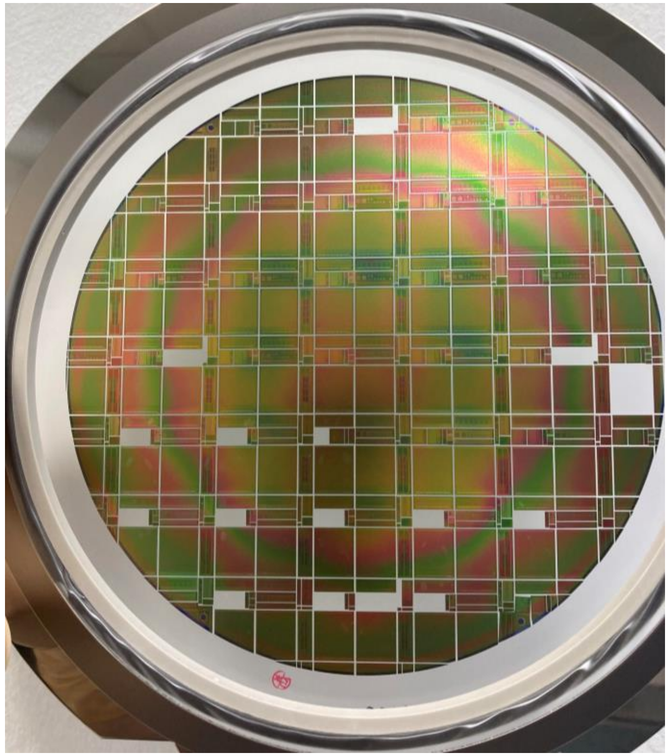
Type 1:
Post-processing: thinning to 100 or 300µm total thickness

Type 2:
Post-processing: thinning, backsided **p+ implantation** and laser annealing

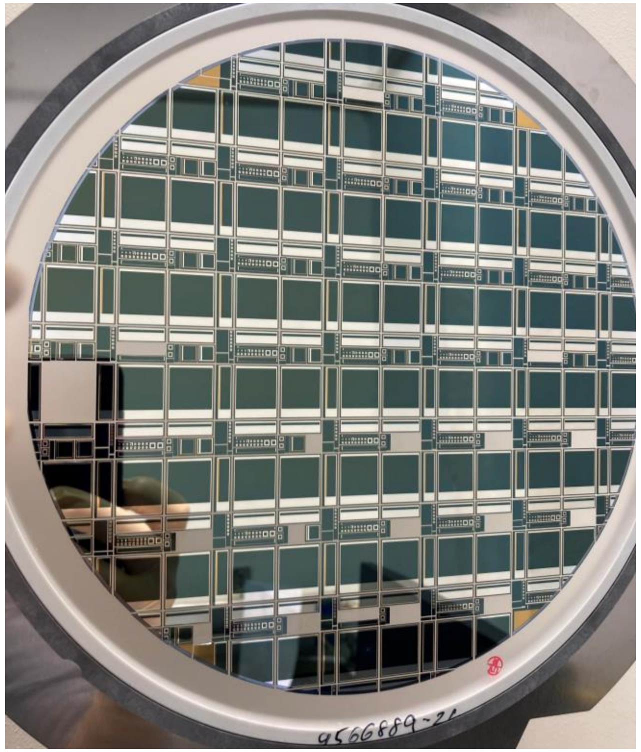
Type 3:
Post-processing: thinning, **lithography**, backside **p+ implantation** and laser annealing, insulators and **metal** deposition

Production

Front side

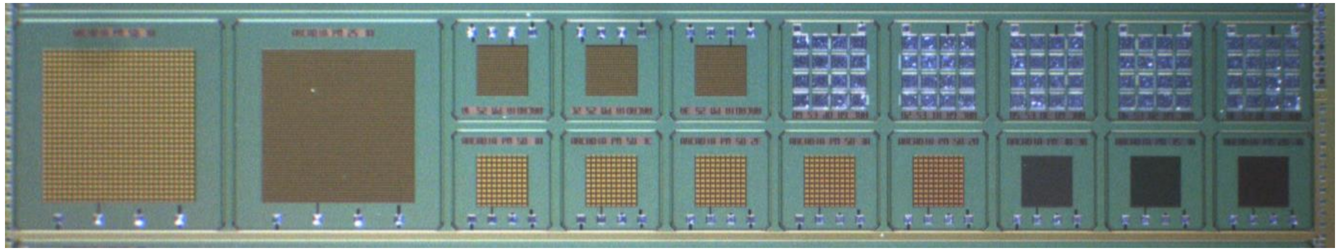


Back side



Devices produced:

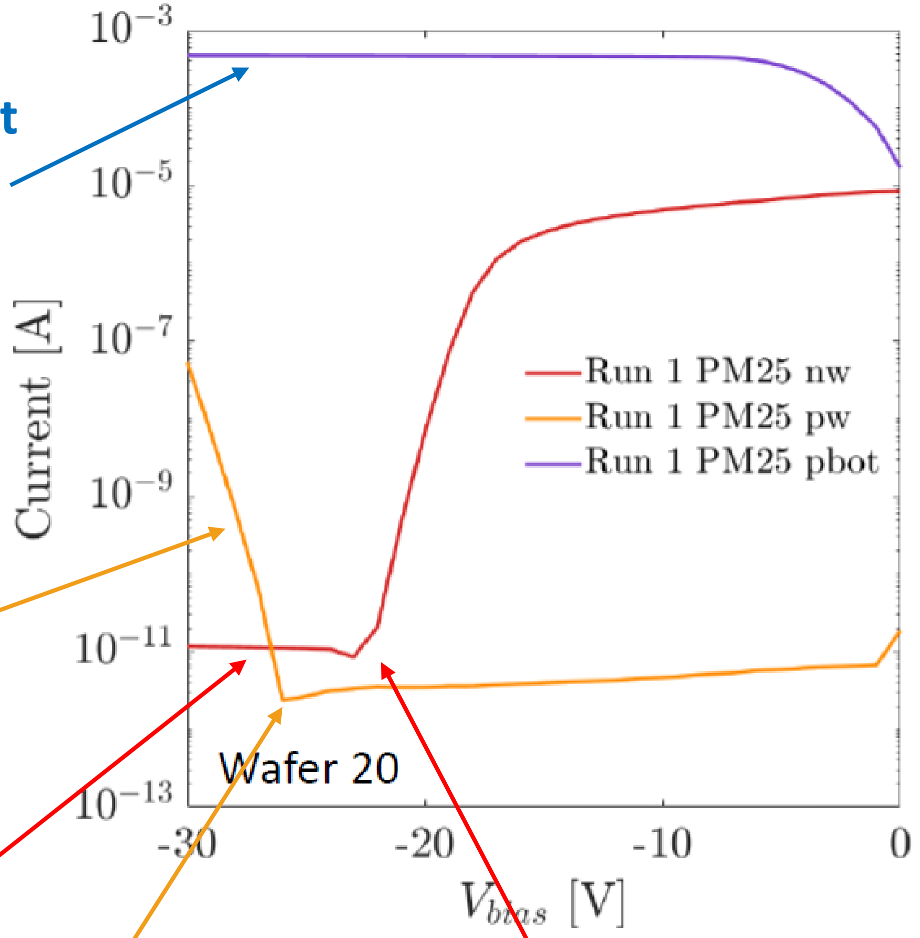
- Main demonstrator: 25µm **pixel** sensor - **512 x 512** array
- Small **pixel arrays** with different **pitch** (10 µm – 25 µm – 50 µm) with and w/o active readout
- **Strip detectors** with and w/o active readout
- **Test structures** for sensors characterization and process qualification



Micrograph of test structures block

Sensor characteristics - IV curves

Backside bias current (thermal generation at the dicing line)



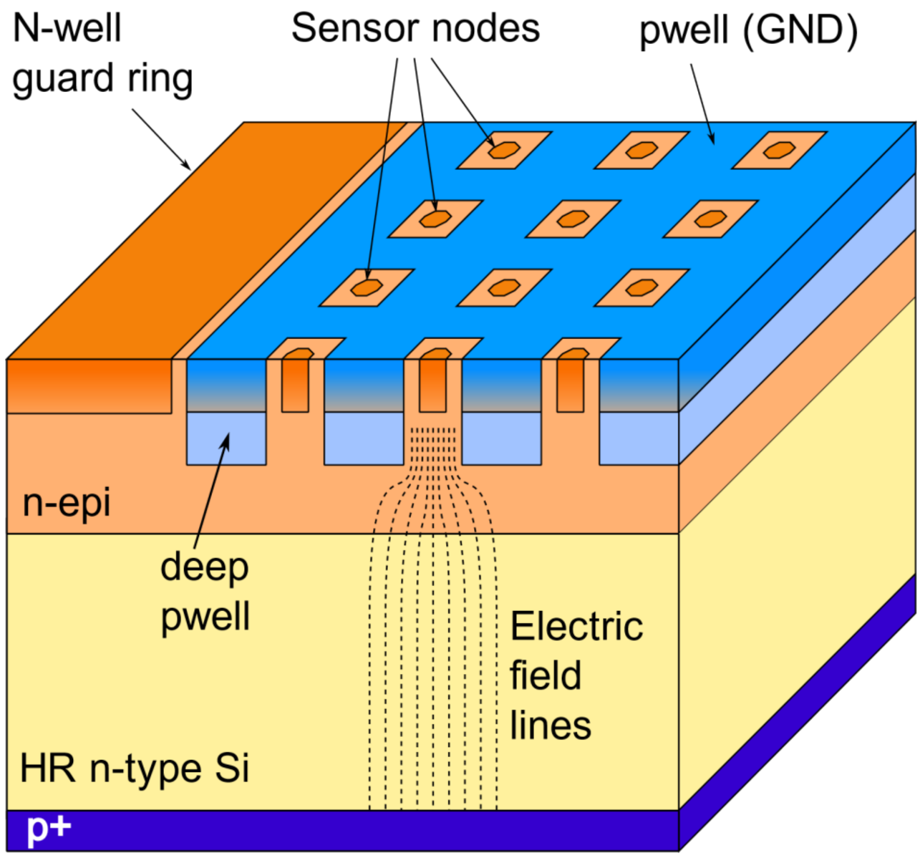
Pwell Punch-through current

Pixel dark current

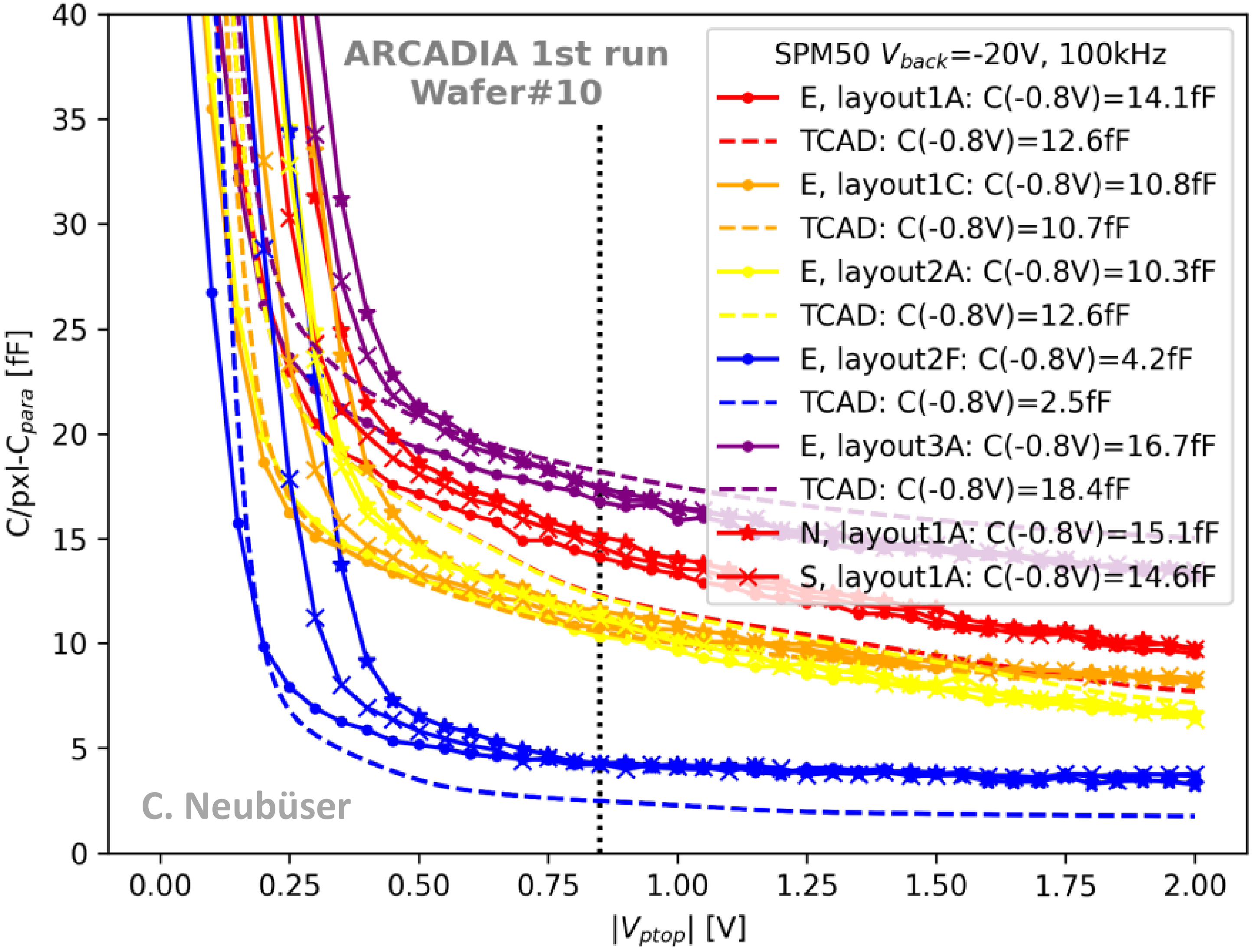
Punch-through onset voltage V_{PT}

Full depletion voltage V_{depl}

Measured on pixel test structures (arrays of pixels connected in parallel)

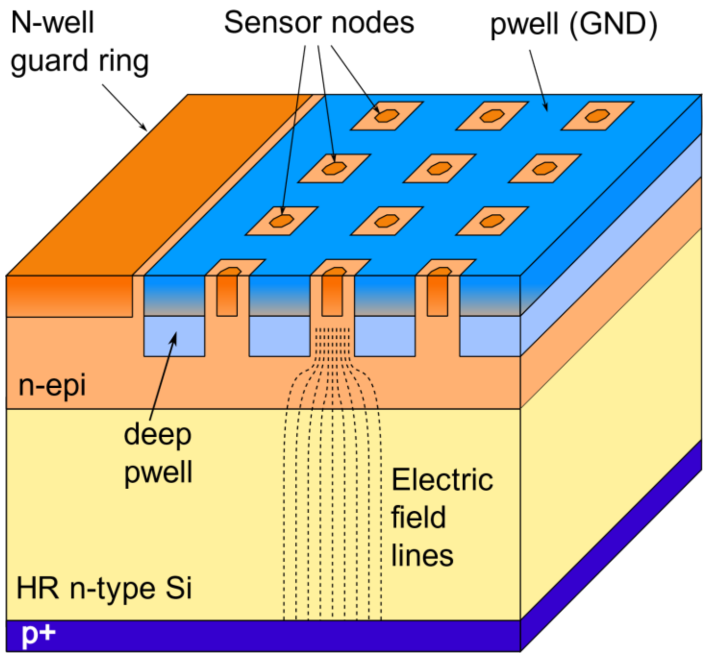


Pixel Capacitance-Voltage curves – comparison with TCAD models



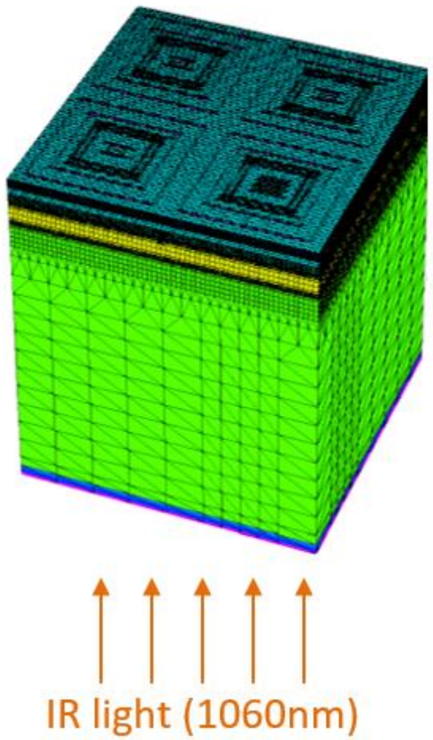
Experimental data for different pixel layouts – 50µm pitch – and comparison with **TCAD simulation results**

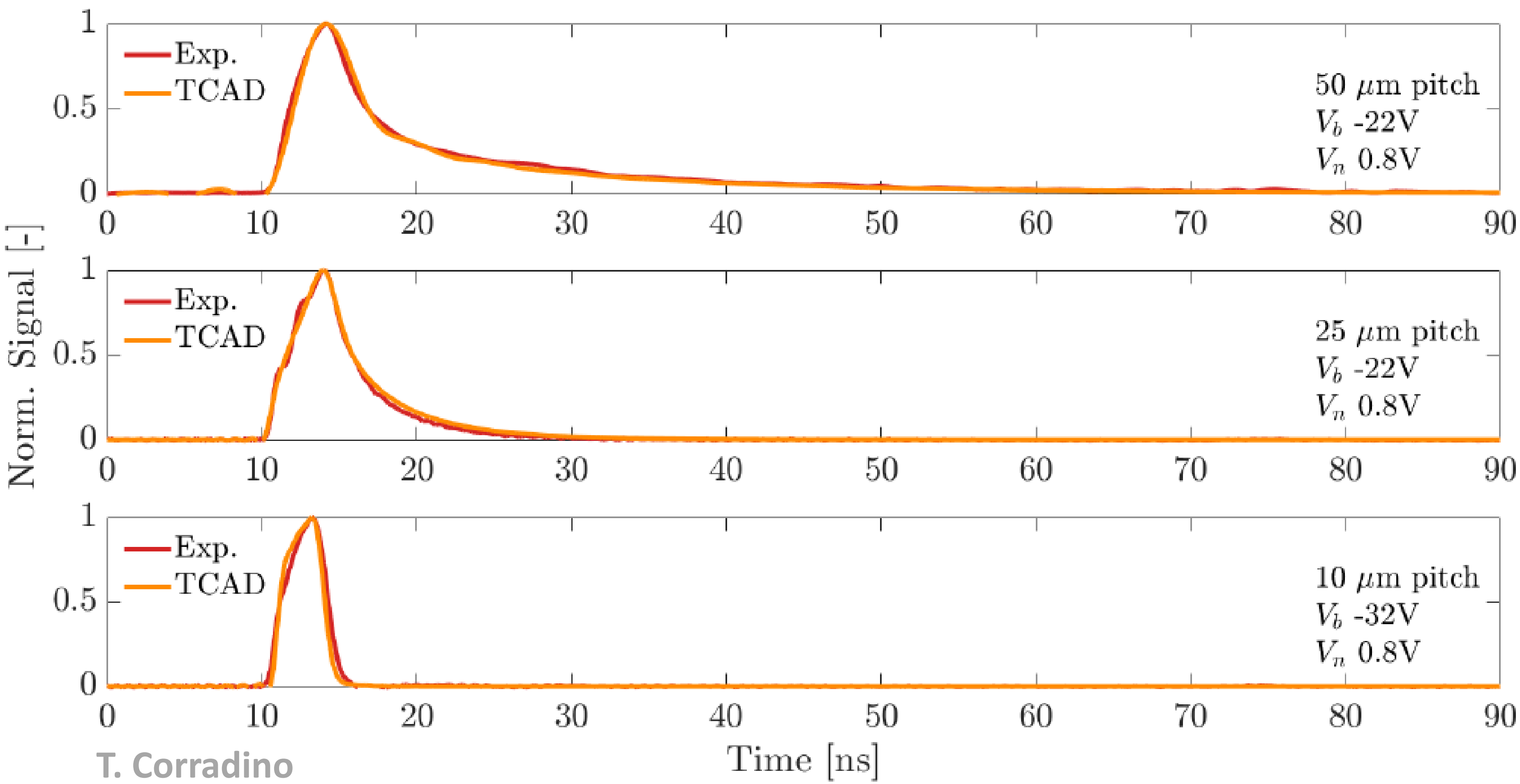
Capacitance is dominated by the **perimeter** of the sensor node



Pulsed laser characterization – comparison with TCAD models

Infrared laser diode @ 1060nm, < 100ps FWHM: generation in the whole active thickness
Pixel array test structures with **100µm active thickness** (maskless backside p+ implantation)

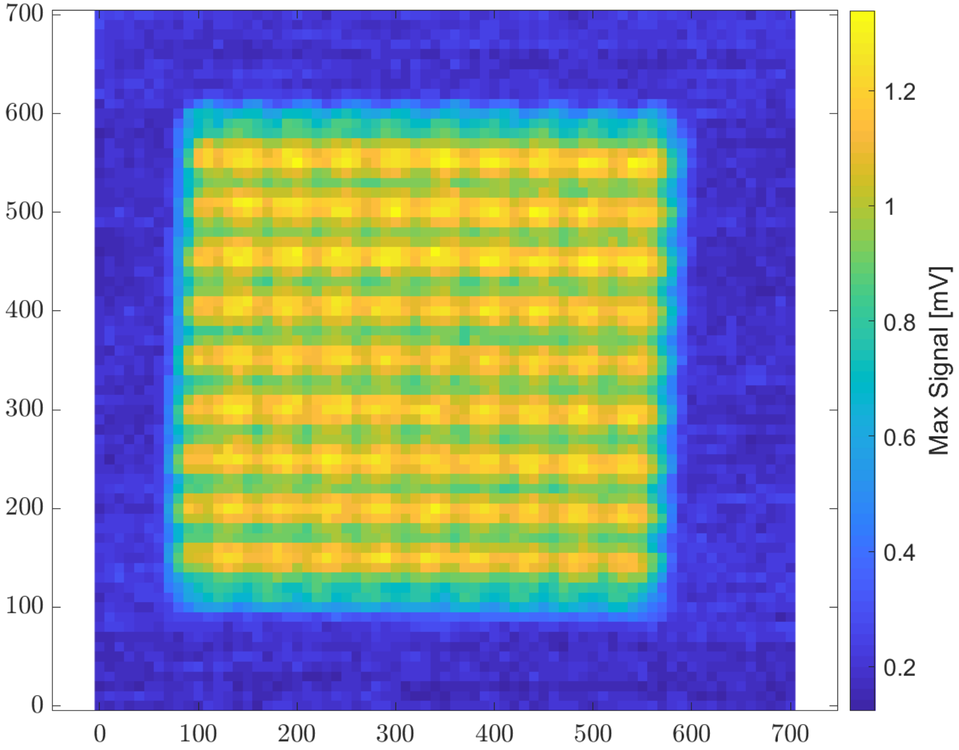




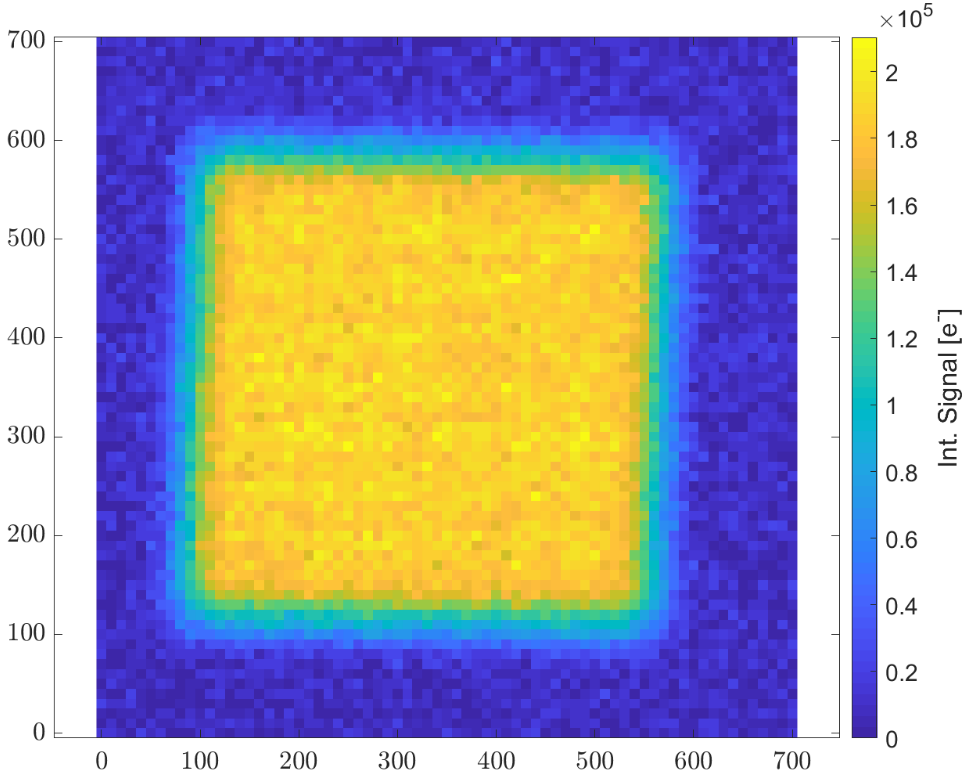
T. Corradino

Red laser scan – test pixel arrays

- 50 µm – pitch pixel test structures
- Focused red laser incident on the backside – spot size 10 µm FWHM
- Mechanical scanning with 10 µm step size in x and y

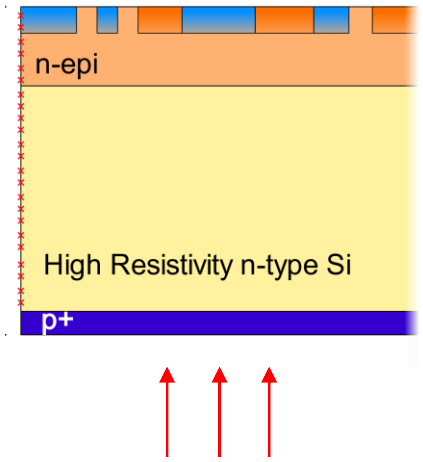


Signal peak amplitude: higher in the Pixel center (fast charge collection)

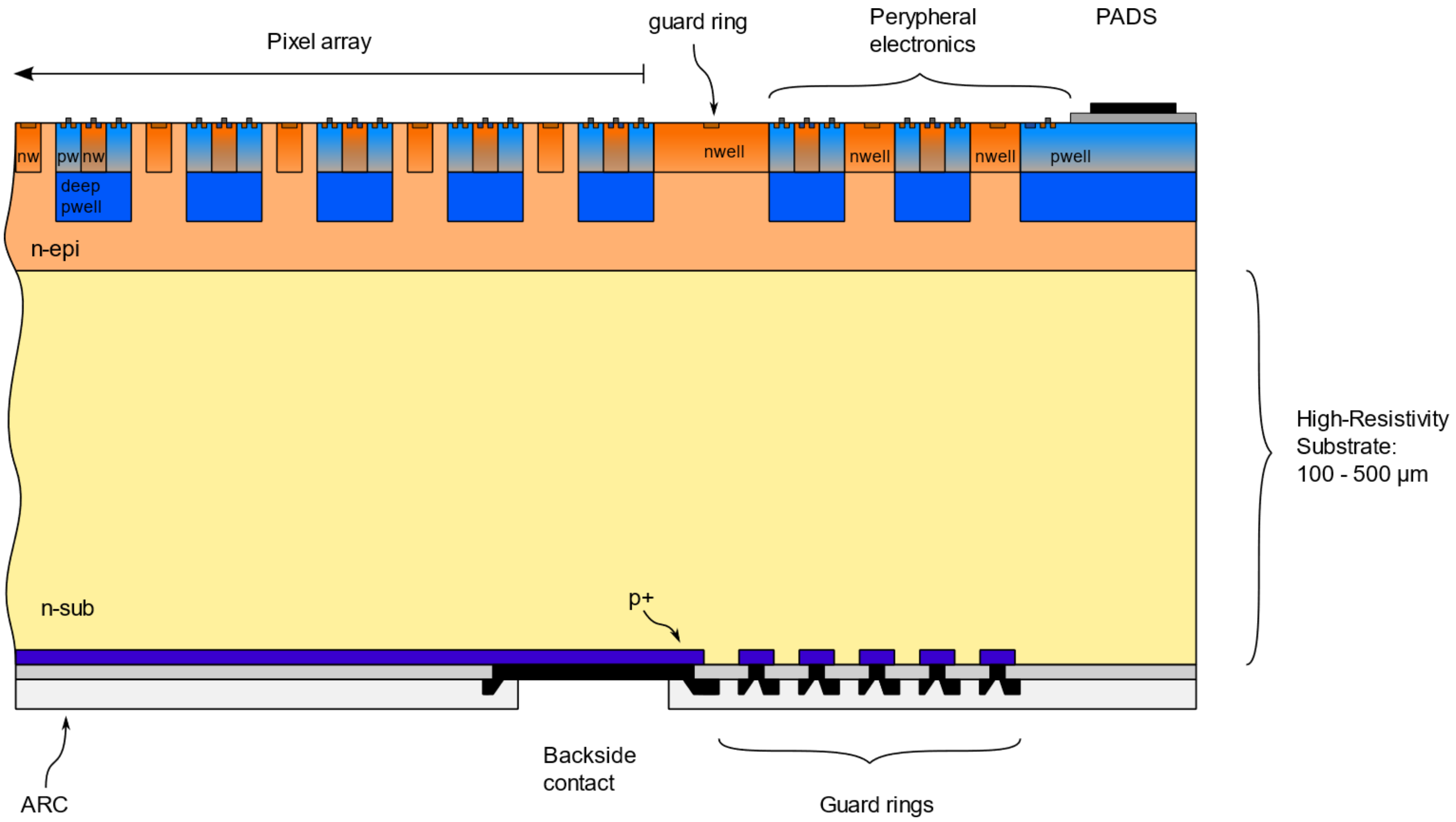


Integrated signal: uniform across the pixel array

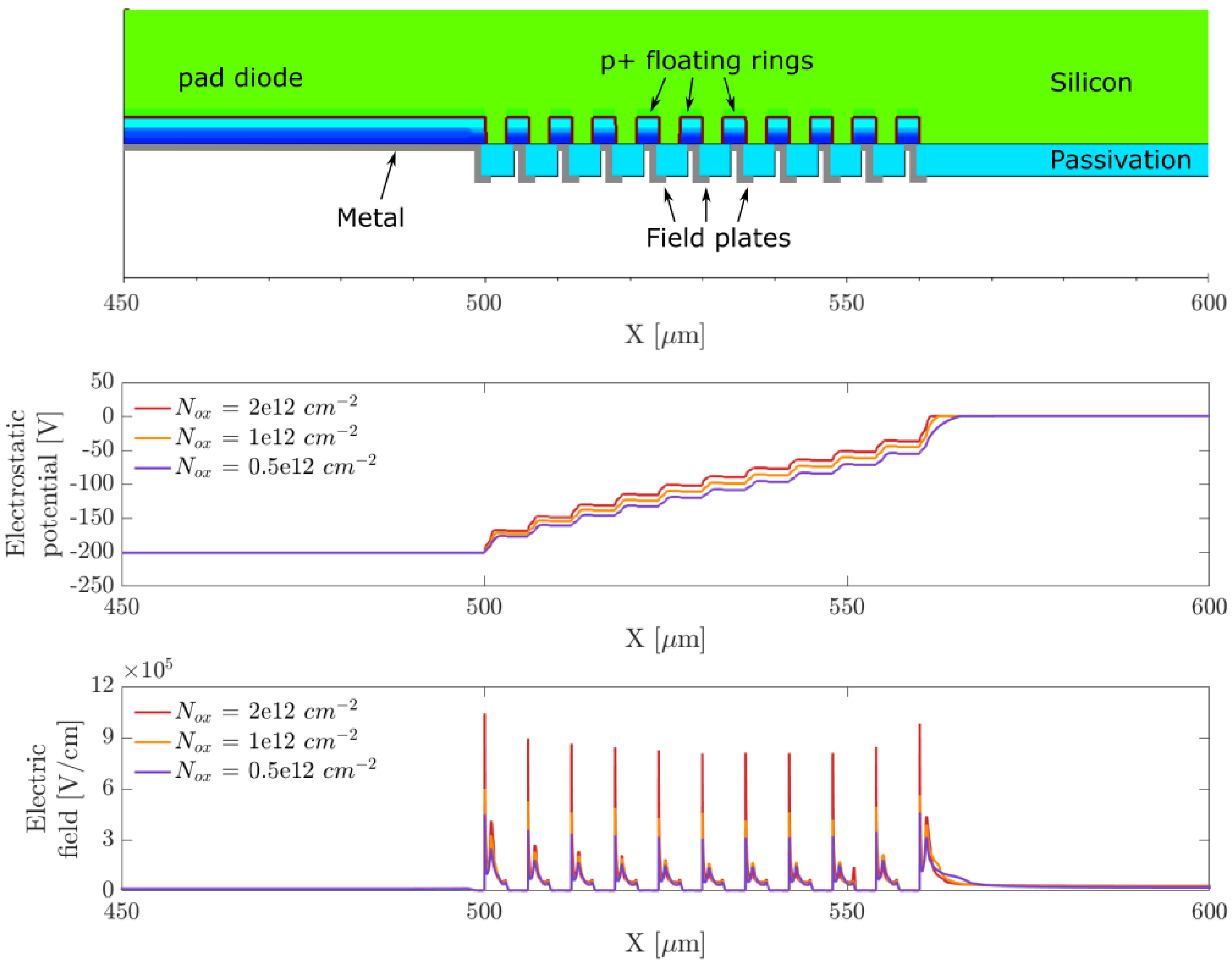
- Sensor voltage: 0.8V
- Backside bias: −22V



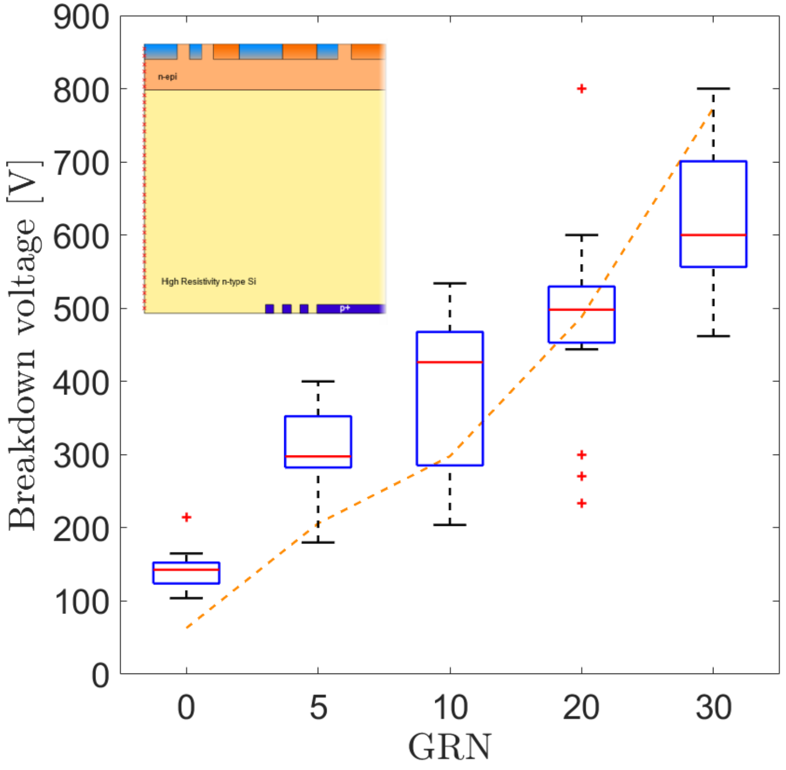
Pixel array cross section – backside lithography – type 3 substrates



Electrical characterization – backside termination



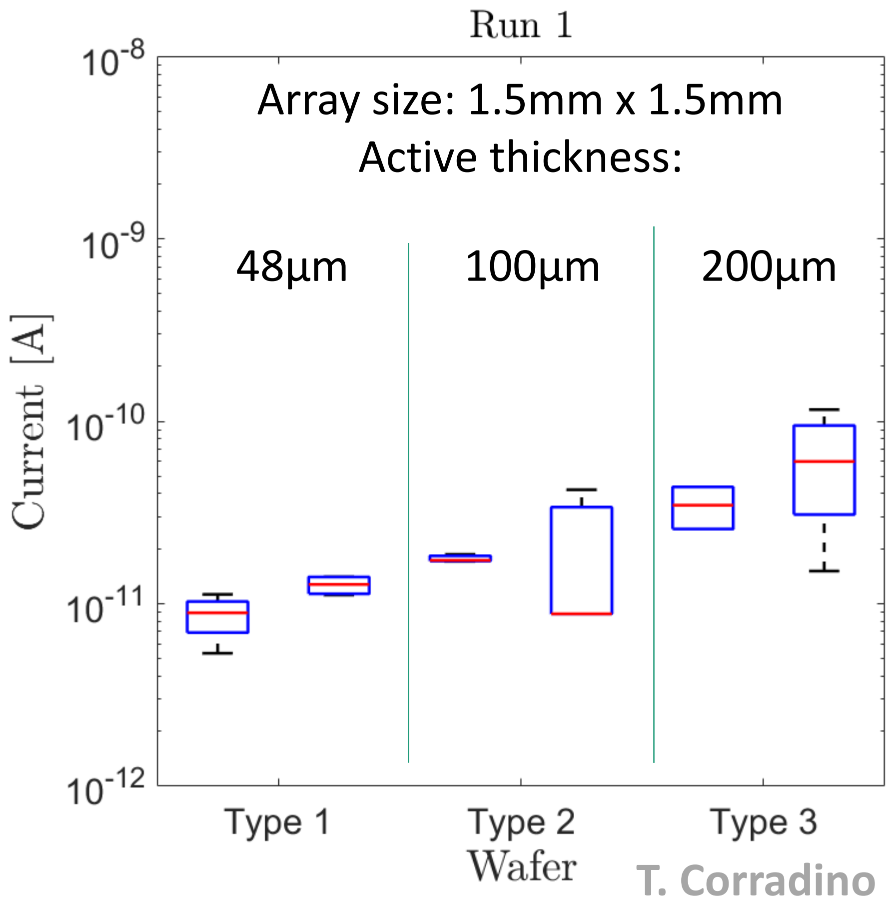
- Backside diodes with variable number of guard rings (GRN)
- Large bias voltage: possibility to deplete a **thick sensor (tested up to 400μm thickness)**



T. Corradino, Sensors 2021, 21(11), 3809
https://doi.org/10.3390/s21113809

Pixel characteristics

- Measured on pixel test structures
- Pixel dark current roughly proportional to sensor thickness



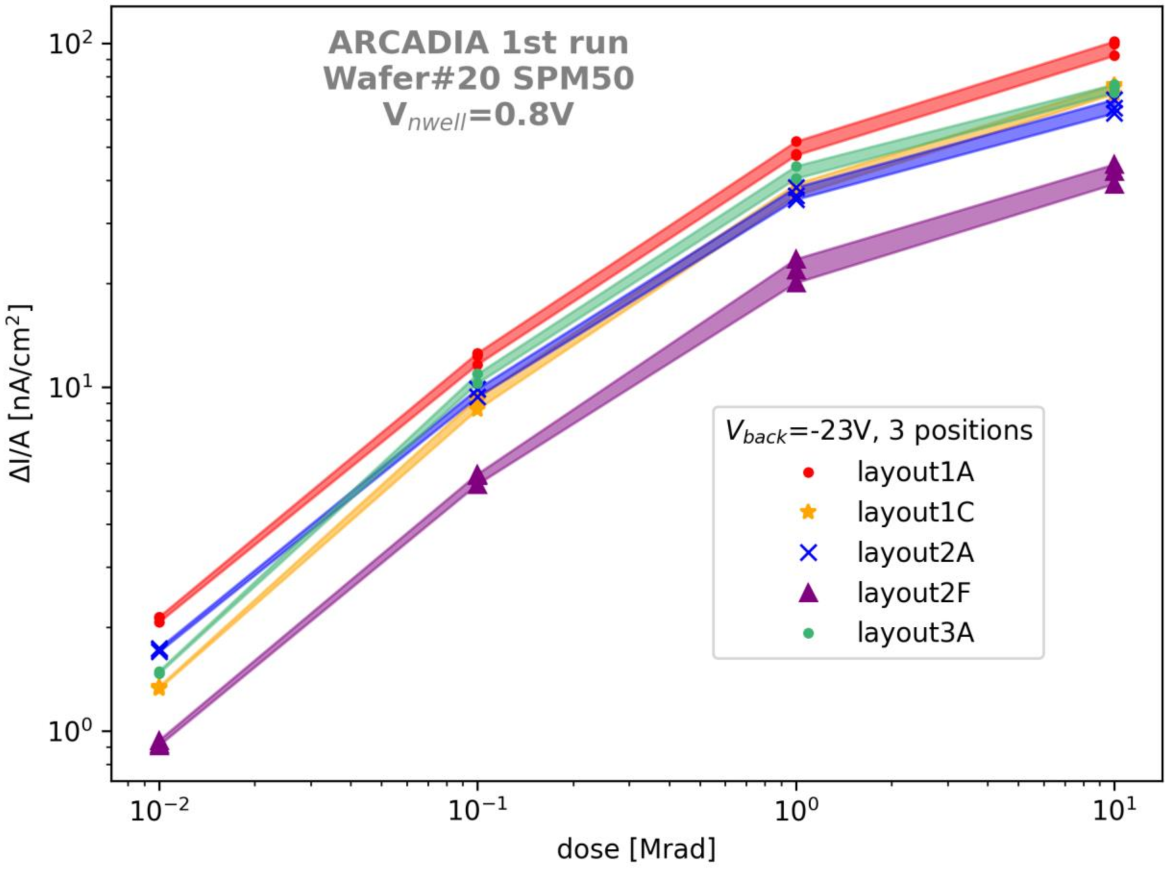
T. Corradino

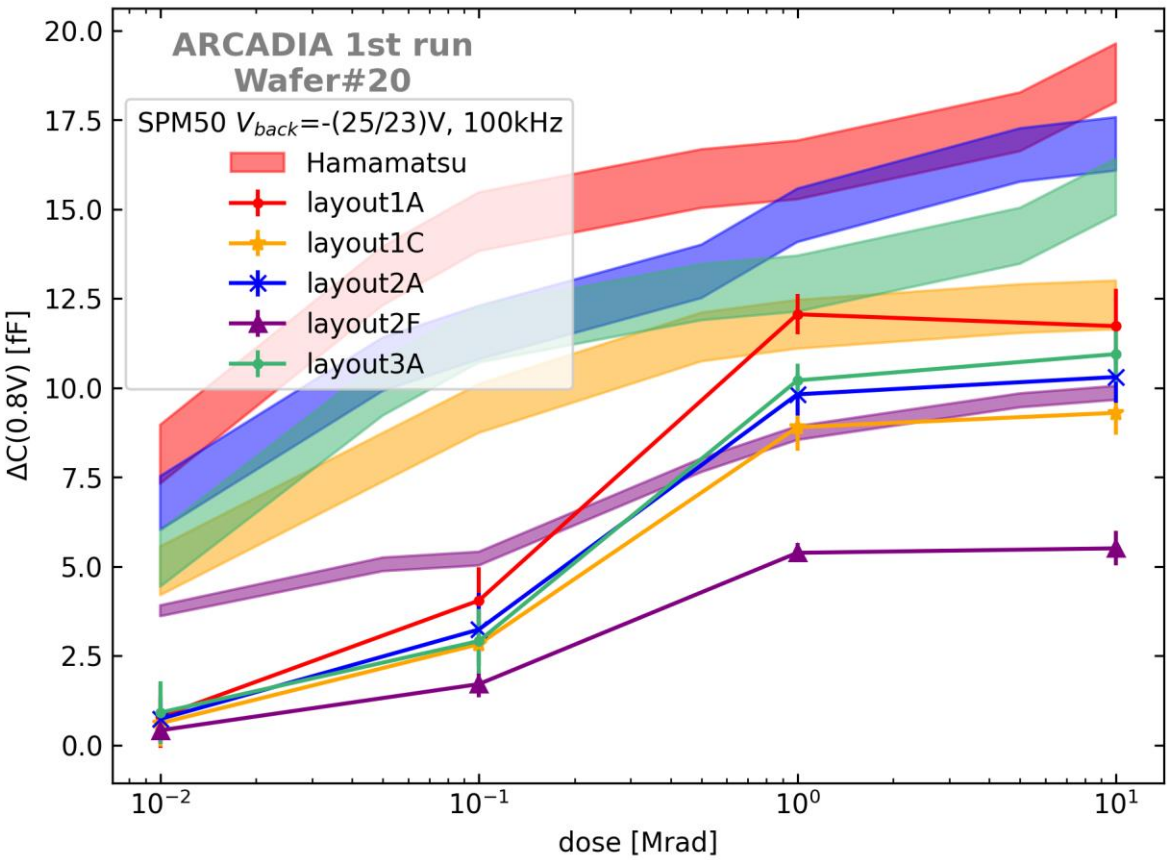
Sensor characteristics vs. active thickness.			
Active thickness (µm)	48	100	200
Sensor bias voltage (V)	25	20-35	60-100
Dark current density (pA/cm^2)	100-350	230 - 500	650 - 2000

Sensor characteristics vs. pixel size (@ 100µm active thickness)			
Pixel pitch (µm)	10	25	50
Sensor area (% of pixel area)	36%	19%	16%
Sensor capacitance (fF)	1.9	3	12.7
Time for 90% charge collection with picosecond IR laser (ns)	4	10	31

Pixel radiation hardness – ionizing radiation

TID with X-rays – Irradiation @ university of Padova, Italy
Main effect: increase of pixel leakage current and capacitance with dose

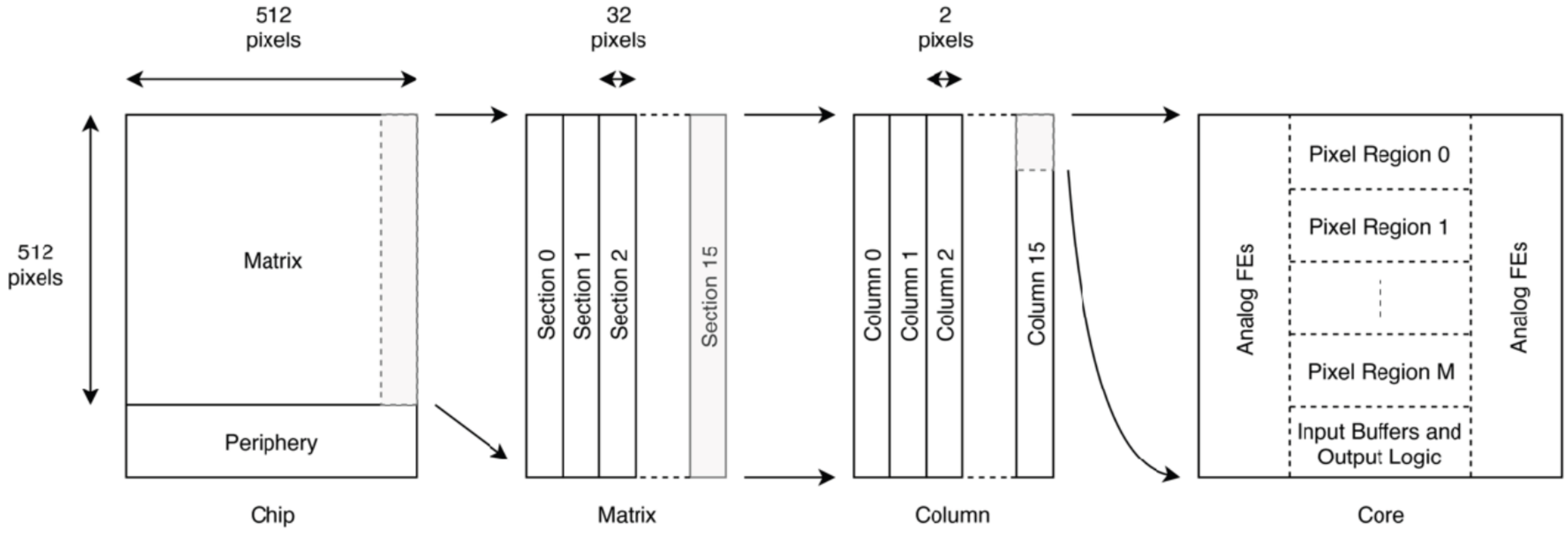




C. Neubüser

Main demonstrator: 512 x 512 pixel array for charged particle tracking

- Pixel pitch: 25µm – Array core area: 1.28cm x 1.28cm
- **Pixel** electronics: **analog and digital**. In-pixel threshold and data storage
- Architecture: **event-driven**. Pixel detecting events (charge pulses) send their address to the chip peripheral circuits
- Low **power** (20mW/cm^2) and high **event rate** (100 MHz/cm^2)



M. Rolo

ARCADIA Main Demonstrator – chip floorplan

ARCADIA

Top Padframe
Auxiliary supply, IR Drop Measure

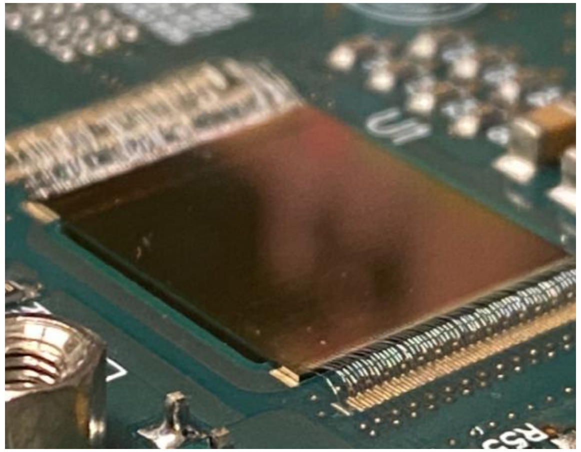
Matrix
512x512 pixels, Double Column arrangement

End of Sector (x16)
Reads and Configures 512x32 pixels

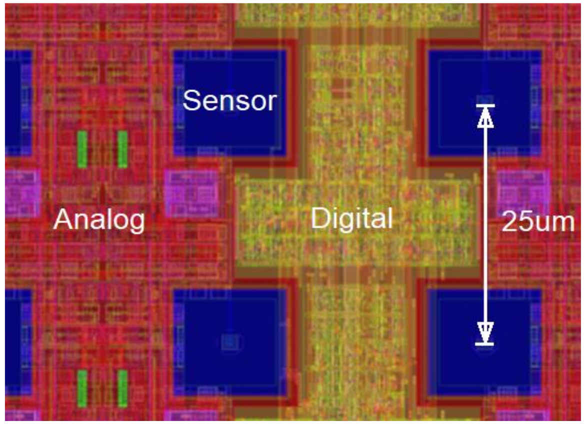
Sector Biasing (x16)
Generates I/V biases for 512x32 pixels

Periphery
SPI, Configuration, 8b10b enc, Serializers

Bottom Padframe
Stacked Power and Signal pads



512 x 512 pixel sensor mounted on PCB

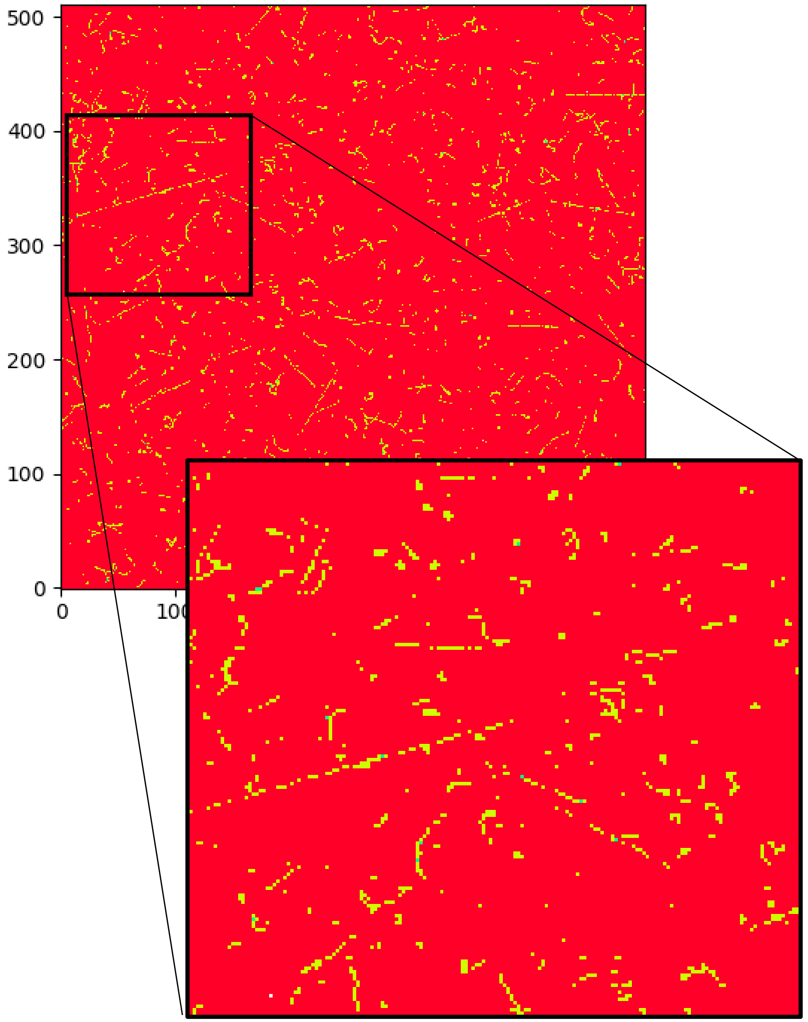


Detail of pixel layout

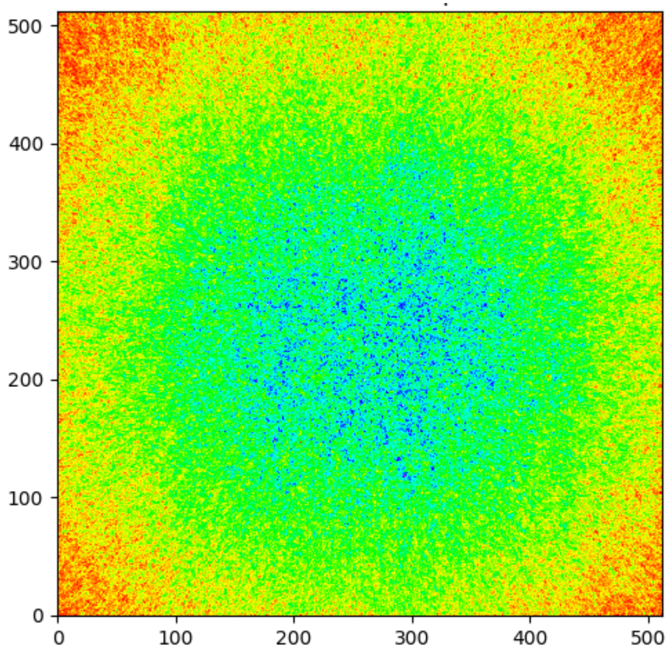
M. Rolo

Main prototype: charged-particle detection

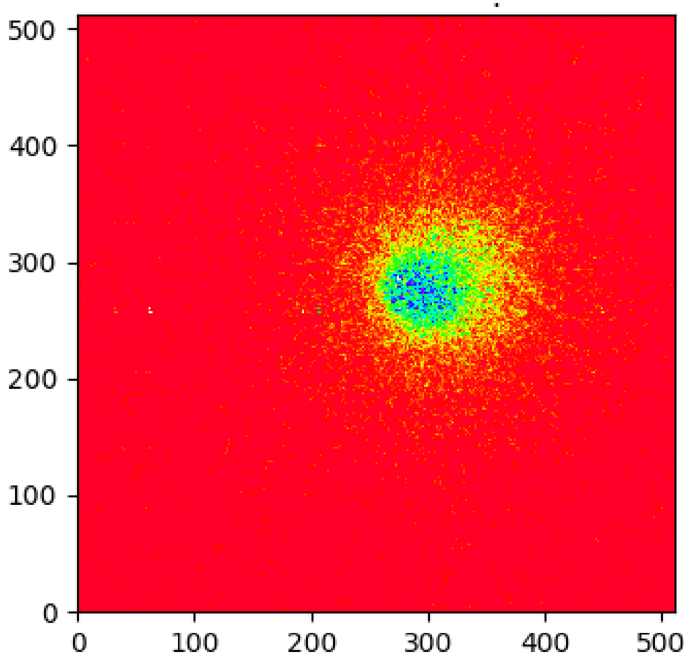
Cosmic rays (4h acquisition)
Sensor placed vertically



^{90}**Sr beta source** (1cm^2) placed at 8 mm from the sensor surface



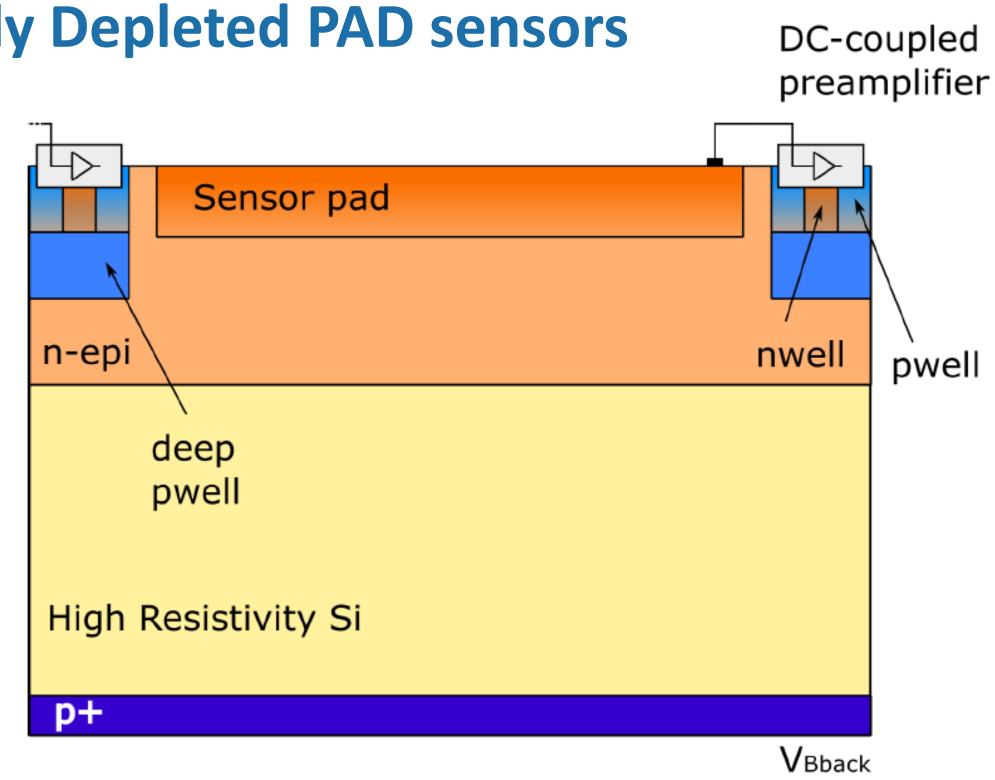
Collimated ^{90}**Sr beta source**
Collimator diameter: 1mm



- Total **power consumption**: 10mW/cm^2 at low event rates.
- Design specification: 20mW/cm^2 at event rates up to 100 Mevents/cm^2 (to be verified in a test beam)

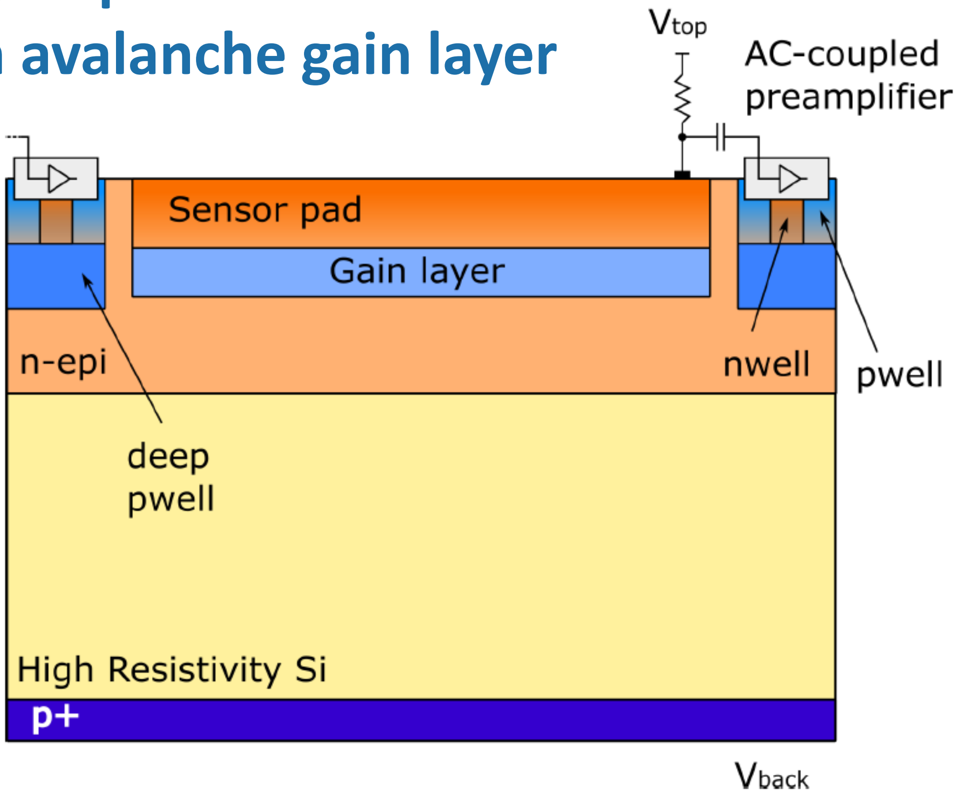
ARCADIA MAPS: gain add-on option

Fully Depleted PAD sensors



- Sensors can be biased at low voltage
- DC coupling with front-end amplifier is possible

Fully Depleted PAD sensors with avalanche gain layer

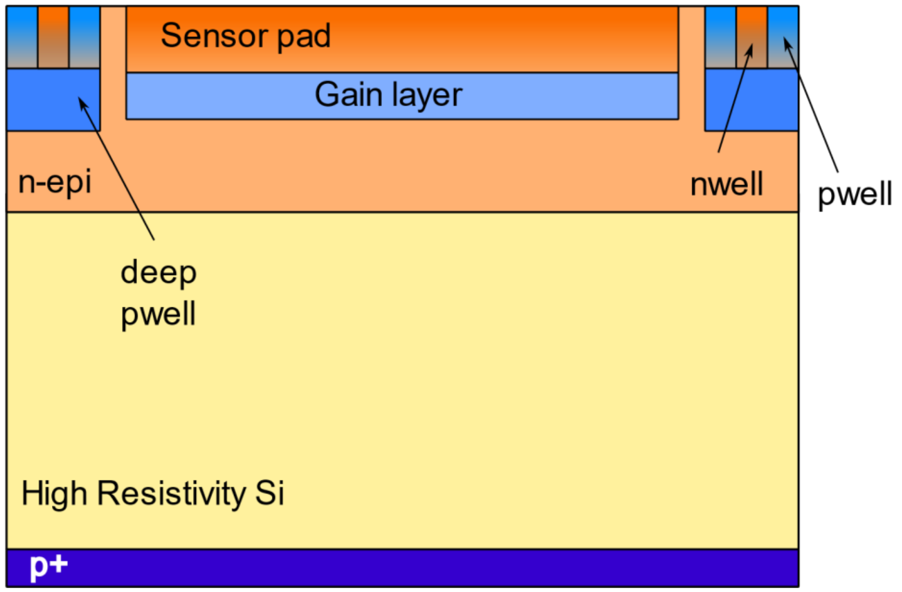


- High voltage is needed on the top side
- AC coupling of front-end amplifier is needed

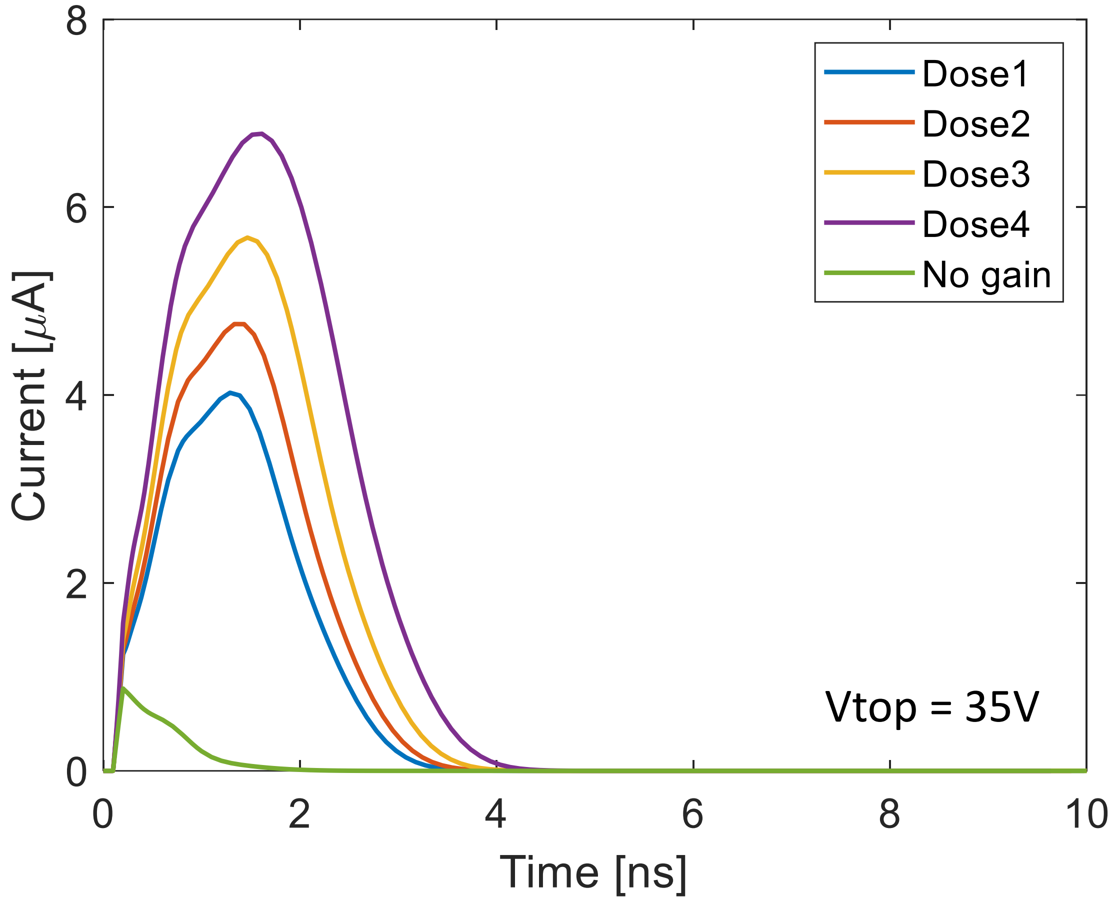
ARCADIA MAPS with gain: TCAD simulation - signal shape

- **TCAD** simulations with MIP-like signal (80 e-h pairs per µm)
- **50µm** active thickness, different **gain dose splittings**

Vtop range: 30 – 40V

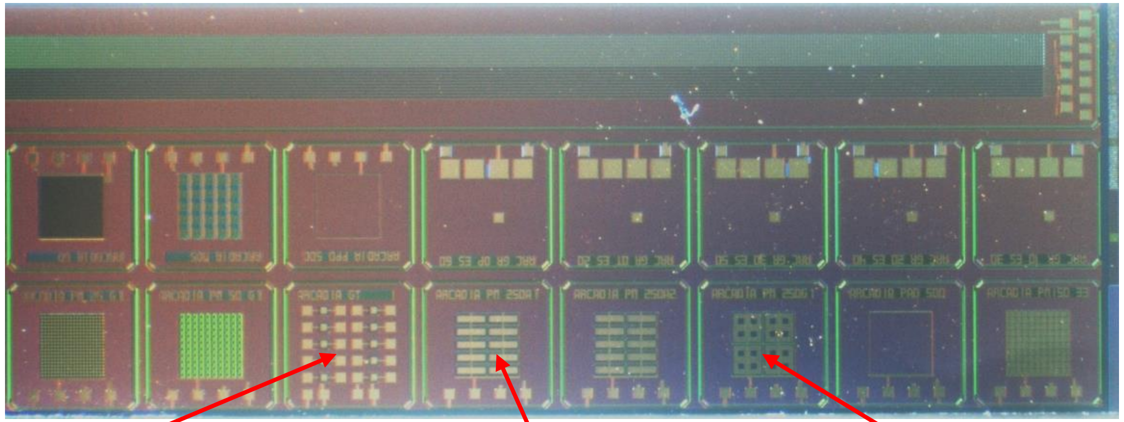


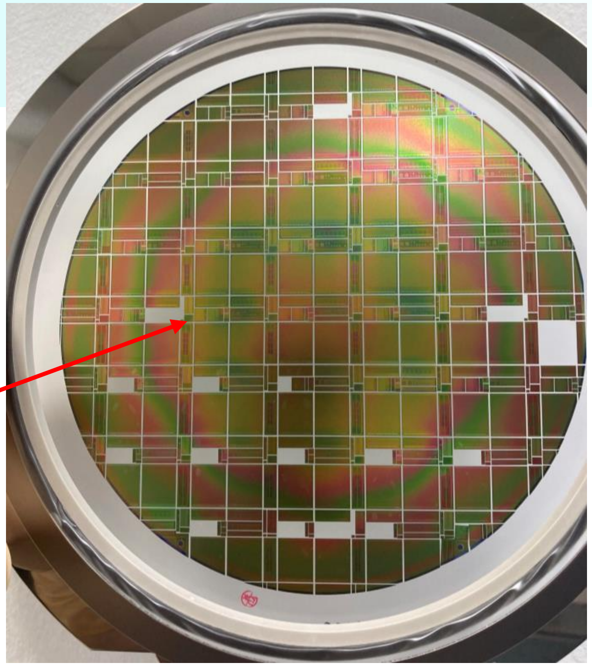
Vback = -30V

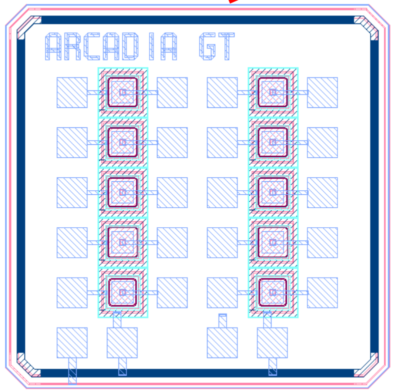


Passive sensors with gain - test structures

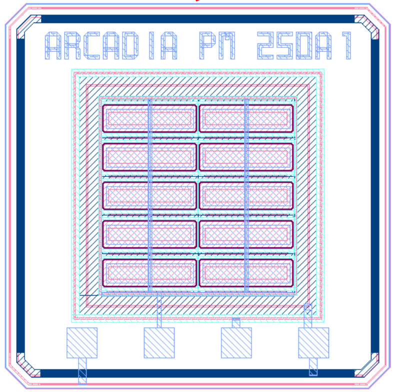
Monolithic test devices with gain included in **engineering run** designed for ARCADIA main demonstrator



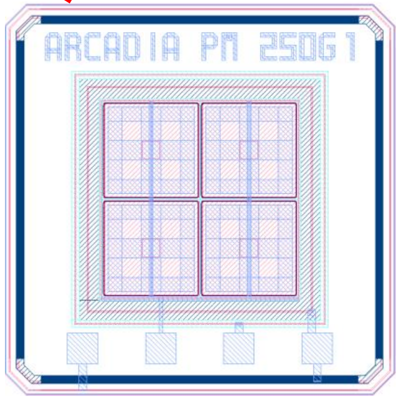




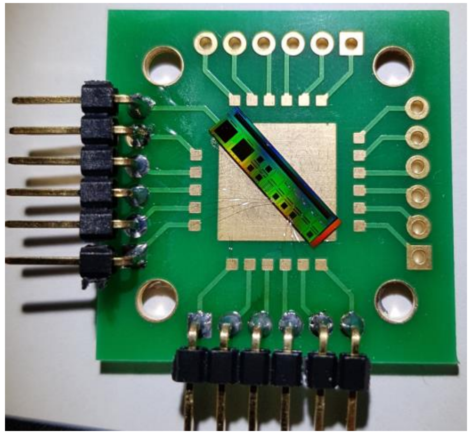
Devices with different terminations



Rectangular pad sensors



Square pad sensors

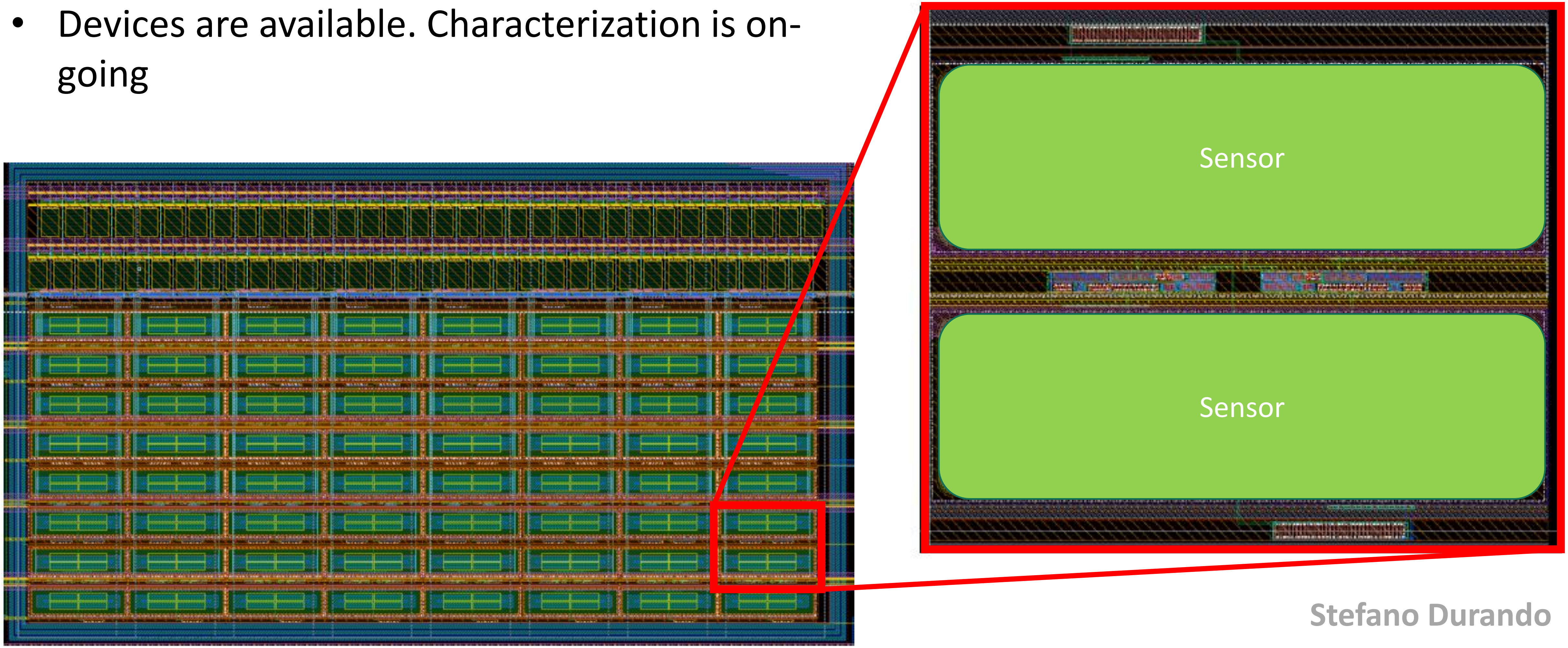


Packaged devices: suitable for testing with laser and light sources

Test array with integrated electronics

- Sensor size limited by layout rules: sub-optimal fill factor
- Devices are available. Characterization is on-going

2-pixel layout

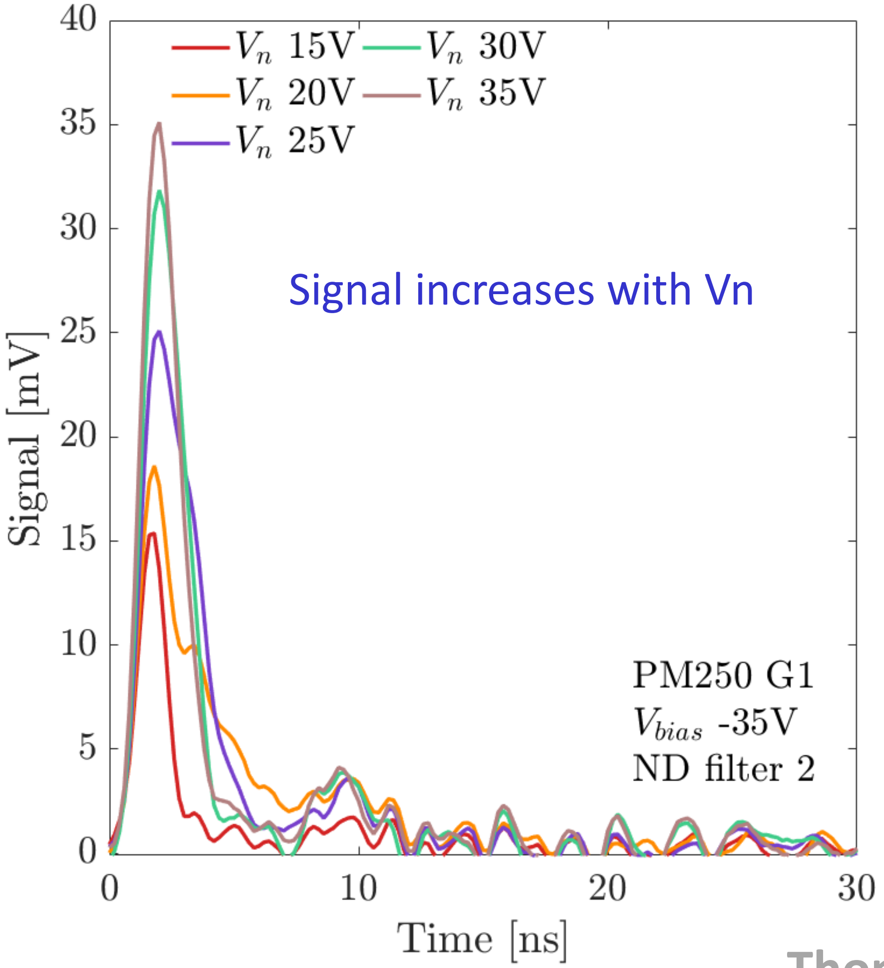


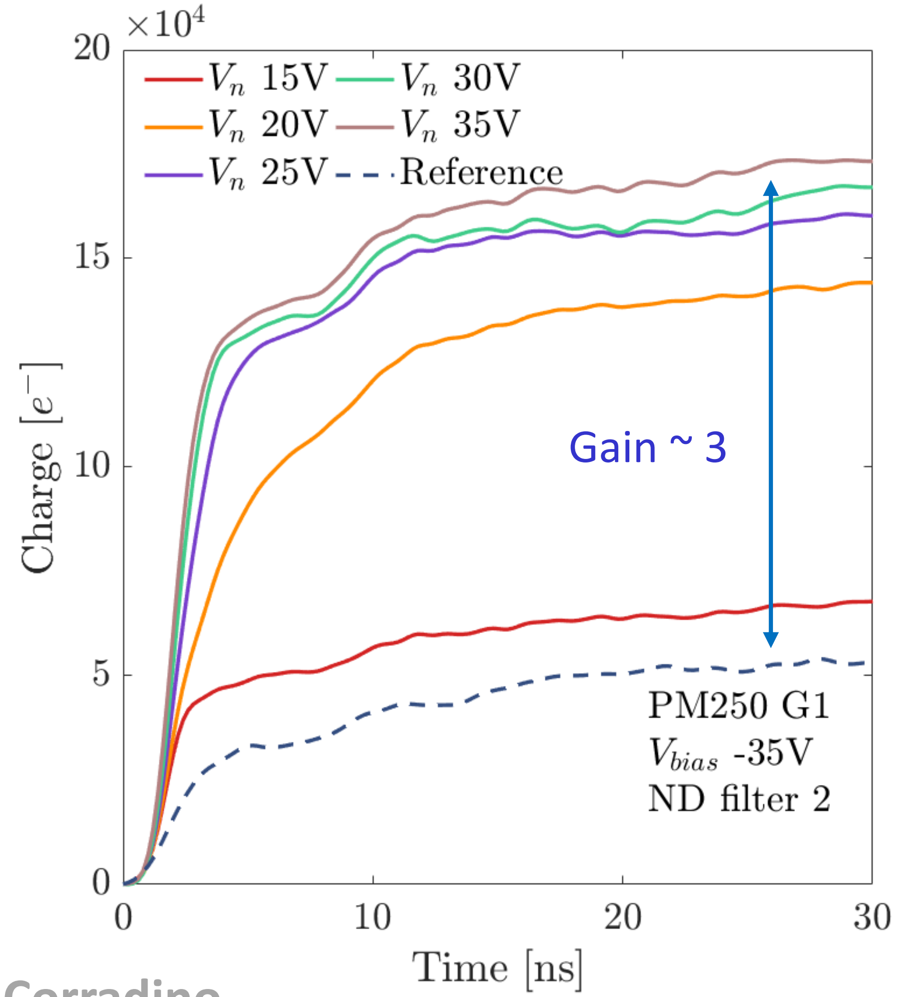
8x8 pixel matrix layout

Stefano Durando

Optical signal with NIR pulsed laser

Effect of **Vtop** - Bottom-side illumination

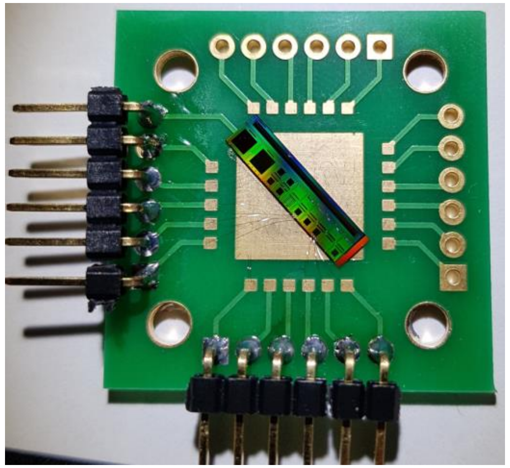




Thomas Corradino

Laser pulse width
< 100ps

Wavelength:
1060nm



Work in progress

Characterization:

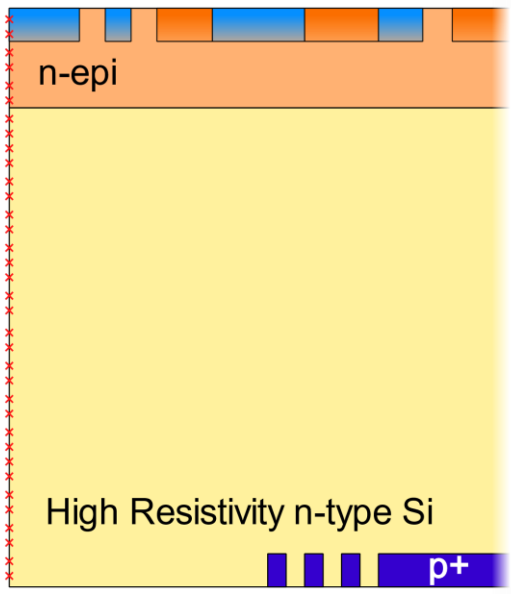
- Extensive **testing** of ARCADIA main array (test beam foreseen in the next months)
- **3-layer telescope** → tracking performance
- Extended **radiation hardness characterization** on test structures and on main demonstrator

Design:

- **Sensors with high timing resolution** (particle ToF – upgrade of ALICE experiment at CERN, ALICE 3 LoI approved)

Perspectives for application of ARCADIA process to XFEL detectors

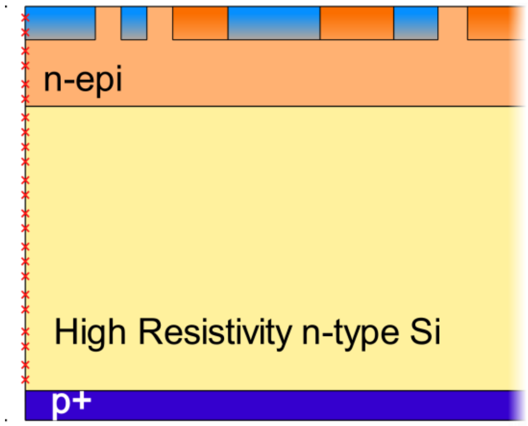
Hard X-rays



- **Thickness** can in principle be increased to 400 – 500 µm. 400 µm thickness verified on test structures.
- Backside **terminations**: designed for large positive oxide charge, in principle could stand high radiation dose – to be tested.
- **Slow lateral drift** (10s ns) in regions far from the sensor nodes: smart geometry for sensing nodes is needed for large pixels (e.g. array of small nodes in each pixel): complicated layout

Perspectives for application of ARCADIA process to XFEL detectors

Soft X-rays



- **Entrance window**: current backside junction depth is thin but not specifically designed for soft X-rays. Further optimization is possible.
- No backside lithography is needed for small active thickness ~100 µm (reduced process **cost and complexity**)
- Low-gain **avalanche** signal enhancement in sensing nodes currently in development phase. Could be an opportunity to enhance the SNR for soft X-rays

Perspectives for application of ARCADIA process to XFEL detectors

Data rate and chip periphery

- Very high event rates: analog and A/D can be integrated monolithically in the pixels. Digital: **3D-integration** of dedicated readout chip in advanced logic process is needed
- **Chip edge dead region**: currently 300 µm for 300 – 400 µm active thickness. Dedicated R&D needed to minimize the size of edge region in thick sensors
- **High photon fluxes**: space-charge effects will slow down charge collection: need to be studied experimentally and in simulation. Test sensors are currently available for these studies

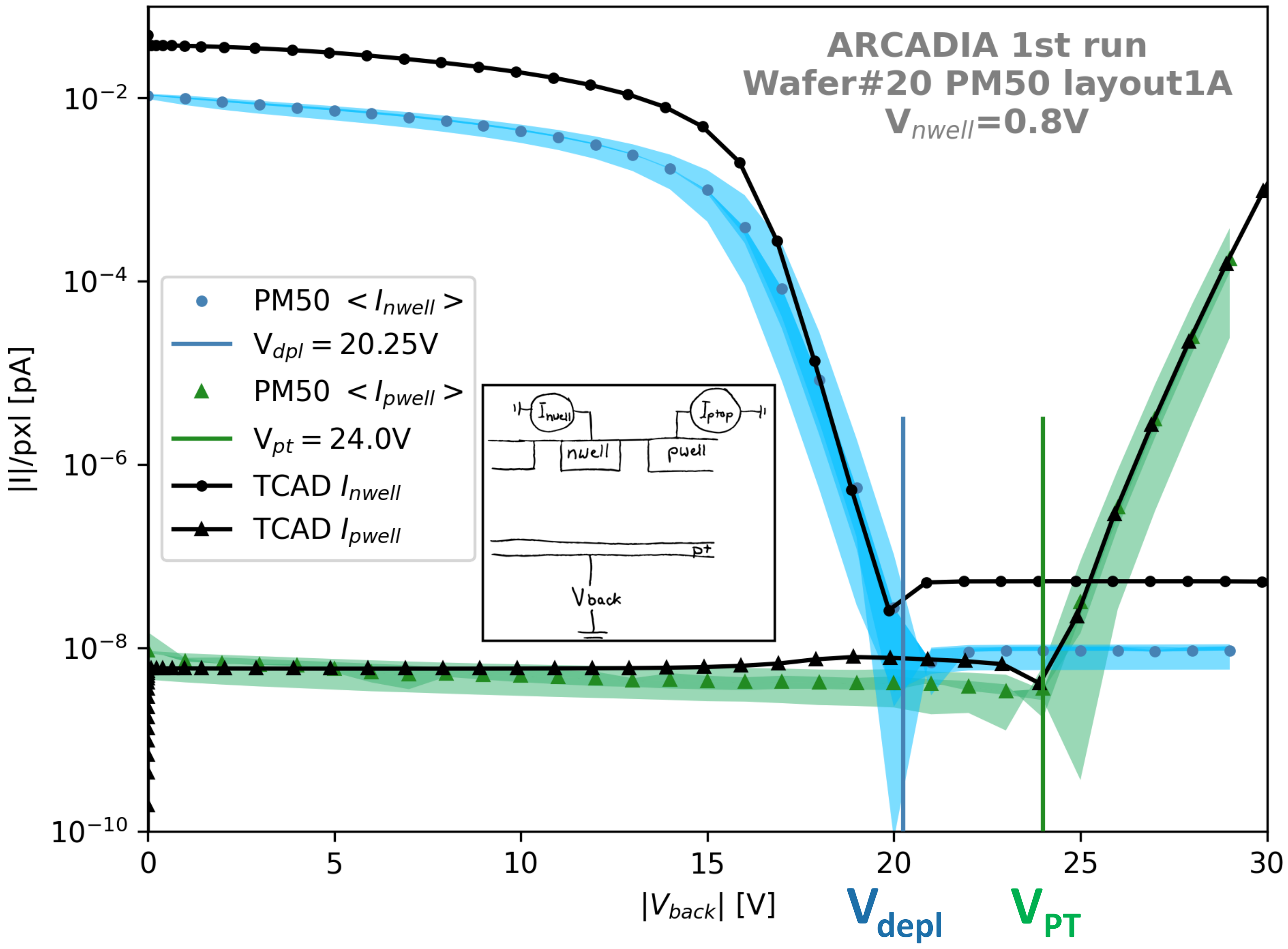
Thank you!

The ARCADIA collaboration:

F. Alfonsi, G. Ambrosi, A. Andreazza, E. Bianco, G. Balbi, S. Beolè, M. Caccia, A. Candelori, D. Chiappara, T. Corradino, T. Croci, M. Da Rocha Rolo, G. F. Dalla Betta, A. De Angelis, G. Dellacasa, N. Demaria, B. Di Ruzza, A. Di Salvo, S. Durando, D. Falchieri, U. Follo, A. Gabrielli, L. Gaioni, S. Garbolino, G. Gebbia, R. Giampaolo, N. Giangiacomi , P. Giubilato, R. Iuppa, M. Mandurrino, M. Manghisoni, S. Mattiazzo, C. Neubüser, F. Nozzoli, J. Olave, L. Pancheri, D. Passeri, A. Paternò, M. Pezzoli, P. Placidi, L. Ratti, E. Ricci, S. B. Ricciarini, A. Rivetti, H. Roghieh, R. Santoro, A. Scorzoni, L. Servoli, F. Tosello, G. Traversi, C. Vacchi, R. Wheadon, J. Wyss, P. Zuccon

Backup slides

Pixel Current-Voltage curves – comparison with TCAD models



Experimental data acquired for different pixel layouts

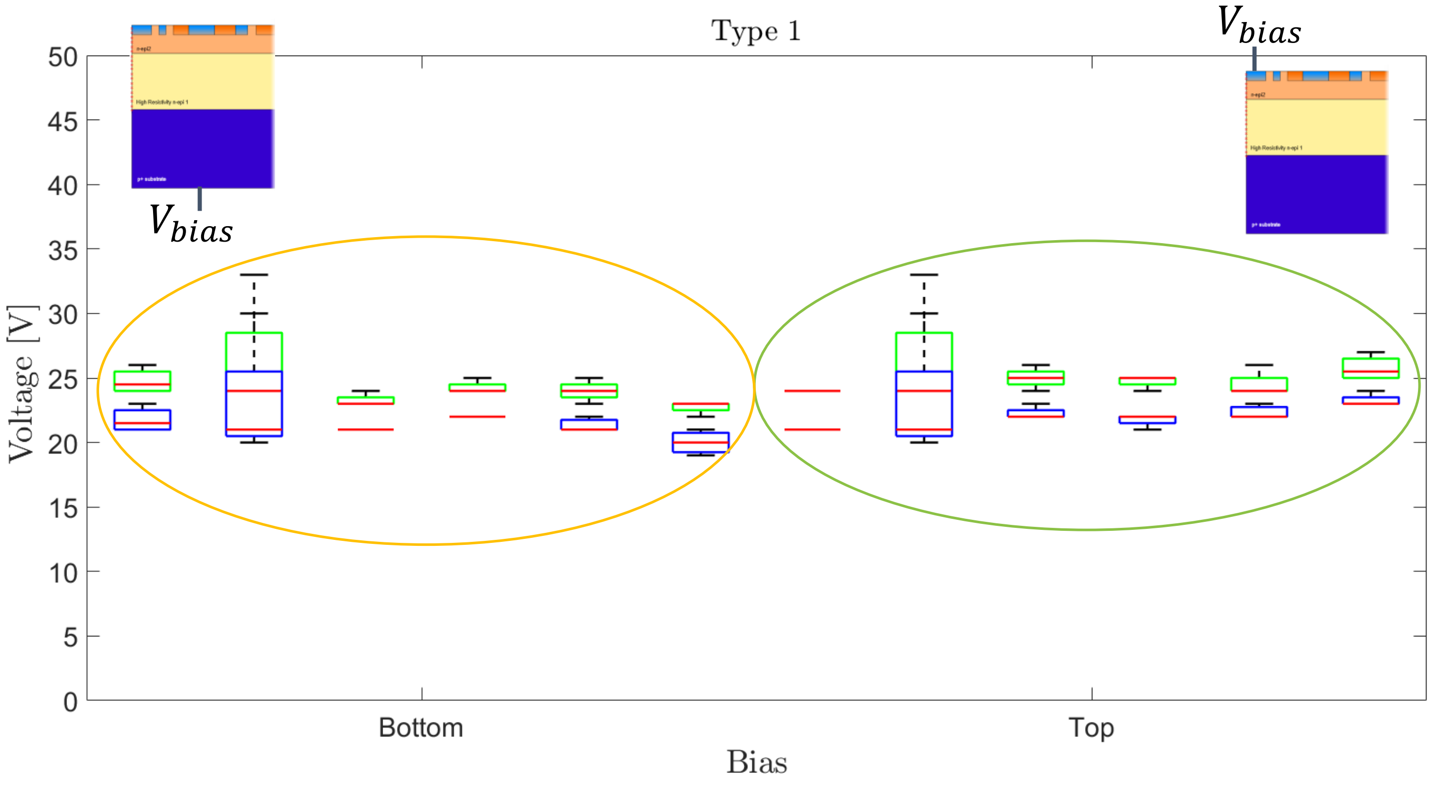
Intra-wafer and inter-wafer variations were evaluated

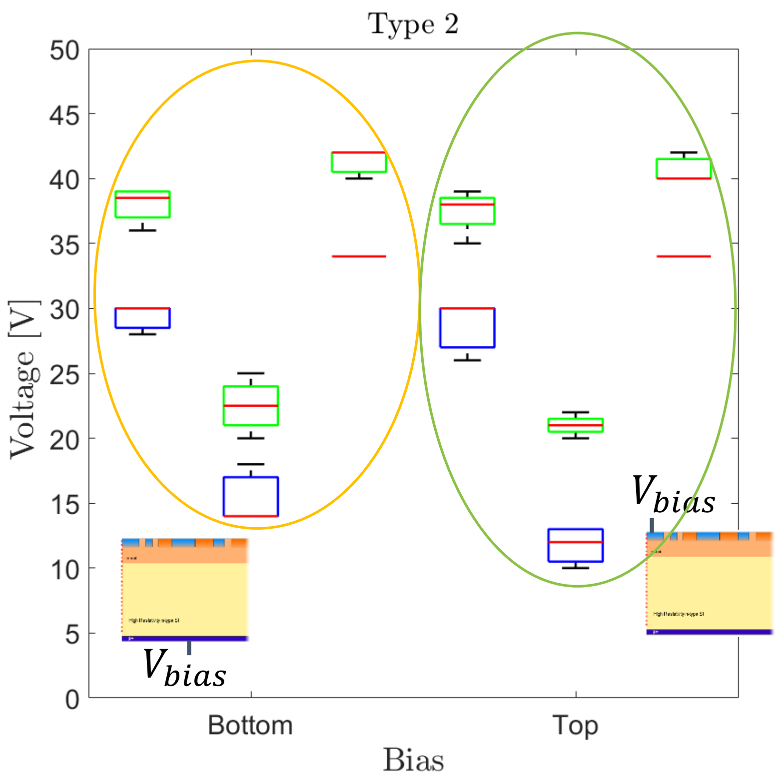
Process parameters in **TCAD simulations** adjusted on experimental results

C. Neubüser

Backside bias: bottom and top

The chip periphery behaves like a resistor: For substrates of **Type 1 and 2**, substrate bias can be applied both from the bottom and from the top



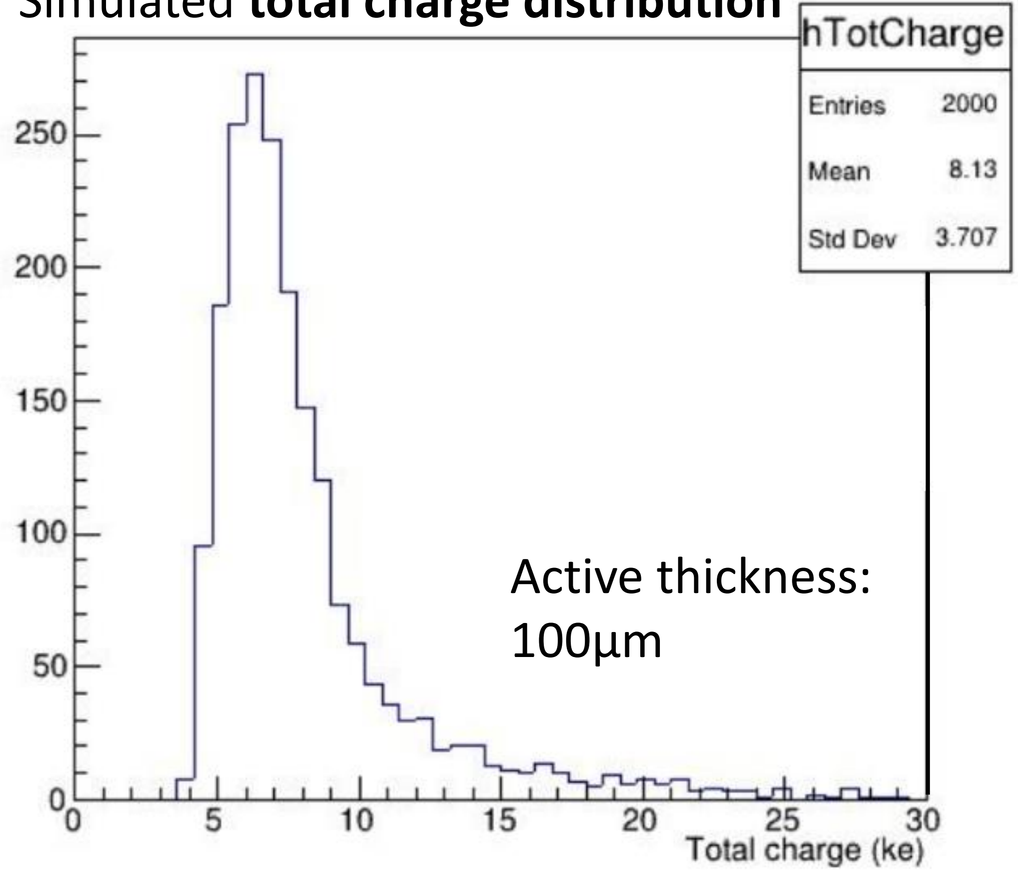


V_{depl} and V_{PT} are very similar for the two considered biasing schemes

Particle detection: Monte Carlo simulation of charge and cluster size

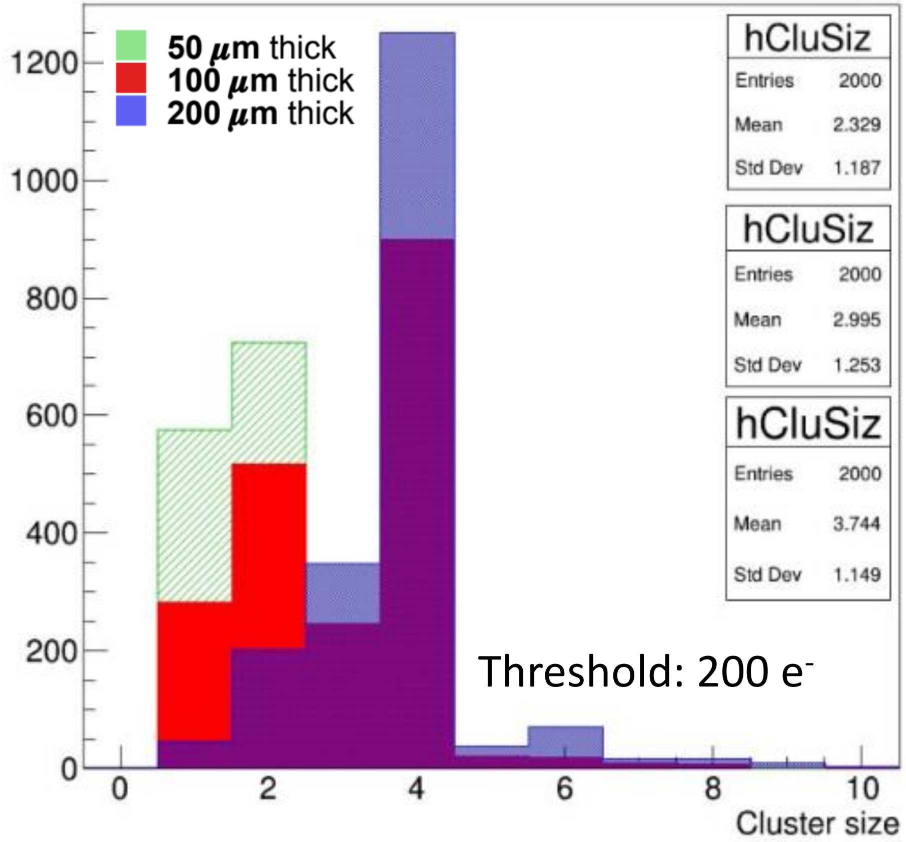
200MeV muons - perpendicular incidence

Simulated **total charge distribution**



C. Ferrero

Simulated cluster size distribution



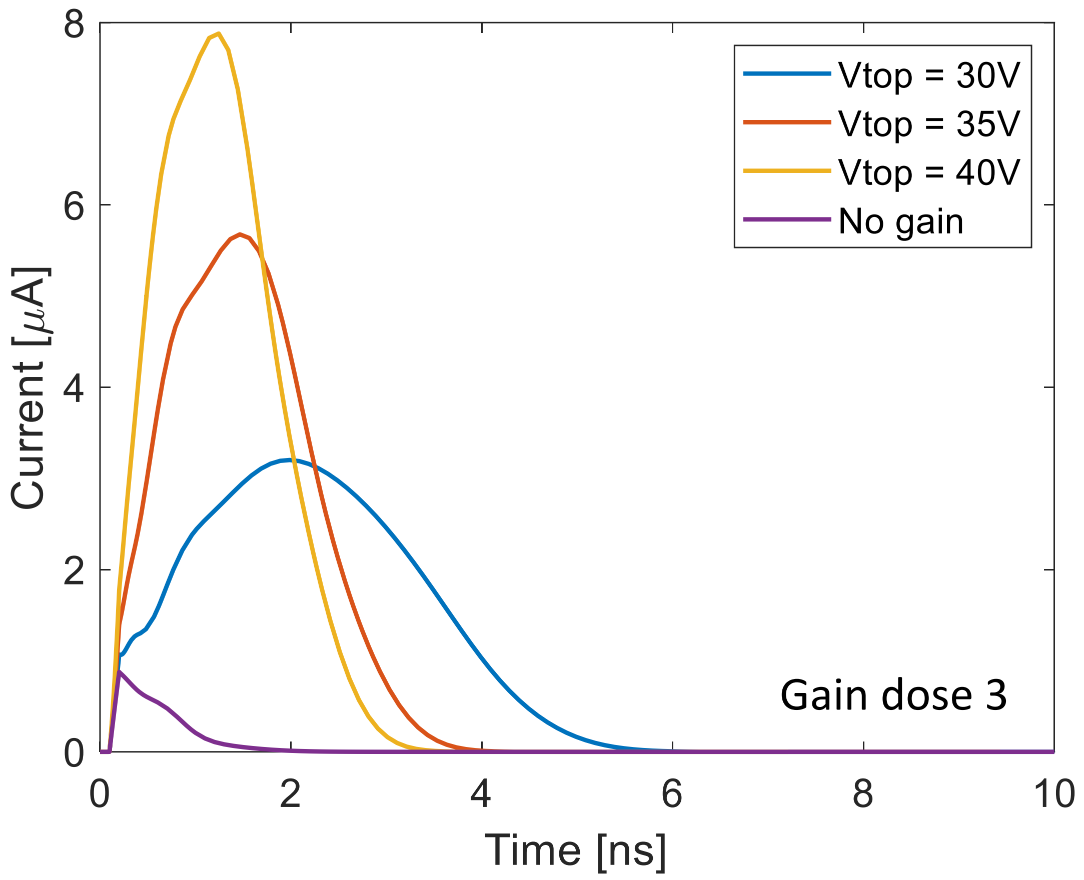
25µm pixel pitch

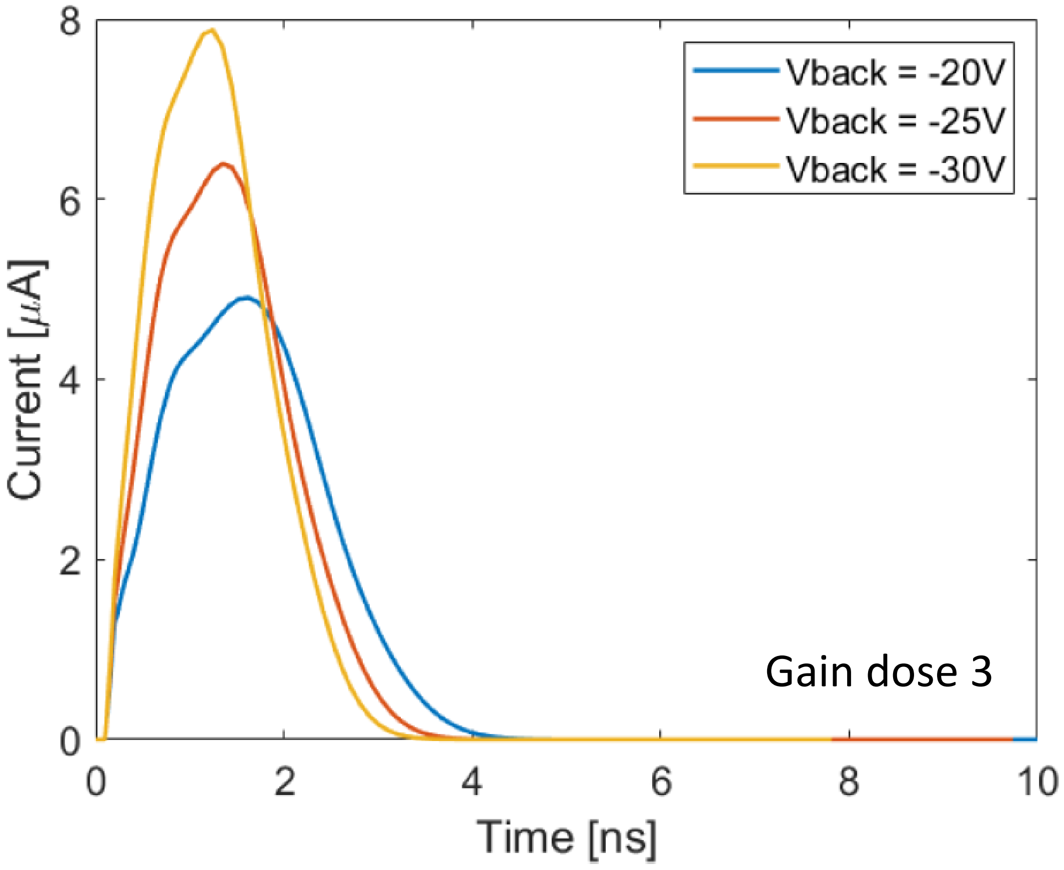
Simulation domain: 5x5 matrix

ARCADIA MAPS with gain: signal shape

Reference voltage: electronics GND, applied at the pwells

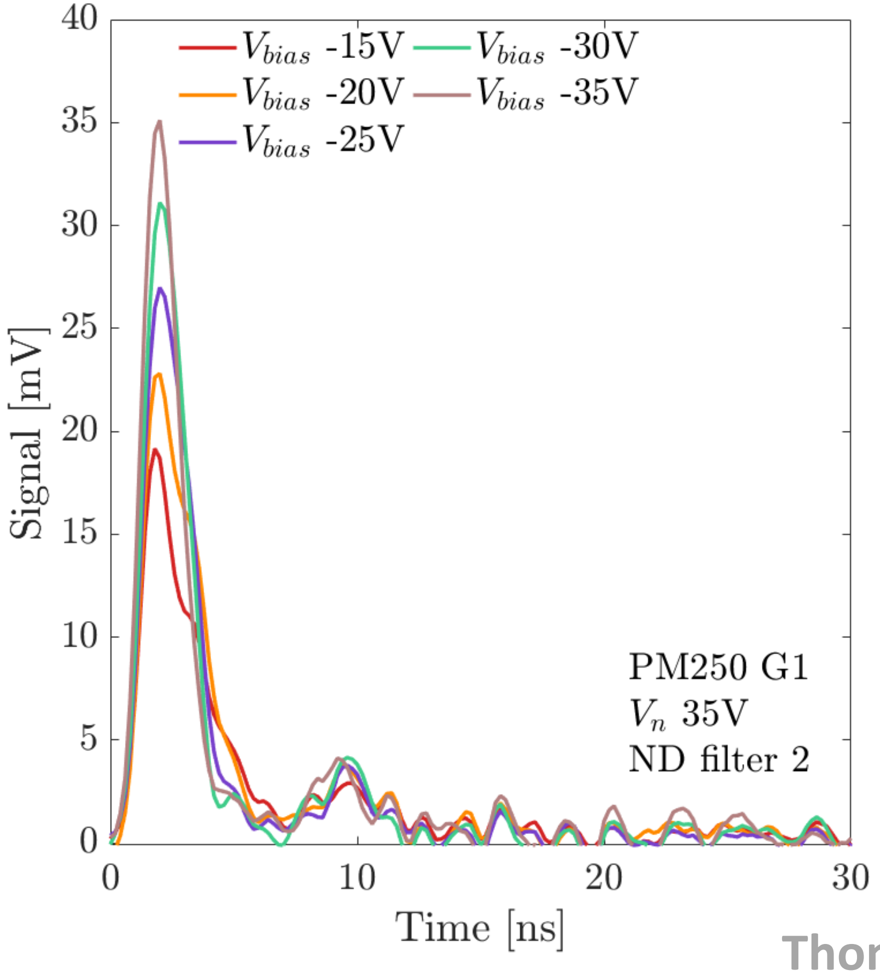
GAIN and **drift field** are defined by a combination of Vtop > 0 and Vback < 0

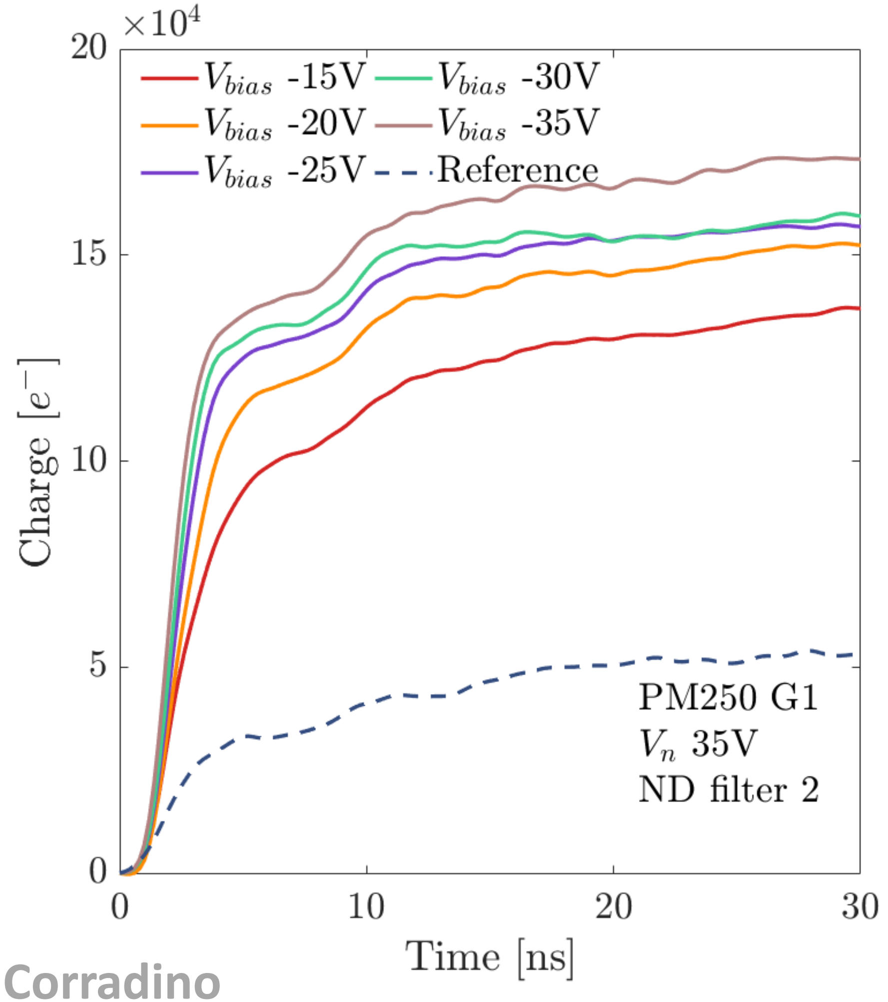




Optical signal with NIR pulsed laser

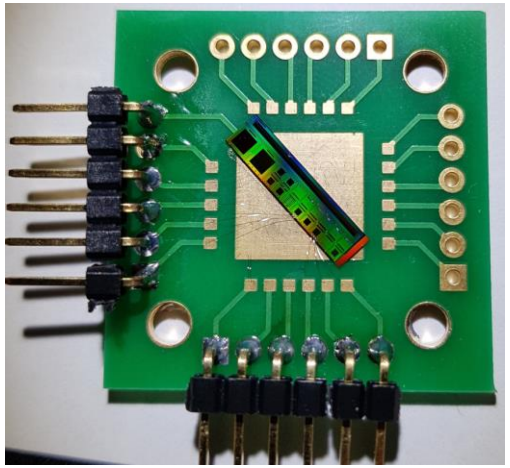
Effect of **Vback** - Bottom-side illumination





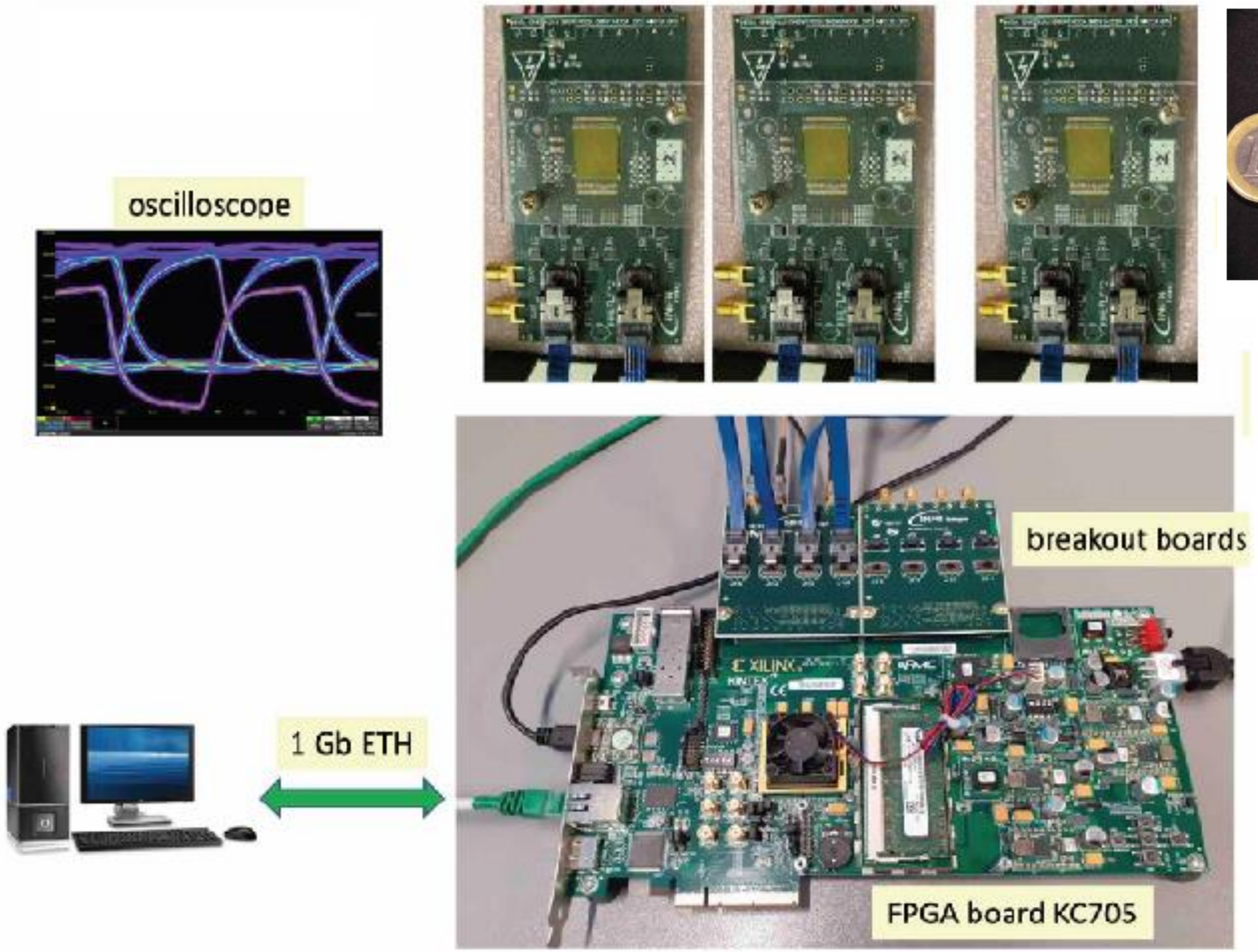
Laser pulse width
< 100ps

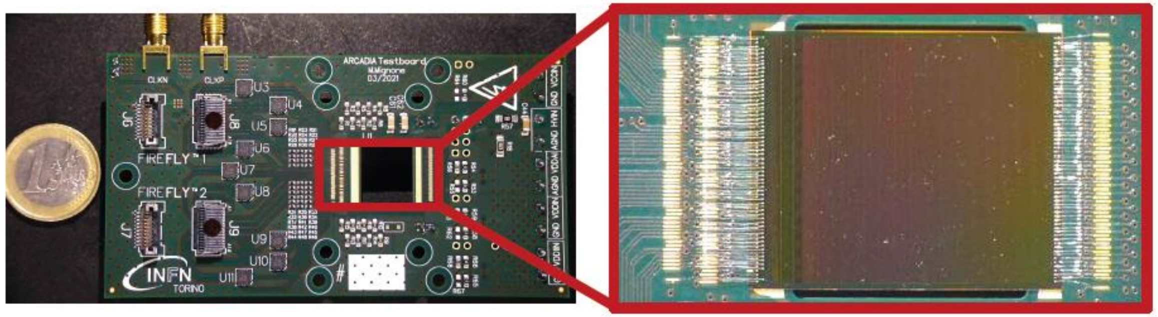
Wavelength:
1060nm



Thomas Corradino

Front-end board and DAQ





- 2 Samtec FireFly connectors for ASIC signals (Clock, SPI, Data)
- Connection to external low jitter Clock (via SMA connectors)
- Bias to the DMAPS backside or (wirebonded) to top pads
- Independent LDOs for IO Buffers, Analog Core, Digital Core
- PCB through-hole for matrix BSI
- custom FMC-to-Firefly breakout board

M. Rolo