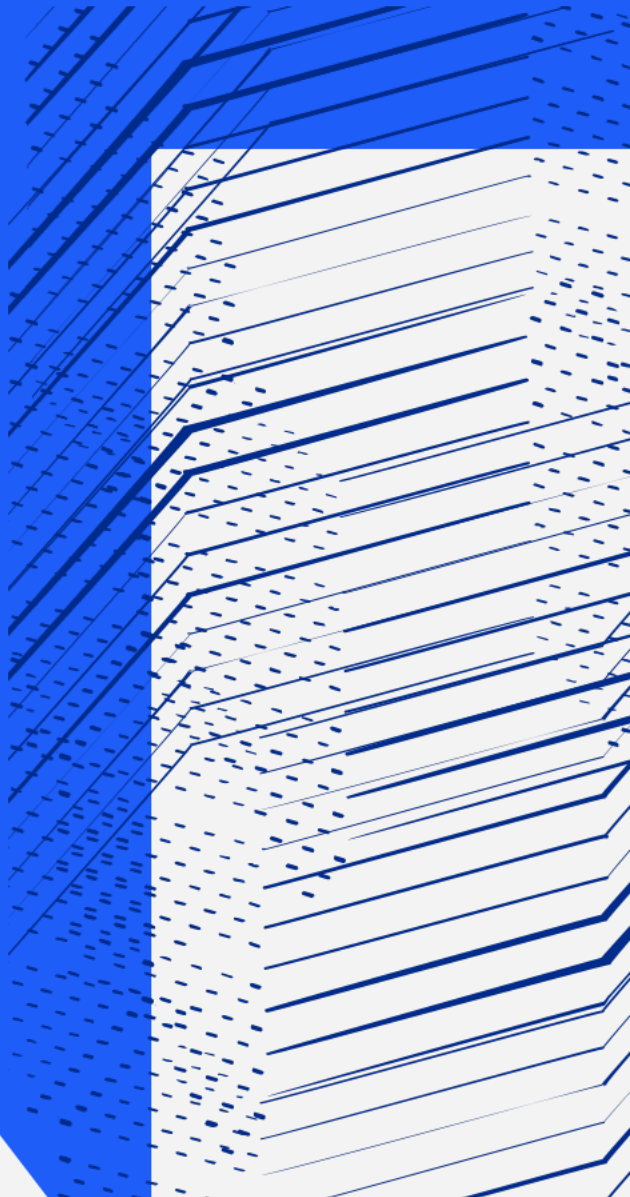
Science and Technology Facilities Council

Latest Developments in Detector Microelectronics and DAQ at STFC

Matthew Hart



Agenda

1 Microelectronics

Relevant Developments from the ASIC design and CMOS sensor design Groups

2 DAQ

Our approach to Control and Data Paths for high rate systems

3 Lessons Learnt in Detector Dev

A look back on 15 years developing for XFEL

Image © STFC Alan Ford

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Part 1
Microelectronics

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The Microelectronics Groups at STFC

ASIC Design

Mark Prydderch
Group Leader

Stephen Bell

Oliver Bowett

Michelle Charrière

Thomas Gardiner

Lawrence Jones

Quentin Morrissey

Alex Steven

CMOS Sensors Design

Nicola Guerrini
Group Leader

Seddik Benhammadi

Sam Hutchings

Deividas Krukauskas

Herman Larsen

Ben Marsh

Neil Raftery

Iain Sedgwick

Bindu Velagapudi

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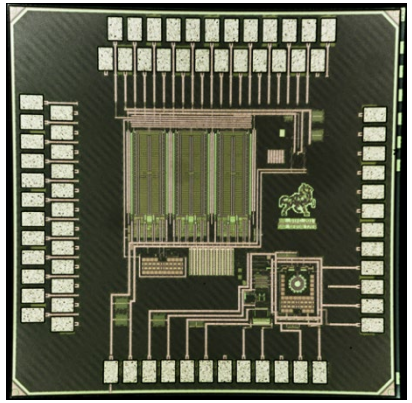
ASIC Design Group

Microelectronics Development Work

Internally funded programmes that develop IP to meet the challenges of tomorrow.

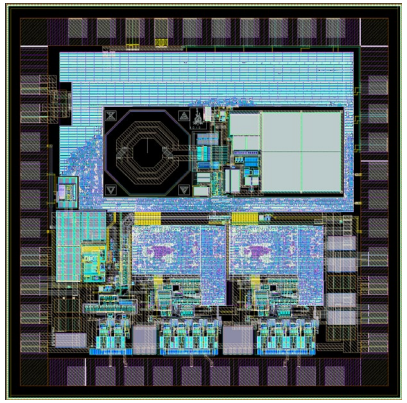
Key system elements – **High speed ADCs, High Speed Serial Data,** Advanced Pixel Designs



65nm IP Test Structure

- Serialiser @ 10Gb/s
- 30Ms/s 16-bit SAR ADC

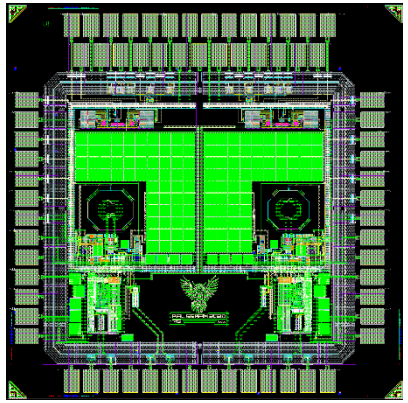
Status: Testing complete



180nm IP Test Structure

- Serialiser @ 5Gb/s-NZR and 10Gb/s-PAM4

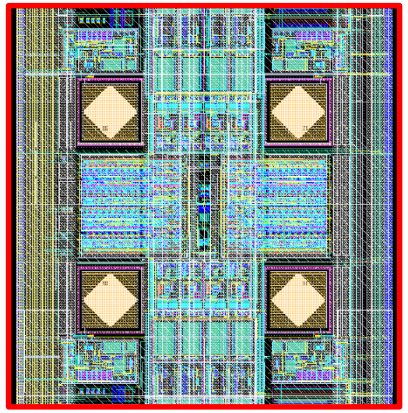
Status: Testing Complete



65nm IP Test Structure

- Serialiser @ 14Gb/s-NZR and 28Gb/s with PAM4
- Alternate version at 10Gb/s-NZR and 20Gb/s-PAM4

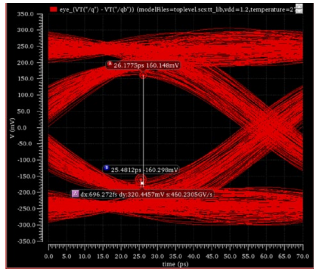
Status: Testing Complete

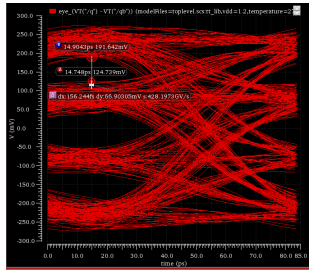


180nm ADC Technology

- In Pixel ADCs @ 1Ms/s (1.6GHz 12-bit TDC)

Status: Hexitec-MHz System in test and DAQ dev.





Example of NZR data compared to PAM4 data

ASIC Design Group

Microelectronics Development Work

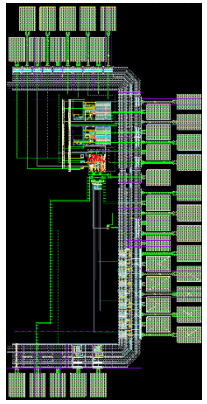
Internally funded programmes that develop IP to meet the challenges of tomorrow.
Key system elements – High speed ADCs, High Speed Serial Data, **Advanced Pixel Designs**.

	Photons 5keV (min)	Photons 5keV (Max)	Trans Noise Sigma/Photons
High Gain	0.1	167	0.15
Middle Gain	176	1284	1.56
Low Gain	1288	11981	15.6

65nm Pixel Design

- A 110um pitch pixel
- Adaptive Gain Amplifier with 10^5 dynamic range

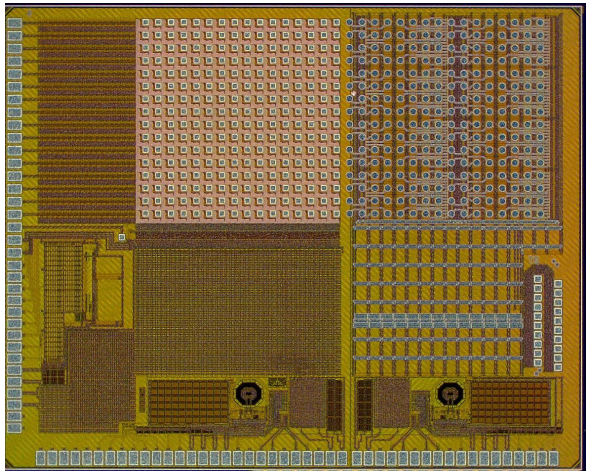
Status: Design complete, not fabricated



65nm Pixel Test Structure

- Charge cancellation pixel – direct to digital
- 10^4 photon dynamic range at 1MHz continuous
- 10^10 photons per second

Status: Testing Complete



65nm Pixel Demo – XIDyn

- 110um Pixel
- For next generation synchrotrons
- Potential for FELs

Status: In testing and DAQ Dev

28nm IP Development

Two Test structures one for IP and another for high time resolution LGAD readout.

- Bandgap
- Beta Multiplier
- IDAC and VDAC
- Rail to Rail amplifier
- Reference driver amplifier
- Slope ADC

Status: Submission in October

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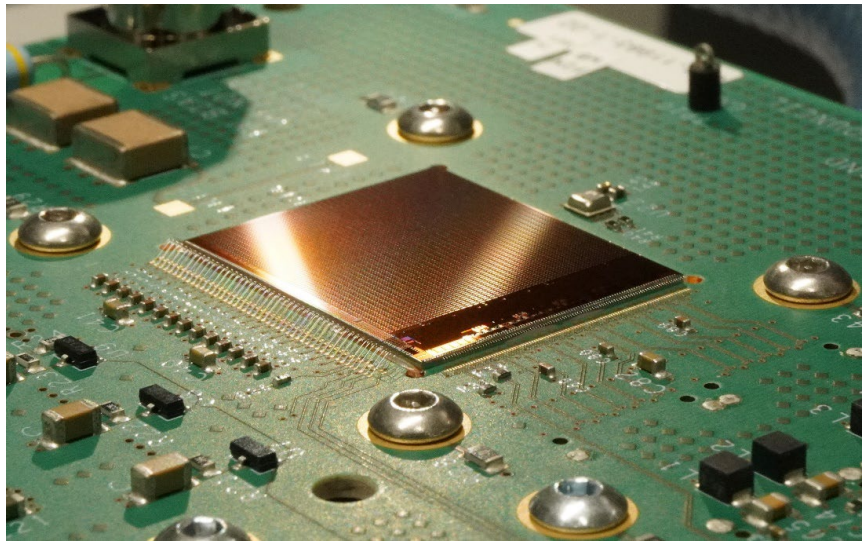
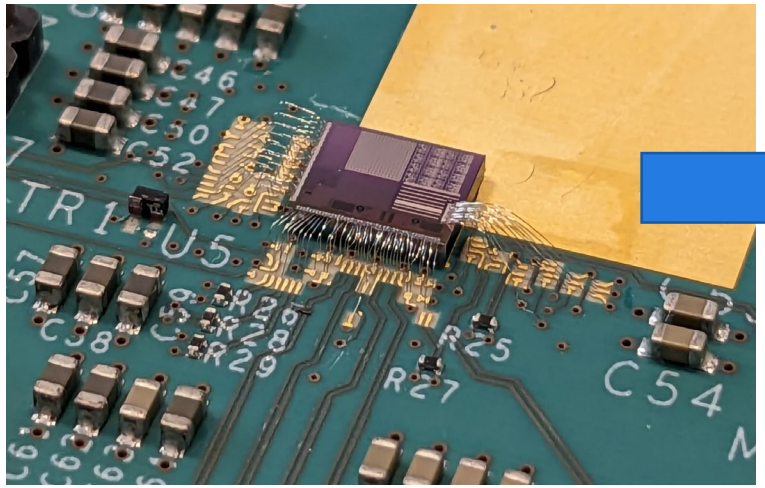
ASIC Design Group

180nm and 65nm IP R&D converted to next gen full systems delivered or in design



Hexitec-MHz (180nm)
1 million frames per second continuous
80x80, 250um pixels
Data Output: 20 x 4.1Gbps



XIDyn - DynamiX Pixels (65nm)
533k frames per second continuous
16 x16, 110um pixels
Range: >10^{11} ph/mm^2/s
Data Output: 2 x 14Gbps (designed as if full columns)

XIDyn Full Reticle ASIC

XIDyn Full Scale (65nm)

- 133k frames per second continuous
- Pixel memory gives options for faster sub frames/bursts
- ~200x200, 110um pixels
- Data Output: 1-8x 14Gbps

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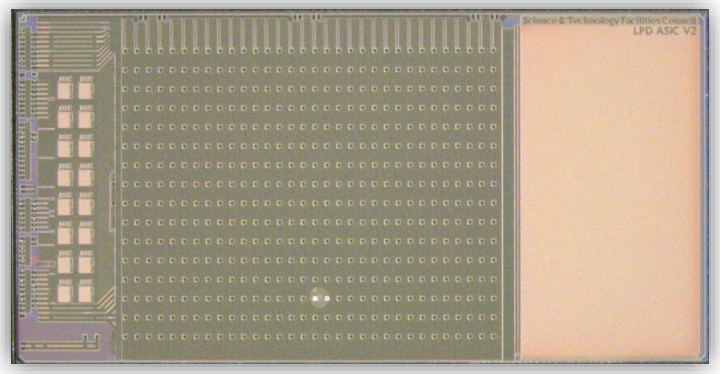
Is a 1MHz continuous system with ~100um pixels possible?
We are temptingly close on single element systems – but when tiled the cost and complexity feels less likely to be adopted.

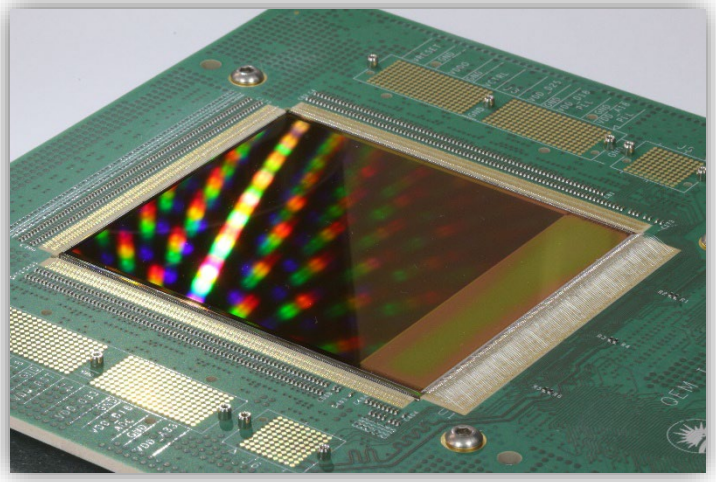
Microelectronics Design @ STFC

Last generation vs the current generation

The following slides give background on core detector technology capability at STFC



LPD ASIC
2.6M Samples/s
16 ADCs

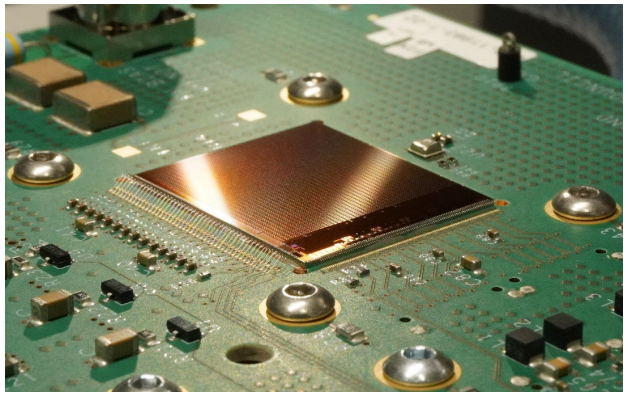


QEM
16M Sensor for EM
16G Samples/s
40000 ADCs

Data Out: 257 LVDS @ 780MHz

The LPD 1M
(contains 2048 ASICs)
5.3G Samples/s
32000 ADCs

Data output: 2048 LVDS @ 100MHz



Hexitec MHz – Spectroscopic Imaging
6.4G Samples/s
6400 ADCs – 1 per pixel

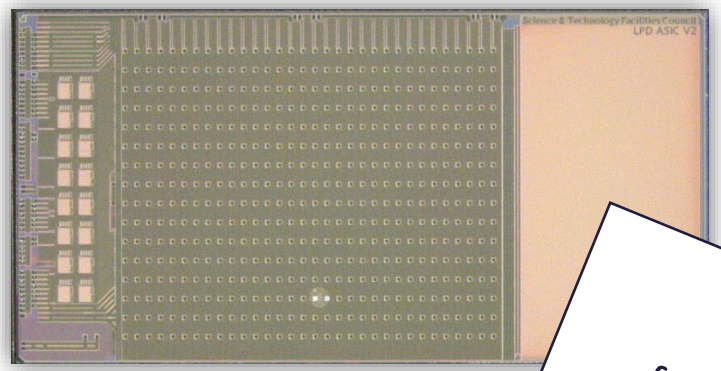
Data Out: 20 CML @ 4.1GHz

Status: In fabrication

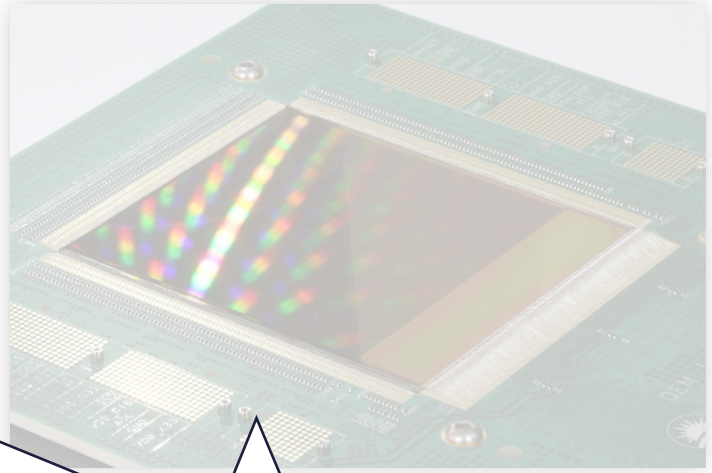
Microelectronics Design @ STFC

Last generation vs the current generation

The following slides give background on core detector technology capability at STFC



LPD ASIC
2.6M Samples/s
16 ADCs



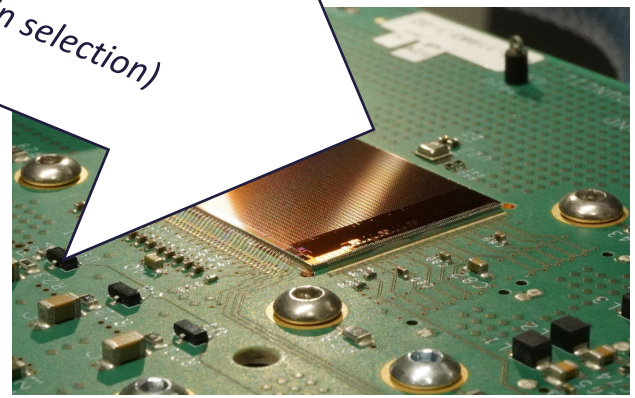
QEM
16M Sensor for EM
16G Samples/s
40000 ADCs

Data Out: 257 LVDS @ 780MHz

2500 times the data rate
for the same unit area *(after gain selection)*

The LPD 1M
(contains 2048 ASICs)
5.3G Samples/s
32000 ADCs

Data output: 2048 LVDS @ 100MHz



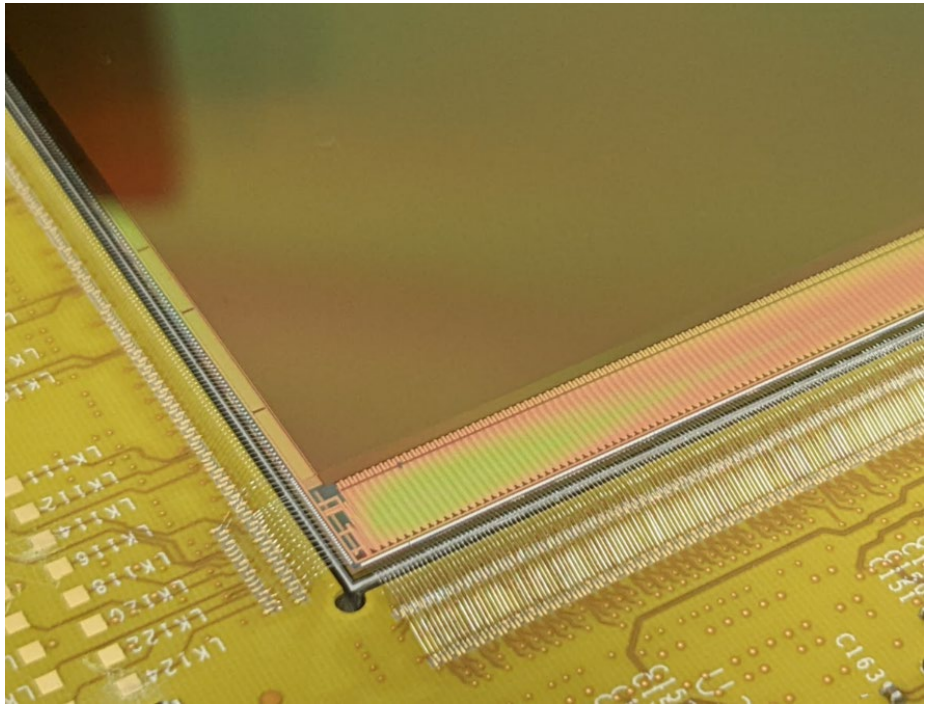
Hexitec MHz – Spectroscopic Imaging
6.4G Samples/s
6400 ADCs – 1 per pixel

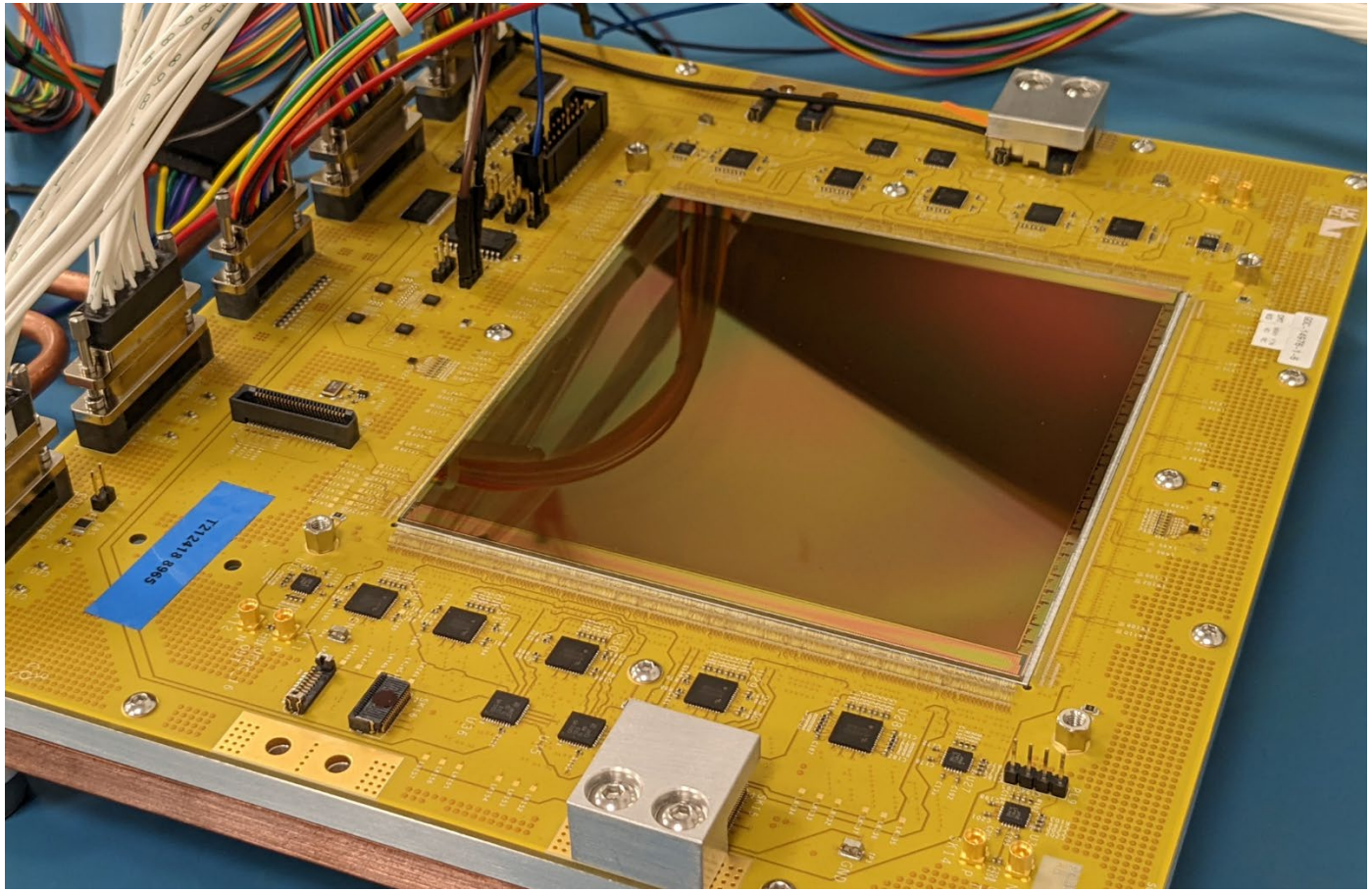
Data Out: 20 CML @ 4.1GHz

Status: In fabrication

CMOS Sensor Design Group

A recent example….
C100 – A sensor for electron microscopy,
4M pixels (2k x2k) ~50um pixels -> 12cm total die size.
Limited to 1-2kHz due to RC load down the columns





ADCs in the periphery pass data to CML serializers at ~4Gbps. Converted to optical on the COB this passes out of vacuum on fibre

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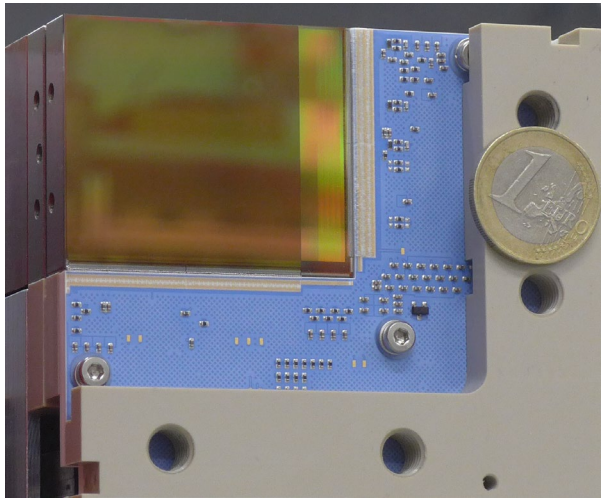
MHz CMOS for Soft X-Ray

PERCIVAL

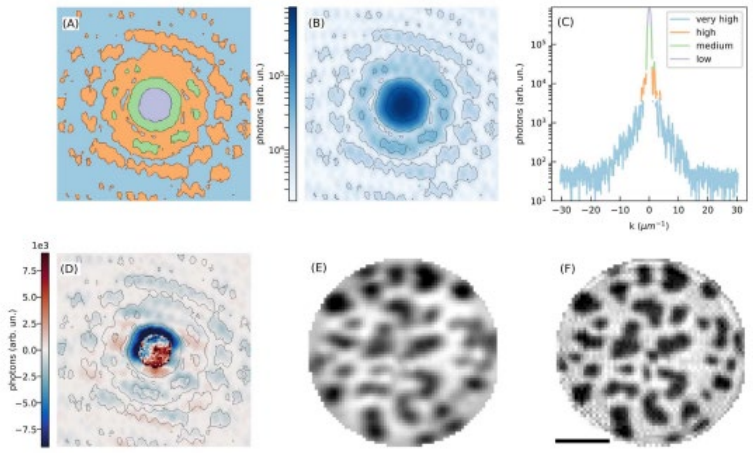
- 2 Mpixels
- 120Hz
- Back Side Illuminated
- Sensitive down to 250eV

The PERCIVAL Sensor



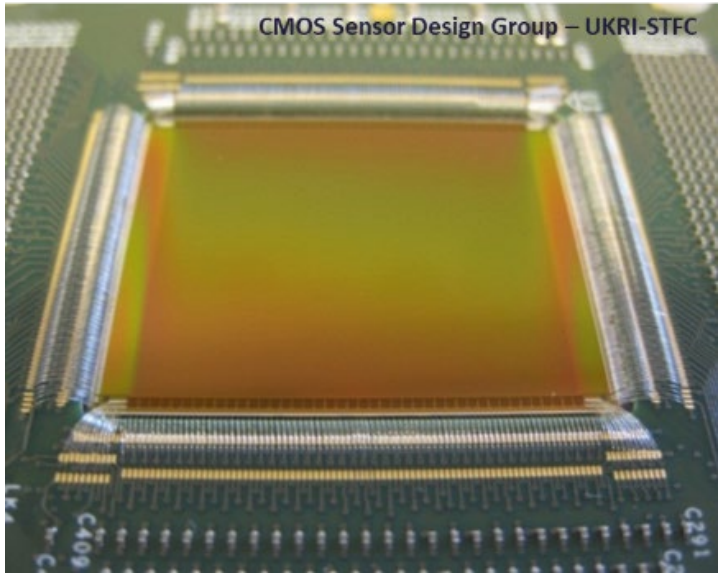
KIRANA – 5Mfps

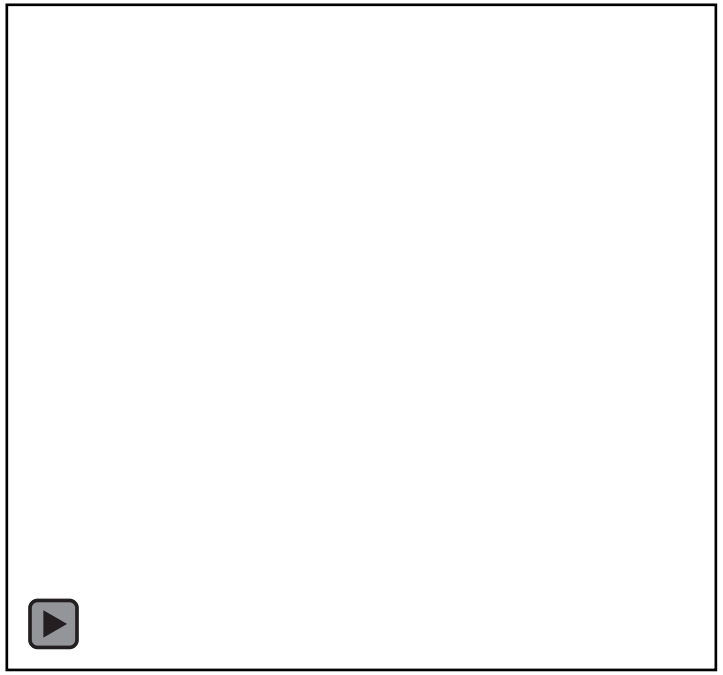
- 0.7 Mpixels
- 5Mfps – 200 frame burst
- 200ms between bursts
- Visible Range



Results from PERCIVAL

The KIRANA CMOS Sensor





Burst image sequence from KIRANA

Science and Technology Facilities Council

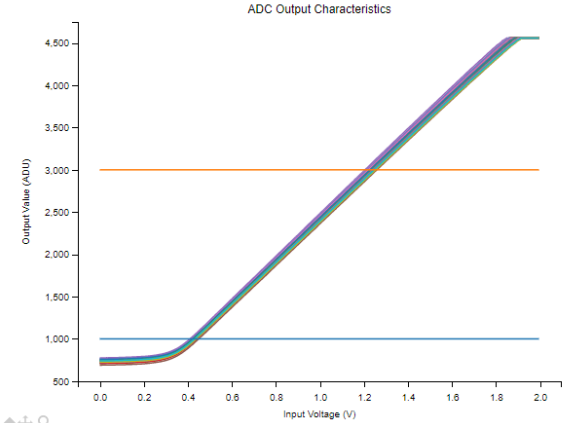
MHz CMOS for Soft X-Ray

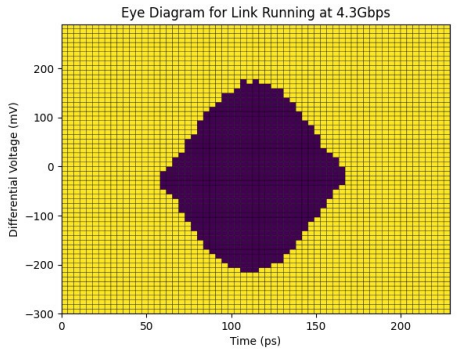
Future Options

- Necessary circuit IP (transmitters, ADCs etc) in preparation for some time. Mostly 180nm and also some 65nm
- Stacked technologies start to become available at the foundry
- Offers the opportunity for high speed BSI imaging, getting past the RC load bottleneck of standard sensors

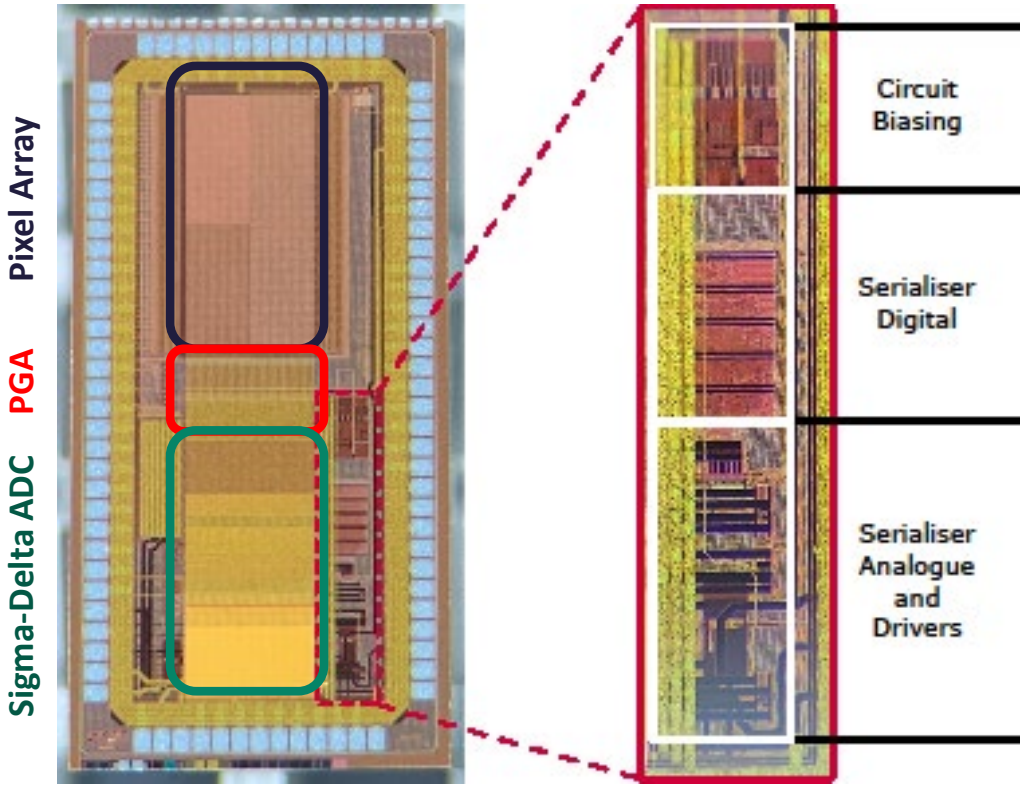
Science and Technology Facilities Council

Results from 1MSPS Sigma-Delta ADC (180nm)





Eye Diagram from 4.3Gbps Serializer in 180nm



Recent 180nm Test Structure

News & Events ▾ Home » Press Releases

TowerJazz Announces the Availability of its Newly Released Advanced Stacked BSI Hybrid Bonding Technology

Manufactured in Company's advanced 65nm 300mm Uozu, Japan facility

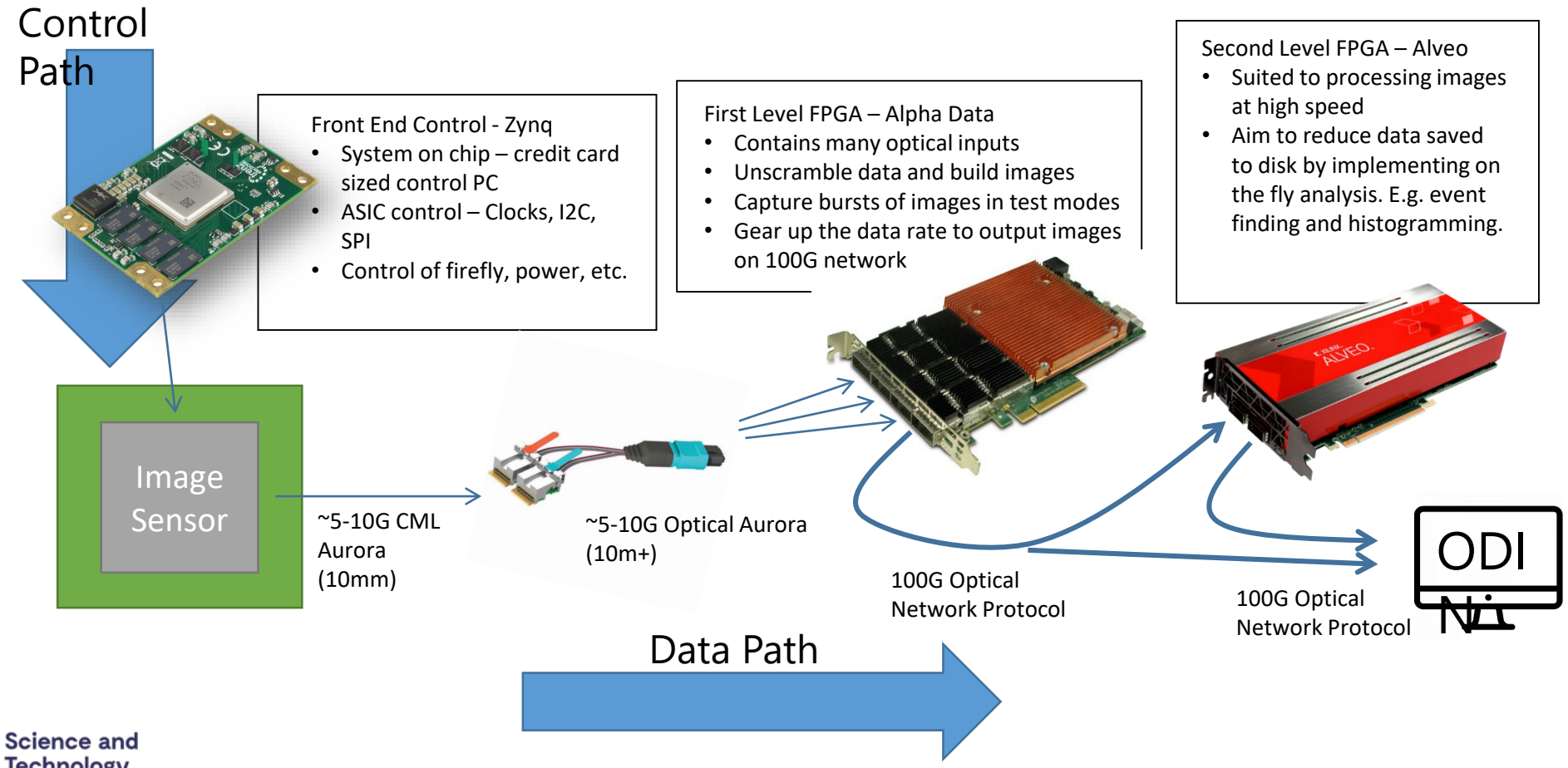
New offering enables outstanding pixel performance and significant competitive advantages for leading growing markets including automotive, event-driven sensors and high-end photography among others

MIGDAL HAEMEK, Israel, September 25, 2019 – TowerJazz (NASDAQ/TASE: TSEM), the global specialty foundry leader, today announced the release of its highly advanced 65nm stacked BSI hybrid bonding technology manufactured in Company's 300mm facility in Uozu, Japan. This new offering, implemented

Part 2
DAQ – Control and Data Paths

DAQ – Control and Data Paths

Sketch from an internal STFC project 2019-2021 to ready our tech for a new generation of ASICs.



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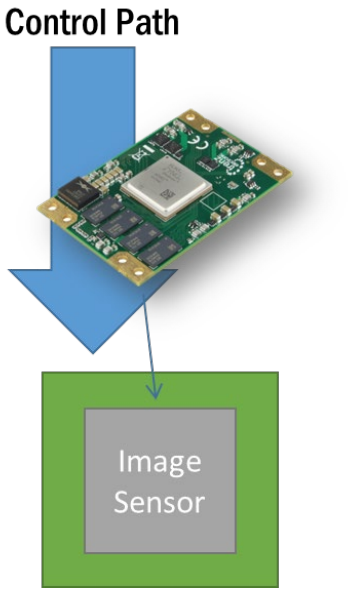
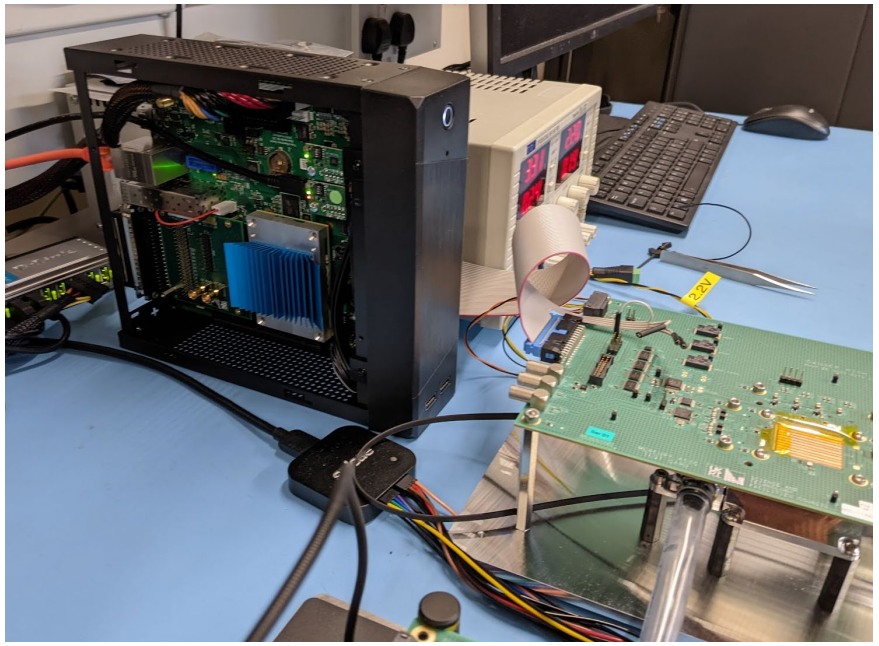
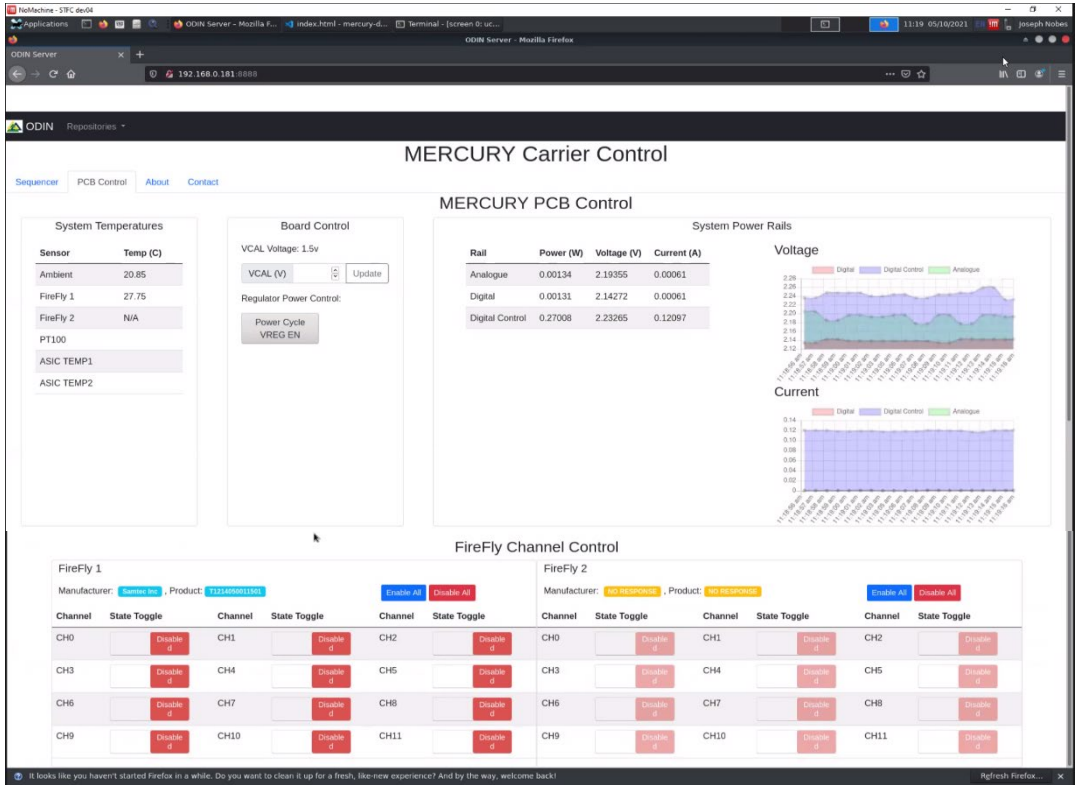
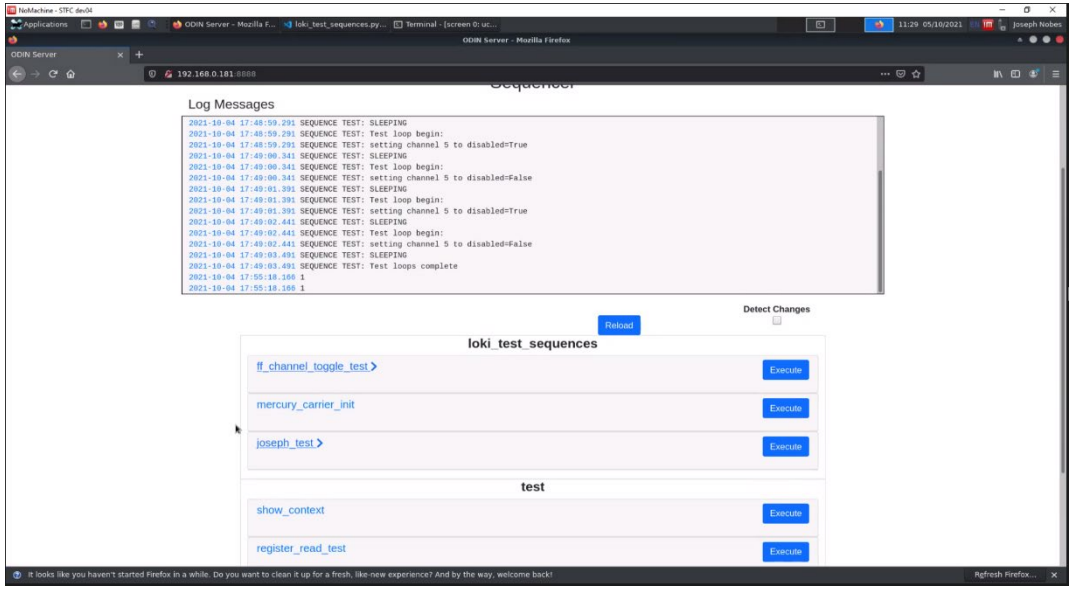
Control Path - ODIN LOKI





Zynq development hardware





Status: The Zynq worked well to develop all the functions needed to control Hexitec-MHz as an example system.

An instance of ODIN control runs on the Zync and is accessed by a web based GUI
Or an API to something like Karabo – same as with LPD PSCU

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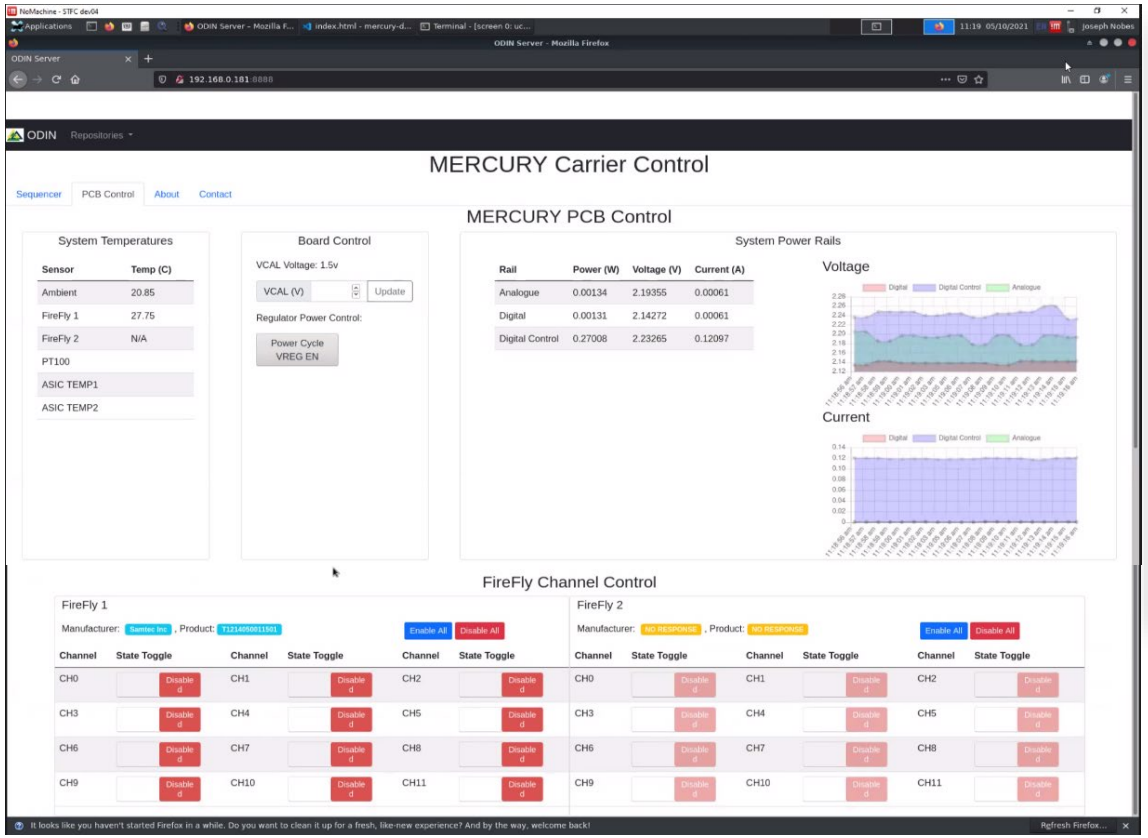
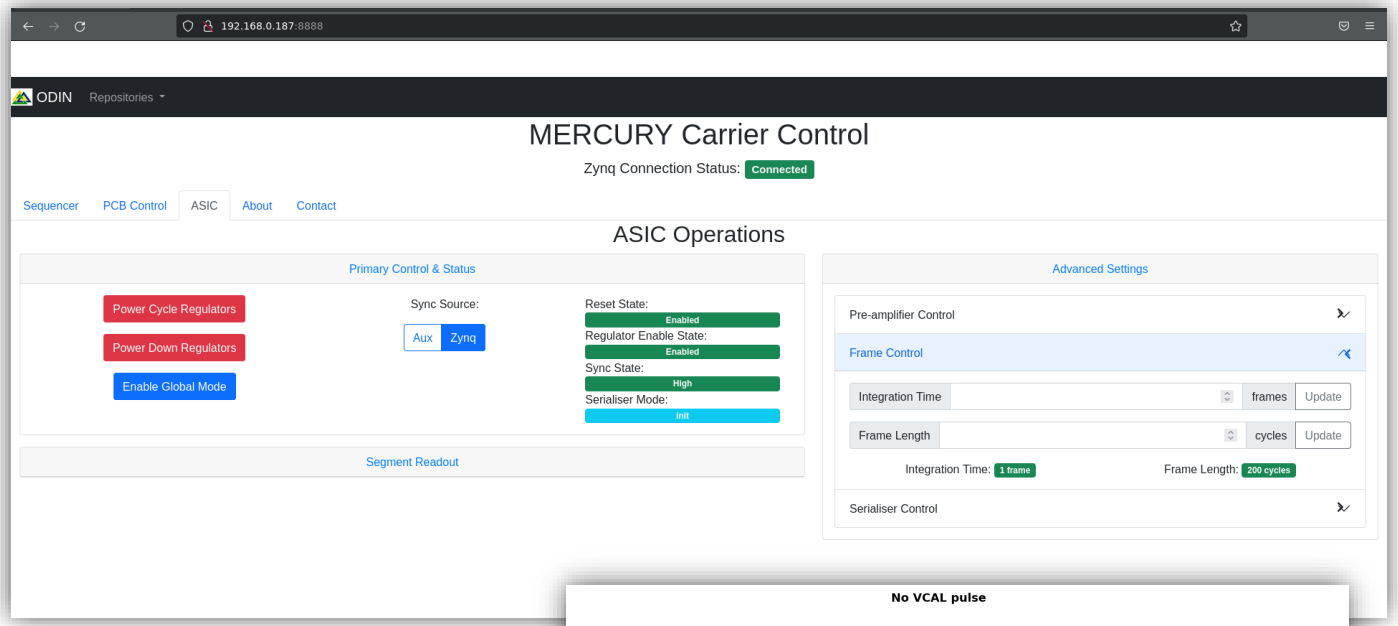
Control Path – ODIN LOKI

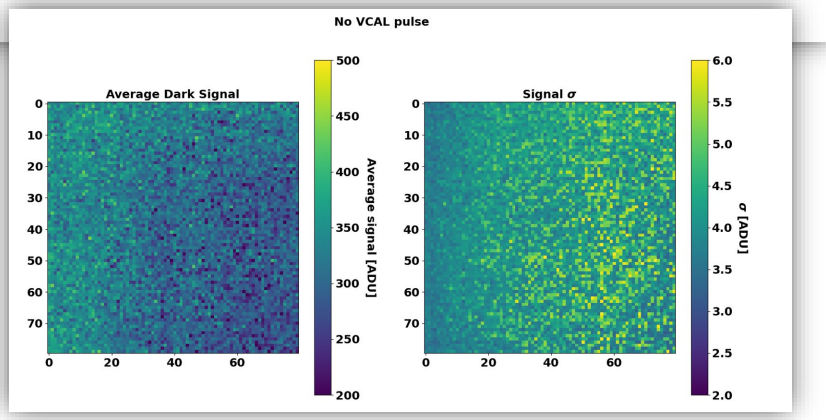
PCB/COB control elements built up in preparation during ASIC manufacture

- ASIC control functions developed dynamically alongside testing
- All core functions easy to control via python scripts
- The most dynamic functions are then pulled up into the GUI
- Development has been fast and flexible.

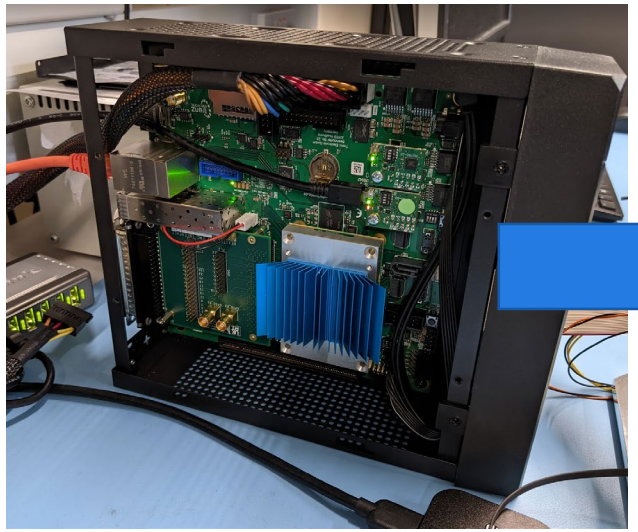


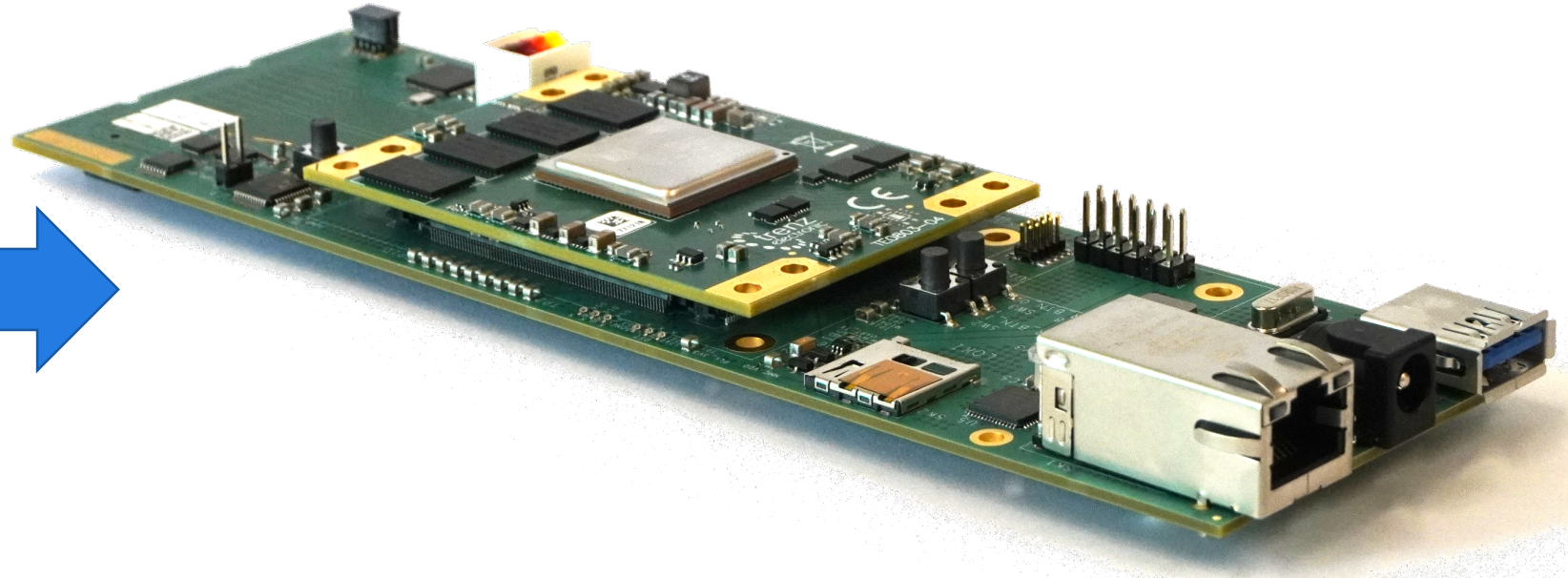


First images readout via slow SPI through control system

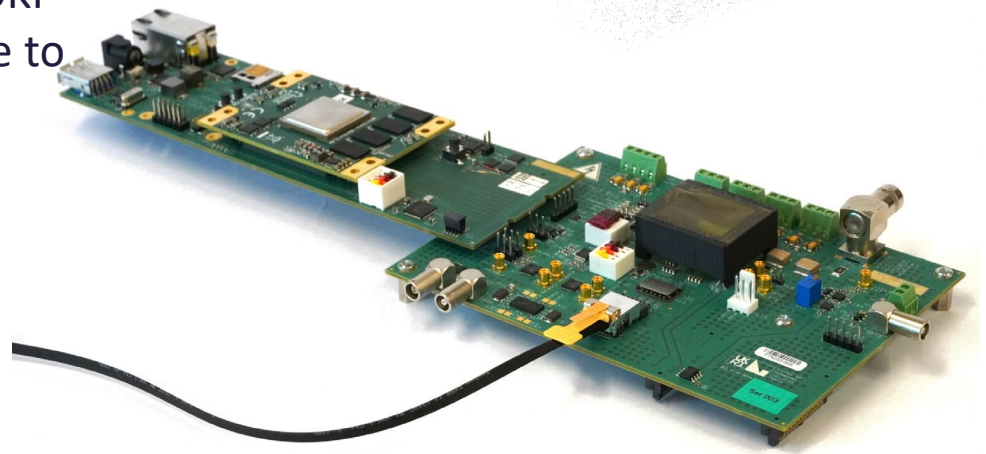


DAQ – Control Path





- Designed and built our own Zynq carrier called LOKI
- Approx. 6cm x 20cm – to be embedded in or close to the detector head
- In use for testing the XIDyn test structure
- Includes:
    - Clock Generation
    - SPI/I2C control
    - DACs
    - Loads of GPIO
    - Some MGTs



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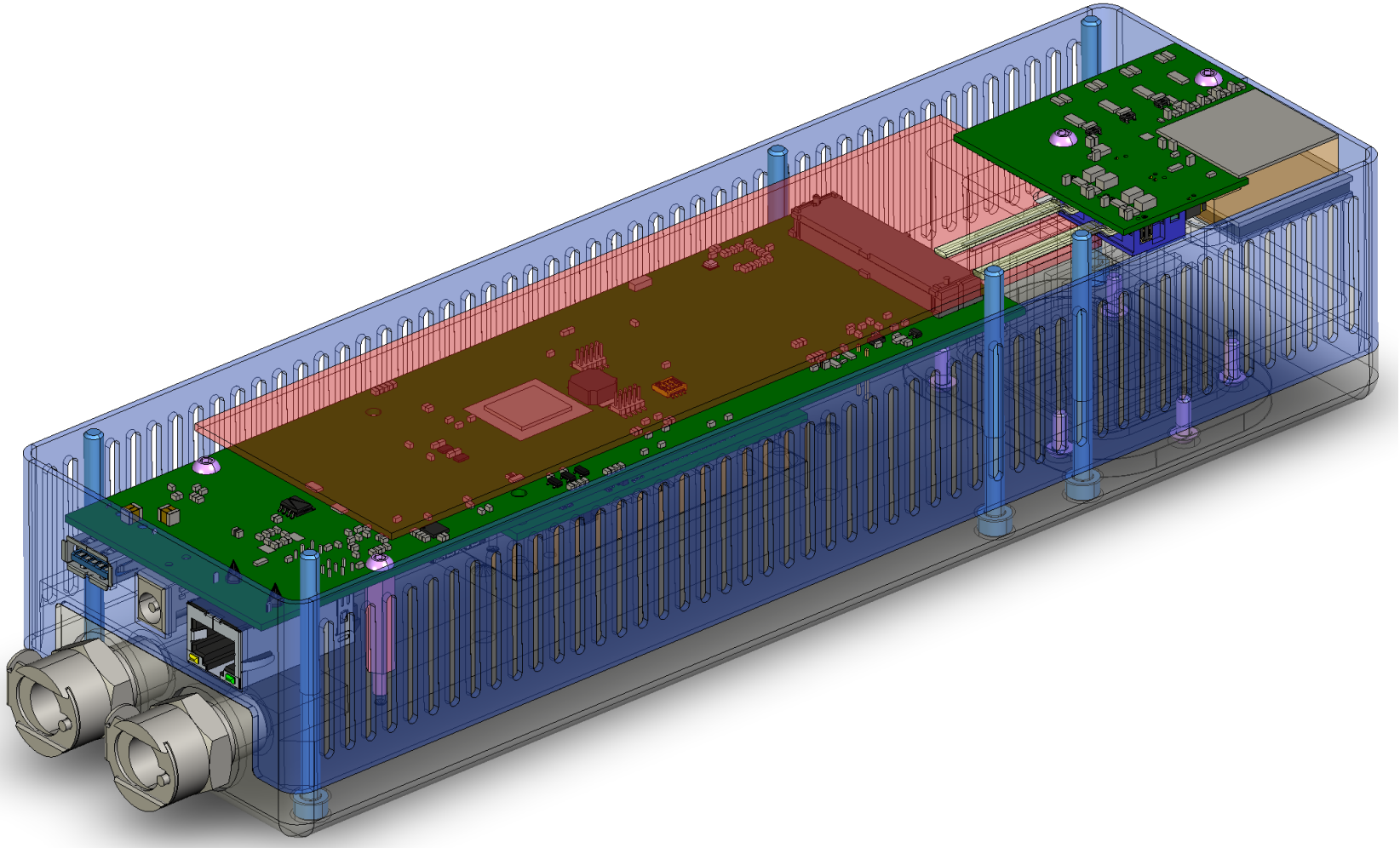

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DAQ – What next for XFEL C&C?

C&C works for this generation of detectors when operated in their original design configuration.

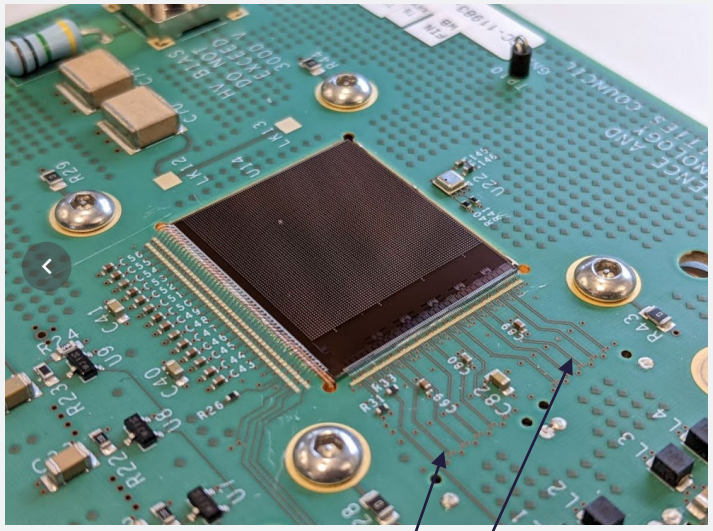
Sometimes it limits our options when trying to do custom modes of operation. E.g. clocking the system more slowly

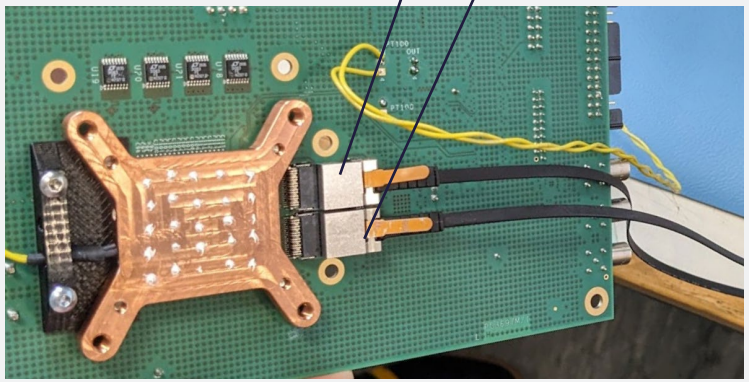
Will there be C&C Version2?

What would that look like?

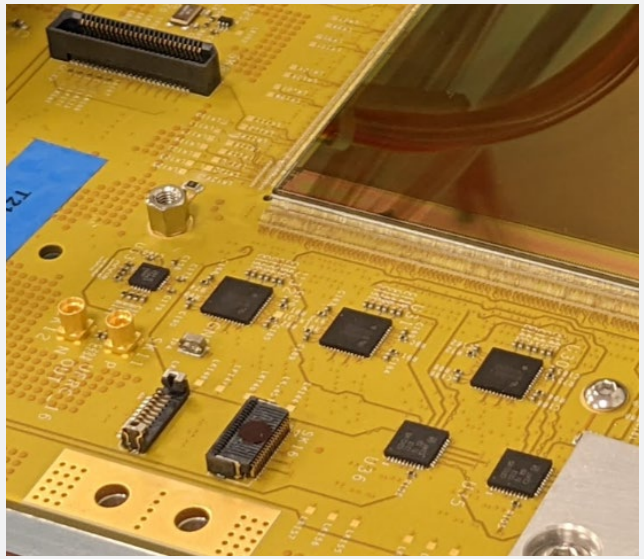
DAQ – Data Path - Chip to Optical

CML Aurora 64/66 can be converted straight to optical

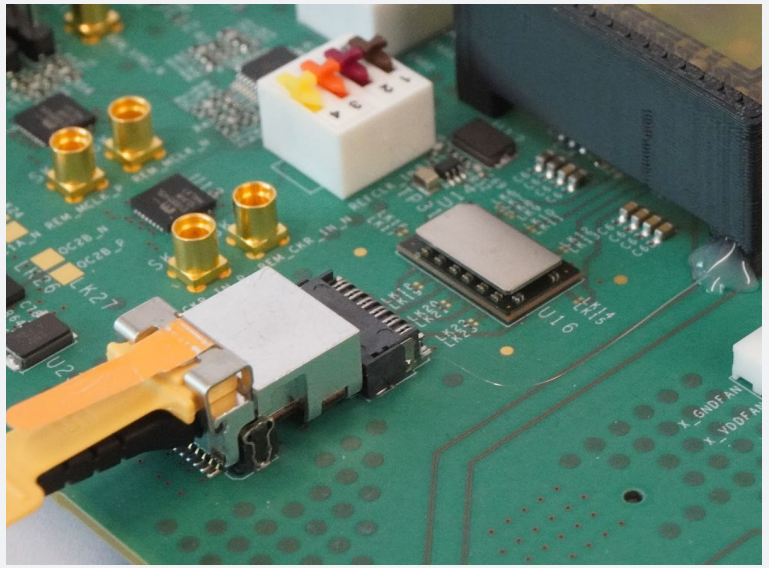




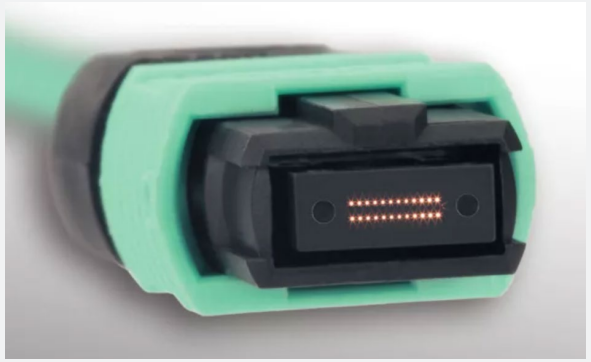
Hexitec-MHz ASIC
Firefly on the backside
No retimers needed at 4.1Gbps



Texas Instruments DS110DF410 Retimer ICs sitting between the **C100 Sensor** and the Samtec Firefly transceiver socket



Texas Instruments DS280DF810 Retimer IC sitting between the **XIDyn Baby-D ASIC** and the Samtec Firefly transceiver



Can fit 24 optical channels into a single MTP connector

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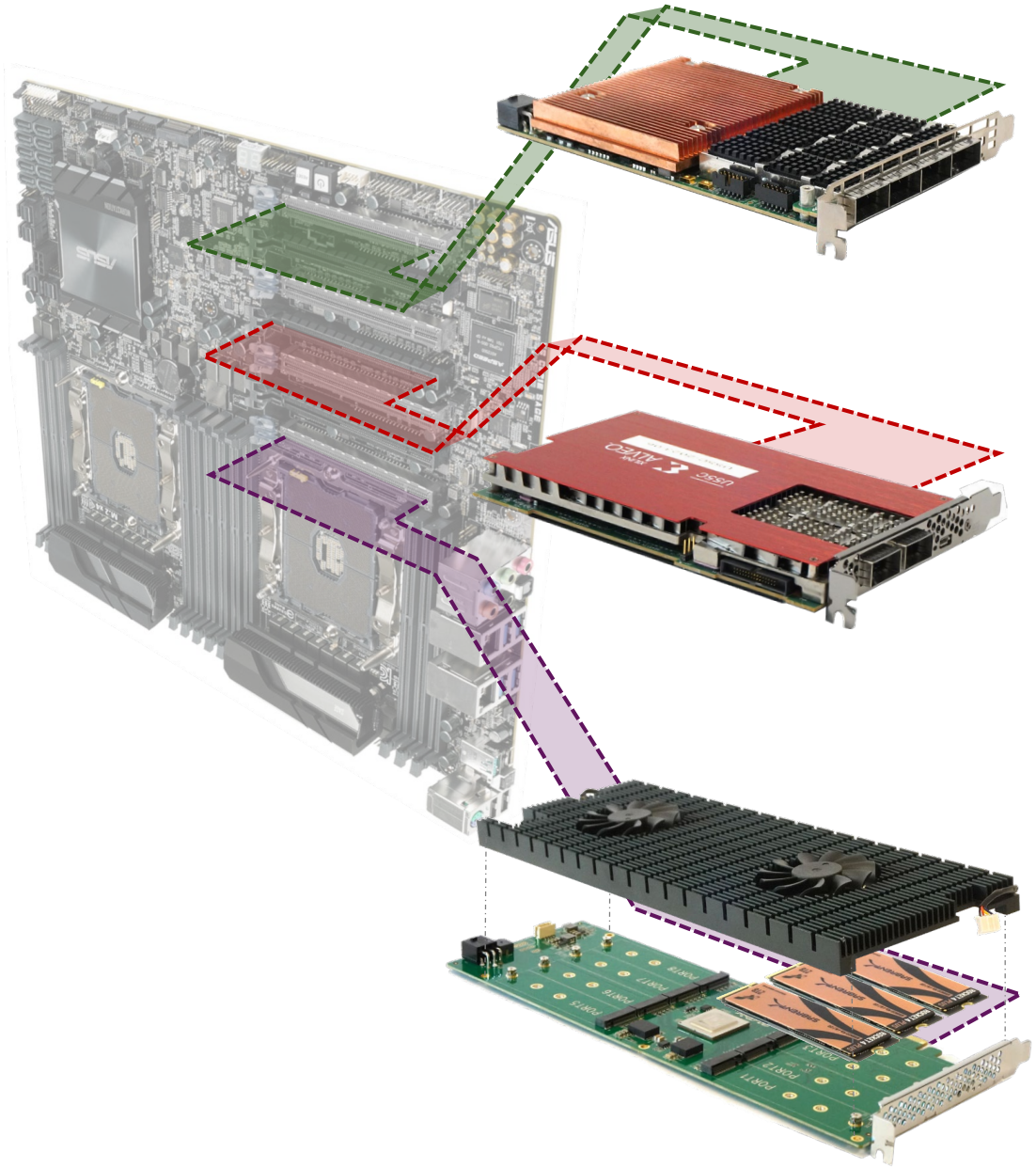
DAQ – Data Path



1st Level FPGA – Frame Building

2nd Level FPGA – Frame Processing

Data Storage @ 100G rates

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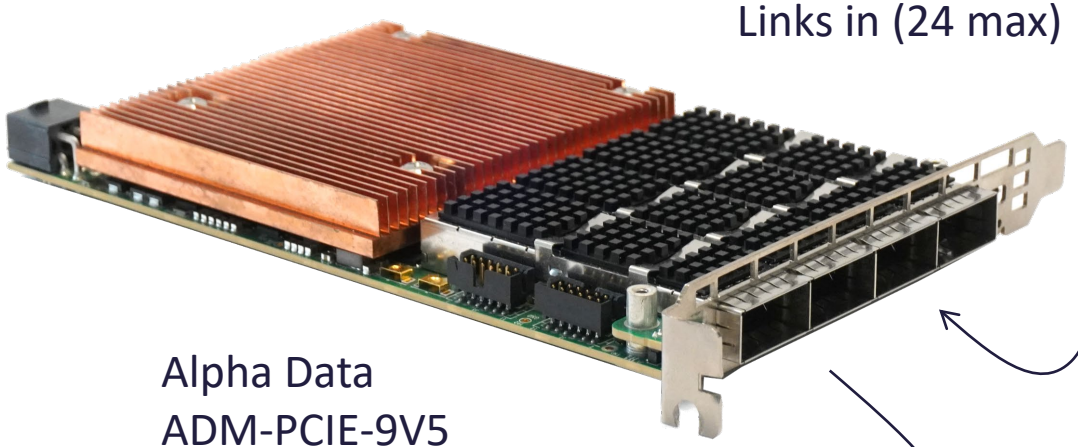
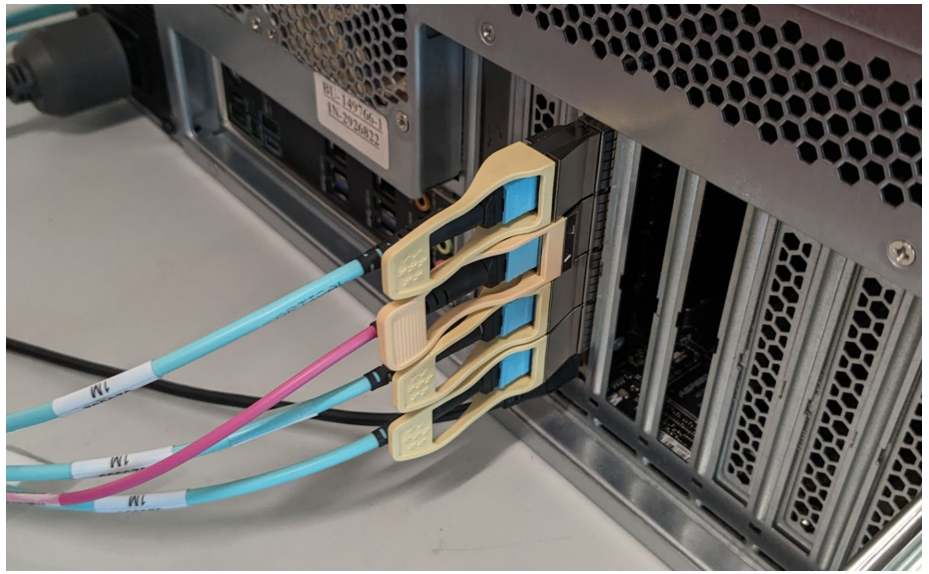
DAQ – Data Path – 1st Level Frame Building



An off the shelf board with large amounts of optical IO is used as a receiver of the serial Aurora 64B/66B data streams from the ASICs.

The purpose of this board is to combine the relatively modest 4-14Gbps streams into full images and then send them back out on 100G Ethernet to be stored or further processed.



Data In 20 x 4.1G Data Out 1-2 x 100G

Results: this has worked well on single channels.
Currently working hard to expand to multiple channels

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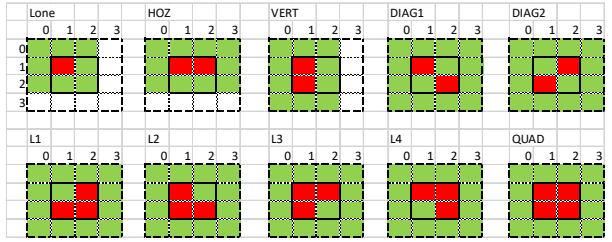
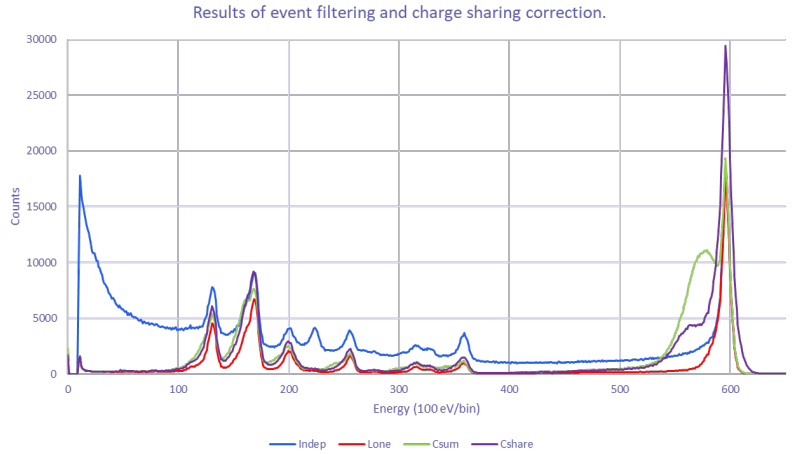
DAQ – Data Path – 2nd Level Frame Processing

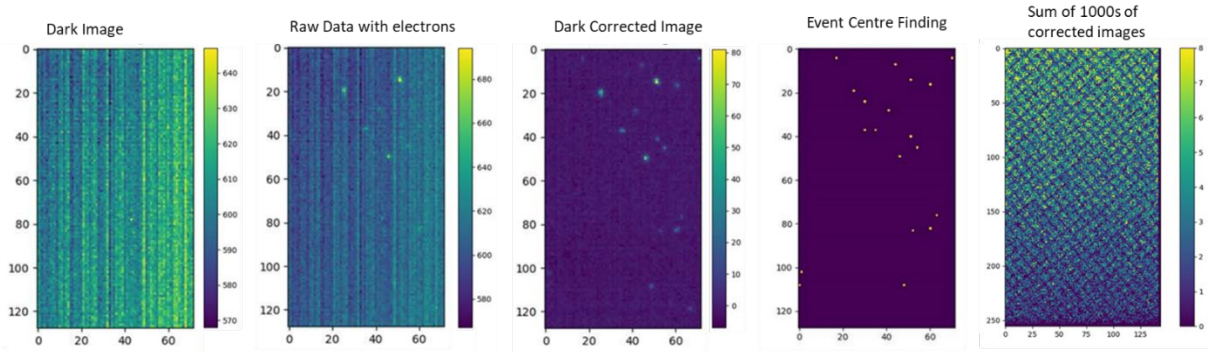
Xilinx Alveo U55C



Left: Classifications of shared pixel events to be identified
Right: Real time generated spectrum from a pixel in Hexitec-MHz following event finding and energy summing across pixels.



Hexitec-MHz is ideally suited to data reduction with histogramming.
What about other sensors and applications? Cryo EM example below



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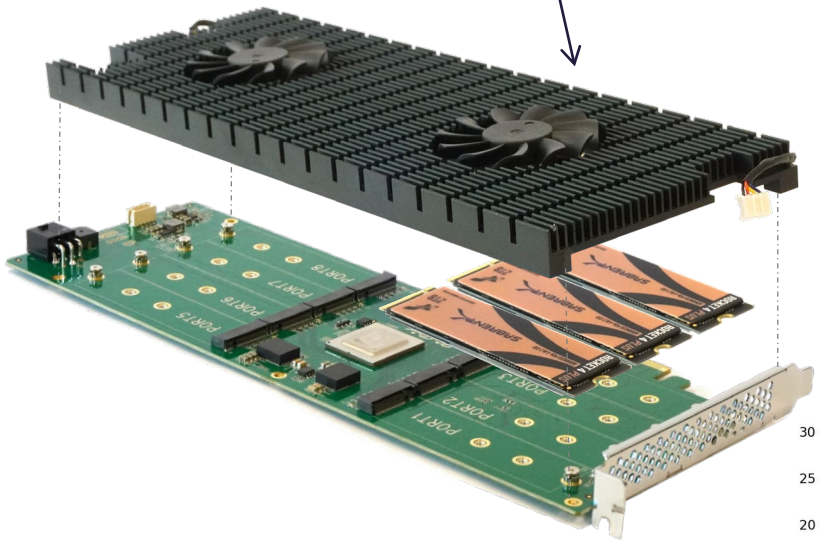
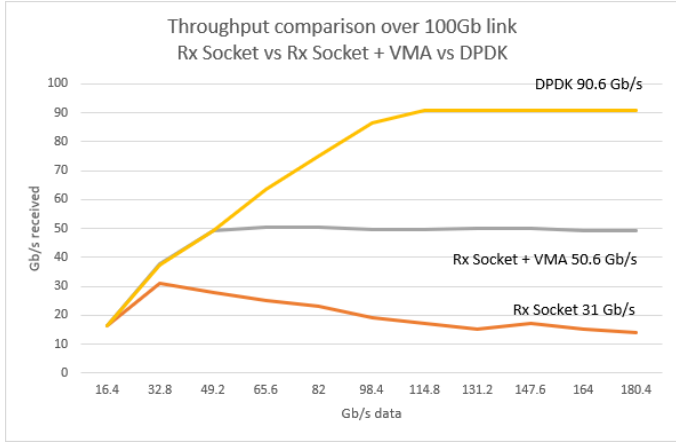
DAQ – Data Path - **Storage**

Data arrives on 100G NIC

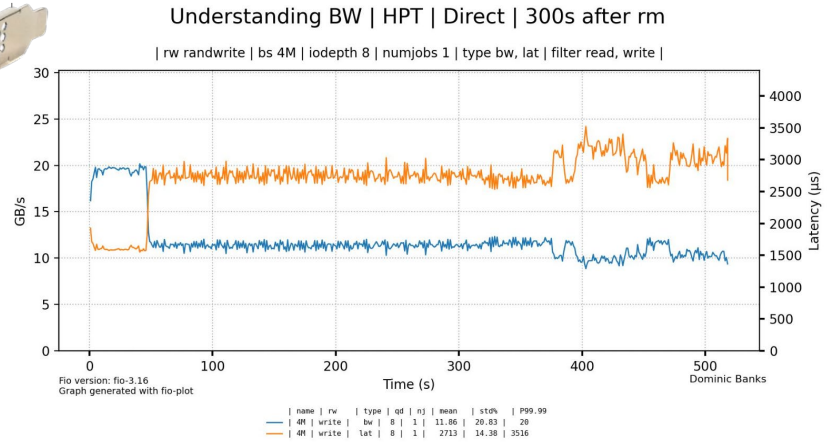


Highpoint SSD7540 PCIe with
SABRENT Rocket4 PLUS 2TB NVMe drives

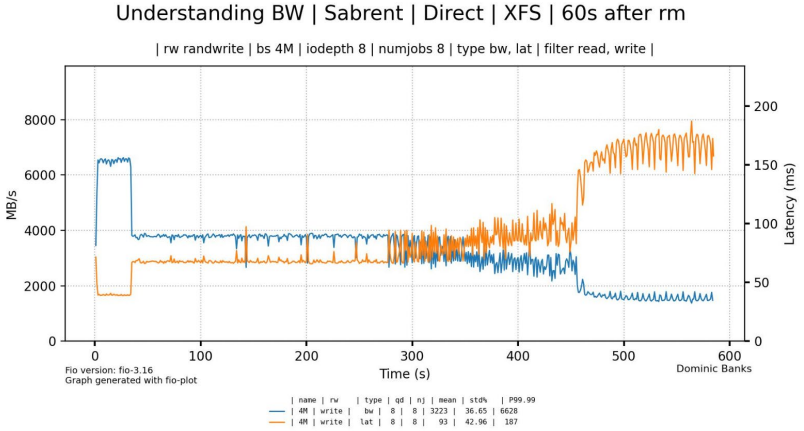
Work to maximize bandwidth from NIC to Disk
Using DPDK (Data Plane Development Kit) – *alternative to RoCE*
Allows us to maintain around **90Gbps over a 100G link**
Rest of the development based around the 100G building block.



In the development phase of these new projects the aim is to be able to save a few mins of raw data. Enough to characterise the sensors and do some meaningful experiments. We are now testing with 16TB arrays of 8x2TB NVMe drives



Results from an array of 8 NVME Samsung 980s



Results from a single Sabrent 2TB drive

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Part 3
Lessons Learnt in Detector Dev

Tips for the inception to first delivery stage

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Planning and Time Scales

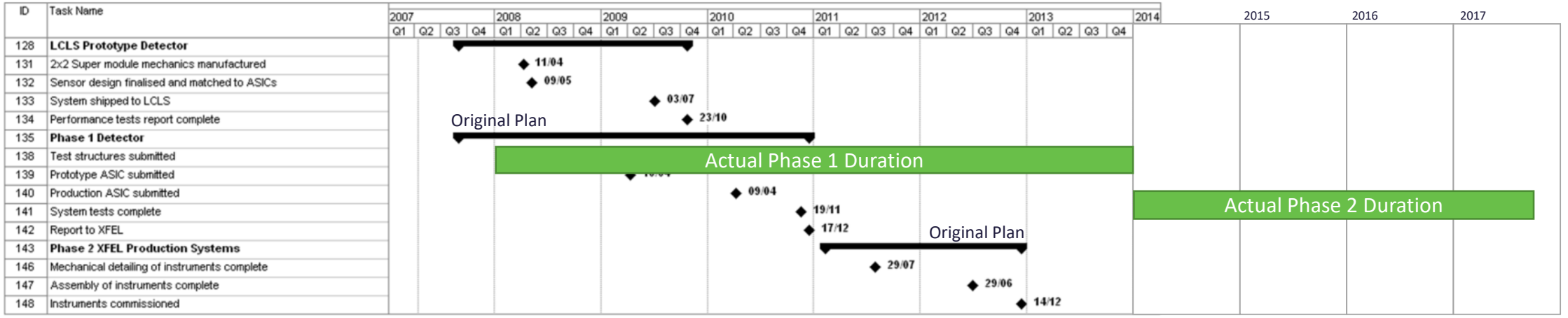


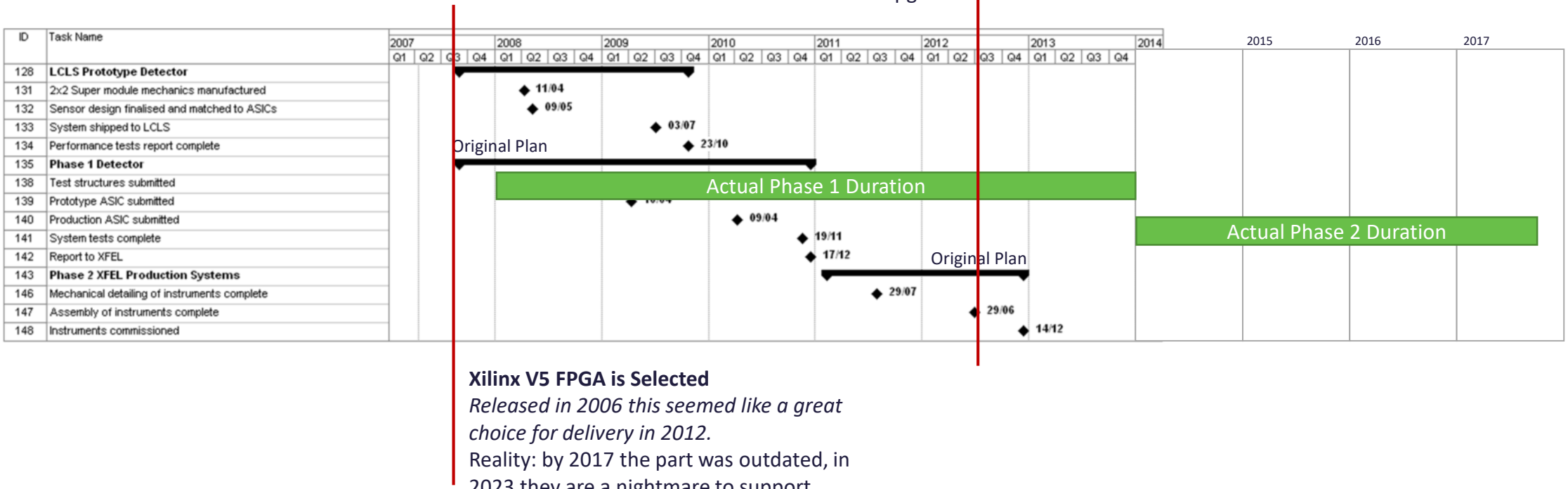
Figure 25: High level plan and key milestones

Phase 1 of the project to make a prototype system – **took around twice as long as planned** and the size of detector was also downscaled to allow us to finish.
Phase 2 of the project was re baselined – though also took 50-100% longer than expected.

Building Large area detectors is way harder than you think. Scheduling during the formation of a project may be very optimistic, the same approach once a project is active can be damaging to internal decision making.

Risks of Over Optimistic Schedules

Chip Design Ends @ V2
One factor is that the final system is expected to be delivered so soon another chip is not possible.
Reality: it's another 5 years until delivery but there is no ASIC upgrade.



Xilinx V5 FPGA is Selected
Released in 2006 this seemed like a great choice for delivery in 2012.
Reality: by 2017 the part was outdated, in 2023 they are a nightmare to support.

Building Large area detectors is way harder than you think. Scheduling during the formation of a project may be very optimistic, the same approach once a project is active can be damaging to internal decision making.

Short timescales are desirable and a tempting way to motivate – **Consider how you plan with realistic schedule uncertainty while maintaining motivation.**

LPD Phase 1 Key Events

Testing and Characterisation

ASIC/Sensor Development

Aug 2008 - Sensor Design – Hamamatsu 1-level metal design with a central pixel array

Sept 2008 – LDP Test Structure 1 – STFCs first 130nm Submission

Jan 2009 – The Interposer is Born – LPD moves to a fully flat design

June 2010 – LDP ASIC V1 – full size readout chip

August 2011 – DORIS Radiation Damage Beam Test – Direct beam irradiations of complete tile

April 2012 – LPD 2-tile system operational

July 2012 – LDP ASIC V2 – Modified 5pF gain, ADC sample timing bug fix, Radiation hardness improvements

Sept 2012 – Radiation Shields Ordered

Jan 2013 – LPD 2-tile Delivered to XFEL

Early May 2013 – 1st LCLS Beam Test – Bias Ω and power supply issues

Late May 2013 – 1st Petra Beam Test – 2-tile system

LPD Phase 2
Key Events

Jan 2014 – 2nd Petra Beam Test –
2-tile system, running with Karabo

Feb 2014 – LPD Quadrant Delivered to XFEL

Sept 2014 – Philipp Lang Joins XFEL

October 2014 – Diamond Beam Time
Mono Chromatic Radiation Damage Study

Sept 2015 - ESRF Beam Time
4 Bunch mode, LPD super-module, FXE like experiments

Sept 2015 – LPD Power Supply Upgrade
1000s x improvement in the noise performance

April 2016 – Diamond Beam Time
Hybrid Mode LPD Testing

May 2016 – LPD 1M Housing Delivered

Nov 2016 – 2nd LCLS Beam Time
GaAs Detectors and Check of LPD

Feb 2017 – LPD 1M 'Finished'

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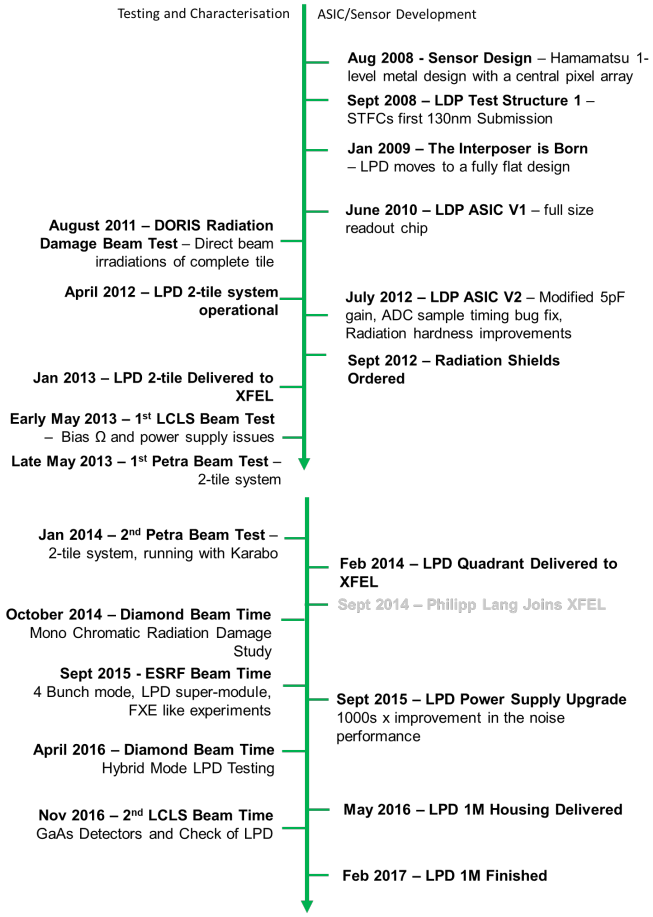
Things to learn from the key events

ASIC Design Timescales

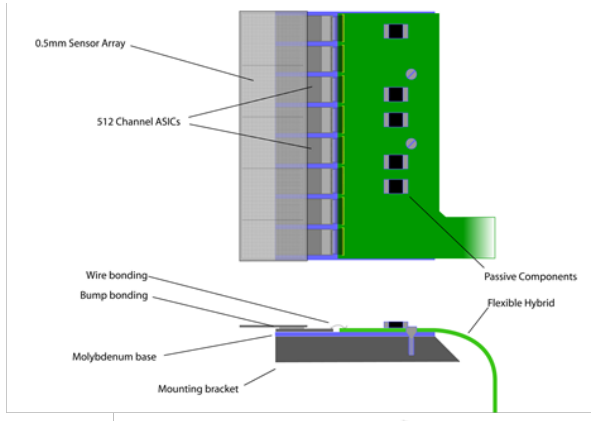
- Test structure – 6 months to 1 year design time (new process)
- ASIC V1 – 2 years design work from submission of test structure
- ASIC V2 – 2 years of test and redesign from submission of previous ASIC
- Despite what seems like a long design process it was only 4.5 year of a 10 year project. **The challenges the ASIC creates are just as big as the original design.** If a month of extra design can make life easier in future it may well be worth the wait.

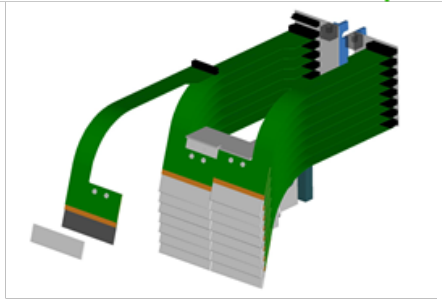
Test and Characterisation

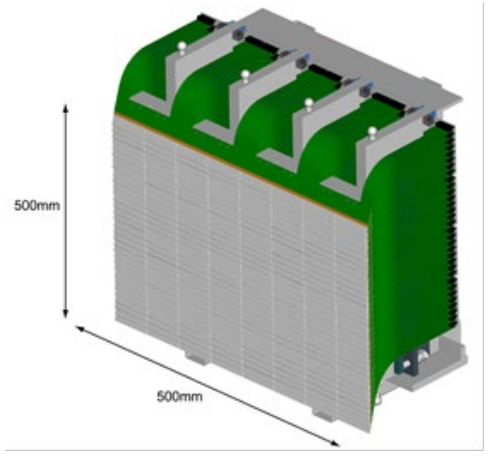
- We planned and budgeted for 1-2 beam tests. In reality there were 8 in total during the project to delivery. Approx. £250k in effort
- **Beam tests need 6 months to 1 year between them** for analysis and corrective action.
- There's been a further 6 x week long detector development tests since 2017 alongside user operation. A week of beam at XFEL is worth 1MEuro. **Straightforward calibration the holy grail**



Design and plan for scale – expect change…







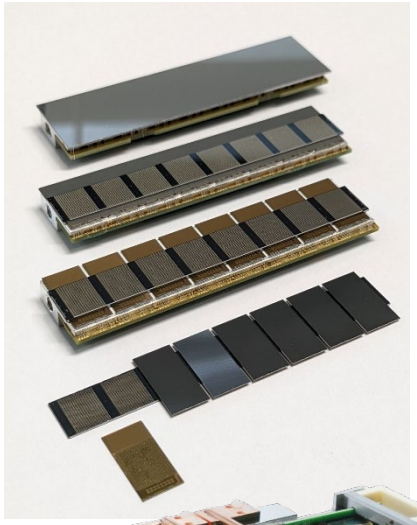
Physically there were massive changes from the concept to the final delivery. Mostly to do with having a completely flat detector face.
…But the core foundations remained the same.

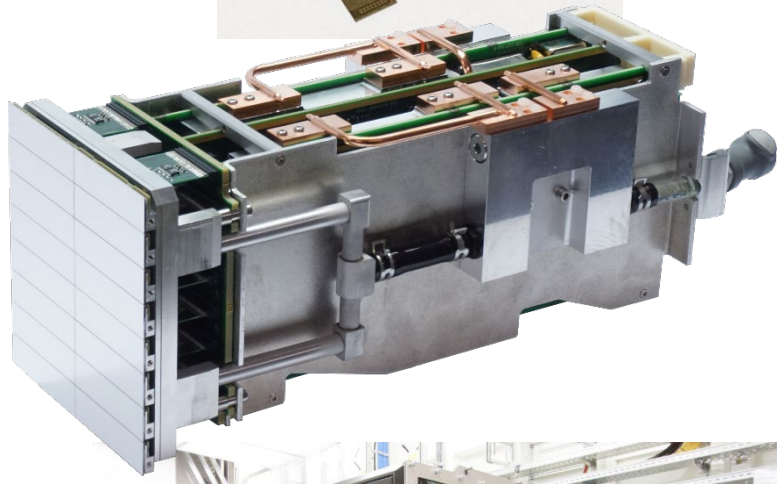
Everything is in base-2

- 16x32 = 512 pixels per ASIC
- 512 memory cells
- 16 ADCs
- 16 bit values (ADC value + Gain bits)
- 8 ASICs per Module
- 16 Modules per Super-module
- 16 SMs per 1M detector

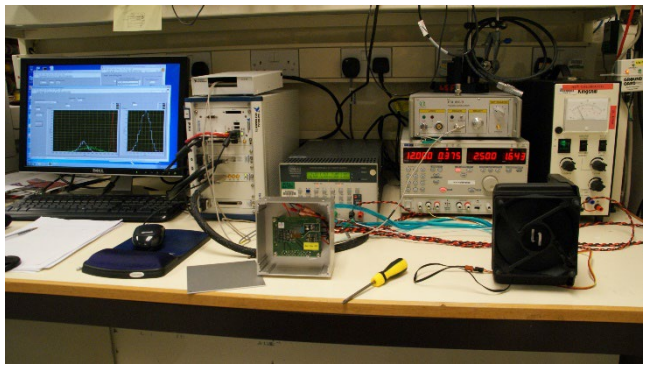
Pixel size is a round number

- 500um is very easy to work out positions
- Gaps between units are a whole number of pixels.

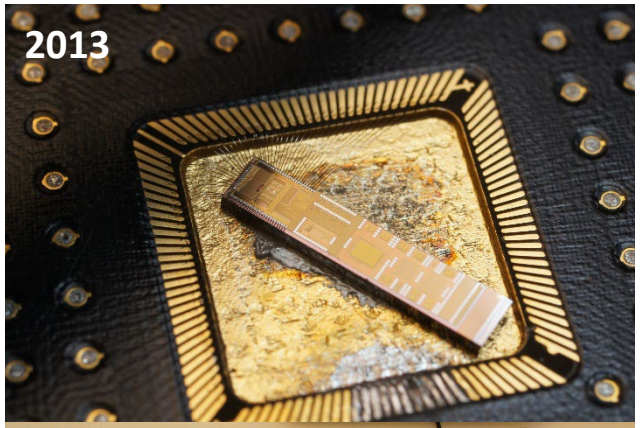


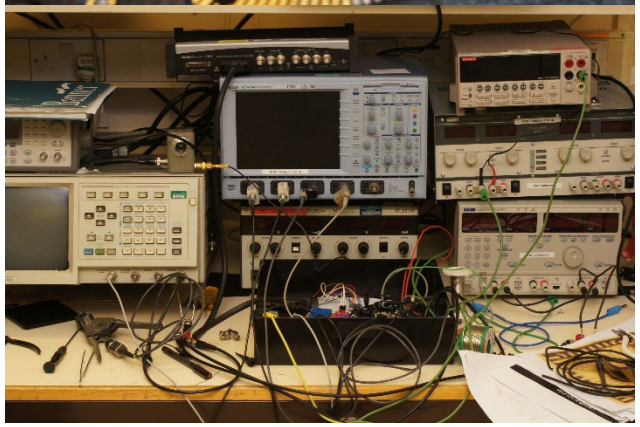


Designed for scale but **tested in baby steps**



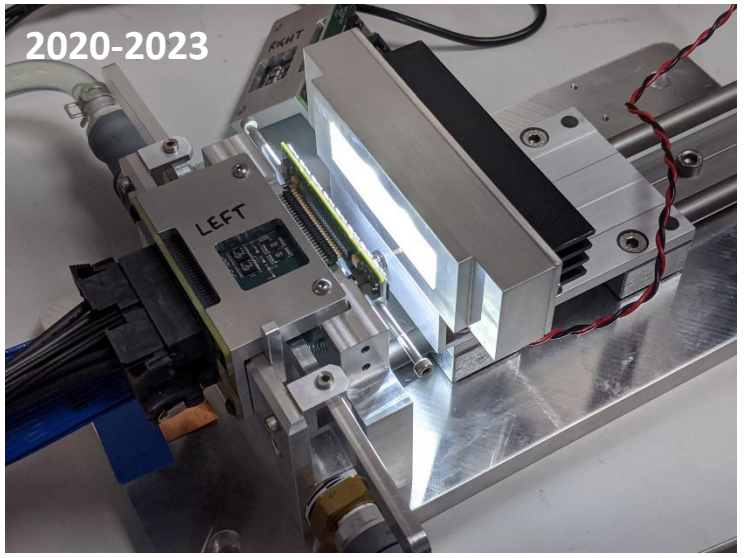
LPD V1 – tested as a single with NI system.
Sensor wire bonded to one side





Second Test Structure – Focus on amplifier performance and noise analysis

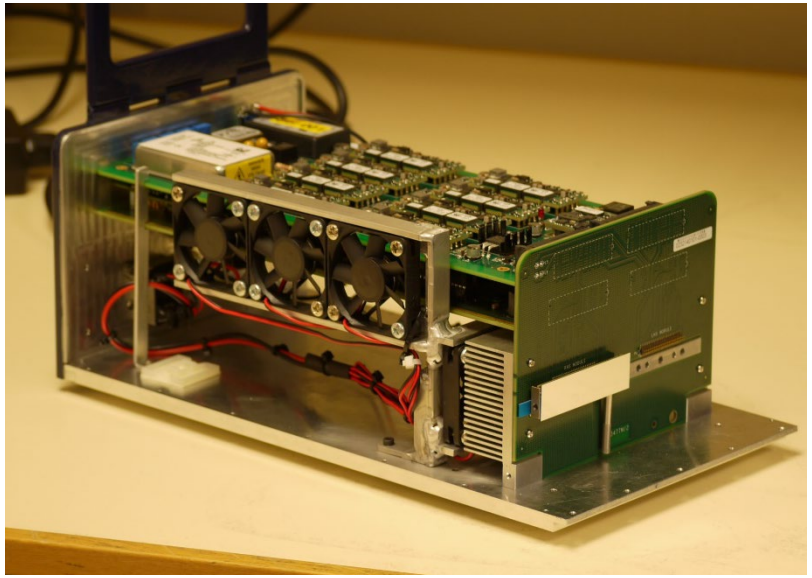
Wafer probe station testing – The ASIC is operated with all pads at full power and full images readout. Same NI systems as original chip tests.



Clean room test station – Tiles are tested 2-3 times during assembly for QA.

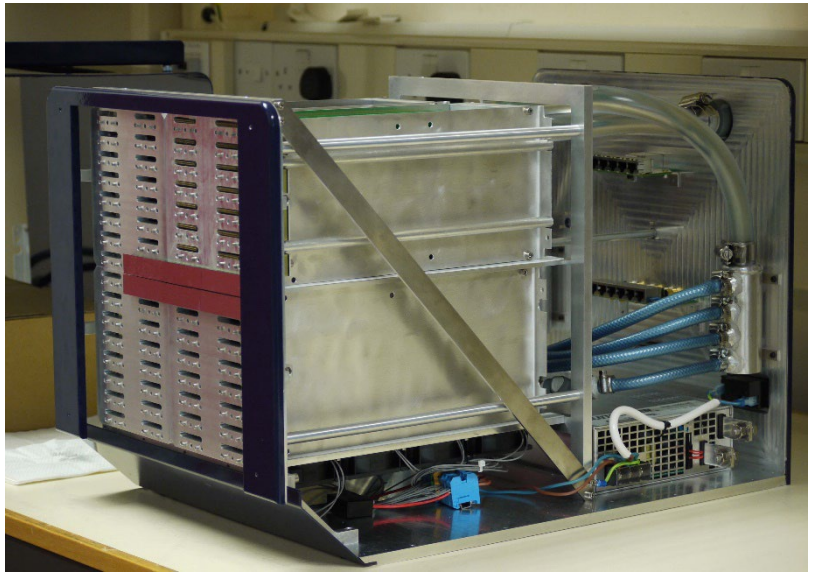
A world leading chip is a complex chip, and will take 6 months to 1 year to really get the basics figured out. Any less and it must have been too simple. **Plan for this and make multiple test systems available for the long term.** Also key for the end game wafer probing and production QA.

Designed for scale and **also delivered in baby steps**



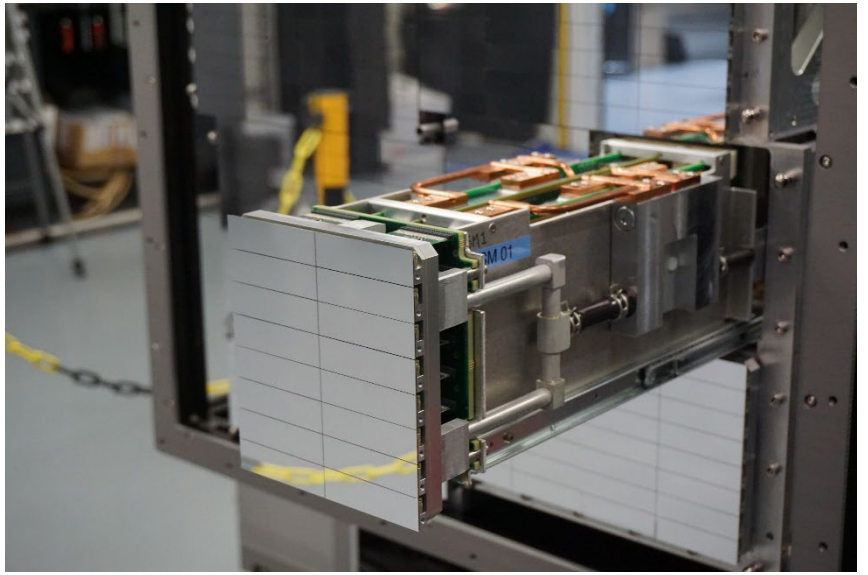
Jan 2013 – first 2 tiles system delivered to XFEL

Allowed the end user to test their clock and trigger systems.
Develop software integration
Learn about how to test with sources.



Feb 2014 – Quad system delivered to XFEL

Allowed the end user to develop the integration and control of multi node systems.

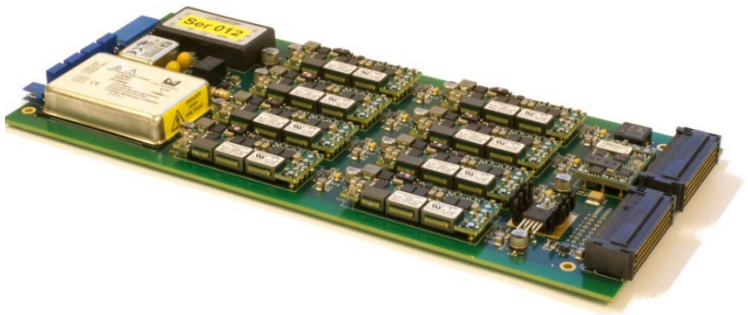


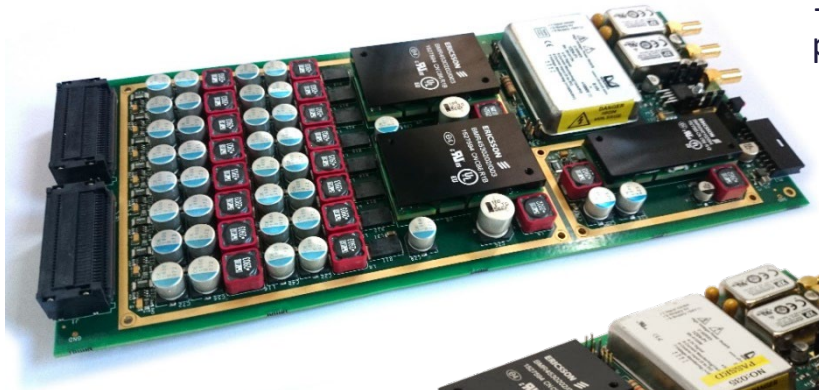
March 2017 – 1M system delivered

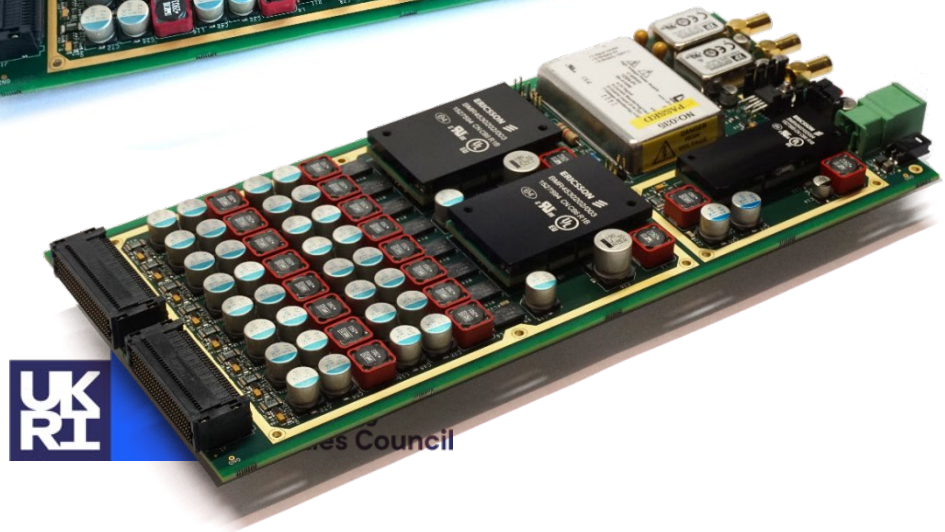
The final system looks completely different but **worked with their systems within days of being delivered.**

Let your users/collaborators access your hardware early as possible – even if bits are missing, they will learn so much.

Risk Balance - Risk Aversion – Sometimes worth taking risks.





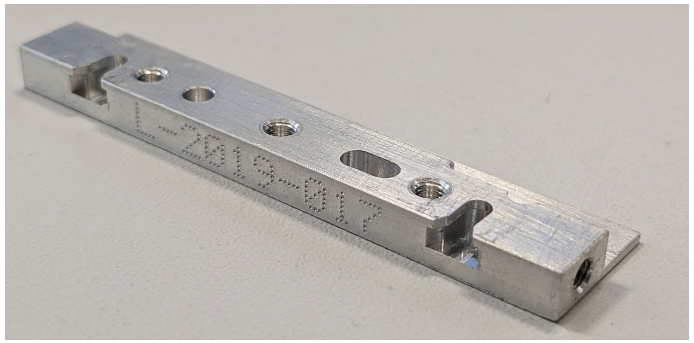


LPD Power Card
6 Revisions to settle on the final design.
vs
1000x times higher performance.

Example here is PCBs, but same can be true elsewhere. How long to spend getting a design perfect vs iteration will depend on the design cost vs manufacture cost.
Aversion to risk can result in very long and costly design times – with iteration still required.
Same can be true in Mechanical design – 3D printing is a great tool to expedite time to test.

LPD Final PCB Iterations

- COB – Version 4
- Feedthrough – Version 6
- Backplane – Version 2
- Power Card – Version 6
- FEM – Version 3
- PSCU – Version 2



LPD Sensor Baseplate
Revision F – optimised for flip chip alignment and rapid bond yield testing.

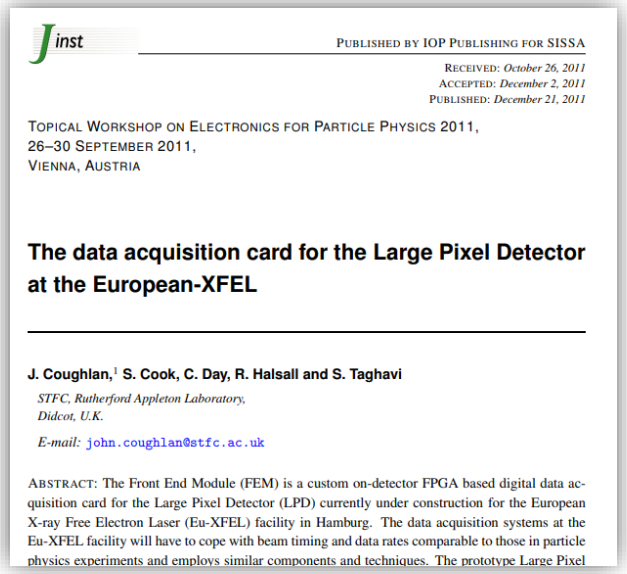
DAQ

LDP had the perfect scenario – 1 lead designer for the last 10-15 years.

We are on Firmware Revision 02e2 = 738 repository updates

The road is long and a challenge as complex as ASIC design.

Staff retention is even less likely for the lifecycle of f/w than ASIC design.
Needs well specified architecture with self contained functional blocks, documented etc.



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VIENNA, AUSTRIA

The data acquisition card for the Large Pixel Detector at the European-XFEL

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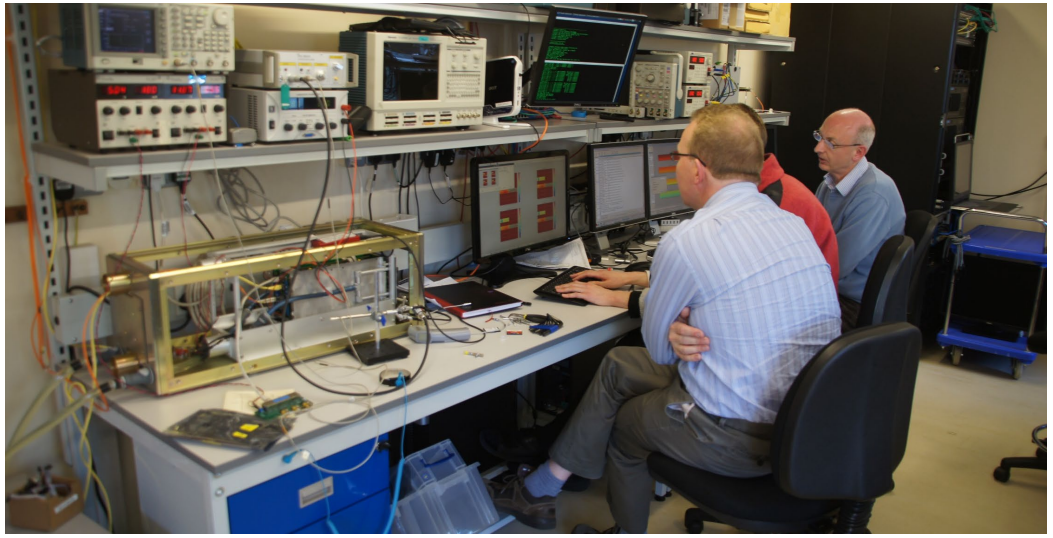
ABSTRACT: The Front End Module (FEM) is a custom on-detector FPGA based digital data acquisition card for the Large Pixel Detector (LPD) currently under construction for the European X-ray Free Electron Laser (Eu-XFEL) facility in Hamburg. The data acquisition systems at the Eu-XFEL facility will have to cope with beam timing and data rates comparable to those in particle physics experiments and employs similar components and techniques. The prototype Large Pixel

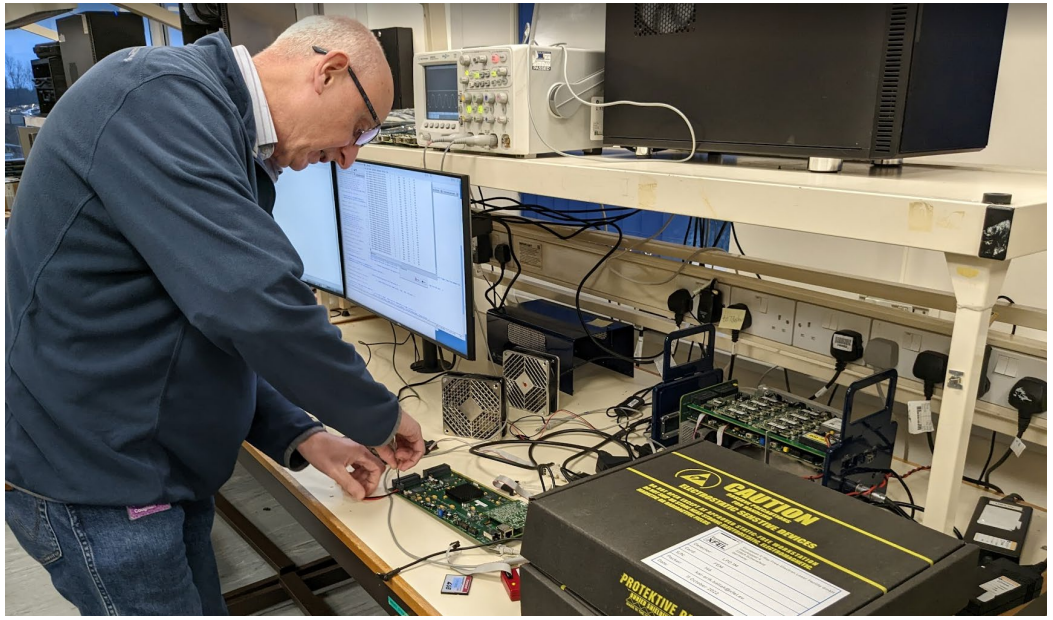
The first boards were complete around 2010,
Papers published in 2011,
First beam tests in 2013,
Full facility spec. f/w in 2018
Fix for performance drift 2023

Firmware was always one step ahead of the current requirement (status of the facility).

2013 – John Coughlan helping preparing for first test at LCLS



2023 – John Coughlan testing with a new firmware version



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Conclusions/Thoughts

- There is ASIC IP out there to accelerate years of development
- We have DAQ in place for development of systems in 100G units.
    - On the fly processing for easy applications.
    - TBC – how does DAQ look/cost when scaled
- DAQ is as hard and long a process as ASIC design
    - Best done very closely with the ASIC designers
    - Rushing ASIC design to meet a budget deadline can make DAQ even harder
    - Can we share IP in DAQ like we do for ASICS?
- Even if your ideas for the next generation may seem more straightforward – it will still take you longer than you think.

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Questions?