DECTRIS

Next Generation MHz Detector with High Dynamic Range

Michael Rissi, Head of Product Management

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DECTRIS - Purpose and Mission

We want

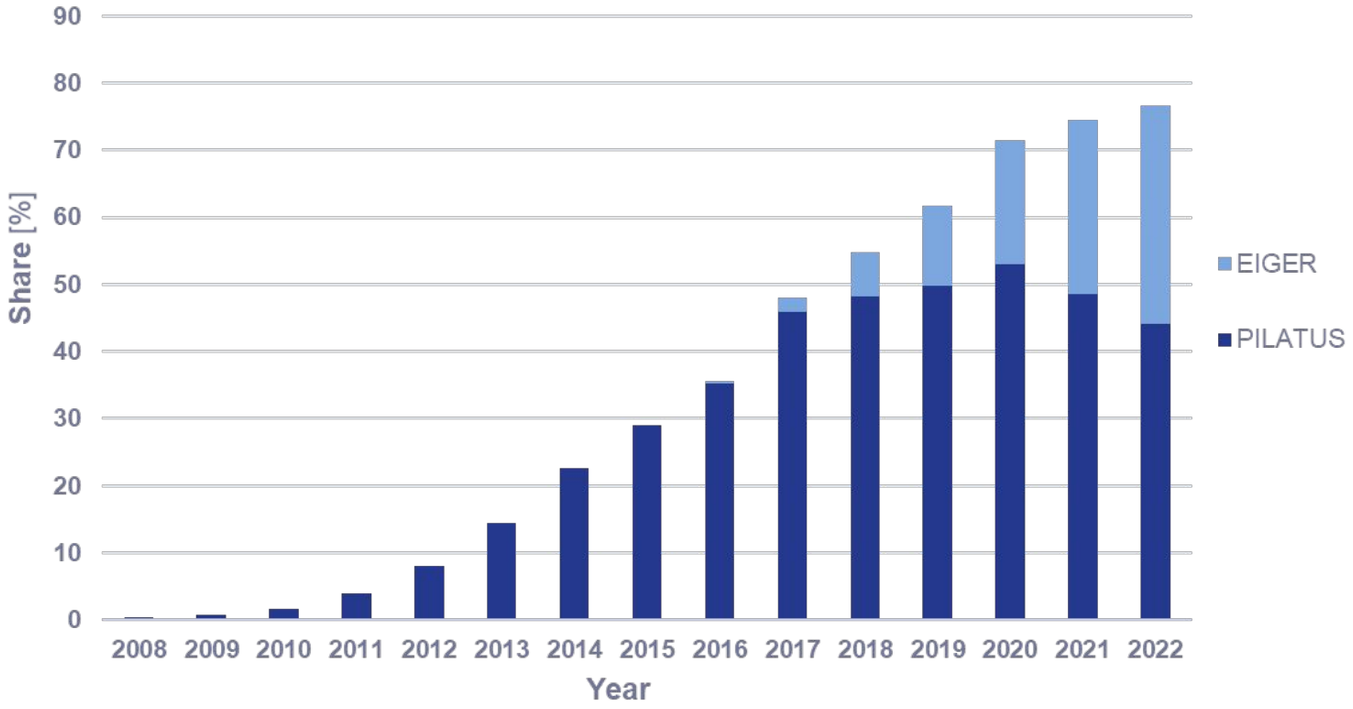
- to serve present and future generations in mastering society's most important challenges by **enabling scientific** and technological **breakthroughs**.

- to **challenge** the **limits of detection technology** and **collaborate with partners** on providing transformative solutions beyond detectors.

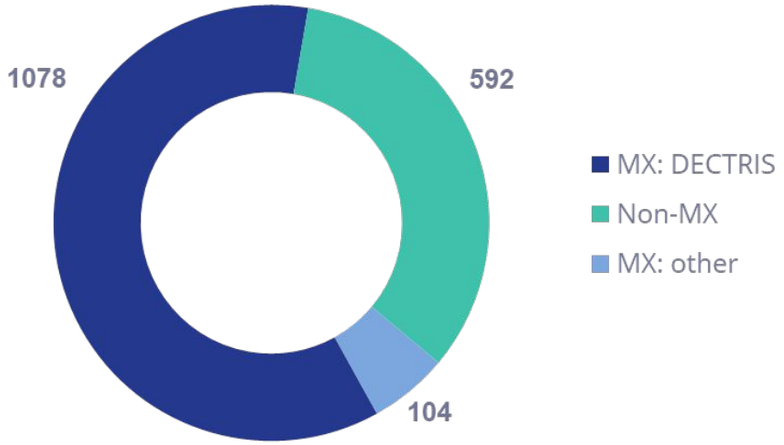
=> We transfer **cutting edge** **technology** into a **reliable** **product** and make it available for the broader scientific community

DECTRIS Detectors Transforming Protein Crystallography

Protein Crystallography structures in PDB determined **with DECTRIS detectors**



SARS-COV2 protein **structures** in PDB determined with **DECTRIS Detectors**



DECTRIS accelerates modern drug development

How can we contribute to a MHz XFEL Detector?

We transfer cutting edge technology into a reliable product and make it available for the broader scientific community

Support and service

- we guarantee support during the full product life cycle

Module production and delivery

- reliable production of modules on an industrial level
- reliable detector systems with systems running for more than 10 years
- stable supply chain

ASIC design

- specialized, application specific
- robust, stable, “they just work”
- designed for testing

Firmware design

- test driven and modular design

Hardware design

- >3k systems in the field

Goal for a MHz Detector and DECTRIS Contribution

The project's objectives is to develop X-ray detectors for the European XFEL GmbH with a frame rate of **1 MHz**, with smallish pixels with a pitch **below 150 µm** and that can measure instantaneous x-ray pulses with a **high dynamic range**. The detectors shall be built up from modules. The detectors are required to be **easily serviceable**, with interchangeable modules. As per the pre-agreed lifetime of the detectors, DECTRIS will offer service and replacement parts.

DECTRIS contribution in a collaboration:

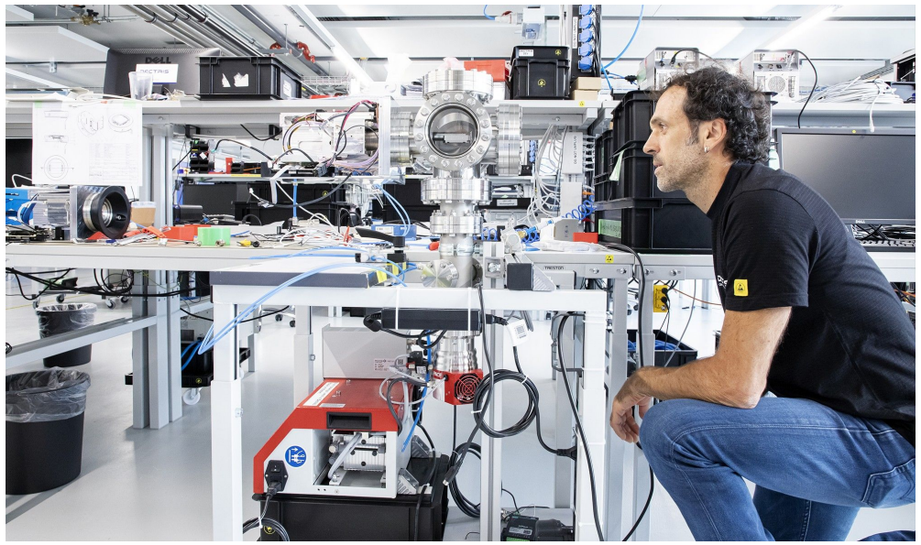
- ASIC design
- ASIC readout (ASIC to FPGA)
- Module hardware and firmware
- Module production + supply chain
- Module servicing during full lifetime

DECTRIS - Balancing Cutting Edge and Reliability

Reliability:

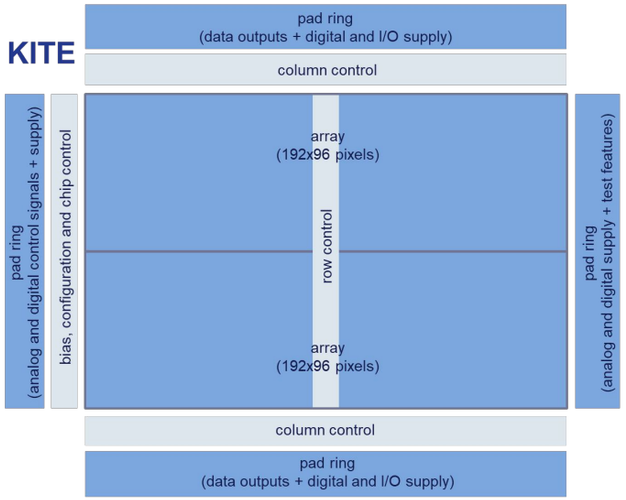
> 3000 Systems in the field

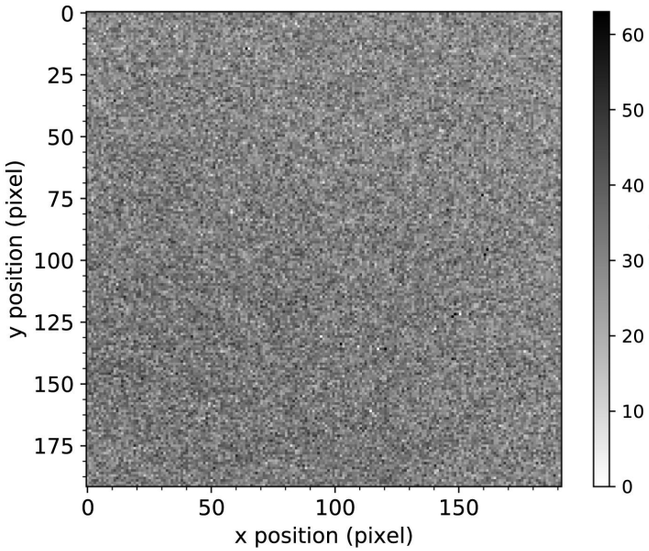
- stable production of modules and systems
- full support of systems with short response times



Cutting Edge:

KITE ASIC enabling 4D STEM Applications

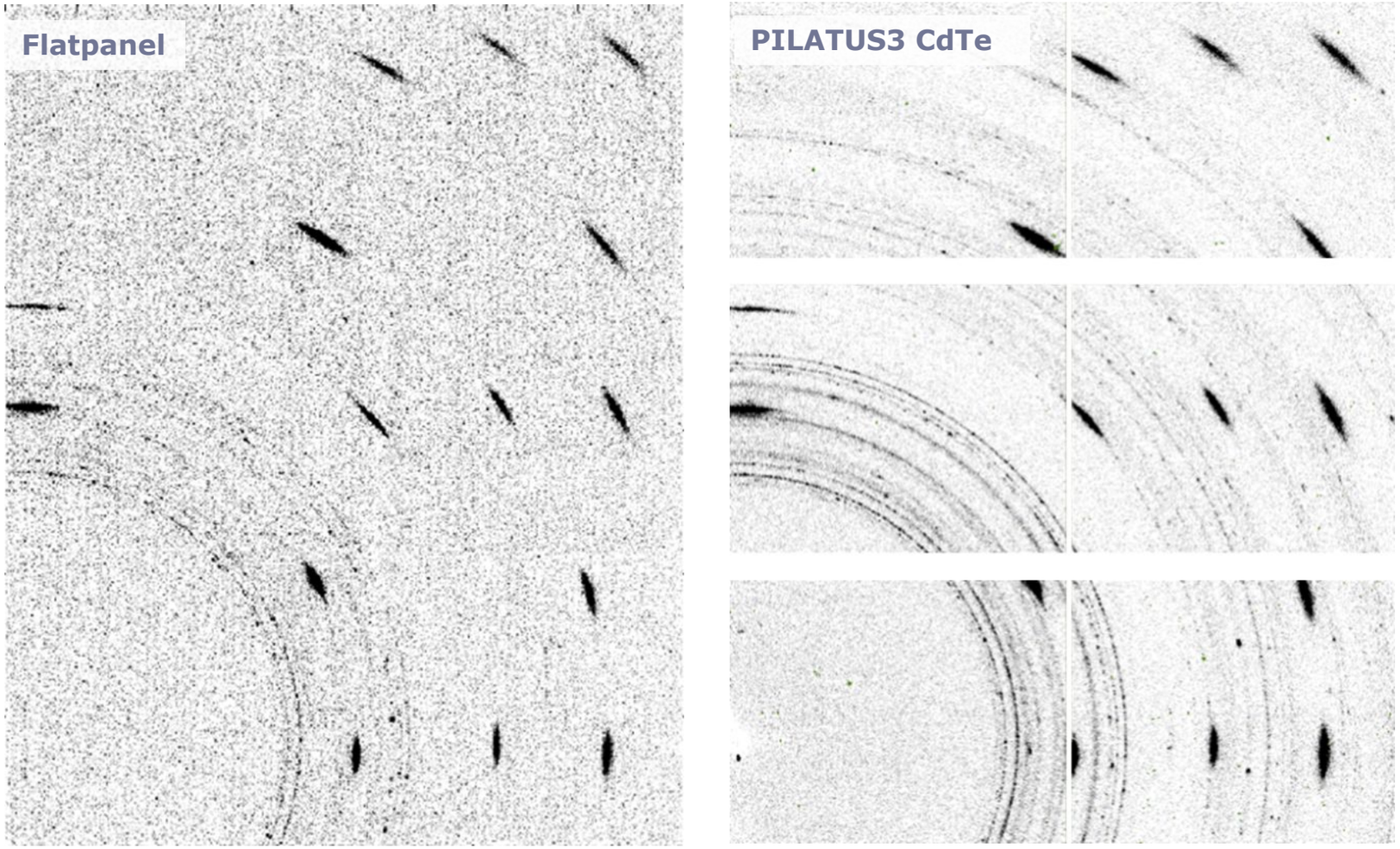




Frame Rate: >100kHz
Count Cutoff: > 80 Mel/p/s
Sensors: CZT / Si

Zambon, P., et al. "KITE: High frame rate, high count rate pixelated electron counting ASIC for 4D STEM applications featuring high-Z sensor." Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment 1048 (2023)

2012-2015: Development PILATUS3 CdTe - Reliable and Cutting Edge



Courtesy ESRF ID15: M. Di Michiel, G. Vaughan, R. Homs, T. Buslaps Univ. Manchester: S. Jacques

Sample:
Superconducting filament containing Nb3Sn powder in a tungsten tube (Ø50µm).

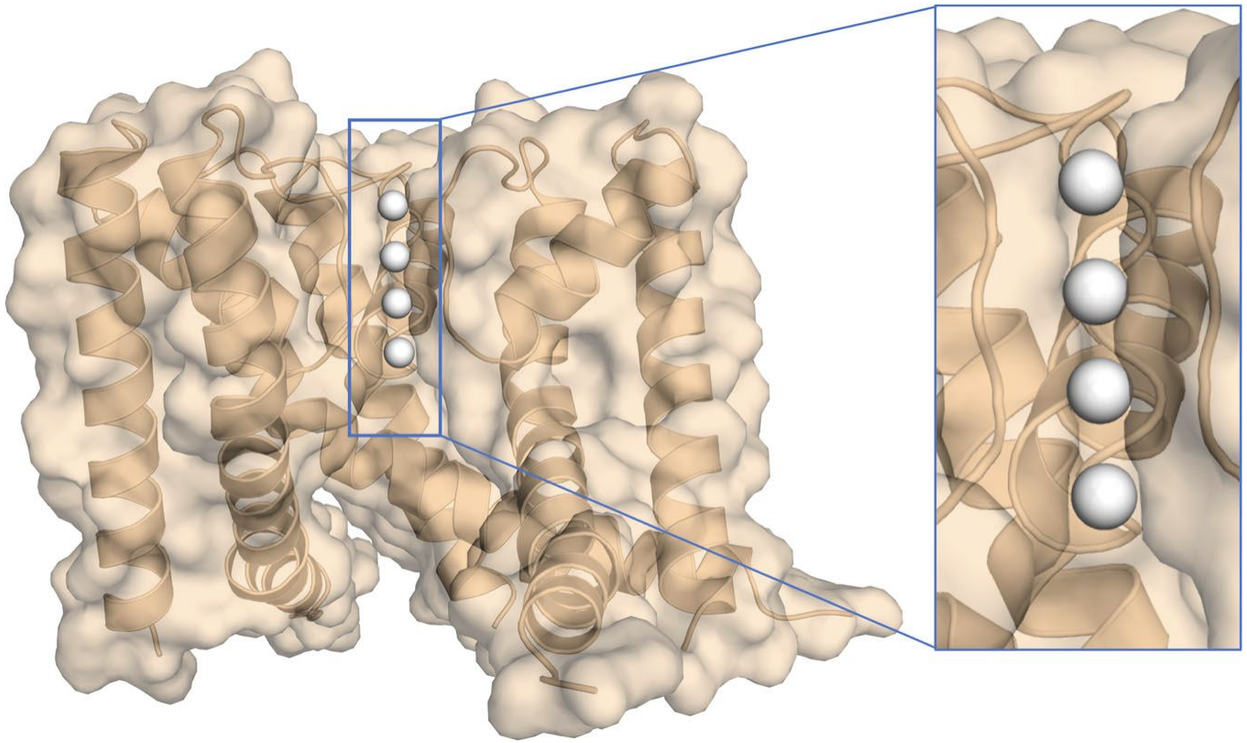
Energy: 46.3 keV

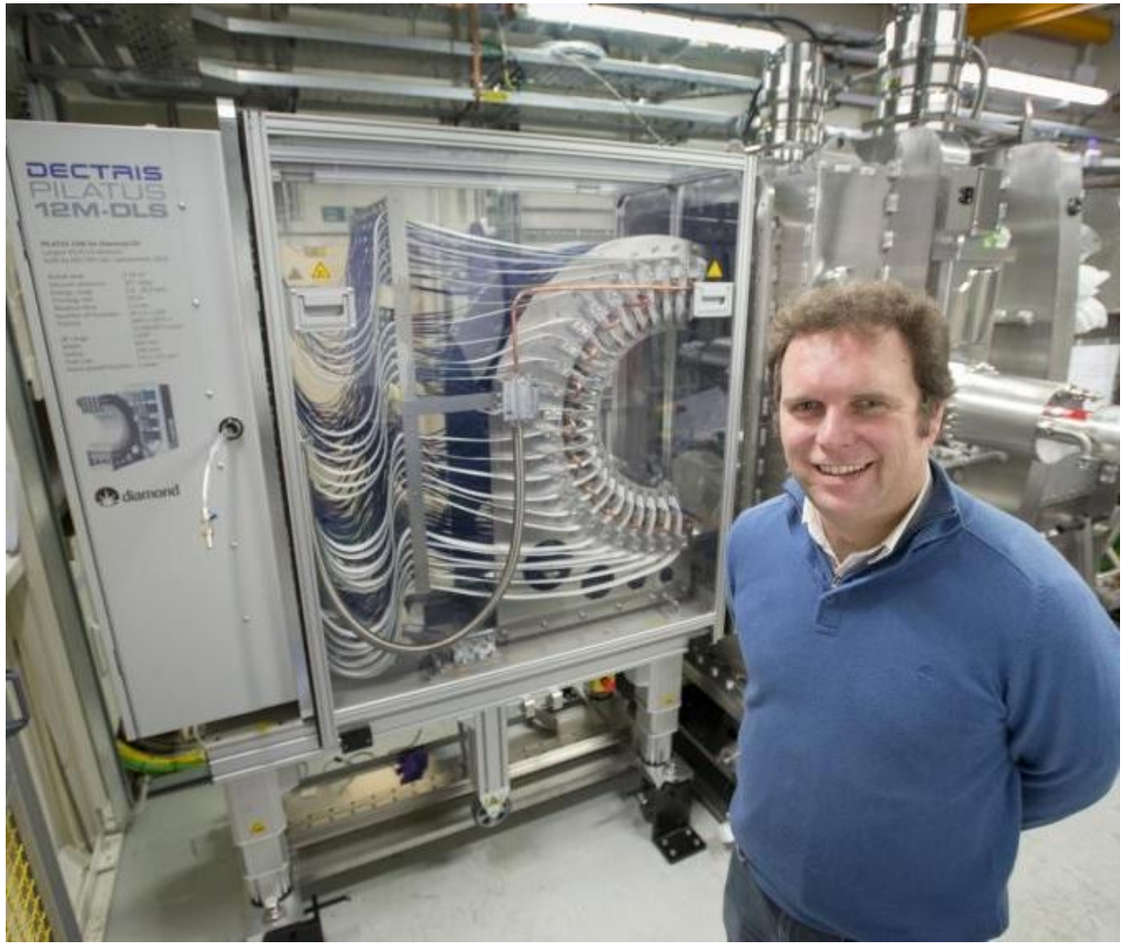
Same static powder diffraction pattern:

- same solid angle (same flux) per pixel,
- same exposure time 100 ms.

Working With Partners:
Push Limits of Detection Technology

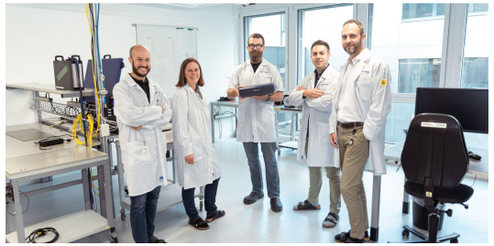
P.S. Langan *et al., NATURE COMMUNICATIONS,* (2018) 9:4540, doi: 10.1038/s41467-018-06957-w





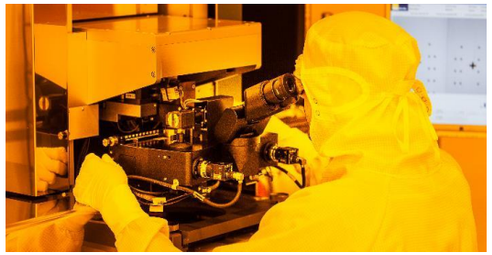
PILATUS 12M @
Diamond Light Source

DECTRIS Facilities in Baden, Switzerland



Development

- >35% of employees
- Software, Firmware, Hardware
- ASICs & Technologies
  - 6 ASIC designers and testers



1000 m² Cleanroom

- Photolithography
- Components assembly and testing

1000 m² Assembly Hall

- System Assembly
- Testing and Calibration
- Service Center

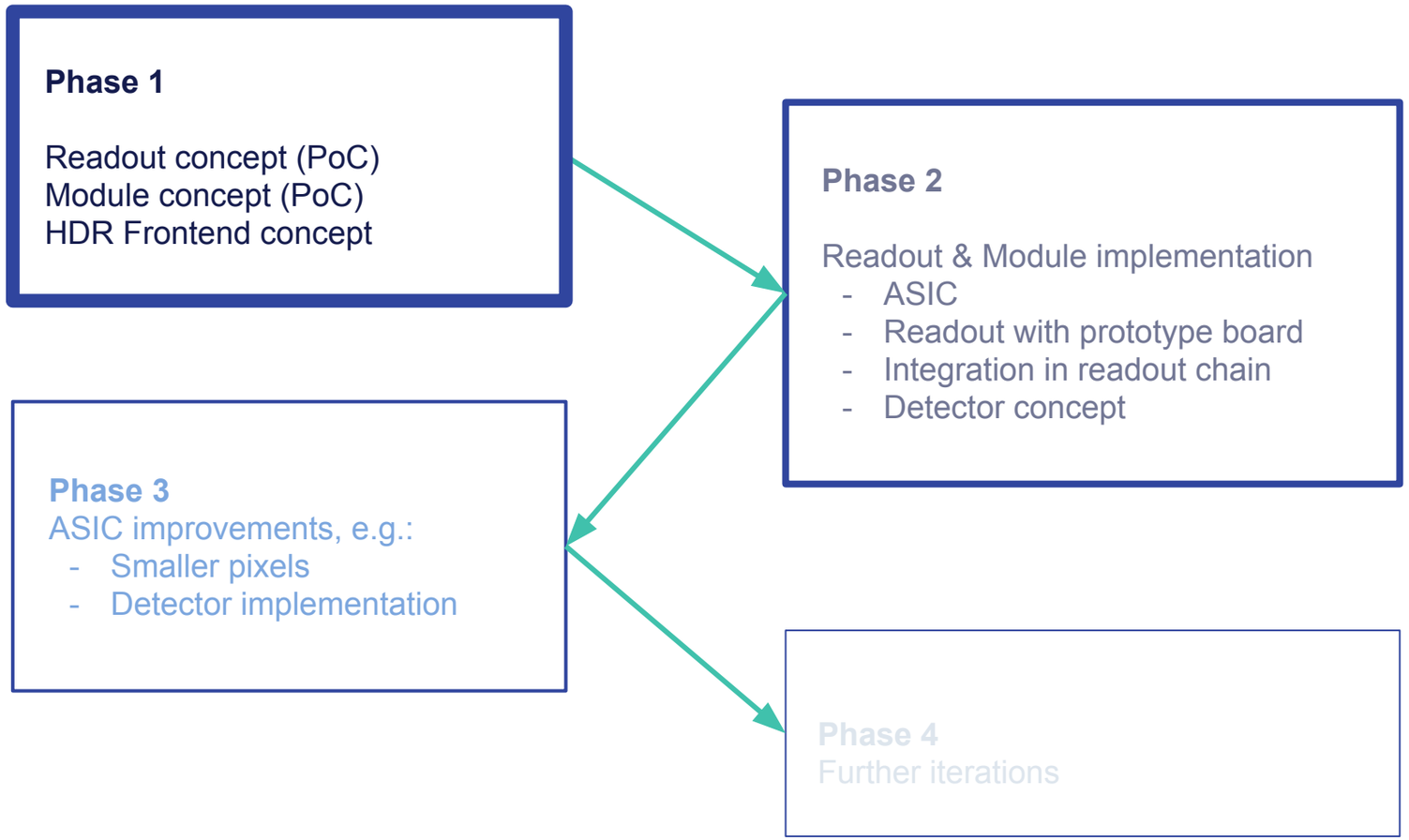
ISO9001: 2015 certified

How we may contribute to a MHz detector: Technology Mastery at DECTRIS

Technology	Tech. Mastery	Remarks
Hybrid Pixel Technology	high	
Integrating Pixel Technology	medium	R&D, derisking
High frame rate readout 2cm x 2cm 200um Pixel 8 bit bit depth (compressed) ***120 kHz*** *frame rate* parallel data bus 10Gbps	high	See: Zambon, P., et al. "KITE: High frame rate, high count rate pixelated electron counting ASIC for 4D STEM applications featuring high-Z sensor." Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment 1048 (2023)
High frame rate readout *450 kHz frame rate* parallel data bus 40Gbps	medium	prototype possible
High frame rate readout serial data bus	medium	
modular firmware, high data rate	medium	prototype

How would we approach a MHz detector module?

Risk Reduction by Phase-Wise Approach. 3+ Phases



Phase Overview

Phase 1

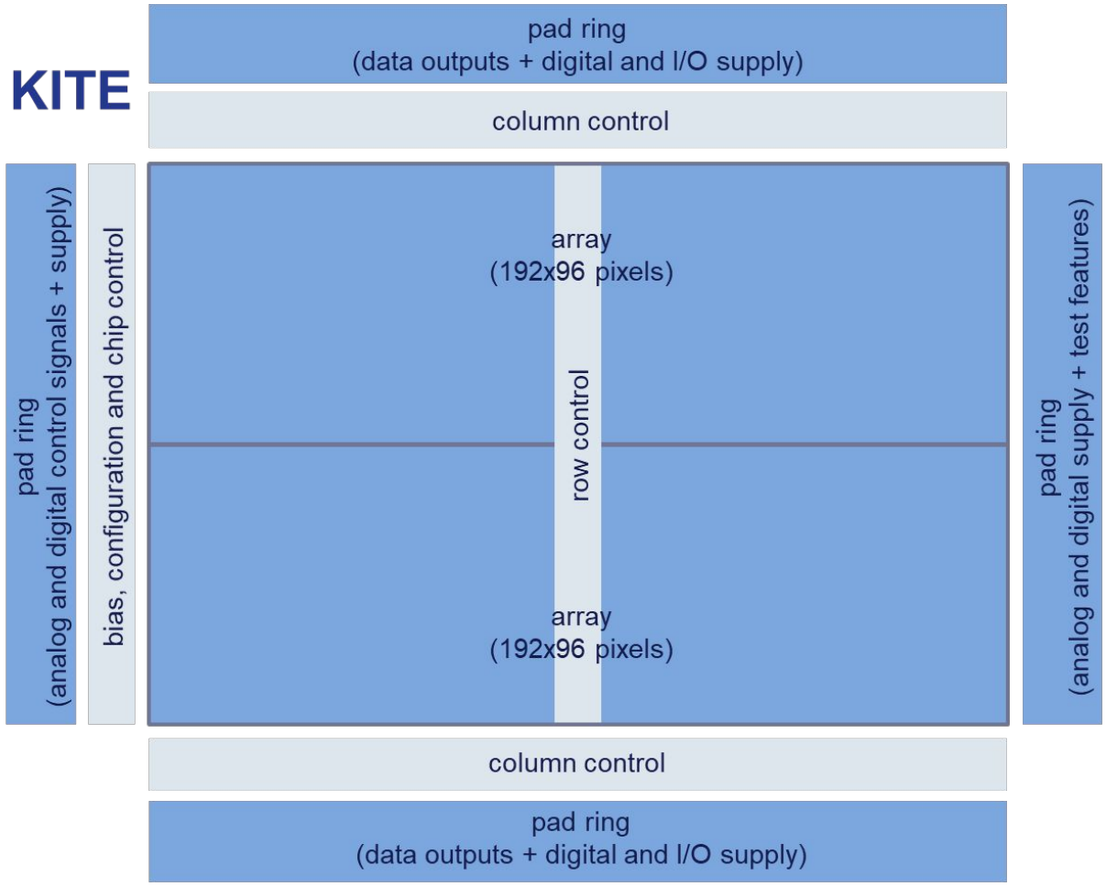
Goals

Reduce largest risks on the way to the MHz detector

Increase TRL of critical components/technologies

Work Packages

- WP1: high data rate readout concept
- WP2: HDR integrating front end evaluation
- WP3: module concept
- Optionally WP4: 450 kHz demonstrator



Phase 1 work packages

WP1: High Data Rate Readout Concept

Scope:

Data transfer from being produced in the pixel (n bits) until the data reaches the FPGA for further processing.

Tasks:

- High Speed serial links for data transfer
- 1x eng. run with 1-4 evaluation ASICs for evaluation of 3D packaging technologies
  - Counting pixel with ~ 150 µm pixel size, 1 threshold, 8bit
- Evaluation of 3D packaging technologies with suppliers, based on existing technology projects
- Development of required readout infrastructure for ASIC

Deliverable:

technology demonstrator at TRL 3

Phase 1 work packages

WP2: Frontend Evaluation

Scope:

Evaluation of integrating HDR pixels

Tasks:

- Design and Evaluation of different HDR integrating frontends with digitization
  - simulations + MPW or eng. run (TBD)
  - requirements engineering with EuXFEL
- Evaluation of technology nodes for these frontends

Deliverable:

Realistic specifications with initial proof of a suitable technology (~TRL3)

Phase 1 work packages

WP3: Module Concept

Scope:

Evaluation of data transfer from ASIC to FPGA to fibre/… on a final module

Tasks:

- HW module concept together with EuXFEL
- Mechanics
- 3D integration
- Data interface definitions

Deliverable:

Agreement of module concept (TRL3)

Phase Overview

Phase 2

Goals

Bring technologies developed in phase 1 towards a demonstrator (TRL4)

Potential Work Packages

- WP1: ASIC bringing together high speed readout, module concept and HDR pixel
- WP2: Demonstrator module based on above ASIC
- WP3: On FPGA data processing

Deliverables

A usable demonstrator (which will most likely not fulfill all desired specifications concerning pixel size, dynamic range or frame rate).

Phase Overview

Phase 3

Goals

Improve upon the demonstrator in phase 2, towards the desired specifications

Potential Work Packages

- tbd

Deliverables

tbd, e.g. demonstrator with desired specifications

Summary

MHz Detector with High Dynamic Range

In detector design, DECTRIS balances cutting edge technologies and reliability

Due to the uncertainties, risks, novel technologies and range of requirements (as usual for such a project), we propose a phase wise approach to develop the module

DECTRIS can develop, produce and service such a MHz module

Developing a MHz detector is a collaborative effort. We are open to be part of such an effort.