Eine kurze Geschichte der FPGA und SPS basierten Steuerungs- und Messsysteme der Experimente und Photonbeamlines beim European XFEL

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SEI Tagung
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Agenda

- Introduction into European XFEL
- Programmable Logic Controller (PLC) based solution for generic control and automation
- MicroTCA as standard platform for decentralized high-speed electronics
- FPGAs as central element for high-speed interfaces and real-time pre-processing

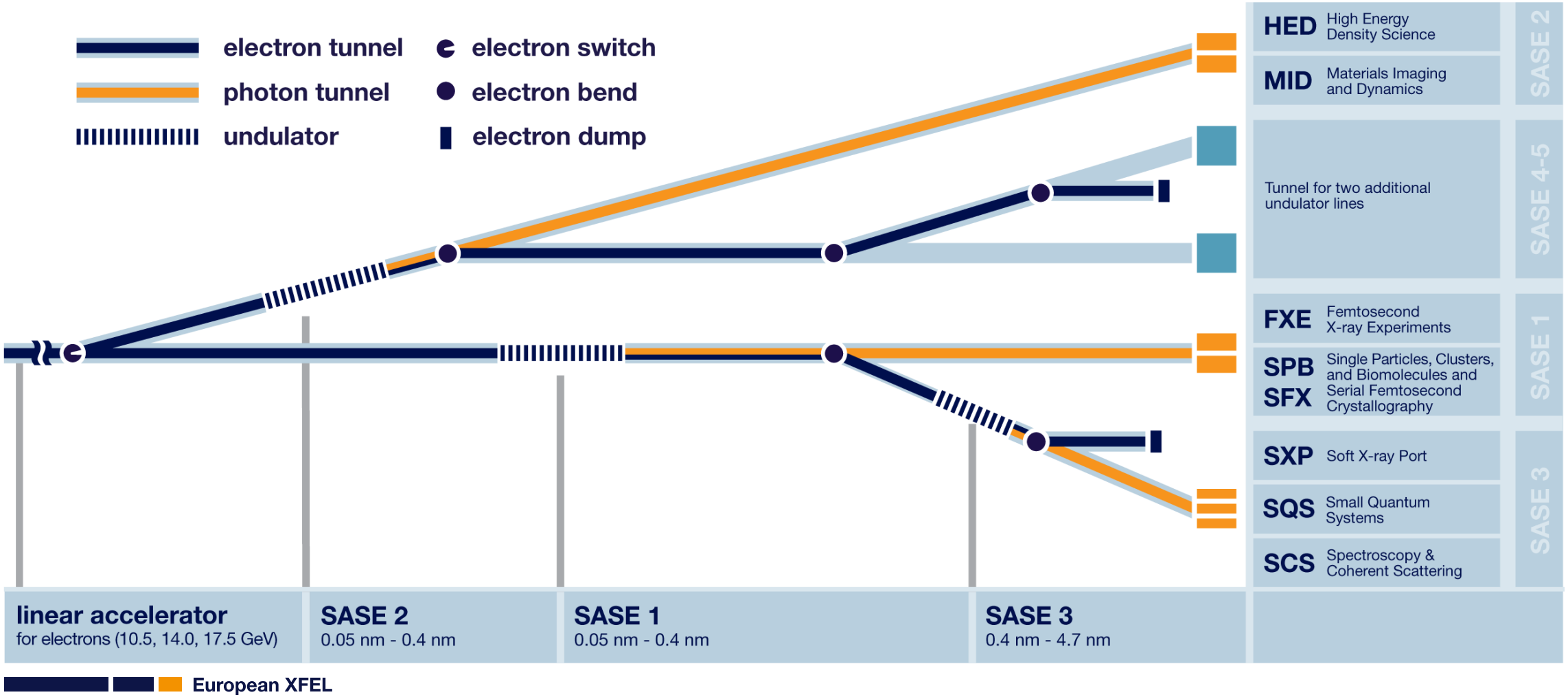
European XFEL – a research facility of superlatives

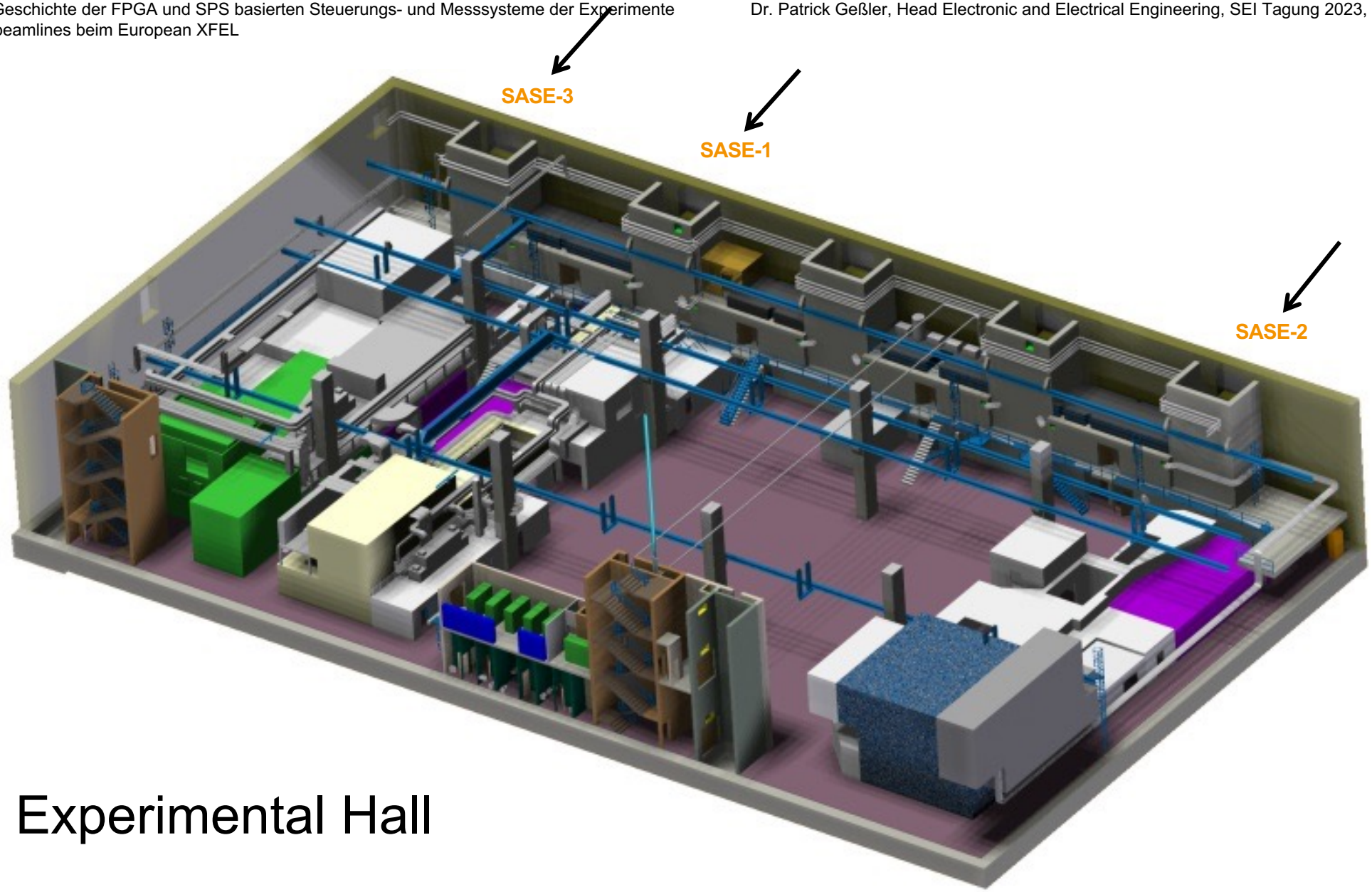
Facts and figures

- Start of construction in 2009
- Start of user operation in September 2017
- Construction costs: 1.25 billion €
- Annual budget: about 140 million €
- More than 500 employees from over 60 countries
- The world's largest and strongest X-ray laser

Aerial view of the Schenefeld research campus from 9 September 2021

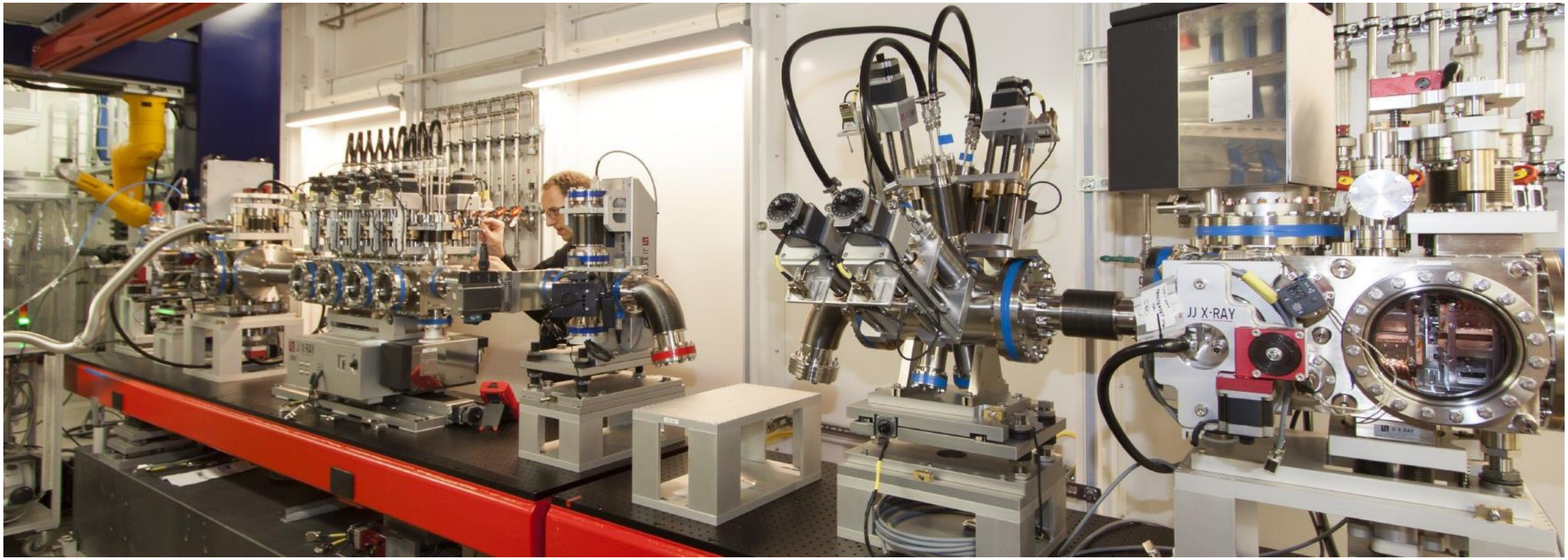
Beamline layout and experiment stations





Experimental Hall

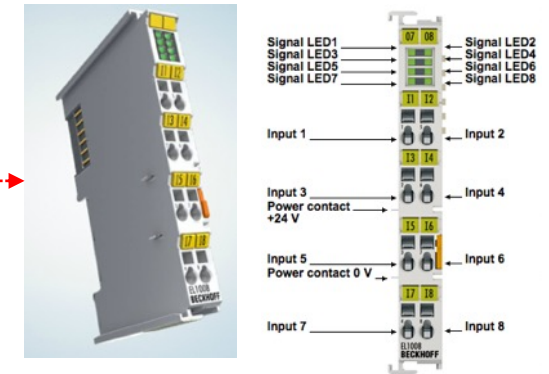
What has to be controlled: motion, vacuum, temperature, power, protection,…



PLC systems – simplified overview

- **P**rogrammable **L**ogic **C**ontroller
- Terminals as interface to h/w
- Terminals are connected together
- PLC CPU
  - Connects via cables to Terminals
  - Implements programs for control
- Computer
  - connects to PLC CPU
  - Implements Control System

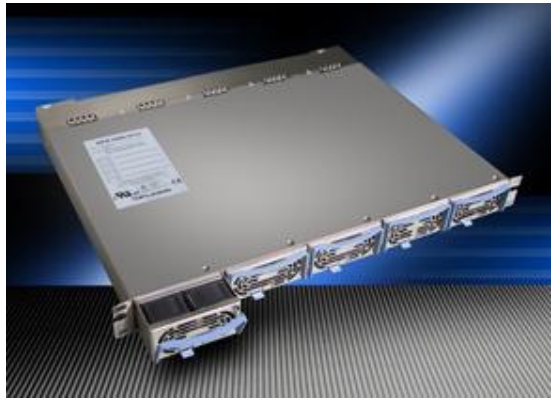
PLC Terminals (i.e. digital input)



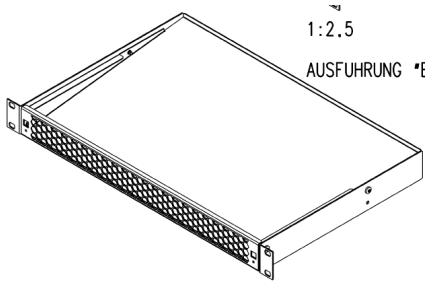
PLC Crate

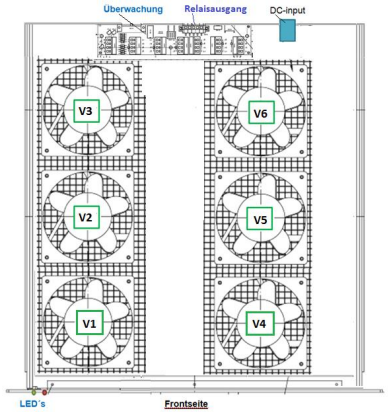
PLC systems – CPUs, Power and Cooling

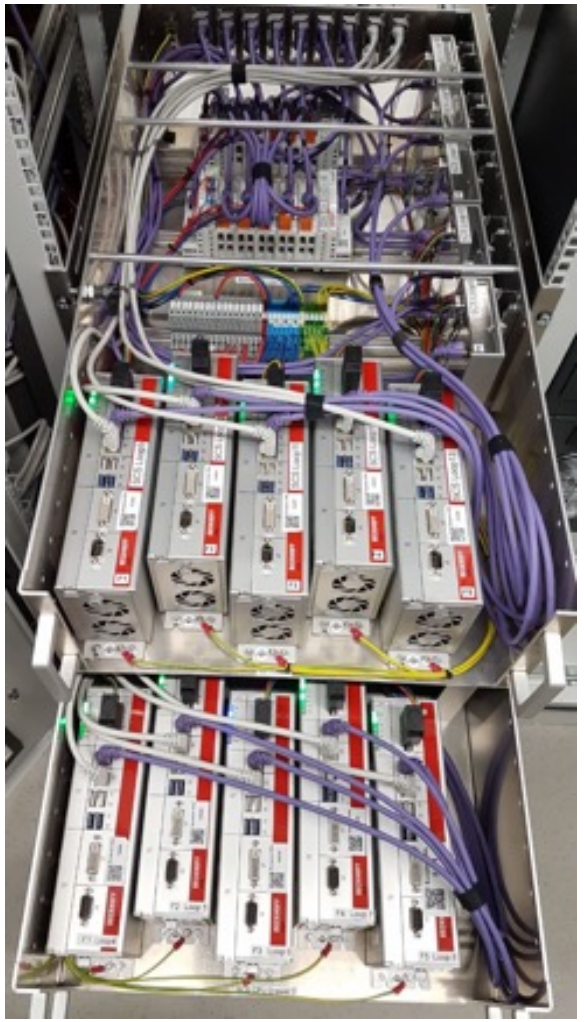
- Besides the PLC modules, the following is required
  - PLC CPUs
    - ► 24V industrial PCs
    - ► About 130 in operation
  - 24V and 48V Power supplies
    - ► redundant and hot-swappable
    - ► Can provide 1600W per slot-in module
  - FANs and air ducts



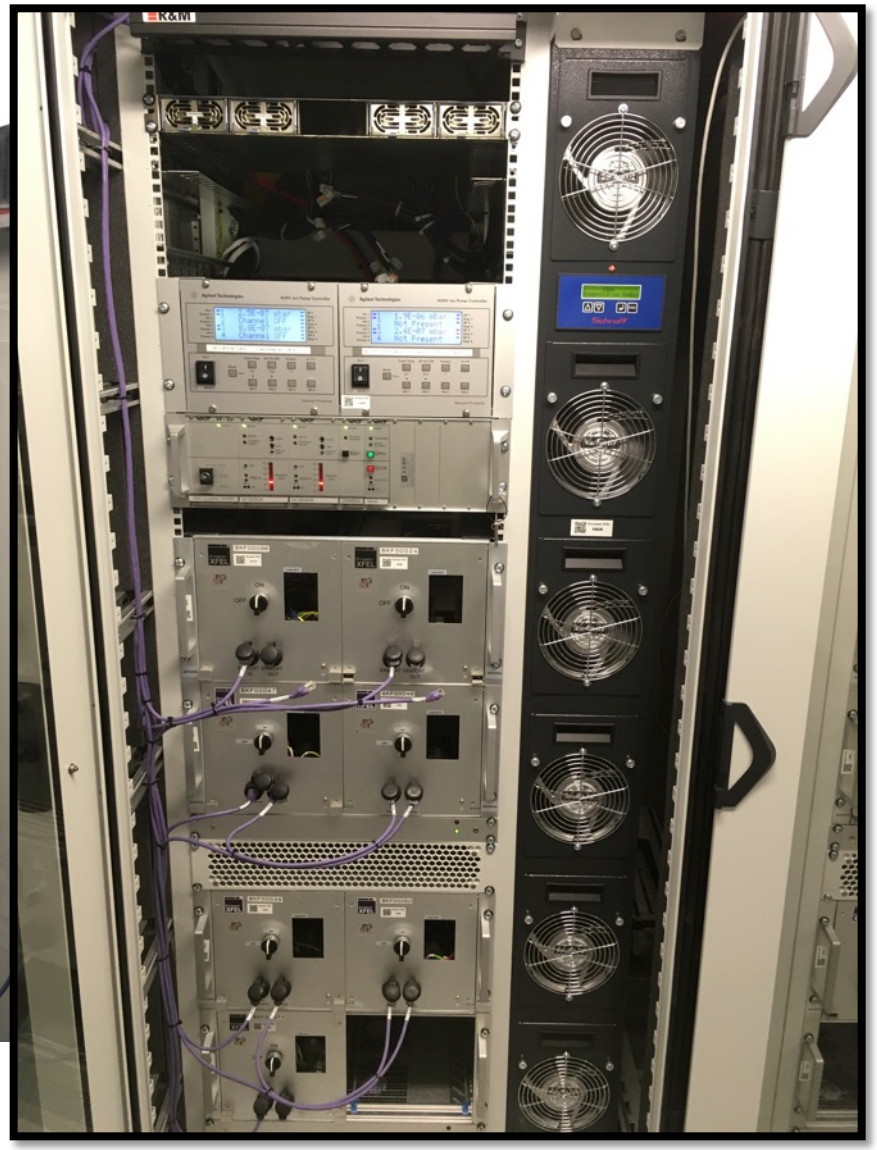
TDK Lambda HFE Supply



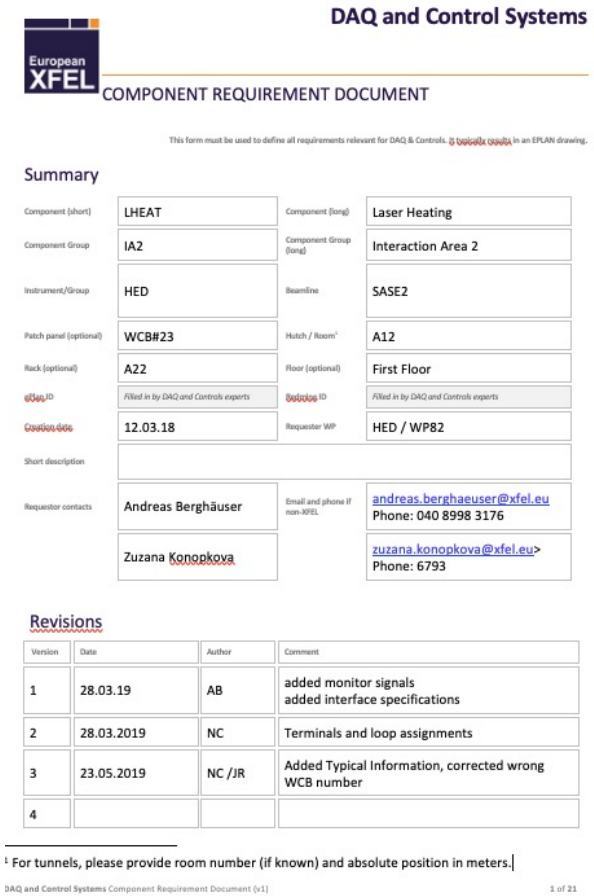




Example of installed PLC systems



Component Requirement Document (CRD) – the starting point



DAQ and Control Systems

European XFEL

COMPONENT REQUIREMENT DOCUMENT

This form must be used to define all requirements relevant for DAQ & Controls. It typically counts in an EPLAN drawing.

Summary

Component (short)	LHEAT	Component (long)	Laser Heating
Component Group	IA2	Component Group (long)	Interaction Area 2
Instrument/Group	HED	Beamline	SASE2
Patch panel (optional)	WCB#23	Hutch / Room[1]	A12
Rack (optional)	A22	Floor (optional)	First Floor
eSAP ID	Filled in by DAQ and Controls experts	Baseline ID	Filled in by DAQ and Controls experts
Creation date	12.03.18	Requester WP	HED / WP82
Short description			
Requestor contacts	Andreas Berghäuser	Email and phone if non-XFEL	andreas.berghaeuser@xfel.eu Phone: 040 8998 3176
	Zuzana Konopkova		zuzana.konopkova@xfel.eu> Phone: 6793

Revisions

Version	Date	Author	Comment
1	28.03.19	AB	added monitor signals added interface specifications
2	28.03.2019	NC	Terminals and loop assignments
3	23.05.2019	NC /JR	Added Typical Information, corrected wrong WCB number
4			

[1] For tunnels, please provide room number (if known) and absolute position in meters.

DAQ and Control Systems Component Requirement Document (v1) 1 of 21

Equipment overview

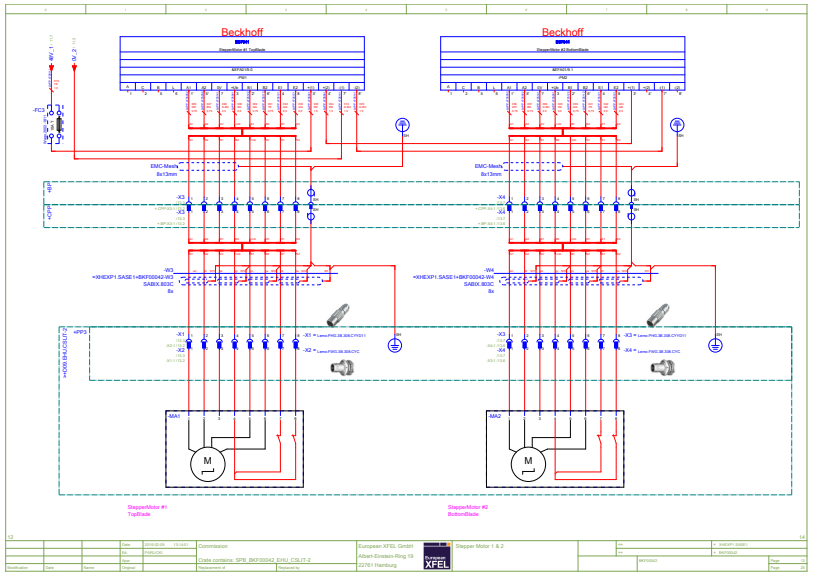
Mention the type and the number of the equipment you need.
All available equipment types can be found in this list.

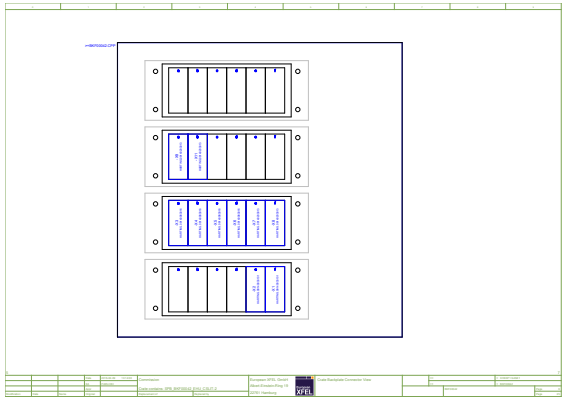
Equipment Type	Quantity	# IP-Addresses needed
Stepper Motor	2	no
Cameras	3	yes
Pneumatic Drive	9	no
Analog Output	4	no
Digital Output	25	no
Digital Input	16	no

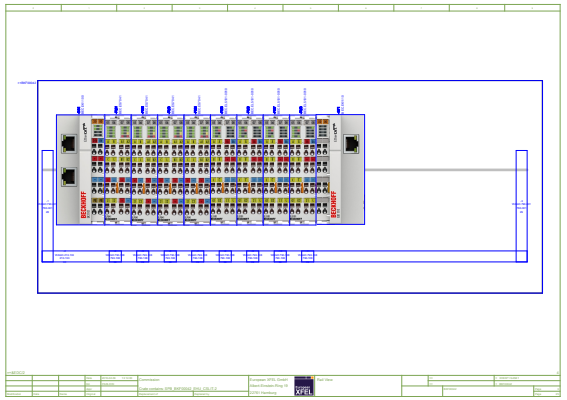
#	Equipment Type	Name	Manufacturer	Model	Data Sheet	Connector Type, Pin Assignment	Comment	Standard	Control Interface Hardware	Driver class (f/w, s/w)
1	Stepper Motor	ROTATOR_1	Newport	NSR-1	Appendix 1	Via WCB 24 WT-215 C_260	Filter rotator	YES	ES7031	SD_MC2MOTOR
2	Stepper Motor	ROTATOR_2	Newport	NSR-1	Appendix 1	Via WCB 24 WT-215 C_260	Filter rotator	YES	ES7031	SD_MC2MOTOR
2	Camera	BASLER_1	Basler	ACA1600-20gm	basler-1600-datasheet	Data: GigE PoE via switch in A22 Trigger: XFEL trigger	Integration in Karabo For EET: no ES2634 terminal is needed			

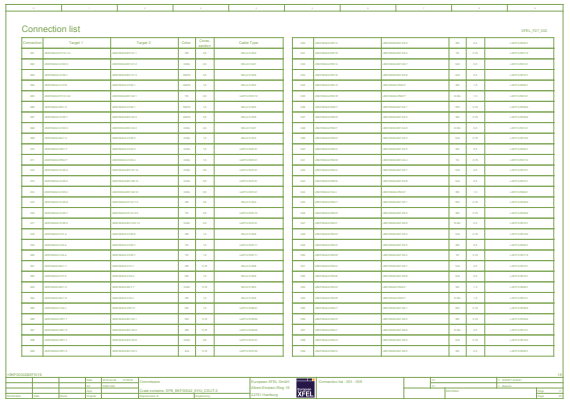
→ On-going R&D project to move to web interface + data base + API

Electrical CAD design (EPLAN P8)



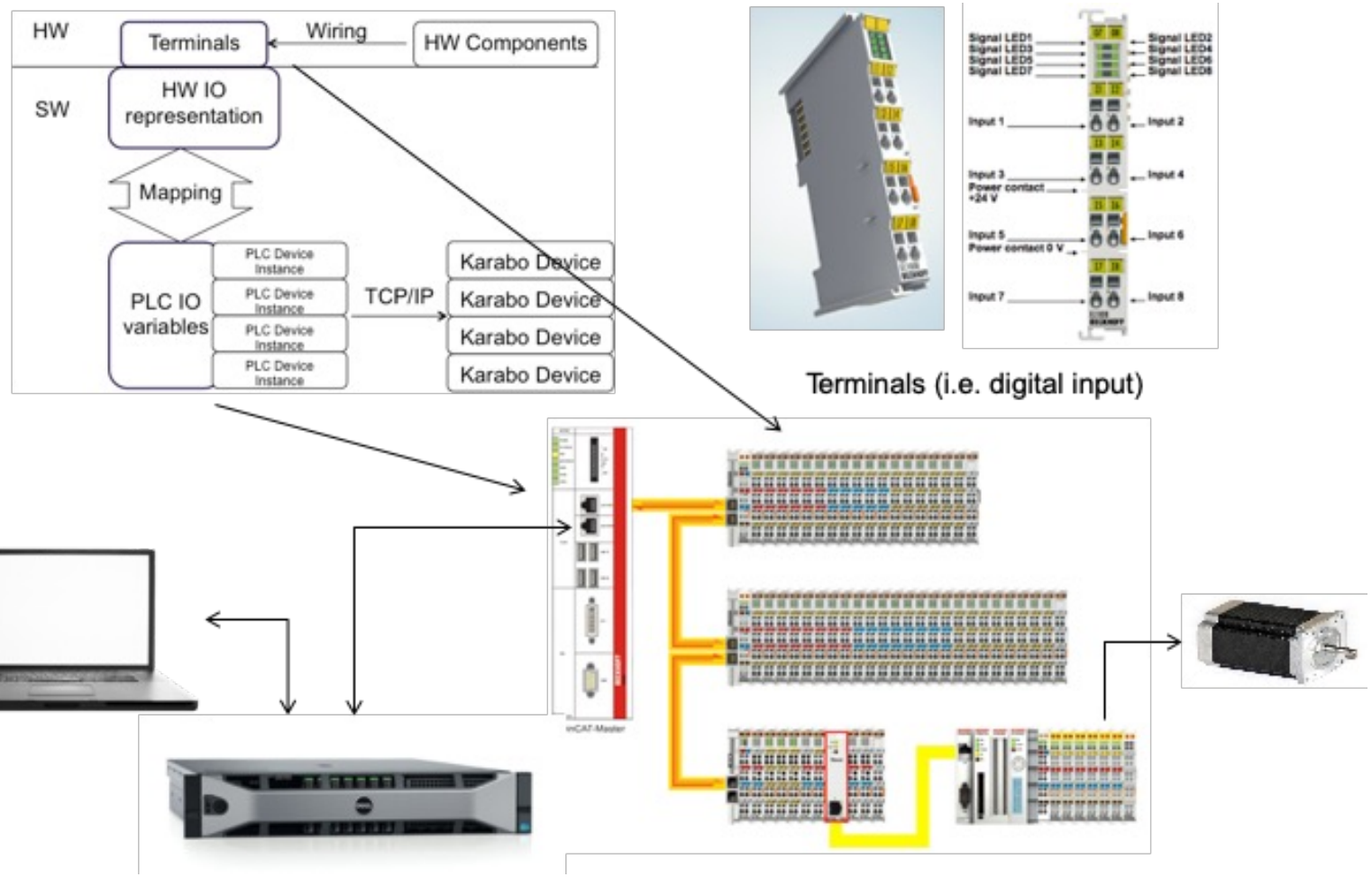






PLC Framework Library

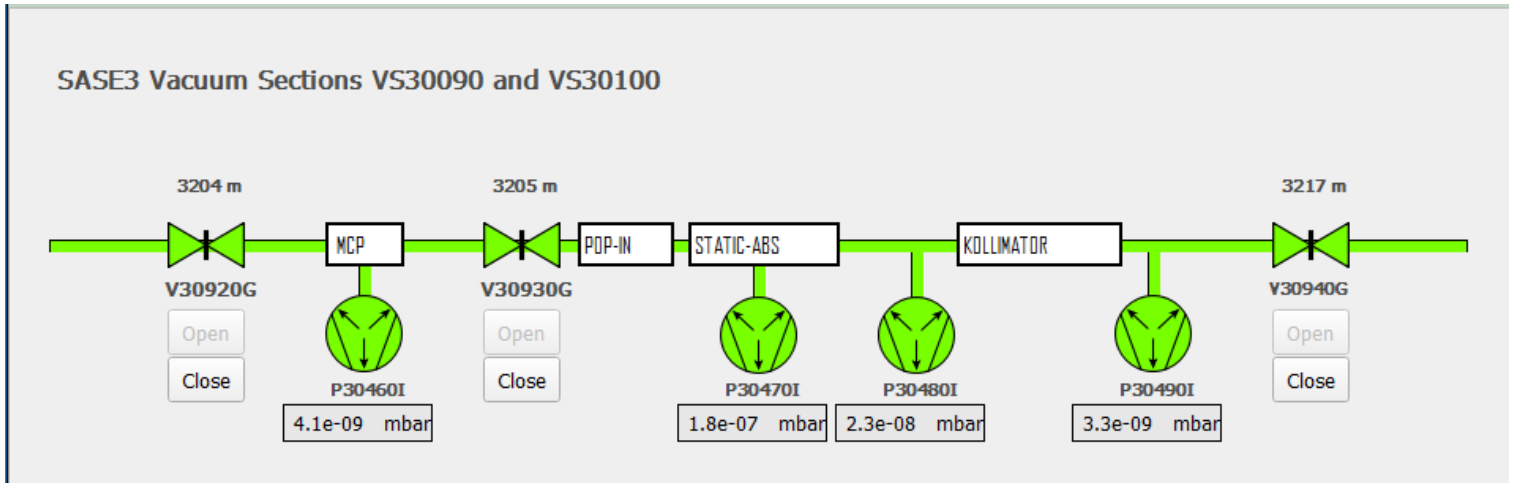
- Abstraction of h/w into softdevice
  - One equipment could be more than one softdevice
- The PLC framework includes
  - All definitions of softdevices
  - Inter-device communication concepts
  - TCP communication to control system (Karabo)
  - General monitoring
- Organized as versioned library



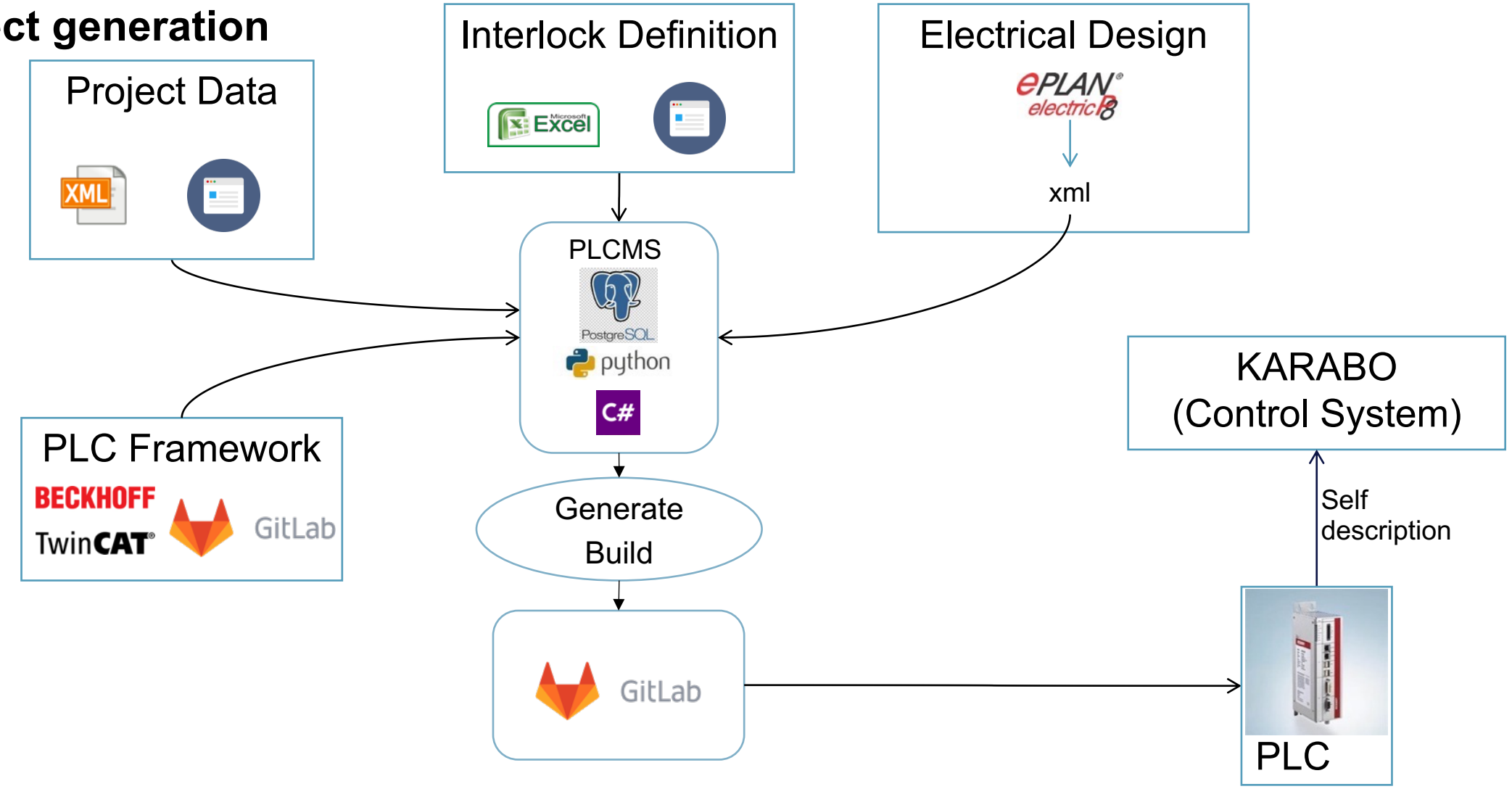
→ On-going re-development of PLC Library

Generic interlock example: Vacuum interlock

2	Device Name	SA3_XTD10_VAC/VALVE/V30930G						
3								
4	**Conditions**	**Signal Source (Device.Parameter)**	**Operator (optional)**	**Signal Source (Device.Parameter)(optional)**	**Operator**	**Limit**	**Hysteresis (optional)**	**Filter time(ms)(optional)**
5	c1	SA3_XTD10_VAC/DCTRL/VS30080.state.value			EQOp	FALSE		
6	c2	SA3_XTD10_VAC/DCTRL/VS30090.state.value			EQOp	FALSE		
7	c3	SA3_XTD10_VAC/DCTRL/VS30100.state.value			EQOp	FALSE		
8	c4	SA3_XTD10_VAC/DCTRL/VS30110.state.value			EQOp	FALSE		
37								
38								
39	**Actions**	**Logic**	**Action**	**Value**	**Latch**	**Lock**	**Toggle**	**Comment**
40	a1	c1 or c2 or c3 or c4	CClose		no	no		
41	a2							
42	a3							

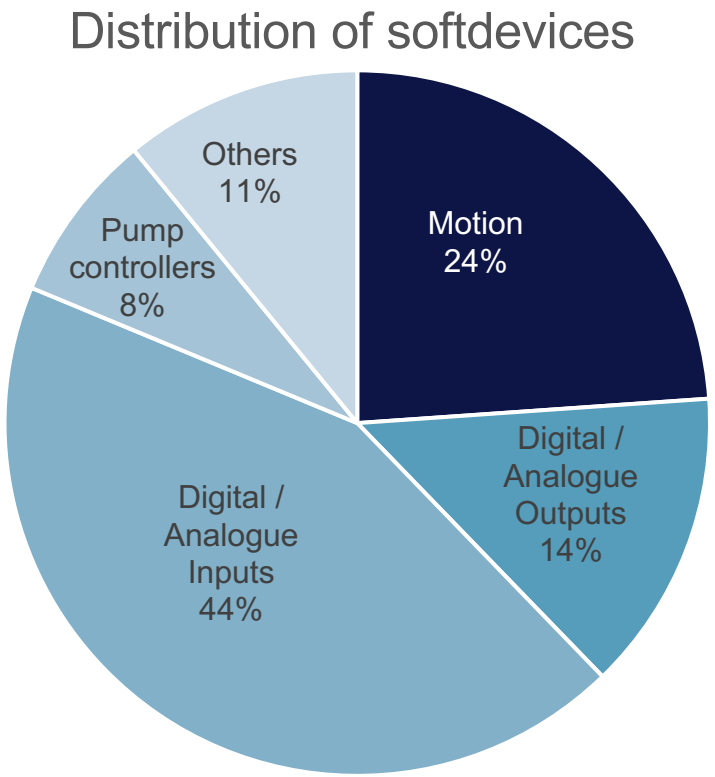


PLC Project generation



Status (12/2020): Integration in Numbers

- Softdevices/Equipment: 10.778
- Number of Terminals: 9.528
- PLC Loops / CPUs: 120
- PLC Modules / crates: >587
- Installed cables: 169km
- MicroTCA Systems: 44
- Digitizer channels: >280



General MicroTCA Infrastructure

MicroTCA Crates

Large 12 slot 9U and small 6 slot 2U (including MCH, Power Supply and CPU)

X2Timer

XFEL Timing System module for synchronization (clocks and triggers) and pulse parameters from NAT

DAMC2

Required for Clock & Control system for fast 2D detectors, VETO System, Machine Protection System and photon beam loss monitors from DESY

SIS8300

Fast 125MSPS ADC with 10 channels and 16bit resolution for diagnostics and detectors from Struck Innovative Systeme

ADQ412/ADQ14/ADQ7

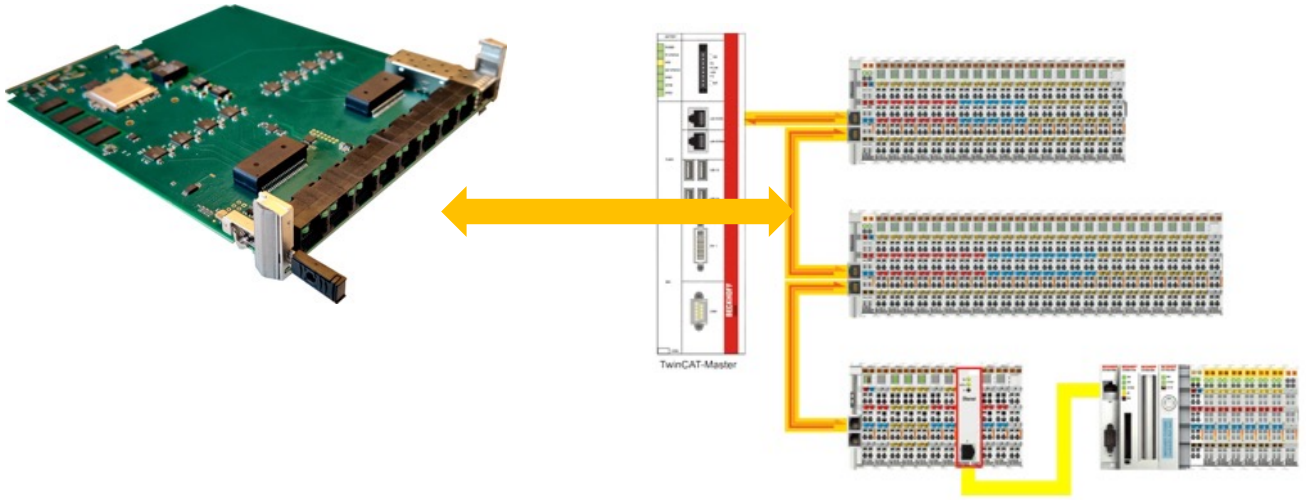
High-speed digitizers from 1.8GSPS to 10GSPS with 12 to 14 bit resolution from Teledyne SP Devices

On-going Integration Projects

- **SIS8300 KU Integration**
  - Update of current hardware platform
  - Uses Kintex UltraScale+ FPGA

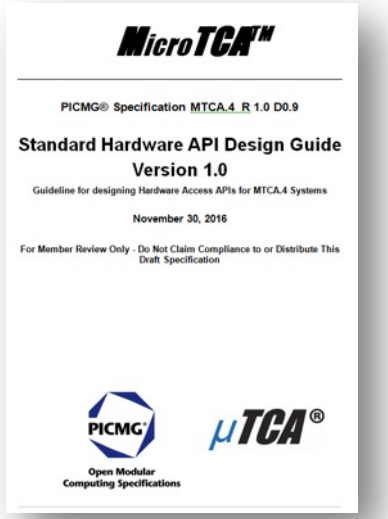
- **Alveo Cards (not MicroTCA)**
  - Evaluating the platform for Machine Learning applications

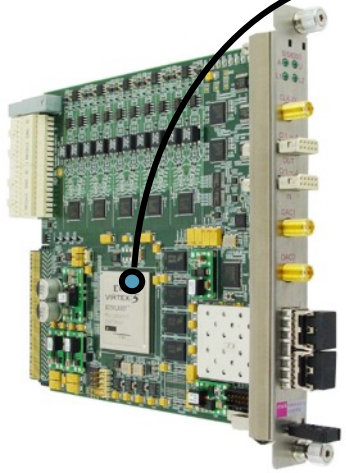
- **EtherCat AMC** solution for communication with the PLC hardware
  - Uses Zynq UltraScale+ FPGA
  - Collaboration between XFEL and N.A.T.
  - Direct communication of Information (TrainID, Beam Modes…)
  - Phase synchronization of PLCs with Machine

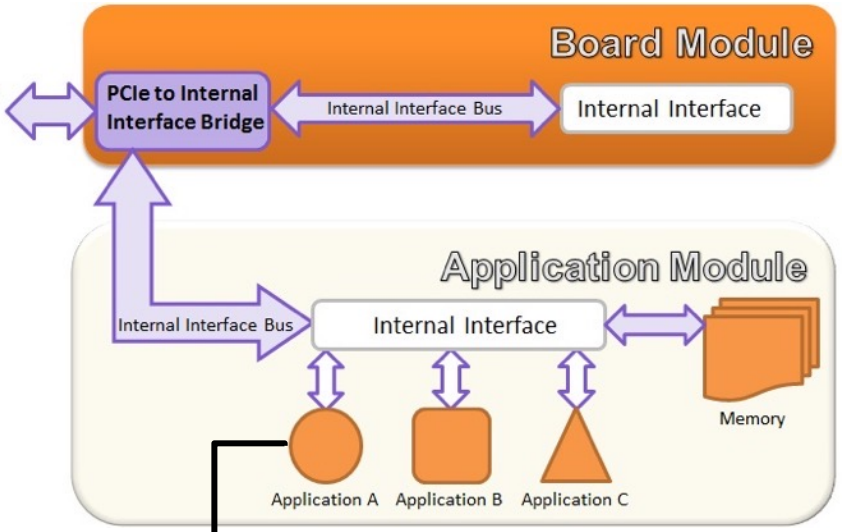


Standard interface in FPGA Development

- Board and Application Module approach
- **Internal Interface (II)** module for Register Definition
  - Information regarding CPU interface is defined directly in VHDL







VHDL Register Definition

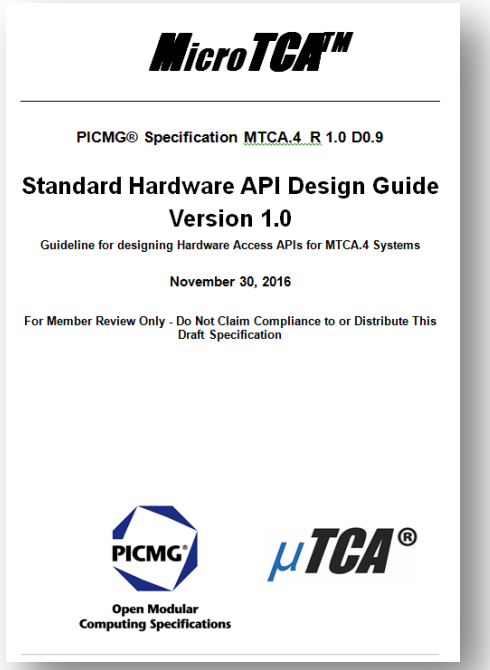
Application A:
…
"Constant Input": Register, Read Only, 14 bits, Floating-Point, 5 bit Fractional, "It's just an Example";
…

MAP/XML Description

SHAPI Design Guide

SHAPI Design Guide version 1.0 accepted and published on PICMG site

- Includes Verilog SHAPI Reference implementation (Github repository)


MicroTCA™

PICMG® Specification MTCA.4_R 1.0 D0.9

Standard Hardware API Design Guide
Version 1.0

Guideline for designing Hardware Access APIs for MTCA.4 Systems

November 30, 2016

For Member Review Only - Do Not Claim Compliance to or Distribute This Draft Specification

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MicroTCA® Overview

µTCA®

MicroTCA® is a modular, open standard for building high performance switched fabric computer systems in a small form factor. At its core are standard Advanced Mezzanine Cards (AMC's – described here: AdvancedMC) which provide processing and I/O functions. Hundreds of different AMC's are commercially available. MicroTCA systems are both physically smaller and less expensive than AdvancedTCA systems, although their internal architectures are largely the same. MicroTCA was originally intended for smaller telecom systems at the edge of the network but has moved into many non-telecom applications, with standardized, ruggedized versions becoming popular in mobile, military, telemetry, data acquisition, and avionics applications. These versions are described below.

The core specification, MTCA.0, defines the basic system, including backplane, card cage, cooling, power, and management. A variety of different sized AMC modules are supported, allowing the system designer to use as much or as little computing and I/O as necessary. Subsidiary specifications (MTCA.1, MTCA.2, MTCA.3 and MTCA.4) define more ruggedized versions specifically suited for mil/aero and other demanding physical environments. These designs have been verified through thorough rigorous environmental testing and the test reports are available.

Because of its modularity and flexibility, the MicroTCA standards are well-suited for a wide range of applications, including industrial control and automation, test & measurement, mobile and fixed mil/aero, avionics, traffic control and transportation, and telecom.

SHORT FORM SPECIFICATION ›

Key Benefits and Features

- Provides computer architecture consistent with Modular Open Systems Approach (MOSA) principles for reduced life cycle costs
- Defines fully redundant and non-redundant system configurations including power budgeting and hot-swap
- Defines complete component and system management that allow failure detection and isolation (enhanced hardware platform management).

Family of Specifications

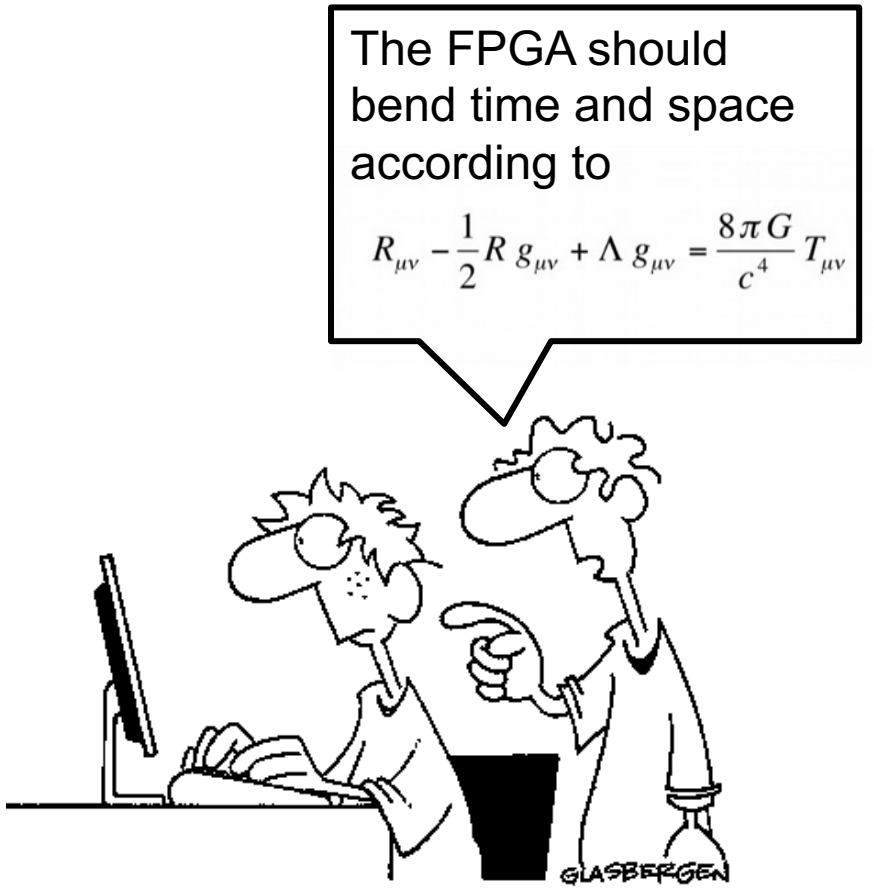
- ▸ MicroTCA Enhancements for Rear I/O and Precision Timing (MTCA.4)
- ▸ Hardened Conduction Cooled MicroTCA (MTCA.3)
- ▸ Hardened Air Cooled MicroTCA (MTCA.2)
- ▸ Air Cooled Rugged MicroTCA (MTCA.1)
- ▸ MicroTCA (MTCA.0)
- ▸ MicroTCA Standard Process Model Design Guide
- ▸ MicroTCA Standard Device Model Design Guide
- ▸ MicroTCA PCI Express Hot Plug Design Guide
- ▾ MicroTCA Standard Hardware API Design Guide

PICMG#	NAME	CURRENT REVISION	DATE	DESCRIPTION
MTCA_DG.1	MicroTCA Standard Hardware API Design Guide	1.0	January 9, 2017	This guideline defines the function and usage for a Standard Hardware API especially for, but not limited to, use in MTCA.4 applications.

High Level FPGA Algorithm Development

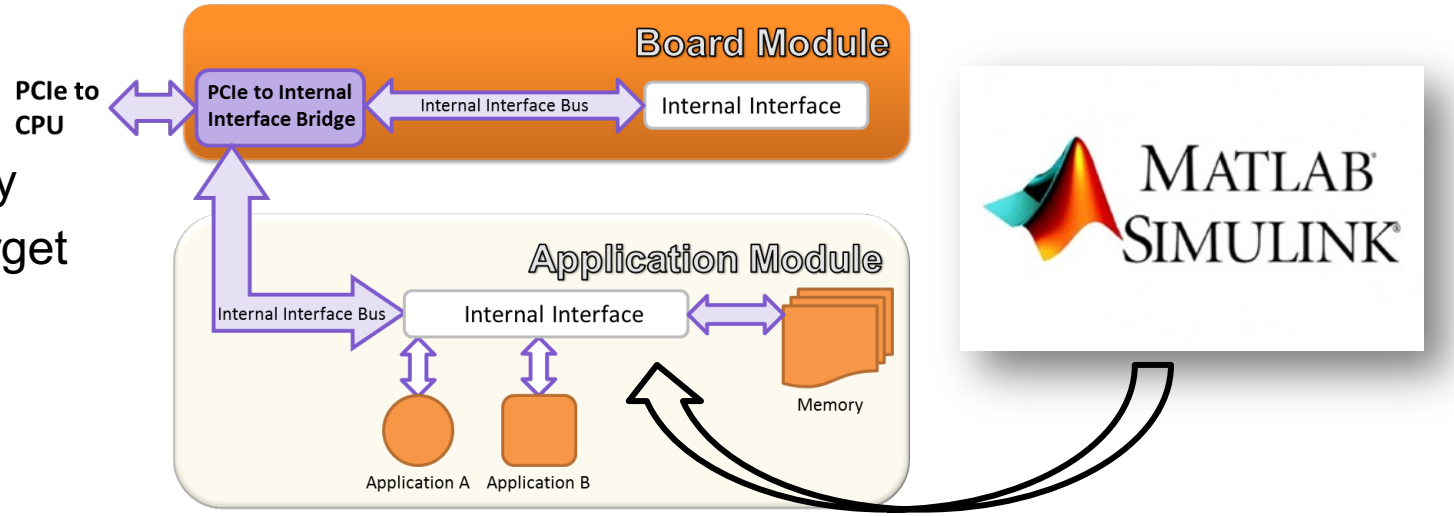
- FPGA programming is time intensive and requires specialists, however most applications and algorithms are conceptualized by users unfamiliar with FPGA programming.

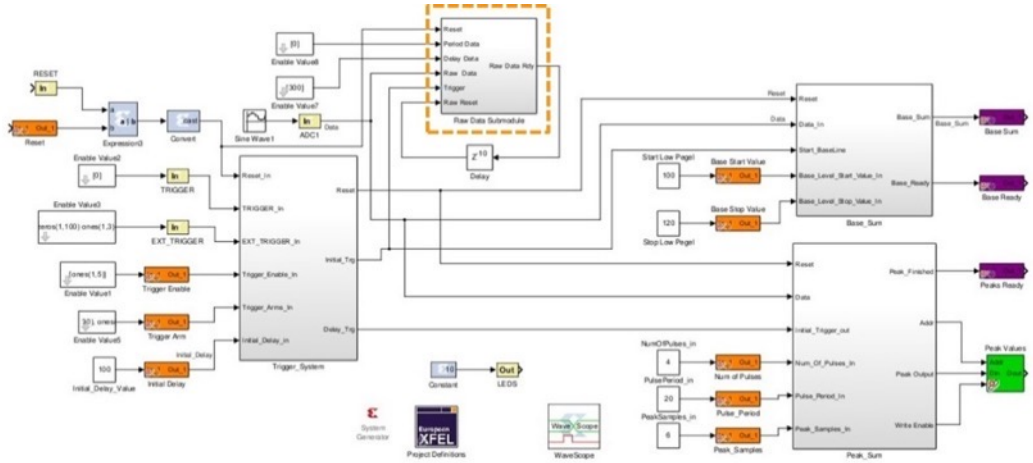
- For the European XFEL, a high level FPGA framework was developed that allows for users with no prior HDL knowledge to develop their algorithm modules which can be integrated in a top VHDL project.



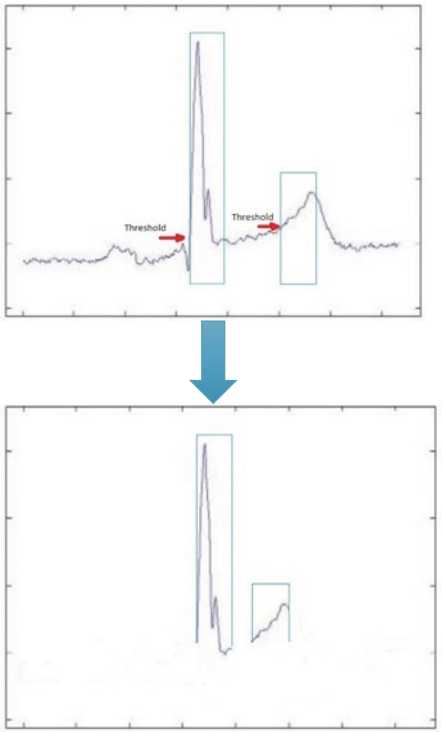
XFEL Simulink Environment

- Simulink environment which automatically setups the design environment for the target board and available features
- Library that allows definition of **registers and memories** to communicate via the chosen protocol
- Easy to **port and distribute applications** to other projects/boards
- Integration of **Matlab** allows for powerful test environments

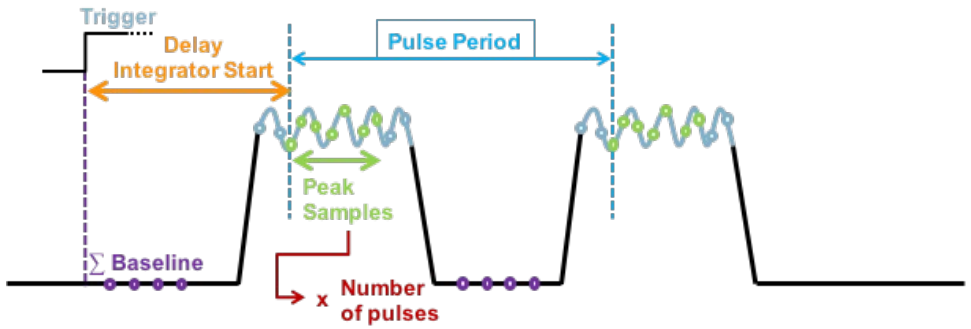




FPGA processing algorithms and interfacing standards – Signal processing

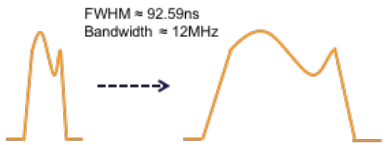


Zero Suppression

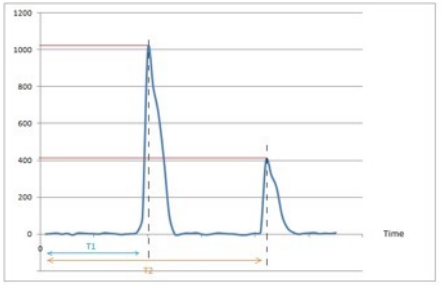


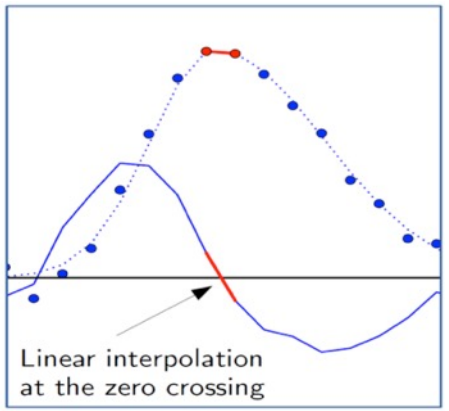
Pulse Stretcher RTM

- 10 SMA Connectors
  - 2 Direct channels
  - 8 Stretched channels
- Configurable DC Output
  - Open/+1.2V/-1.2V



Pulse Integration





Peak Time Detection

Thank You for Your Attention