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SI LAB
Silizium Labor Bonn

Large-area passive CMOS sensors for radiation tolerant hybrid pixel detectors

CMOS Verbundmeeting 2023, Heidelberg

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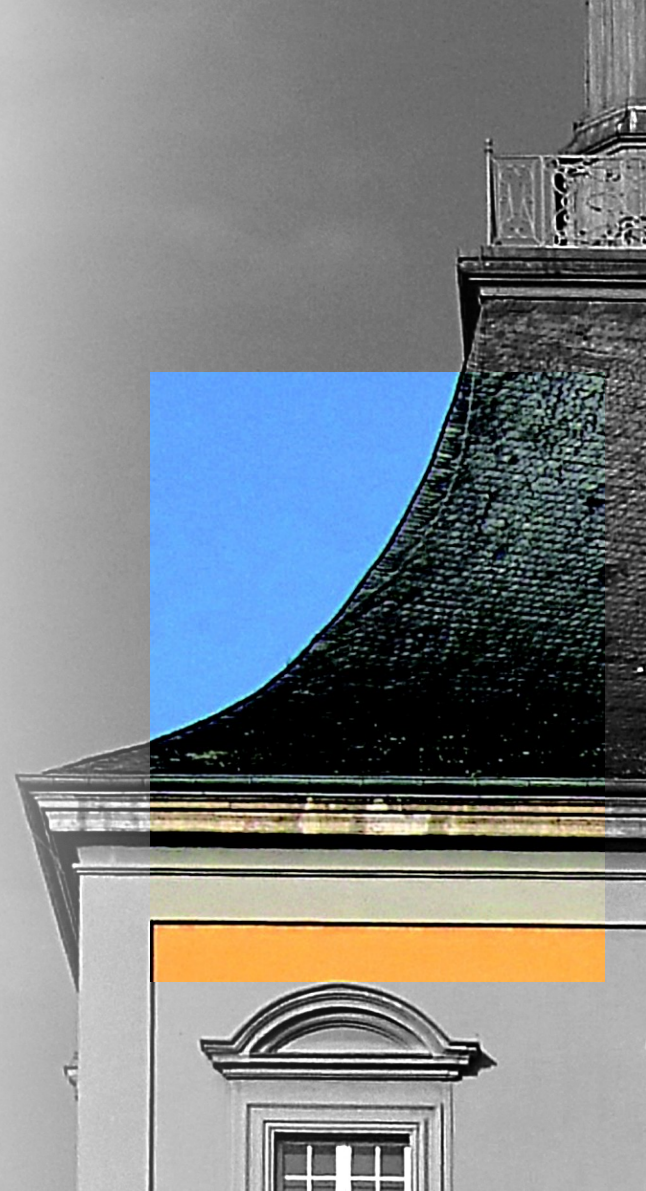
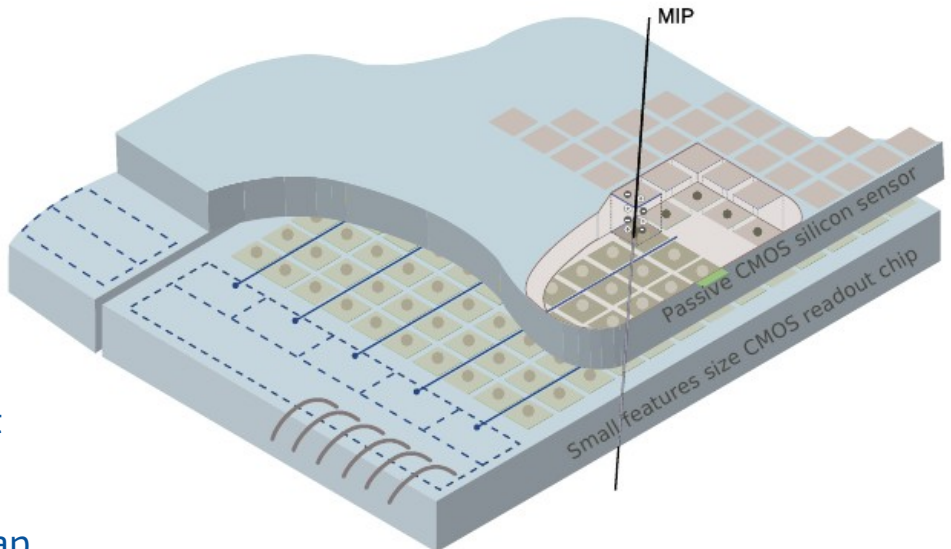
Physikalisches Institut der Universität Bonn



WHY CMOS PROCESS?

- **Hybrid pixel detectors**: Sensor + R/O chip
- Use commercial high-resistive CMOS processes for planar sensor production:
  - Large wafers (200 mm)
  - High production through-put, low costs
  - Poly-silicon resistors → connection to bias grid
  - MIM-capacitors for AC coupling → no leakage current compensation circuit needed
  - Metal layers for redistribution → no enlarged inter-gap pixels
- No active components → **passive CMOS sensors**

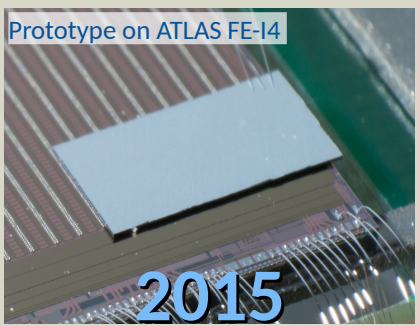


[Pohl, David-Leon: 3D-Silicon and Passive CMOS Sensors for Pixel Detectors in High Radiation Environments]

PASSIVE CMOS SENSORS USING LFOUNDRY PROCESS

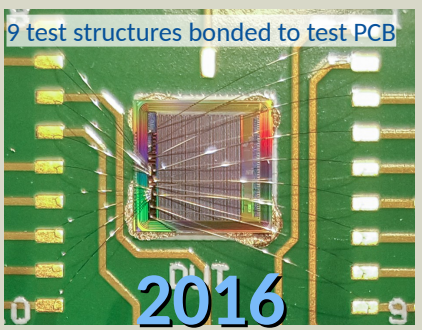
Large pixel prototype

- 50 x 250 um² pixels, ATLAS IBL planar geometry
- Performance comparable to ATLAS IBL sensors after irradiation > 1 x 10^{15} neq/cm²
- Investigation of AC-coupling schema, pixel biasing schemes (bias dot vs. resistor biasing)



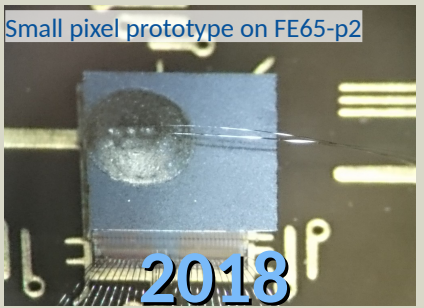
Test structures

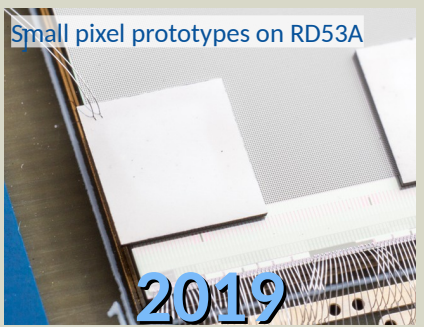
- Many structures produced (> 15)
- Varying designs: guard rings, pixel isolation, implantation geometries
- Investigations of break down with TID (2 master theses)
  - → Identified enhanced guard ring structure
- Investigation of sensor capacitances (2 bachelor theses)



Small pixel prototype

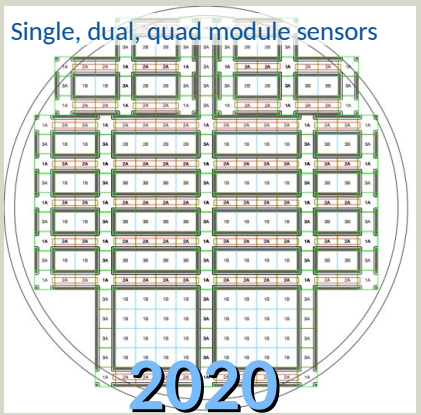
- 50 x 50 um² pixels, ATLAS ITk pixel geometry





Sensor for ATLAS ITk modules

- 50 x 50 um² pixels, 25 x 100 um² pixels
- Full-size ATLAS ITk pixel modules
- RD53A and RD53B compatible



From D.-L. Pohl Trento 2020

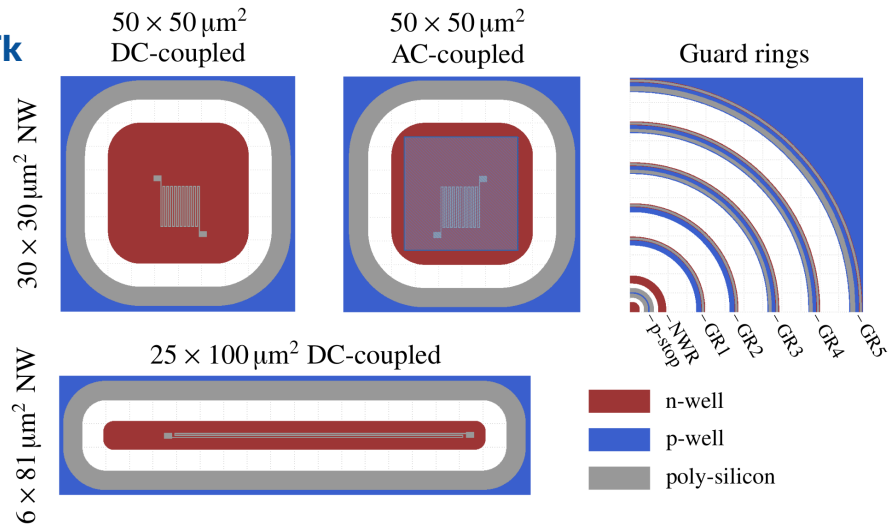
Byproducts of DMAPS efforts

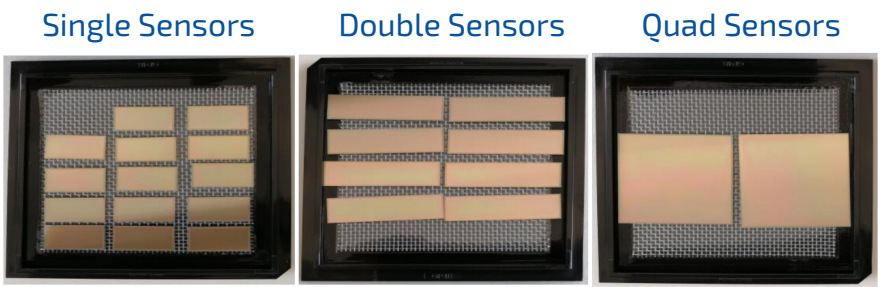
[https://doi.org/10.1016/j.nima.2020.164130]

Dedicated design

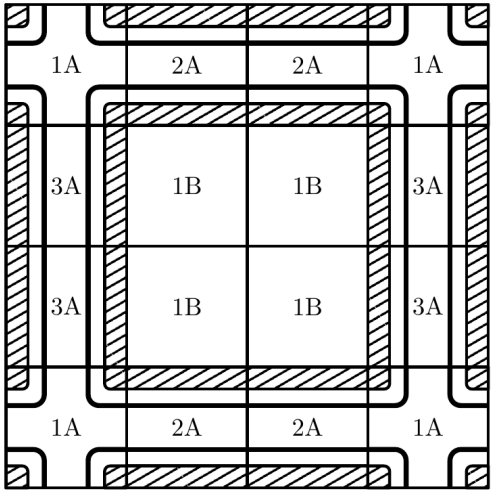
PIXEL SENSOR DESIGN

- **N-in-p** pixel sensor in 150 nm LFoundry technology for **ATLAS-ITk**
- Float-Zone wafers: ~8 kΩcm bulk resistivity, **150 µm thin**
- Different pixel designs**:**
  - 50 x 50 µm² and 25 x 100 µm² pixels
  - Poly-silicon as bias resistor (R_{bias} ~4.6 MΩ)
  - DC- or AC-coupled sensors (C_{AC} ~560 fF)
- **Reticle stitching to obtain large sensors (RD53-size)**
- Mainly single-chip sensors used for characterisation
- Irradiated at Bonn Isochronous cyclotron to
  2 x 10^{15} n_{eq}/cm² and 5 x 10^{15} n_{eq}/cm²

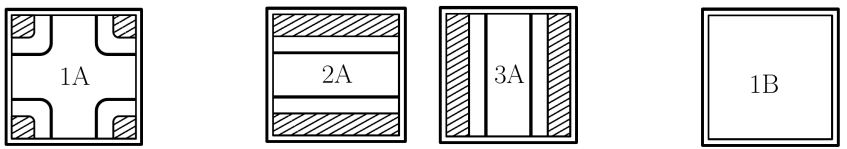




RETICLE STITCHING



- CMOS reticle: ~ 1 cm² → limits size of sensor
- To produce larger sensors → **reticle stitching**
- Requires that sensor can be subdivided into smaller blocks

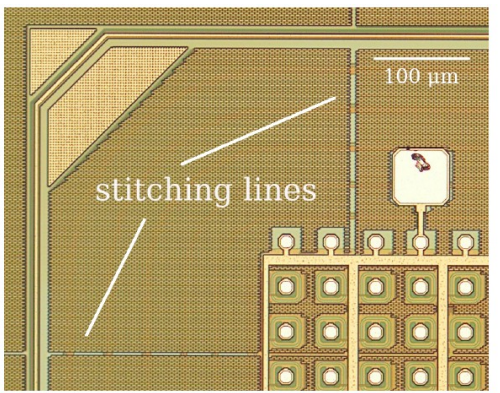


corner edges centre

- Different reticles are illuminated one after another and stepped accordingly

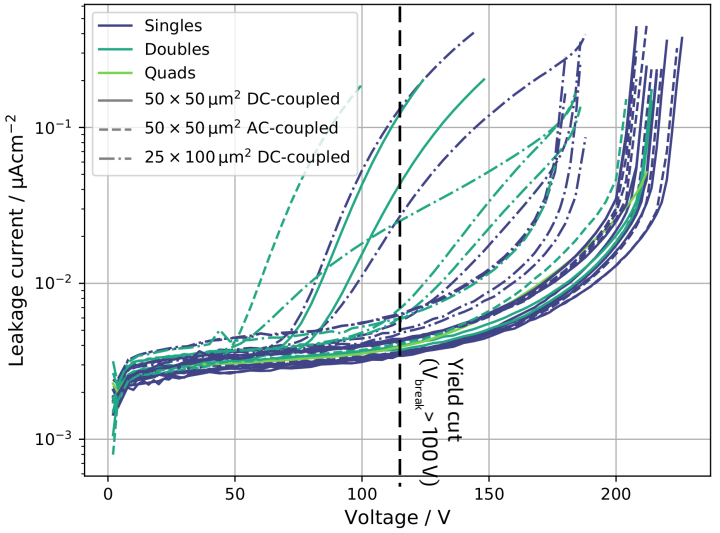
→ **Size of sensor not any more limited by reticle size**

→ Quad-module sensors with size of **4 x 4 cm²**

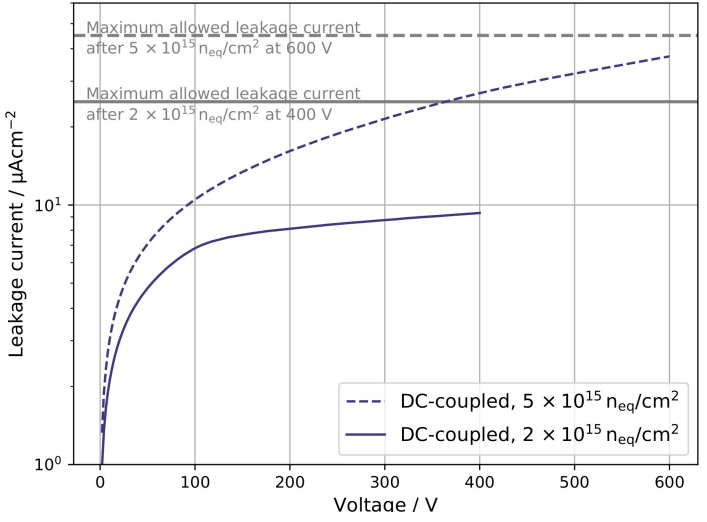


IV-CURVES

- Production yield: **~80 %**
- Similar behaviour for all sensors → **process variations negligible**
- Before irradiation:
  - Breakdown voltage: ~ 220 V
- After irradiation:
  - No breakdown visible up to 400 V / 600 V for both fluences
  - **Leakage current in agreement with requirements for ATLAS ITk**



At wafer level

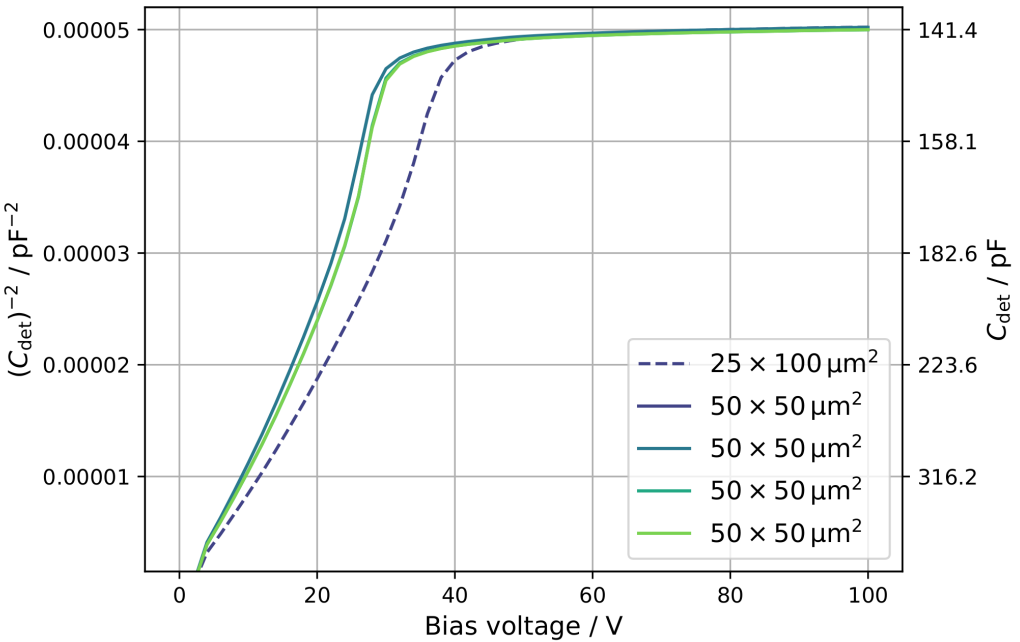


Assembled sensor (on SCC)

CV-CURVES

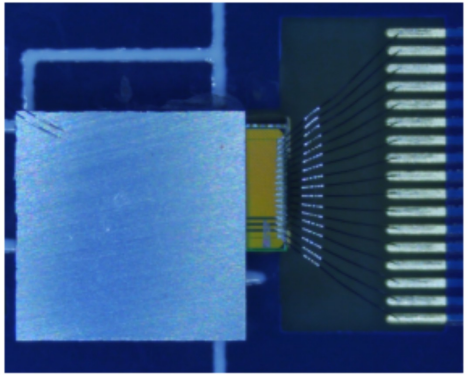
- Measurement of bulk capacitance using bias box and LCR-meter
- Measurement precision of 0.5 pF, f = 10 kHz
- HV connected to back side, GND connected to bias grid (connected to all pixels)
- Full depletion voltage
  - **50 x 50 um²: ~35 V (→ 8–9 kΩcm)**
  - 25 x 100 um²: ~40 V

    → Slightly larger full depletion depth due to stronger lateral expansion of depletion zone in rectangular geometry



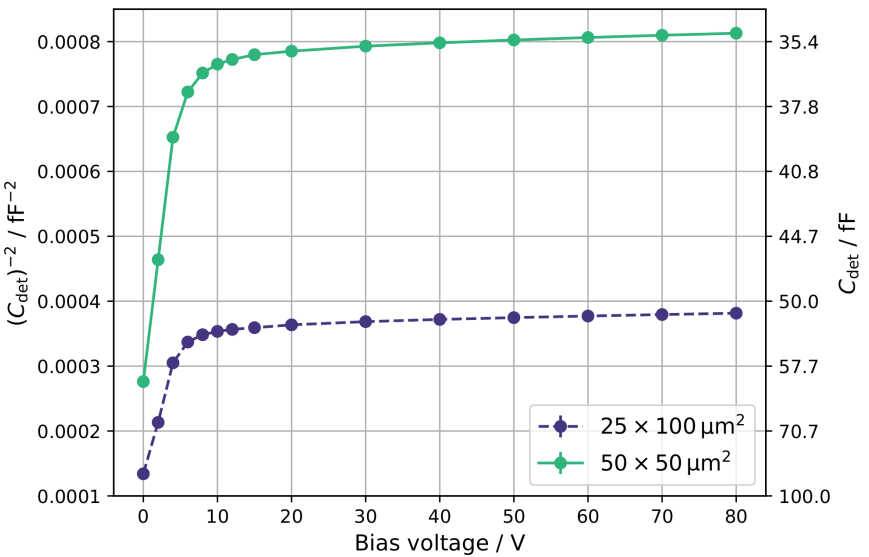
More information about setup/method:
https://iopscience.iop.org/article/10.1088/1748-0221/16/01/P01029

PIXEL CAPACITANCE



- Measurement of pixel capacitance with PixCap65 using CBCM
- Measurement precision: 0.3 fF
  - Allows measurement of capacitance of single pixel
- Shown values include parasitics (routing, bump-bonds) of 10 fF
- Dominant contribution in this design: Capacitance between p-stop and pixel implant (see referenced paper)
- Pixel capacitance:
  - **50 x 50 um²: ~35 fF**
  - **25 x 100 um²: ~51 fF**

    → due to larger area (C ~ A) and smaller distance (C ~ 1/d)

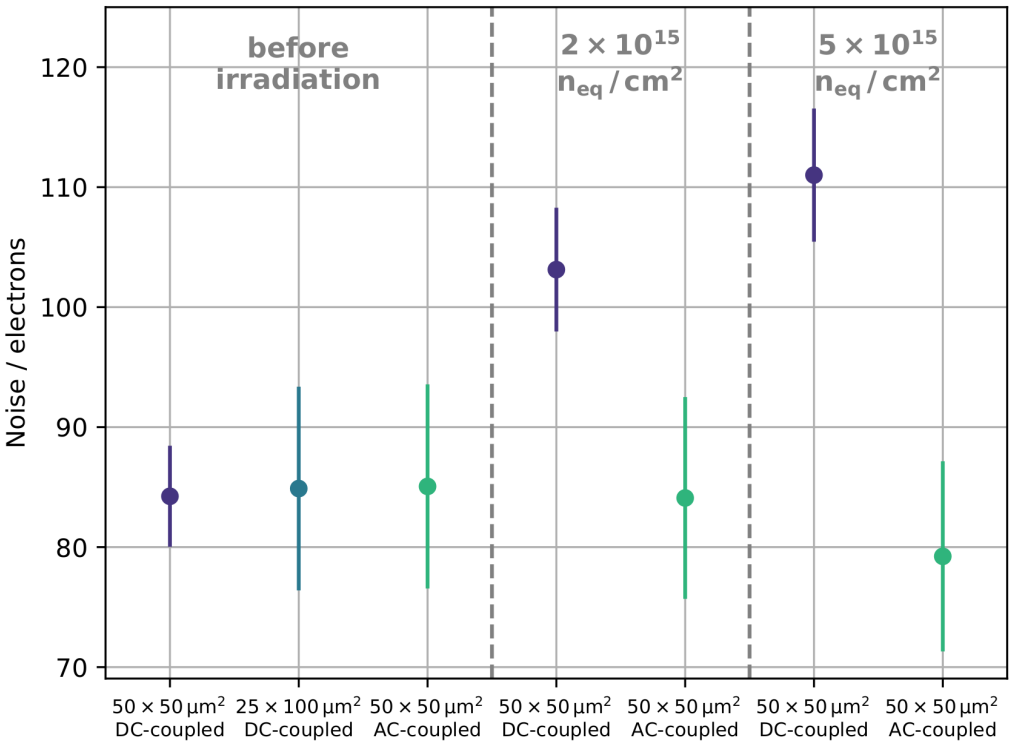


ELECTRONIC NOISE

- Noise measured in threshold scan using the Linear front-end of the RD53A readout chip
  - Noise: steepness of s-curve
- Before irradiation: **~85 e electronic noise**

  → No difference between sensor variants observed
- After irradiation:
  - ~100 e electronic noise (DC-coupled)
  - Noise remains the same for AC-coupled detectors

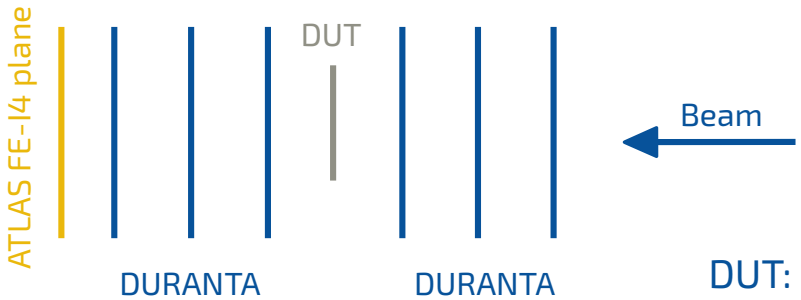
    → DC-component of noise is blocked



TESTBEAM SETUP

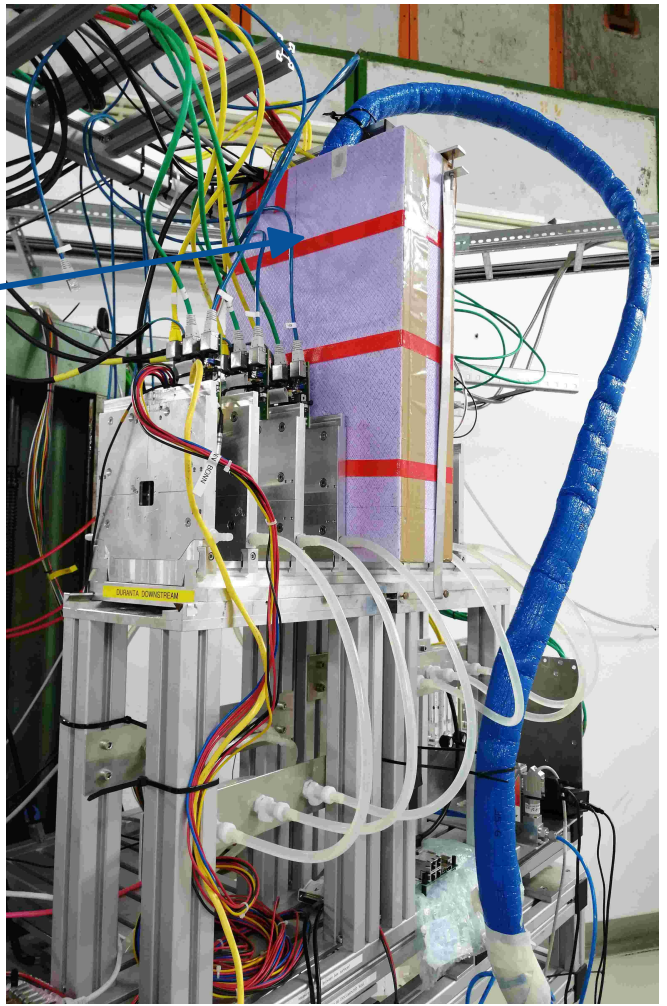
- Testbeam done at DESY
  - Perpendicular, 5 GeV electron beam, trigger rate: 3 - 5 kHz
- DUT installed into telescope setup (EUDET-type)
  - 6 Mimosa26 planes → 5 um spatial resolution
  - ATLAS FE-I4 plane → 25 ns time-stamping capabilities

  → precise tracking + proper time-stamping
- DUT read out using BDAQ53 R/O system [10.1016/j.nima.2020.164721]



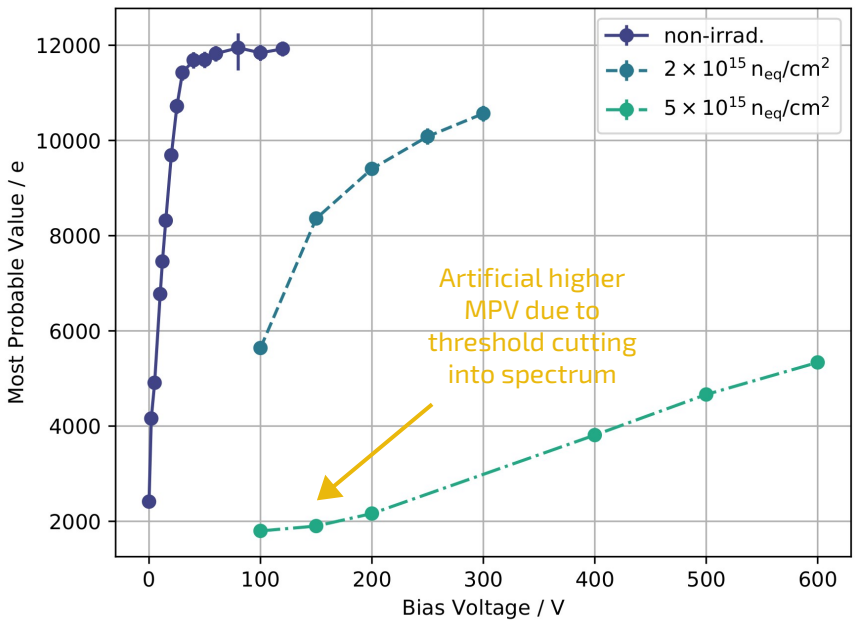
DUT: **D**evice **U**nder **T**est

Cooling box with DUT (-15 °C)

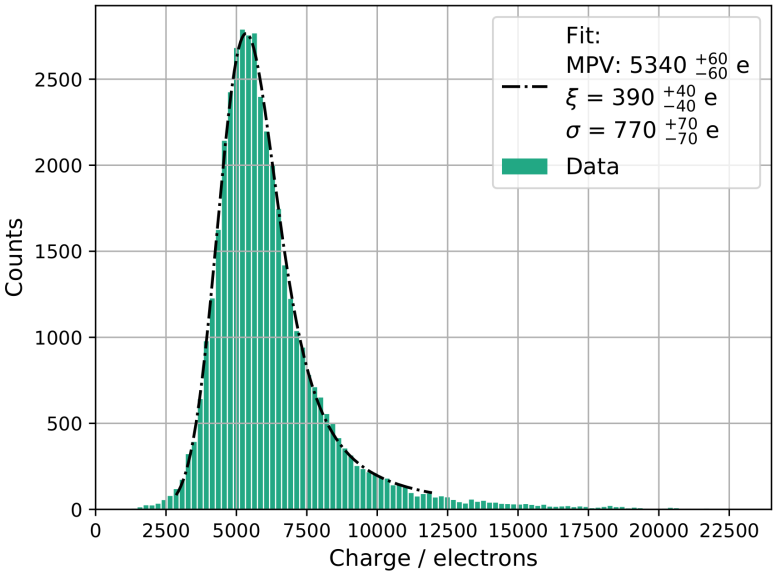


CHARGE COLLECTION

- Charge measured using high precision TDC-method
- After 5 x 10^{15} n_{eq}/cm^2: 5300 e charge signal @ 600 V



5 x 10^{15} n_{eq}/cm^2 | 600 V | DC-sensor

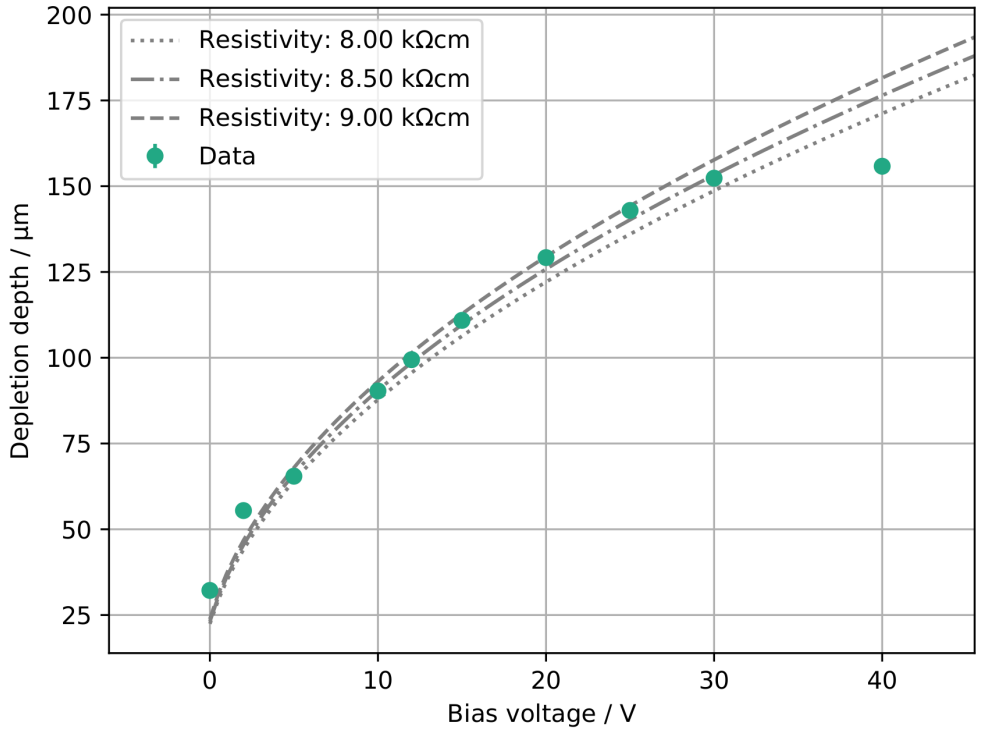


- Before irradiation:
  - **~ 12000 e charge signal** (full depletion)
- Charge collection efficiency after irradiation:
  - **2 x 10^{15} n_{eq}/cm^2: ~ 85 %** (10500 e) @ 300V
  - **5 x 10^{15} n_{eq}/cm^2: ~ 45 %** (5300 e) @ 600V

BULK RESISTIVITY

- Using 75 e/h-pairs per um:
  - Charge signal can be translated into depletion depth (assuming only depleted region contributes to signal)
- **Extracted bulk resistivity: 8 – 9 kΩcm**
  - **Fully depleted at around 30 – 40 V** (150 um thin FZ-bulk)
- In agreement with CV-measurements

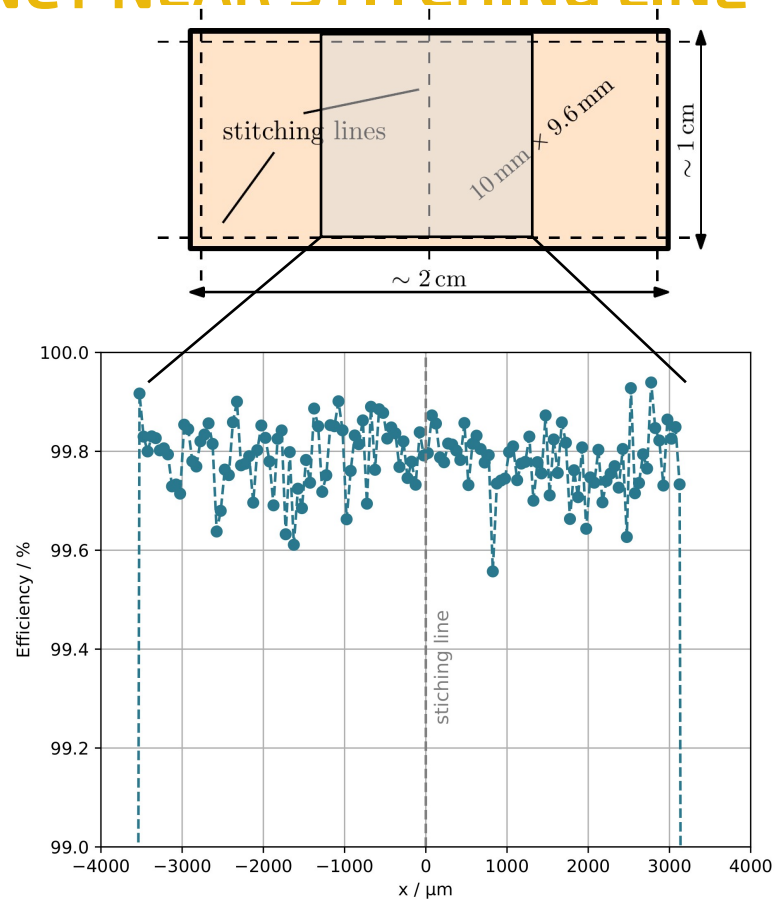
$$d\,[\mu\mathrm{m}] \approx 0.3\sqrt{V_{\mathrm{bias}}\,[\mathrm{V}] \cdot \rho_{\mathrm{bulk}}\,[\Omega\,\mathrm{cm}]}$$



HIT-DETECTION EFFICIENCY NEAR STITCHING LINE

- Investigate efficiency close to stitching line
- No efficiency drop near stitching line observed

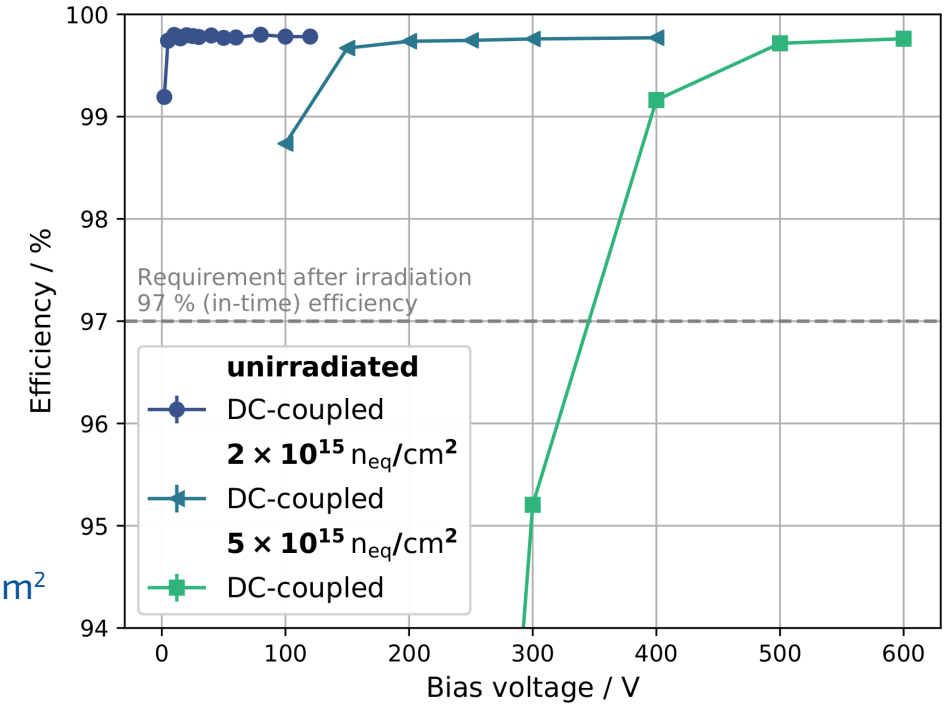
  → **Stitching works!**



HIT-DETECTION EFFICIENCY

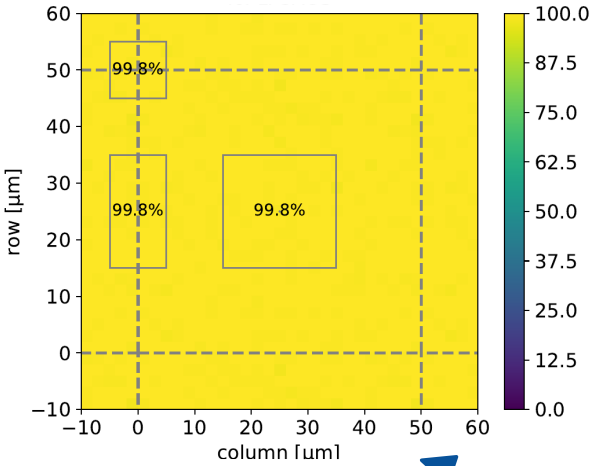
- Hit-detection efficiency measured using 5 GeV electrons at DESY
- Detector tuned to ~1200 e threshold with noise occ. < 10^{-6}
- Before irradiation:
  - Fully efficient at very low bias voltage (~5V)
  - **At 80V: 99.8 % efficiency**
- After irradiation:
  - **~99.7 % efficiency after 5 x 10^{15} n_{eq}/cm^2**
  - Fulfills ATLAS ITk requirement (> 97 %)
- In-time hit efficiency (< 20 ns): > 99.4 % after 5 x 10^{15} n_{eq}/cm^2

Efficiency | DC-coupled 150 um thin passive CMOS

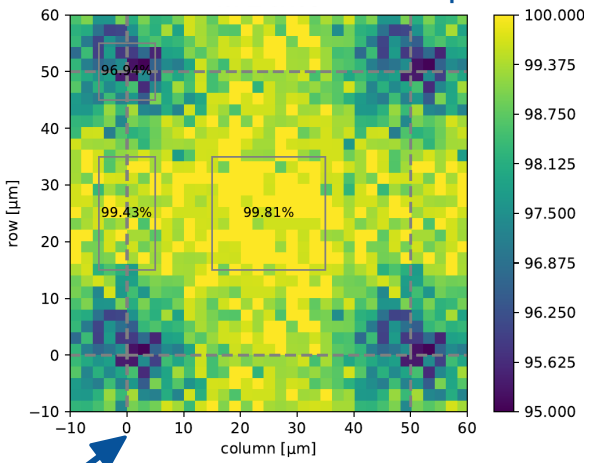


IN-PIXEL EFFICIENCY/CHARGE

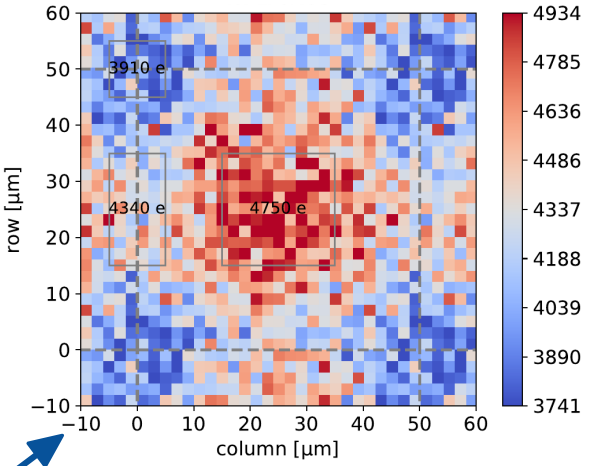
In-pixel efficiency | **non-irrad.** | 80 V



In-pixel efficiency | **5 x 10^{15} n$_{eq}$/cm²** | 400 V



In-pixel charge | **5 x 10^{15} n$_{eq}$/cm²** | 400 V



Efficiency

Charge

→ Efficiency loss mainly in pixel corners

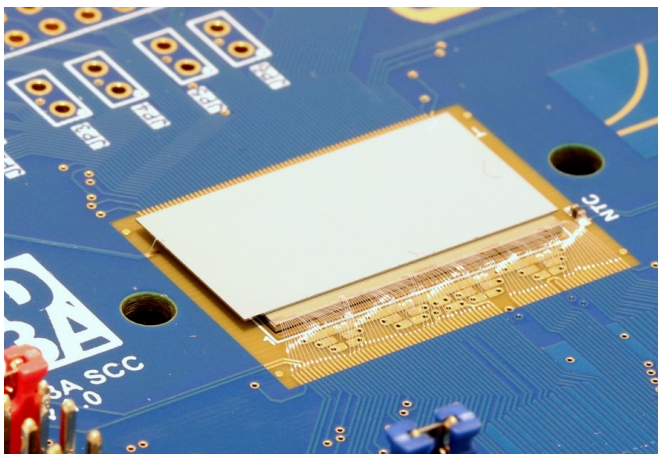
→ Can be explained with lower charge in pixel corners due to lower electric field and more charge sharing in pixel corners

CONCLUSION

- Demonstrated that large-area passive CMOS pixels sensors compatible with the future ATLAS ITk readout chip can be manufactured

  → Reticle stitching was successfully used

- Radiation hardness up to fluence of 5 x 10^{15} n_{eq}/cm^2 demonstrated:
  - Sensors are functional up to 600 V
  - > 99 % (in-time) hit-detection efficiency (@ > 400 V)
  - Charge signal at 600V: ~ 5300 e (5 x 10^{15} n_{eq}/cm^2)
- Cost-effective solution for pixel sensors of large-area detectors
- Suitable for radiation harsh environments like ATLAS/CMS exp.



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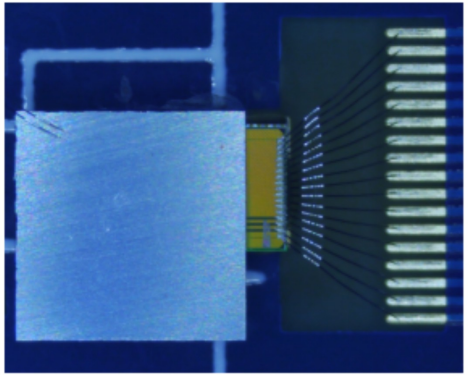
THANK YOU FOR YOUR ATTENTION

The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF)

More information about setup/method:
https://iopscience.iop.org/article/10.1088/1748-0221/16/01/P01029

PIXEL CAPACITANCE



- Measurement of pixel capacitance using PixCap65 using CBCM
- Measurement precision: 0.3 fF
  - Allows measurement of capacitance of single pixel
- Shown values include parasitics (routing, bump-bonds) of 10 fF
- Dominant contribution in this design: Capacitance between p-stop and pixel implant (see referenced paper)
- Pixel capacitance:
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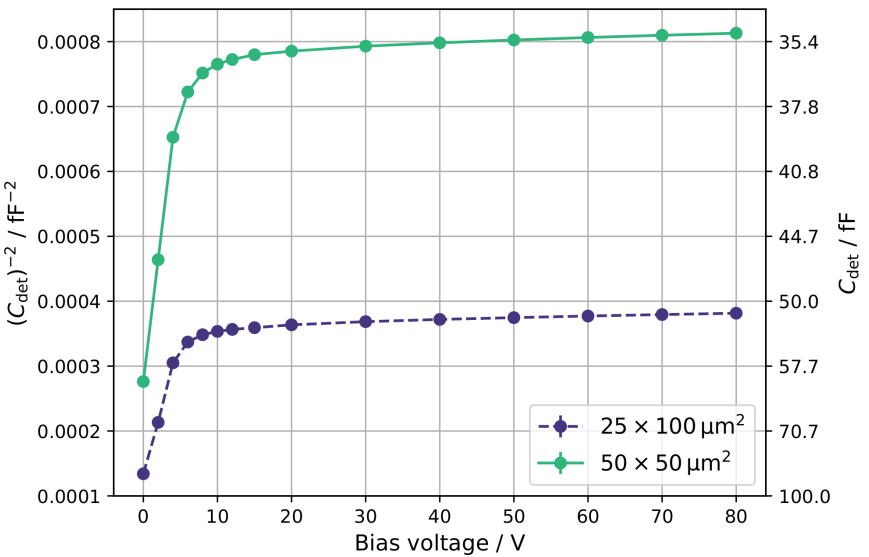
  - **25 x 100 um²: ~51 fF**

    → due to larger area (C ~ A) and smaller distance (C ~ 1/d)



CROSS-TALK

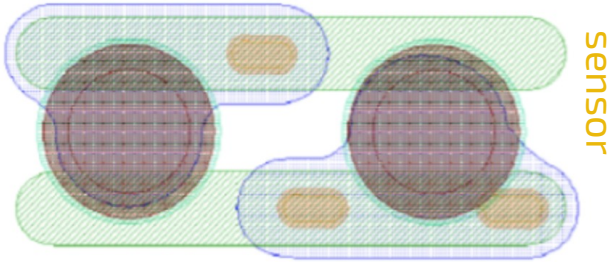
- 10 % cross-talk measured with convential 25 x 100 um² sensors measured using the RD53A readout chip

  → Due to unavoidable overlap of metal layer and pixel implant

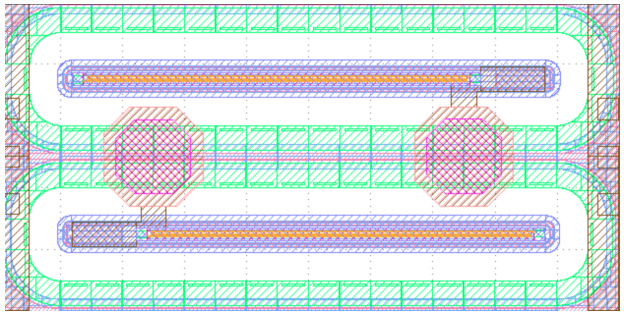
- No overlap for passive CMOS sensors
- **No cross-talk measured for passive CMOS sensors**
  - 50 x 50 um²: < 0.6 % cross-talk (minimal measurable cross-talk)
  - 25 x 100 um²: < 2.5 % cross-talk (minimal measurable cross-talk)

$$\text{cross-talk}\,[\%] = \frac{\mu_{\text{reg}}}{\mu_{\text{x}} \cdot n_{\text{inj}}} \times 100$$

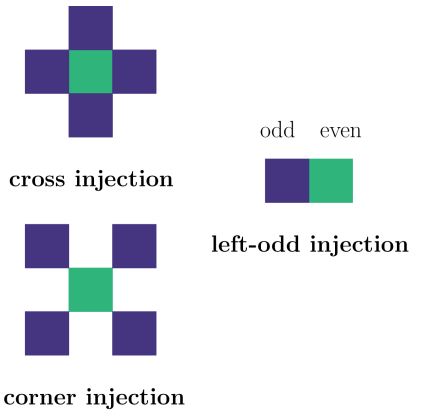
Overlap of metal layer and pixel implant



Conventional sensor

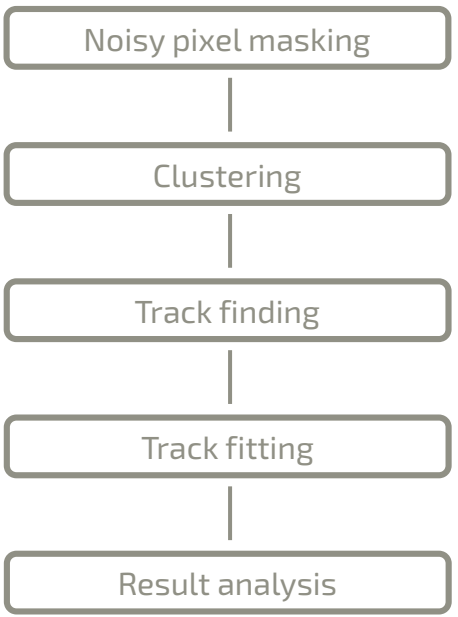


CMOS sensor



TRACK RECONSTRUCTION USING BTA

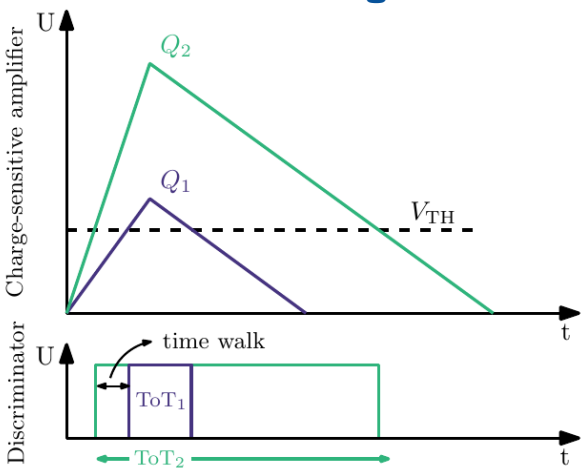
- Data analysed with beam telescope analysis (BTA): https://github.com/SiLab-Bonn/beam_telescope_analysis
- Kalman Filter algorithm used for track fitting (unbiased residuals)
- Hit-detection efficiency: # number of track assoc. to DUT / # total number of tracks
- Association distance: 120 um

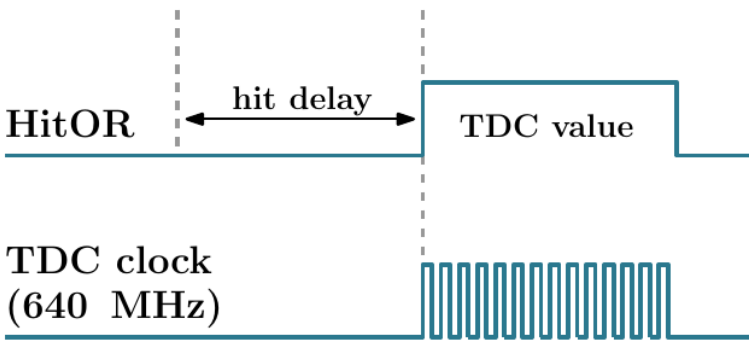


CHARGE MEASUREMENTS

- Instead of on-chip charge measurement (ToT) use TDC-technique to precisely measure charge
  - Discriminator output signal (length ~ charge) sampled with 640 MHz
  - 1.5625 ns discretisation error
- **Precise charge calibration using X-ray sources possible for every detector**
- **Measurement of charge collection behaviour of pixel detector**

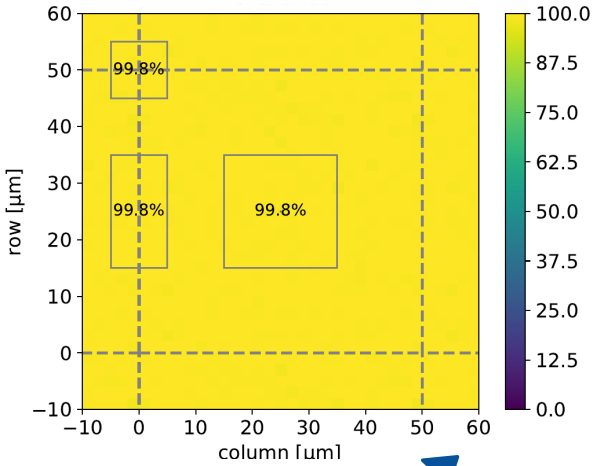
For simplicity:
Consider only
single-hit events



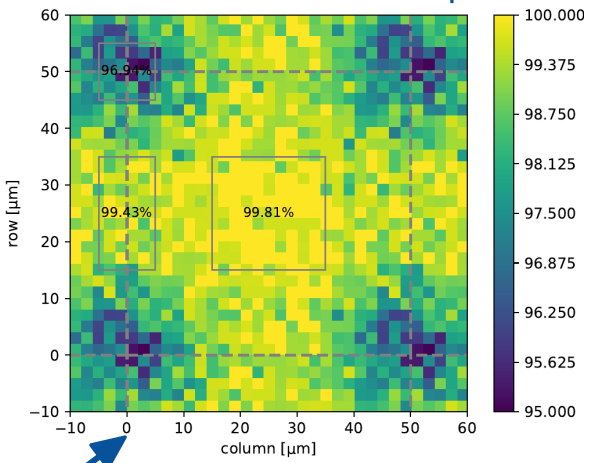


IN-PIXEL EFFICIENCY/CHARGE

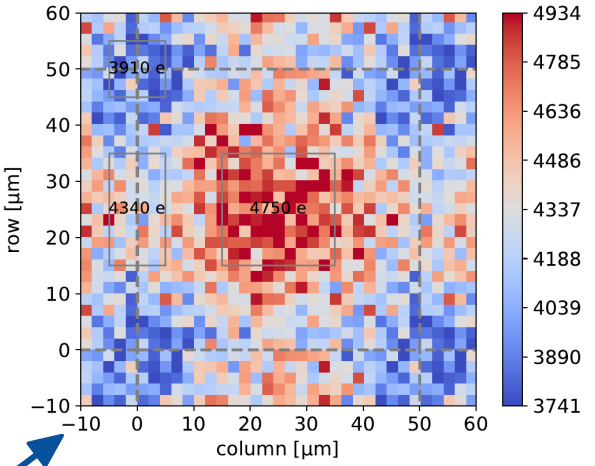
In-pixel efficiency | **non-irrad.** | 80 V



In-pixel efficiency | **5 x 10^{15} n$_{eq}$/cm²** | 400 V



In-pixel charge | **5 x 10^{15} n$_{eq}$/cm²** | 400 V



Efficiency

Charge

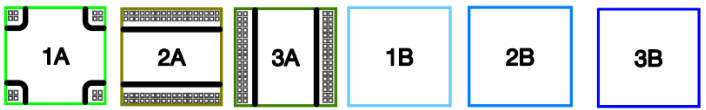
→ Efficiency loss mainly in pixel corners

→ Can be explained with lower charge in pixel corners due to lower electric field and more charge sharing in pixel corners

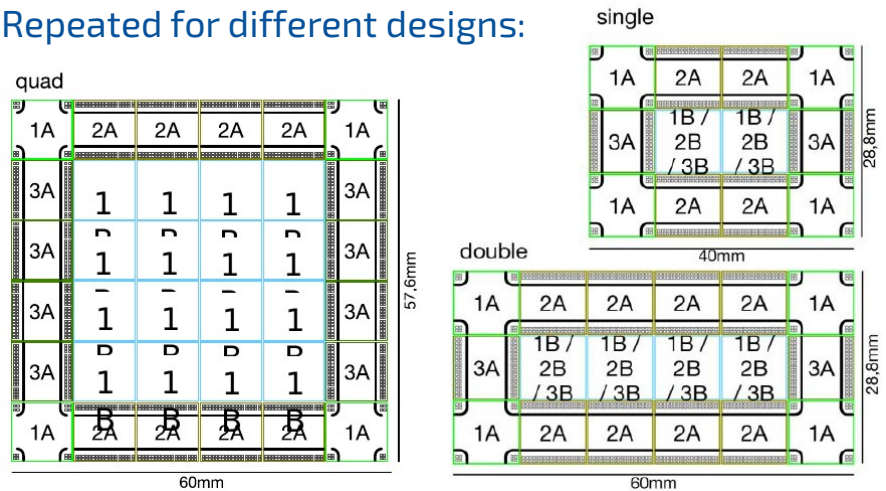
STITCHING AND BIASING

- Sensor size > reticle size → **reticle stitching** required
- Different reticles:

Edge pixel reticles Center pixel reticles

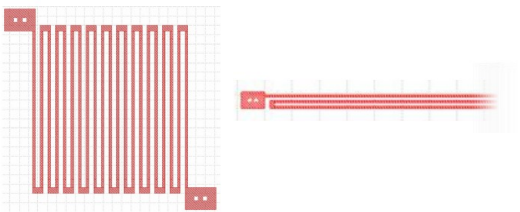


- Repeated for different designs:

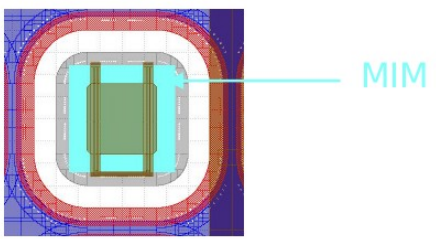


- **Resistor biasing** for every pixel flavors, likely benefitial to prevent cross-talk
- Bias resistor: ~ **4.5 MΩ**

50 x 50 um² 25 x 100 um²



- MIM capacitators for AC-coupling: 0.56 pF



IN-TIME EFFICIENCY MEASUREMENT

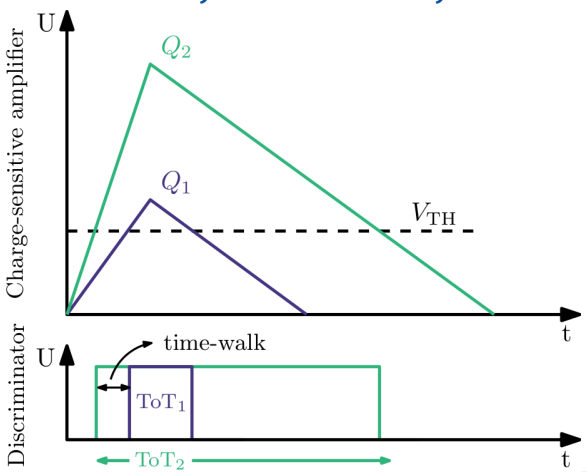
- At the LHC, particle bunches collide every 25 ns

  → Necessary to detect all hits of a single collision within 25 ns to disentagle them

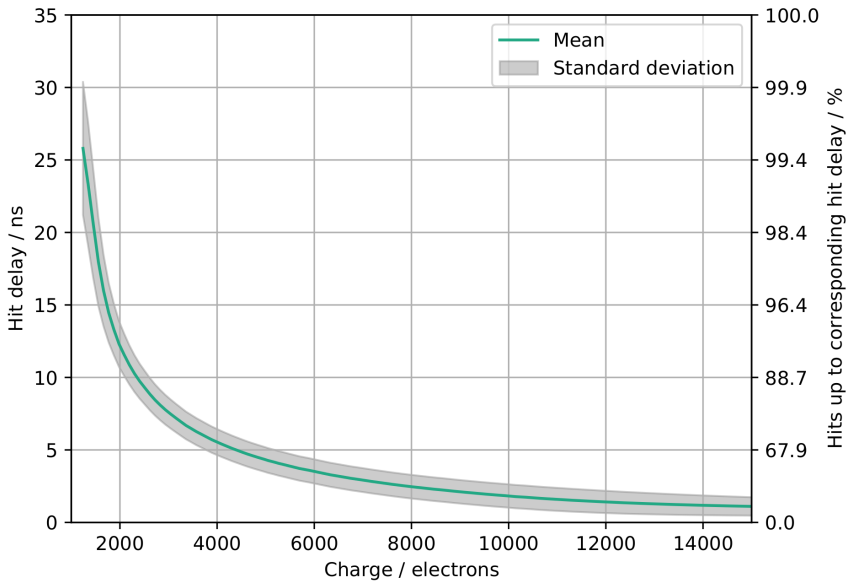
  → **In-time efficiency**: „Probability to detect a hit within a given time window“

- Important is variation of hit delay: „time-walk“
- Mainly influenced by the design of analogue front-end

Hit delay: time between trigger and hit detection



The smaller the input charge, the larger the hit delay



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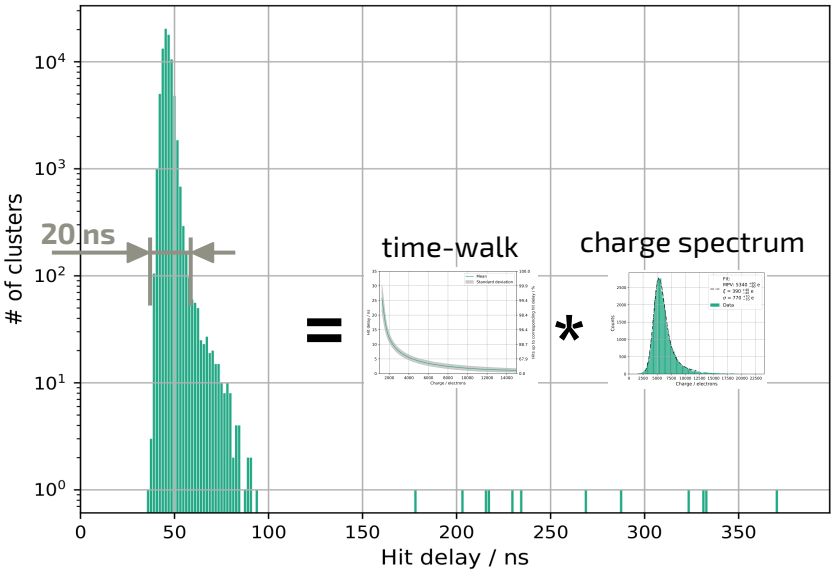
- Hit delay in test beam is measured by recording the difference of scintillator signal and discriminator output using TDC-method
- Define a time window: 20 ns



“regular” efficiency

$$\epsilon_{\mathrm{in-time}} = \epsilon_{\mathrm{hit}} \times P_{\Delta t}$$

in-time efficiency

in-time probability

IN-TIME HIT-DETECTION EFFICIENCY

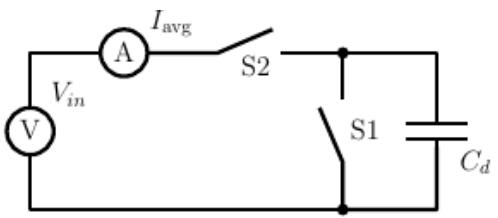
- Measurements done using the Linear front-end of the RD53A readout chip
- For sufficient high bias voltage: **In-time efficiency larger than ATLAS ITk requirement (> 97 %)**
- Reason for lower in-time efficiency at smaller bias voltage:
  - Smaller charge signal due to smaller depletion depth (only depleted volume contributes)
  - Larger hit delay variations (→ time-walk)
  - Lower in-time efficiency (in-time probability)

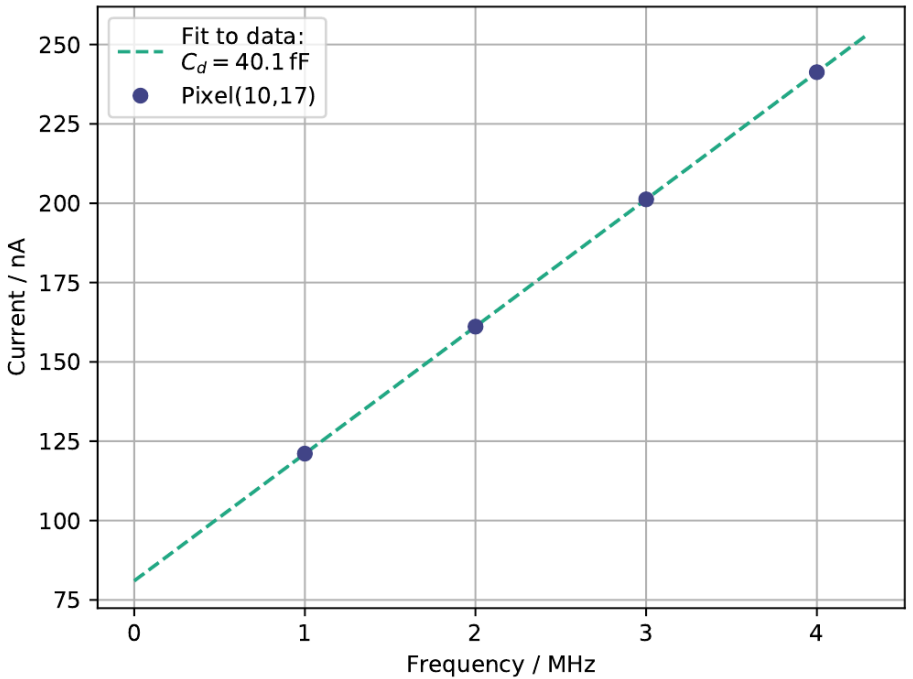
	2×10^{15} n_{eq}/cm^2		5×10^{15} n_{eq}/cm^2	
	100 V	400 V	400 V	600 V
Regular efficiency / %	98.74	99.77	99.16	99.76
In-time probability / %	97.14	99.82	97.29	99.65
In-time efficiency / %	95.91	**99.59**	96.47	**99.41**

Charge-Based Capacitance Measurement (CBCM)

- Periodic switching of switches S1 and S2 lead to average current

$$C_d = \frac{Q}{V_{in}} = \frac{\int_0^T I(t)\mathrm{d}\,t}{V_{in}} = \frac{\frac{1}{T}\int_0^T I(t)\mathrm{d}\,t}{f \cdot V_{in}} = \frac{I_{\mathrm{avg}}}{f \cdot V_{in}}$$

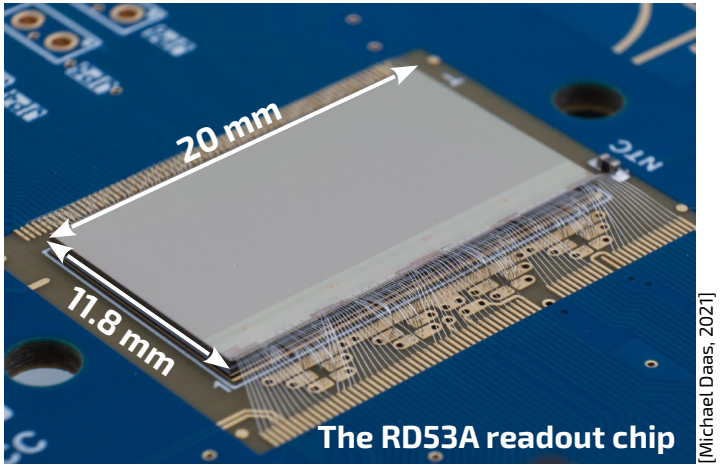




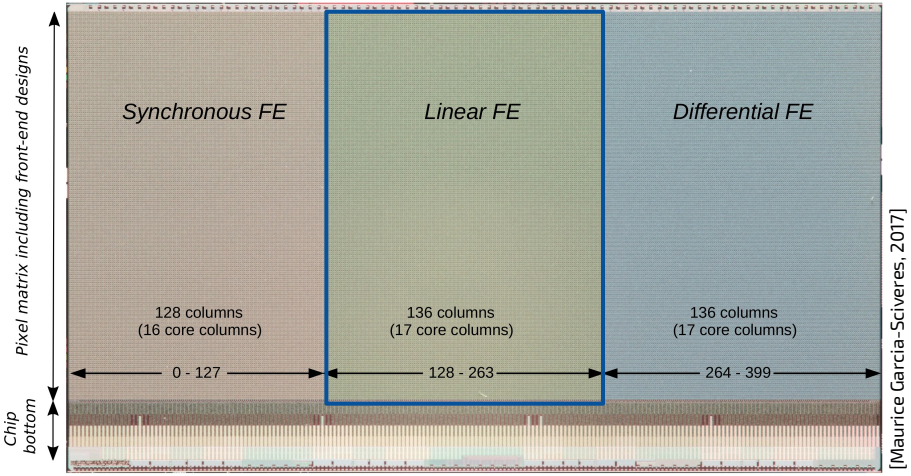
More information about setup/method:
https://iopscience.iop.org/article/10.1088/1748-0221/16/01/P01029

THE RD53A READOUT CHIP

- Signal processing → **Fast charge digitisation**
- RD53A prototype readout chip for ATLAS/CMS pixel detectors:
  - Demonstrate suitability of 65 nm CMOS process for HL-LHC
  - Choose optimal analogue front-end design
- 400 x 192 pixels with size of 50 x 50 µm²
- In this work: Linear front-end used for sensor characterisation



[Michael Daas, 2021]



[Maurice Garcia-Sciveres, 2017]