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SI LAB
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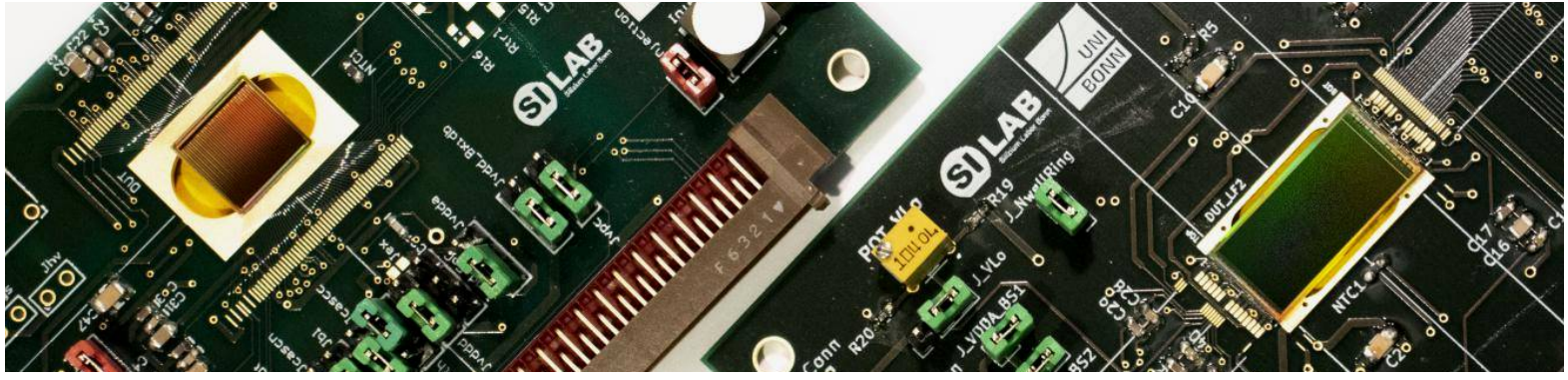
VERBUNDSMEETING
LF-MONOPIX2 UPDATE

Lars Schall on behalf of the LF-Monopix testing team

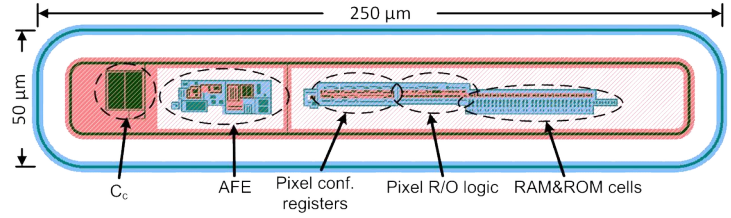
Outline

- The LF-Monopix Family
- Laboratory test of irradiated LF-Monopix2
- Testbeam results of irradiated LF-Monopix2
- Conclusion and upcoming plans

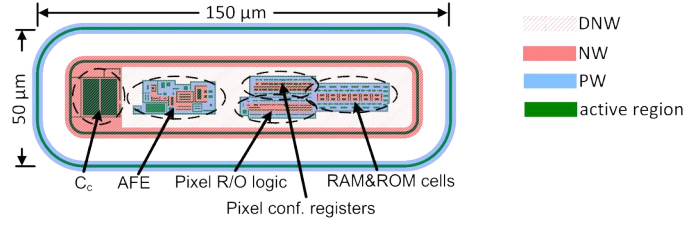


The LF-Monopix Chips

- 150nm LFoundry CMOS Technology
- **Large collection electrode** design
- **LF-Monopix1**: ~1x1 cm² matrix
  50x250 µm² pixel pitch
- **LF-Monopix2**: ~2x1 cm² matrix
  50x150 µm² pixel pitch
- Substrate resistivity > 2 kΩcm
- Fast **column drain readout** architecture (FE-I3 like)



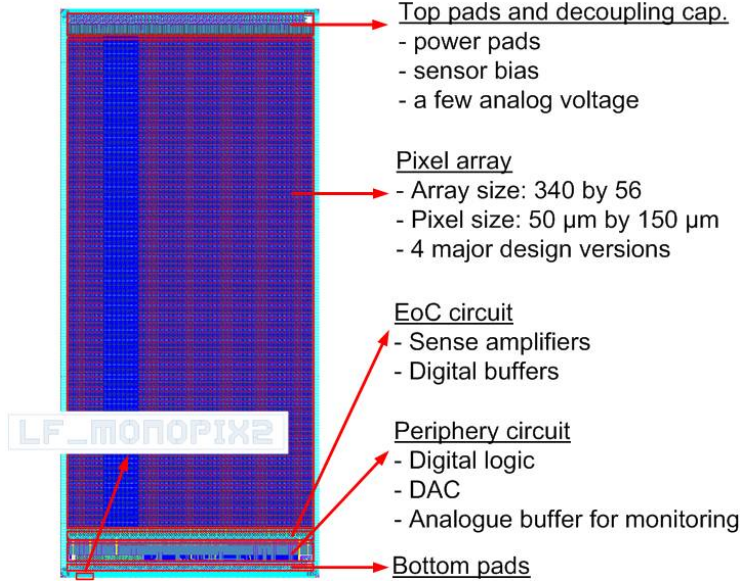
LF-Monopix1 (Mar 2017)



LF-Monopix2 (Feb 2021)

LF-Monopix2: Design

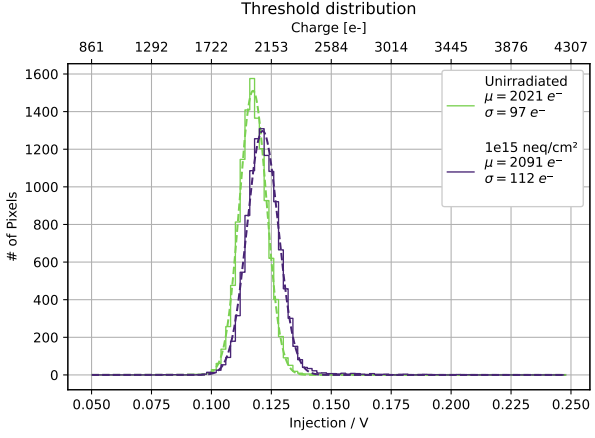
- First chip with column drain readout architecture and **full column length**
  - Improved pixel layout to **mitigate cross-talk**
- Total of 6 matrices with 3 CSA types
  - Matrix 1-4 proven FE design from LF-Monopix1
- **6 bit ToT** information
- 4 bit **in-pixel threshold DAC**
  - Two different tuning circuit designs
- 40MHz / 160MHz CMOS or LVDS serial output

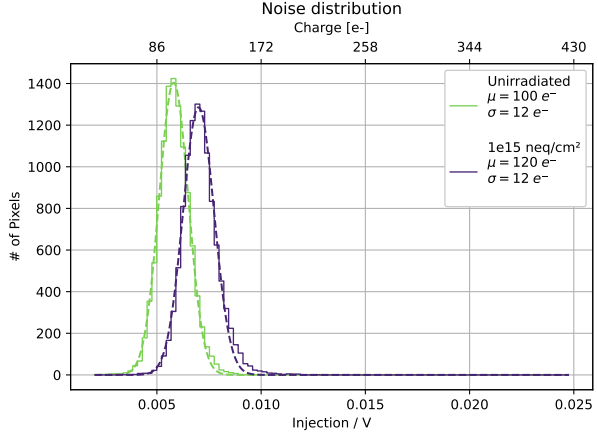


Matrix	Column	CSA	Feedback cap.	Discriminator	Logic
1-1	55 - 52	V1	1.5 fF	Bidirectional tuning	Falling
1-2	51 - 48	V1	5 fF	Bidirectional tuning	Falling
1-3	47 - 40	V1	5 fF	unidirectional tuning	Rising
1-4	39 - 16	V1	5 fF	unidirectional tuning	Falling
2	15 - 8	V2	1.5 fF	Bidirectional tuning	Falling
3	7 - 0	V3	1.5 fF	Bidirectional tuning	Falling

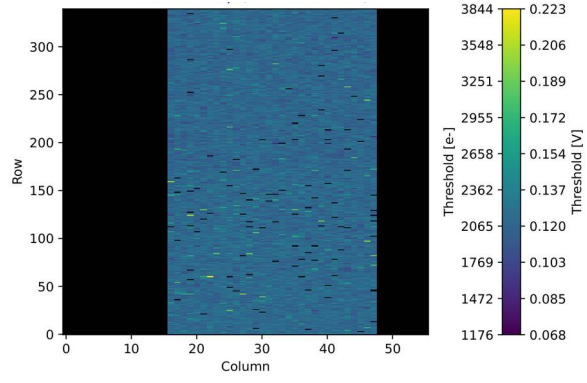
Tuning of Irradiated LF-Monopix2

- Operate irradiated chips at -20°C
  - Unirradiated results at room temperature for comparison
- Able to tune all matrices to approx. **2ke⁻ threshold** after irradiation *(here Matrix 1-3/4)*
  - **Uniform threshold distribution** across matrix (threshold **dispersion ~100e⁻)**
  - Slight increase in **ENC** after irradiation





Threshold Map

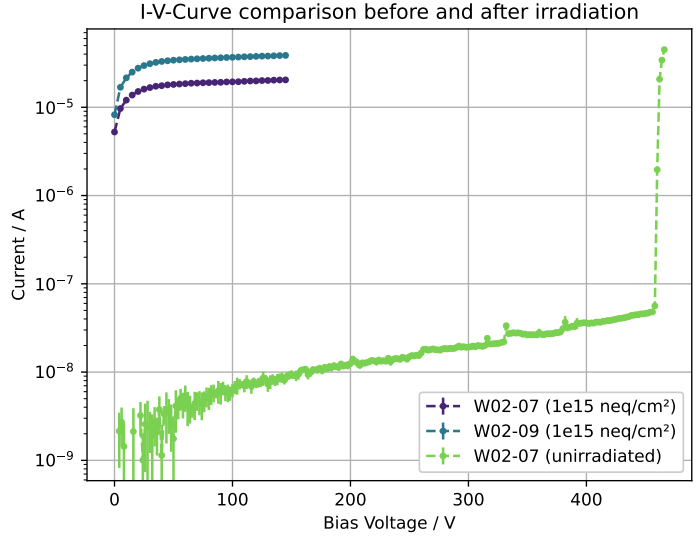


I-V-Curves of Irradiated LF-Monopix2

- **Breakdown** voltage >**400V** for unirradiated chips

- Expected increase in leakage current after irradiation
  - **Unirradiated** I-V curve @ **room temperature**
  - **Irradiated** I-V curves @ **-15°C**
  - No temperature scaling done here!

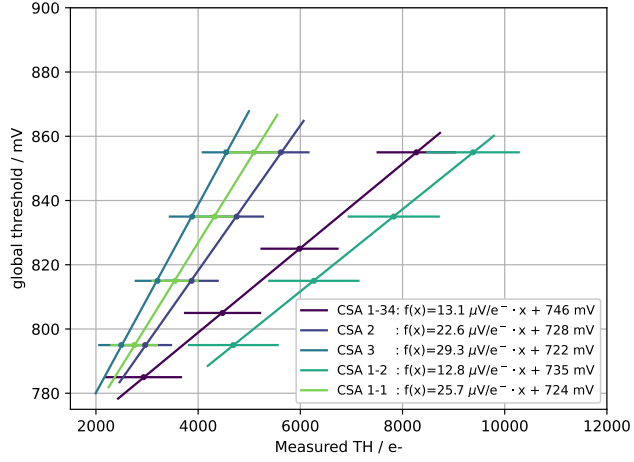
- Difference after irradiation still under investigation



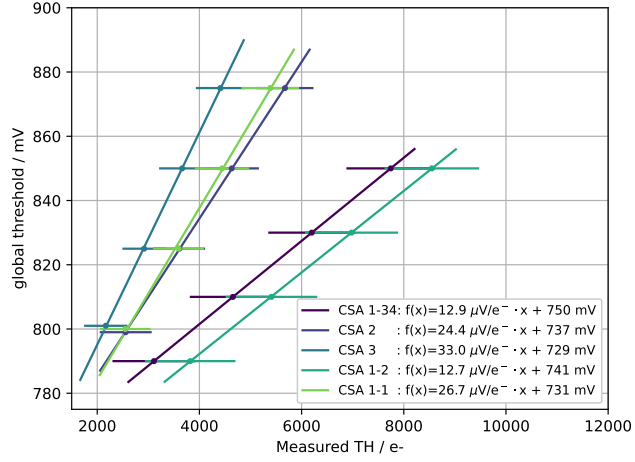
Gain Measurements

- Measure untuned threshold at different global threshold settings
- Gain extracted from linear regression
  - Gain slightly increased for large gain matrices after irradiation
- Smaller $C_{feedback}$ → larger gain → faster LE rise time

Gain Unirradiated



Gain Irradiated



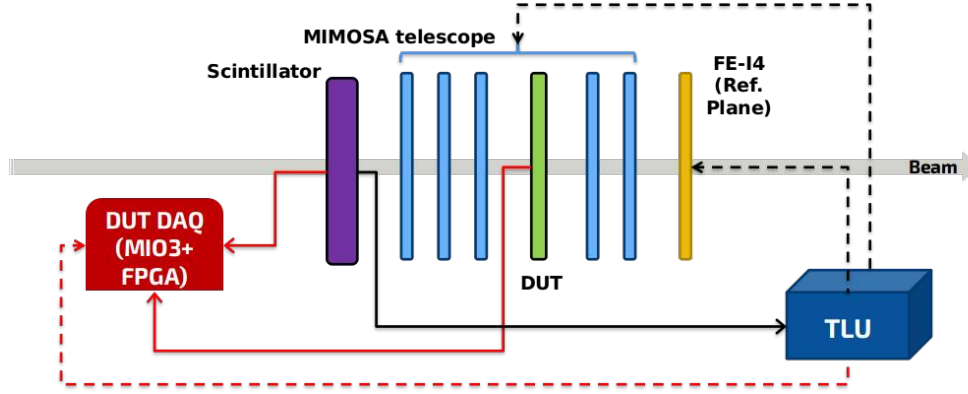
Testbeam Setup

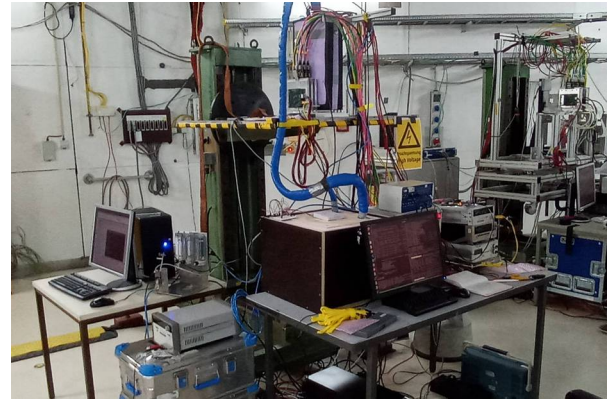
- DESY: **5 GeV electron beam**

- Telescope setup:
  - Scintillator
  - EUDET type beam telescope
  - FE-I4
  - Trigger Logic Unit (TLU)
  - DUT (LF-Monopix2)

- **Irradiated DUT cooled to -20°C**

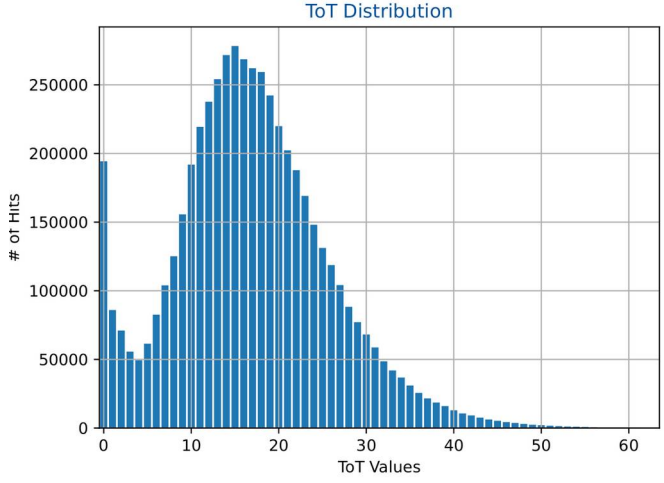
- Sample **Scintillator**, **DUT hit**, **TLU trigger** in DAQ for event building

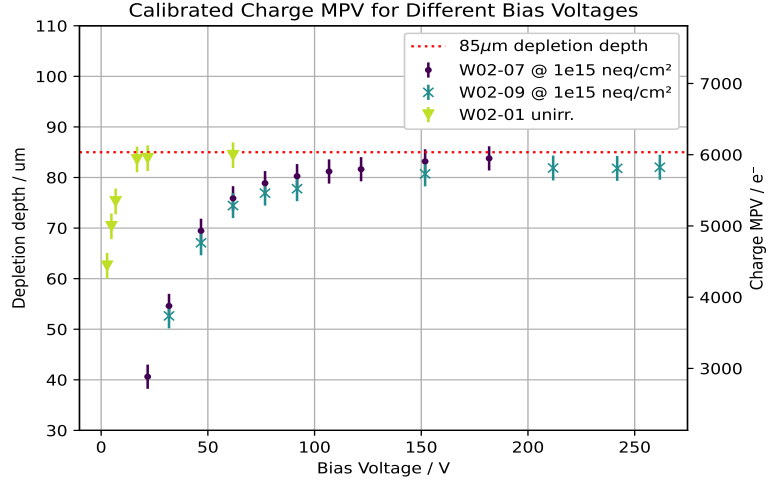




Depletion Depth

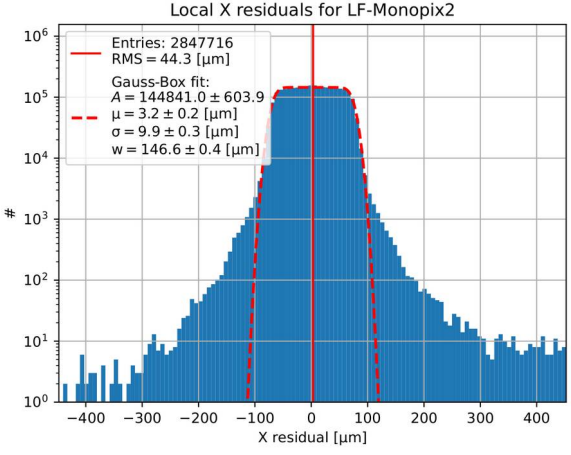
- Calculate calibrated charge MPVs from ToT distribution
- **Depletion depth profile of both chips in very good agreement**
  - Shows consistency of Bonn Cyclotron irradiation site
- Plateau starting around 100V bias instead of 15V for unirradiated chips
  - All chips operated at roughly 2ke⁻ threshold

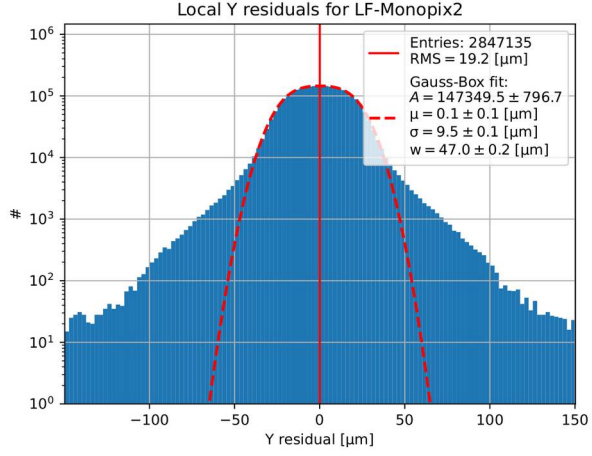


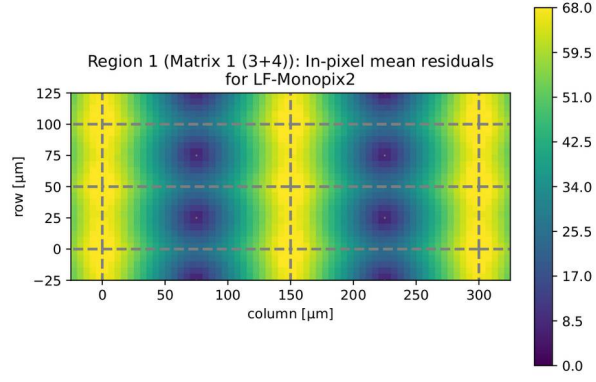


Residuals

- Testbeam analysis done using *Beam Telescope Analysis*
- Residuals as expected
- Fitted Box-Gaussian to distribution
  - Box width in good agreement with pixel pitch (150 x 50 µm²)

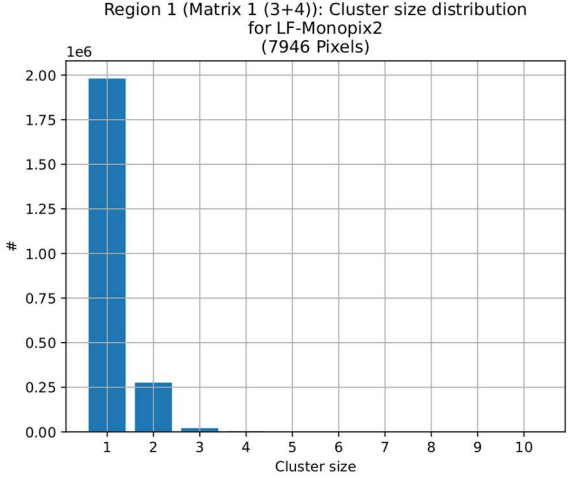


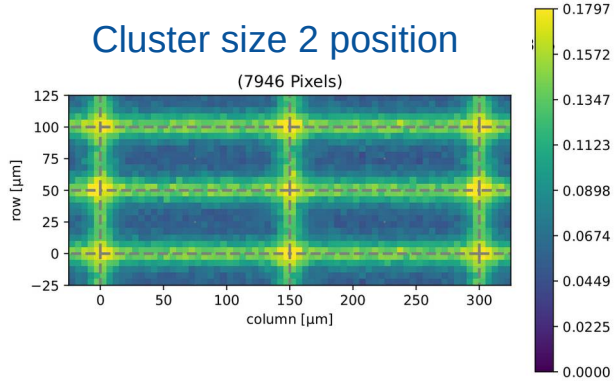


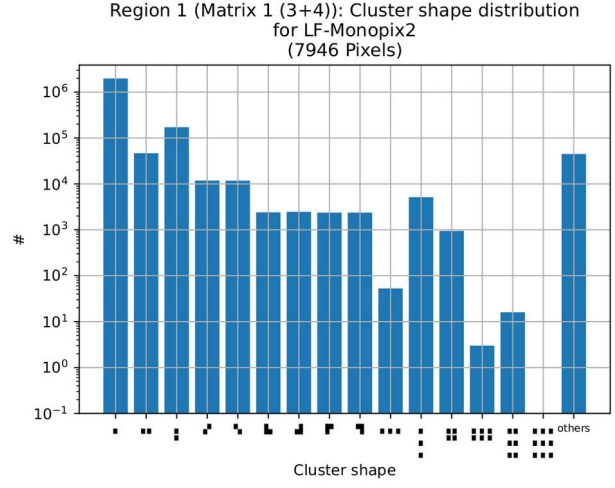


Cluster Size

- Mostly observe single pixel clusters
- Charge sharing likely at pixel edges
- Vertical clusters more likely than horizontal clusters (pixel shape)

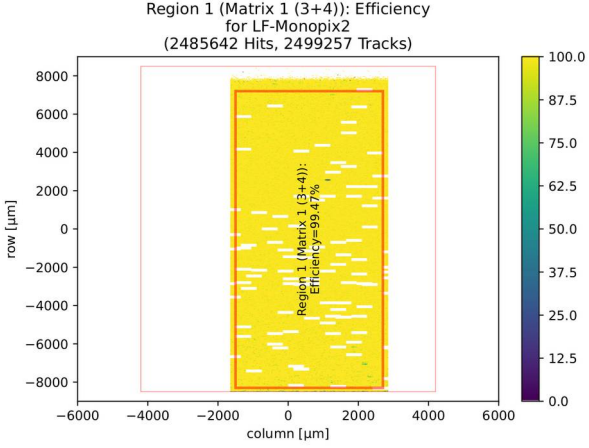


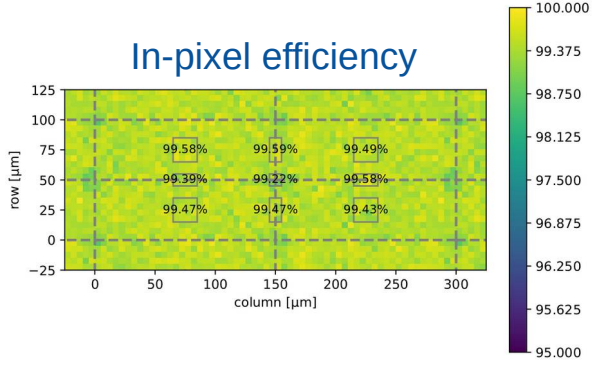


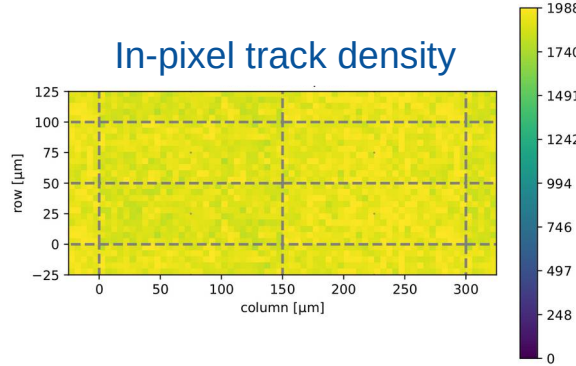


Efficiency Results

- **Uniform hit detection** and **in-time efficiency** across matrix (150V bias, 2ke⁻ threshold)
  - *Shown here Matrix 1-3/4*
- Projected onto **2x2 in-pixel** plots for in-pixel studies
- Combine data runs to achieve higher statistics (if necessary)





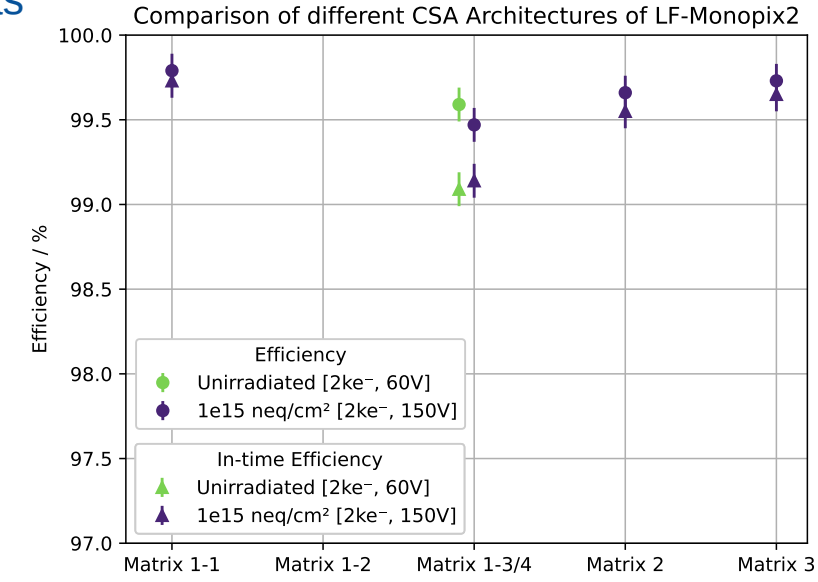


Efficiency Results

- **Hit efficiencies** and **in-time efficiencies >99%** for all matrices at **2ke⁻ threshold** and **150V** bias voltage **after irradiation**

- **Unirradiated** result for Matrix 1-3/4 at **2ke⁻ threshold** and 60V bias voltage as comparison

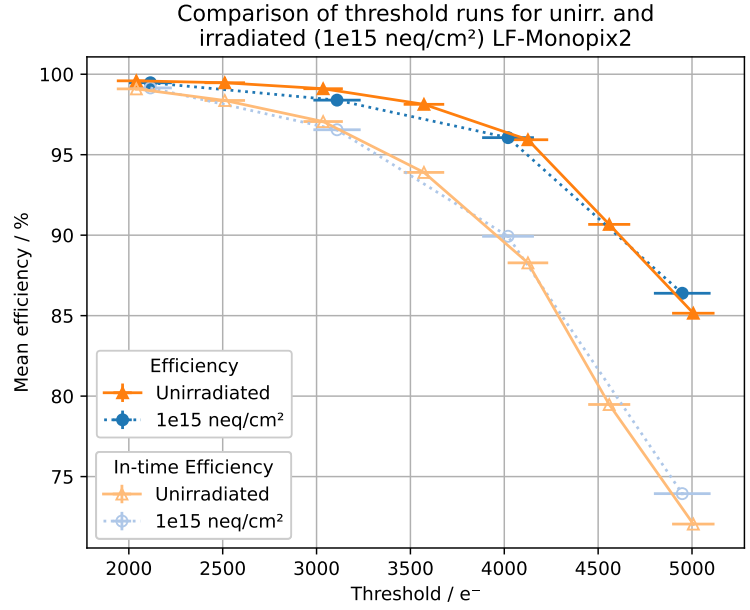
→ **No significant efficiency** loss after irradiation to 1e15 neq/cm²



Efficiency at Different Thresholds

- Measured with matrix M1-3/4 for higher statistics
  - Unirr. 60V bias voltage
  - Irr. 150V bias voltage

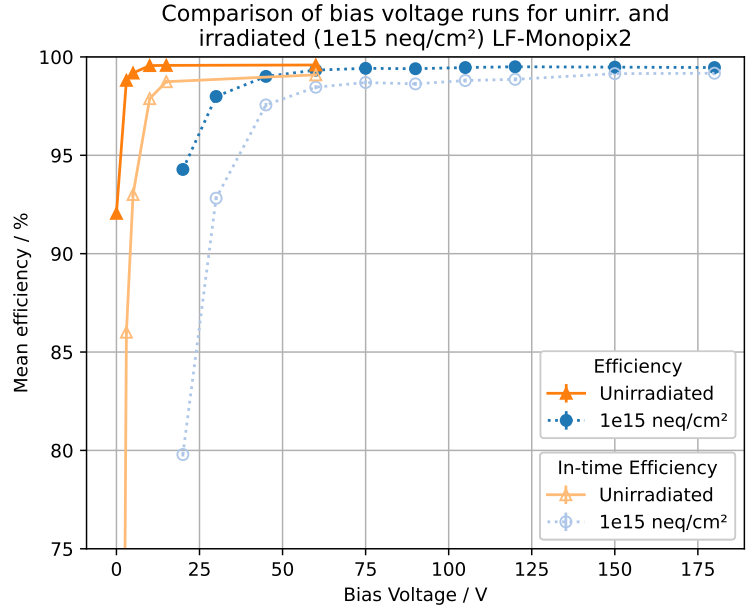
- Efficiencies at different thresholds:
  - Expected **decrease in efficiency for higher thresholds**
  - Discrepancy between in-time and hit detection efficiency increases similarly



Efficiency at Different Bias Voltages

- Measured with matrix M1-3/4 for higher statistics

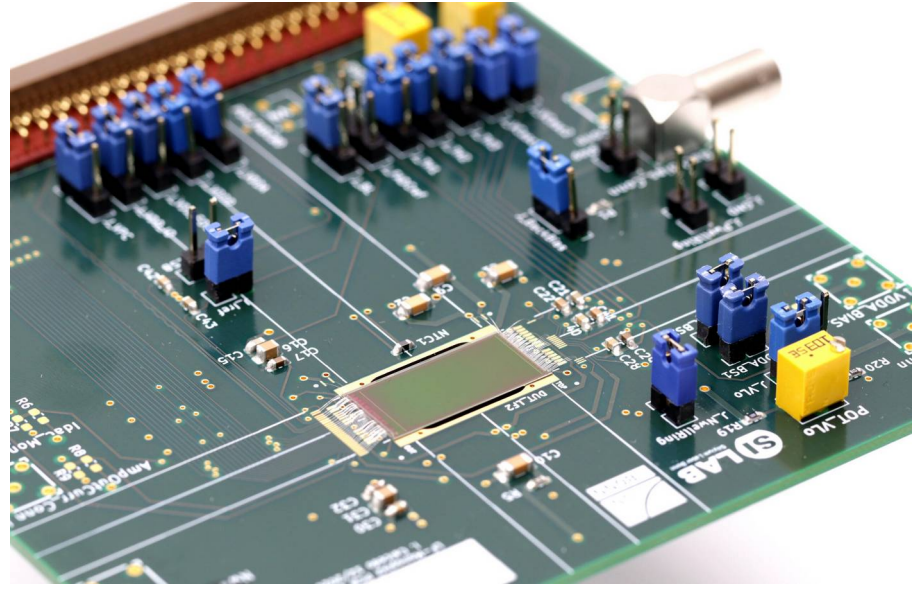
- Efficiencies at different bias voltages:
  - **Expected increase in efficiency for higher bias voltages** until full depletion of sensor
  - Efficiency results correlated to depletion depth profile w.r.t. bias voltage



Conclusion and Outlook

- **LF-Monopix2** fully functional and efficient after **irradiation to 1x10^{15} neq/cm^2**
  - Measured **hit detection efficiencies >99%** for all matrices

- **Upcoming**:
  - Irradiation to 2x10^{15} neq/cm^2 and further
  - Testbeam campaigns
  - TID measurements



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Thank you for your attention!

The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF)

This project has received funding from the European Union's Horizon 2020 Research and Innovation programme under GA No. 675587-STREAM, 654168 (AIDA-2020) and 101004761 (AIDA-Innova)

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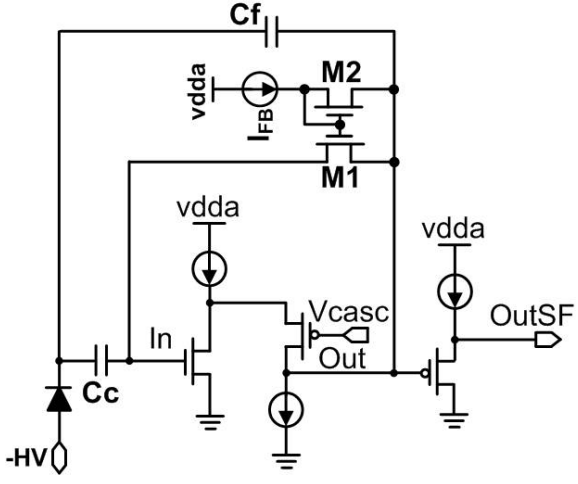
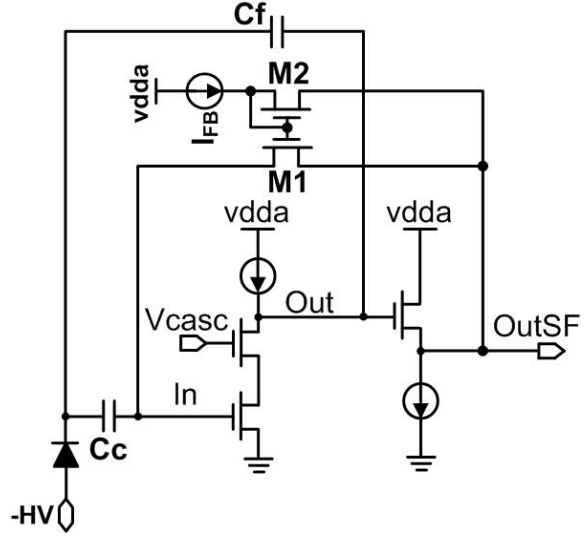
Backup

CSA Types of LF-Monopix2

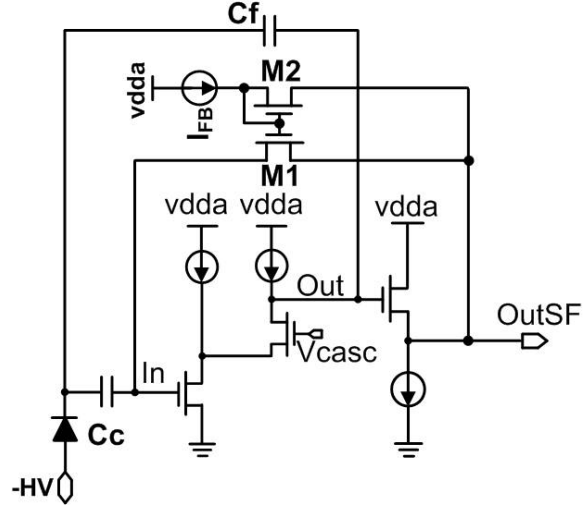
CSA 1
NMOS amplifier from LF-Monopix1



CSA 2
Telescopic cascaded structure

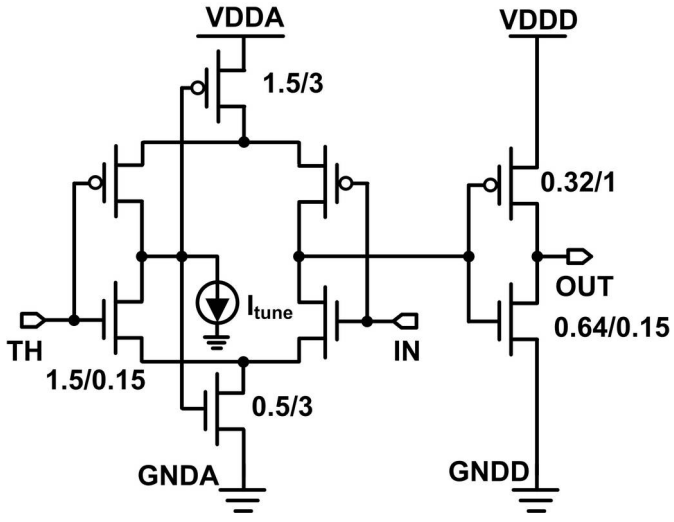


CSA 3
Current into input transistor from two separately adjustable branches

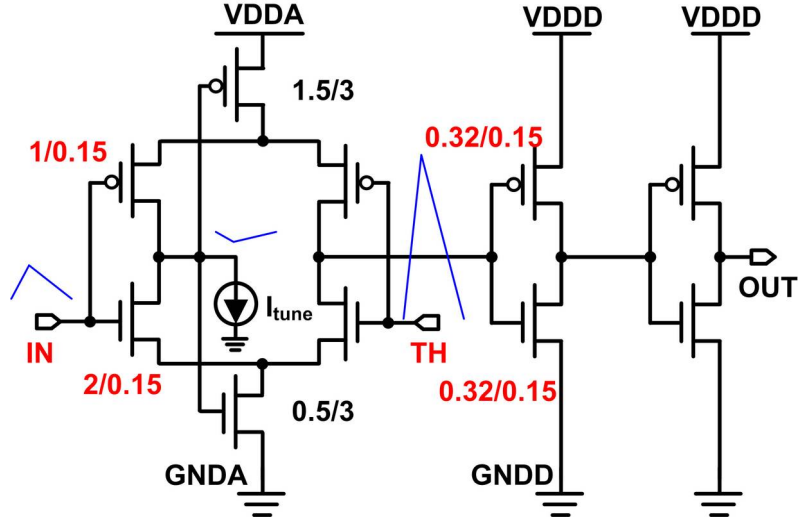


Discriminator Types of LF-Monopix2

Unidirectional
Self-biased differential amplifier followed by a CMOS inverter

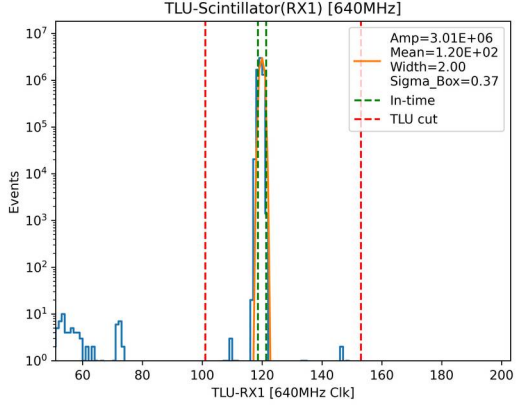


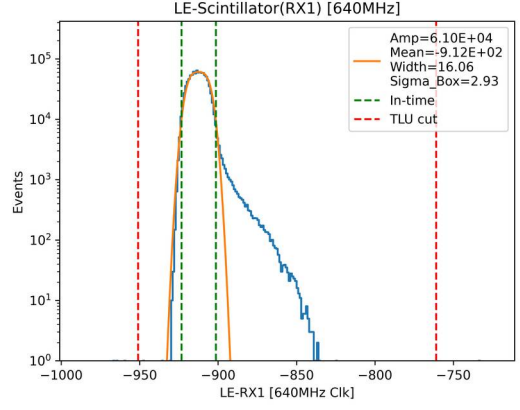
Bidirectional
Optimized transistor dimensions and swapped input ports for faster speed



Event Building

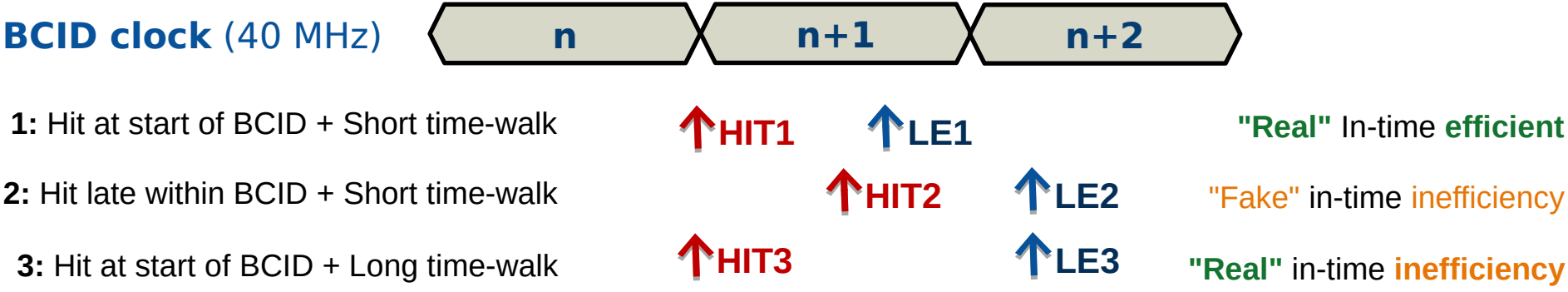
1. Match TLU640 with closest Scintillator and TLU timestamp in raw data
2. Look for most frequent frequent value and cut on it (both LF-Monopix2 and FE-I4 data)
3. Match TLU640 with closest DUT hit (leading edge) timestamp
4. Assign corresponding Scintillator timestamp to DUT hit





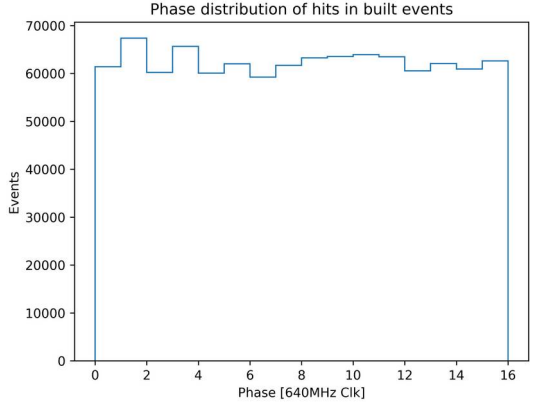
In-Time Events

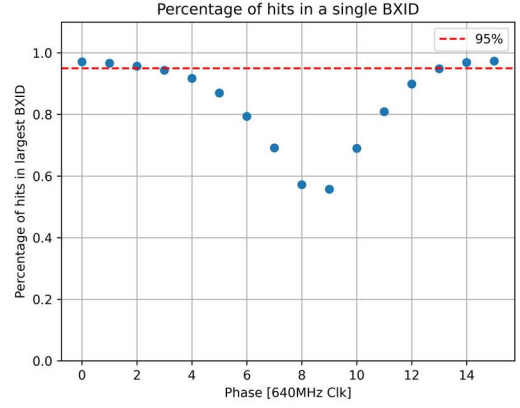
- LF-Monopix2 is **triggerless**
- Leading edges (LE) sampled at 40MHz (25ns)
- Look at the matched scintillator signals (640 MHz), and find the **time frame where most hits have its leading edge in a single BCID.**



In-Time Events

- Events are equally likely to come at any time within a single BCID
- Look at each 640MHz clock within 25ns and quantify percentage of hits in single BCID
- Take events of highest percentage hits in single BCID to analyze **in-time efficiency**
  - Due to jitter of TLU also take the phase before and after into account





In-Pixel Efficiency for Non-Optimal Operation

- Efficiency loss most prominent in pixel corners (expected)
  - Significant efficiency loss (<96%) already present at:
    - → **3ke⁻ mean treshold** @ 150V bias voltage
    - → **45V bias voltage** @ 2ke⁻ mean threshold