

High Voltage – Monolithic Active Pixel Sensors

detection and readout on one chip

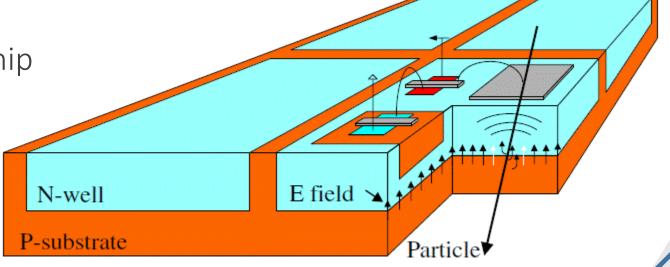
b in-pixel electronics

• high voltage:

b fast charge detection via drift

b large depletion area

commercially available processes



I. Peric, P. Fischer et al.: NIM A 582 (2007) 87

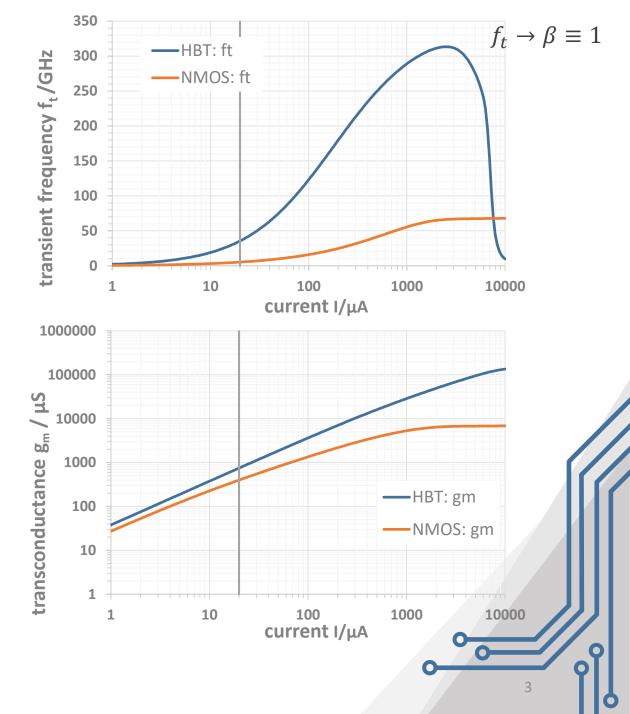
BiCMOS Process

- combines bipolar (HBT) and MOS transistors
 - allows to benefit from CMOS logic
- advantages of bipolar transistors:
 - **b** fast switching times
 - b large current gain

scales with current

Idea:

- → build HV-MAPS in a BiCMOS process
- → use single HBT to boost the performance of the in-pixel amplifier
- → achieve very good time resolution



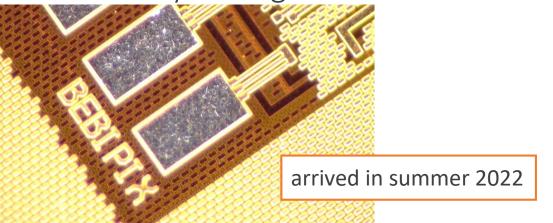
Existing Projects

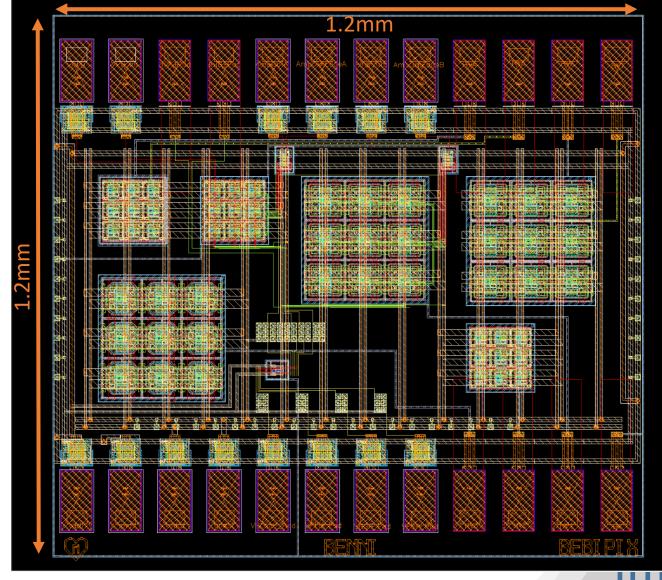
University of Geneva:

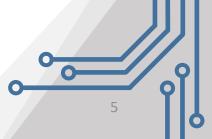
- general R&D chip: G. lacobucci et al., doi: 10.1088/1748-0221/17/02/P02019
 - **b** hexagonal pixels with $65\mu m$ side
 - **b** time resolution of $\sigma_t \approx 80 \ ps \ (I_{preamp} = 20 \mu A)$
- ASIC for the FASER experiment: s. Gonzalez-Sevilla, doi: 10.1088/1748-0221/18/02/C02002
 - b first test looking good
 - o no results for the time resolution published yet



- small test chip produced in the BiCMOS Process SG13G2 by IHP
- ◆ 2 active 3 × 3 pixel matrices, characterised in simulations
- focusing on a small pixel layout with in-pixel amplifier
- fully analog read-out



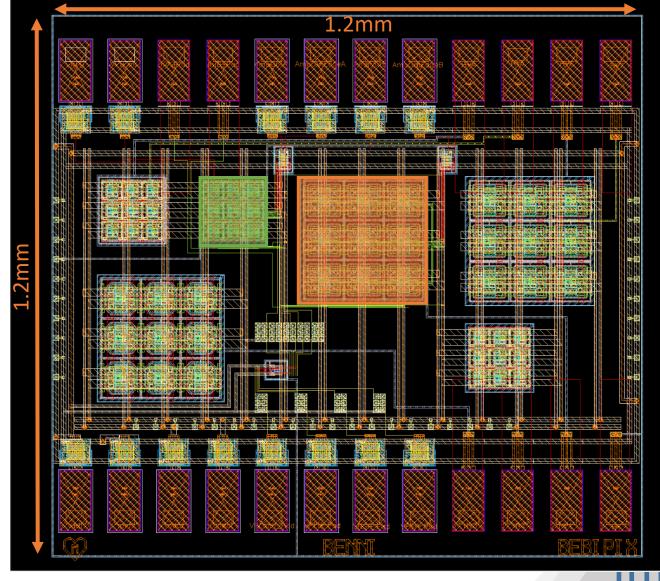


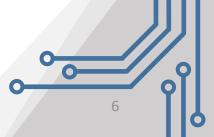




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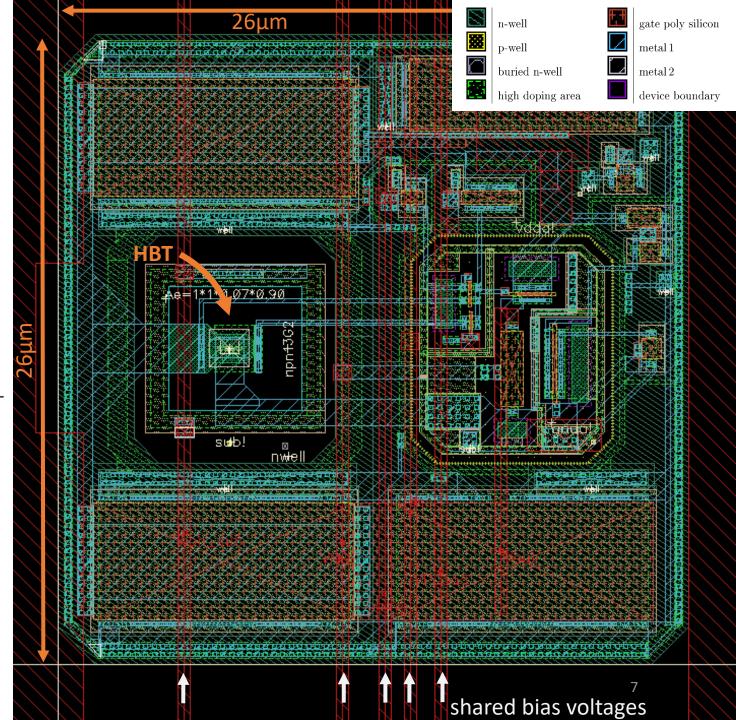
Small Pixel Layout

- implant size $26 \times 26 \mu m^2$
- pixel size $41 \times 41 \ \mu m^2$

Simulation results:

b input signal corresponding ≈ $2800 e^{-}$

Amplitude	$149.8 \pm 3.1 mV$
Rise Time	$741 \pm 340 \ ps$
SNR	27 ± 3.9
ToA Jitter	$481 \pm 33 \ ps$



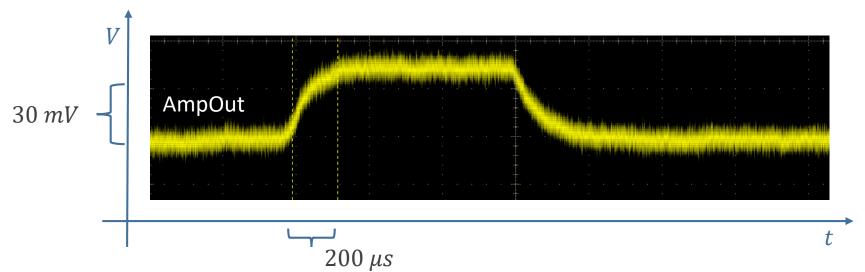
...However

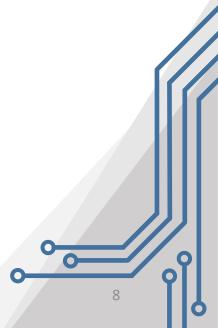
Problem 1: early breakdown

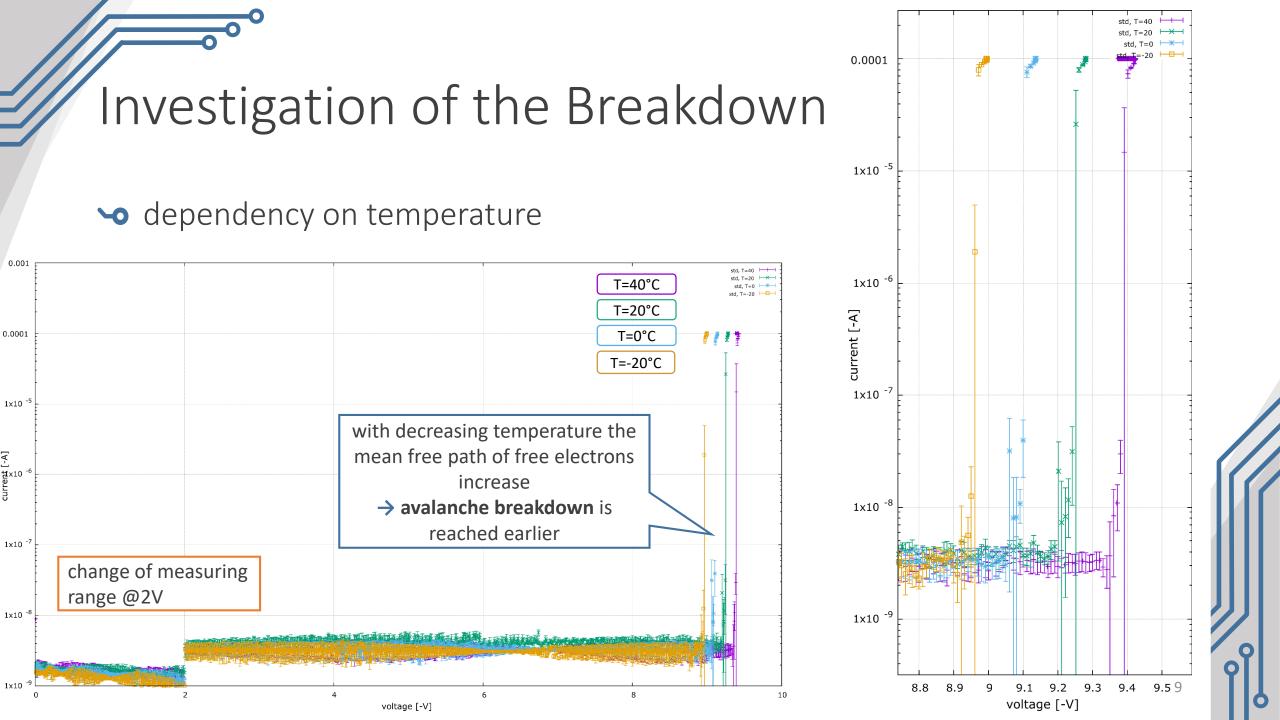
- expected $BDV \approx 90 V$ from TCad simulation
- measured $BDV \approx 10 V$

Problem 2: poorly functioning amplifier feedback

only slow and large input signals (from red laser) are visible

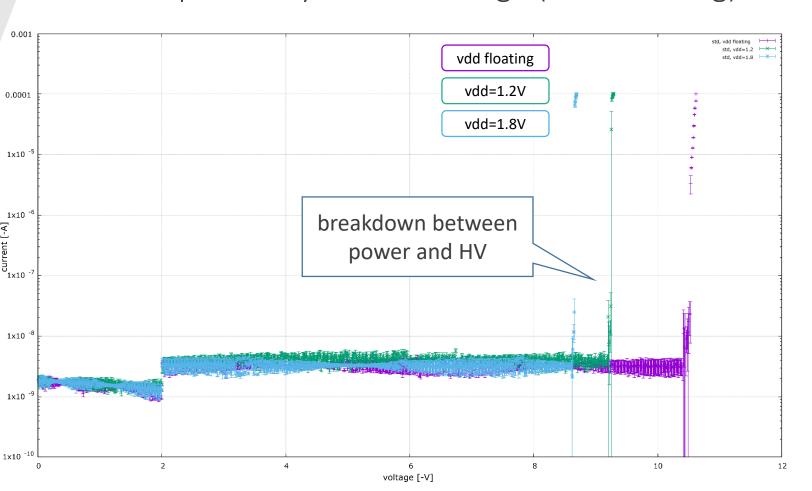


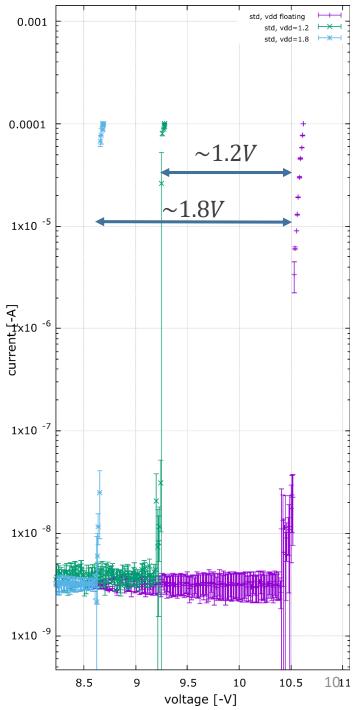




Investigation of the Breakdown

dependency on vdd-voltage (vdda floating)





Investigation of Breakdown

Light Emission Test (LET)

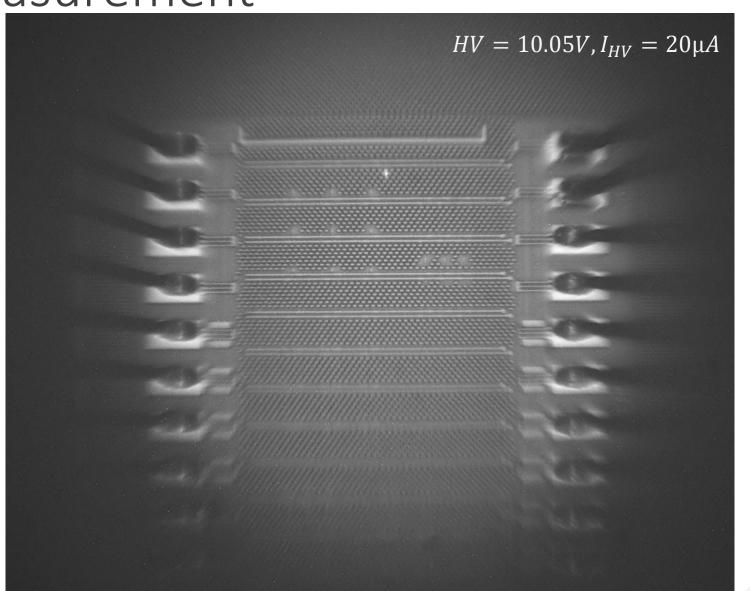
- opn-junctions at avalanche breakdown emits light
 - Intra-band transitions → mostly Bremsstrahlung
 - \triangleright Inter-band transitions \rightarrow e-h pair recombination
- light is emitted from localized spots, with highest electrical field
 - b increasing current results in an increasing number of spots

- → use CCD camera in light-tight box to capture emission
- → light spots indicate position of the breakdown

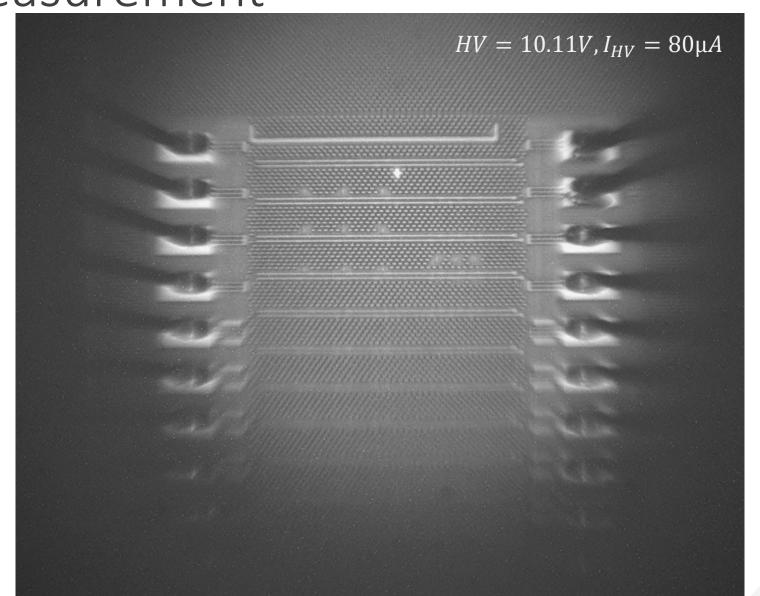
- > exposure of a part of the BeBiPix
- sensor breakdown: $BDV \approx 10.1 V$
- > LED is used to illuminate the sensor



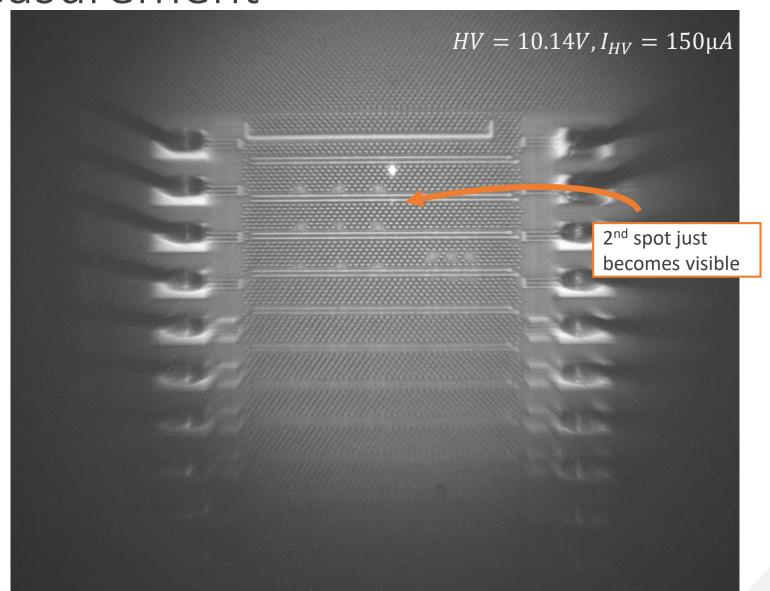
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- **b** 10min exposer



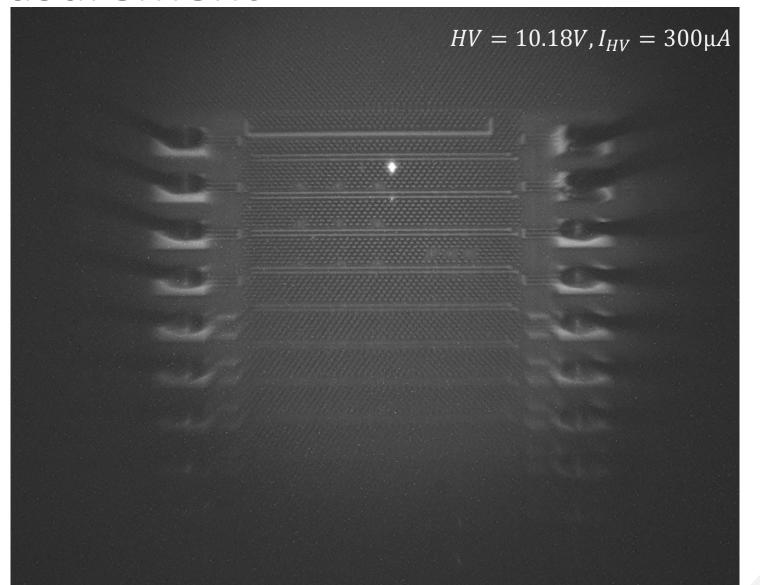
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- sensor breakdown: $BDV \approx 10.1 V$
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- exposure of a part of the BeBiPix
- sensor breakdown: $BDV \approx 10.1 V$
- **b** dim LED
- **b** 10min exposer

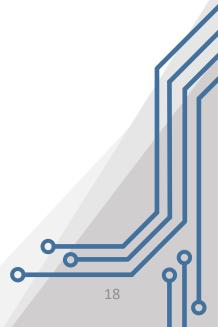


- exposure of a part of the BeBiPix
- sensor breakdown: $BDV \approx 10.1 V$
- **b** without LED
- **b** 30min exposure

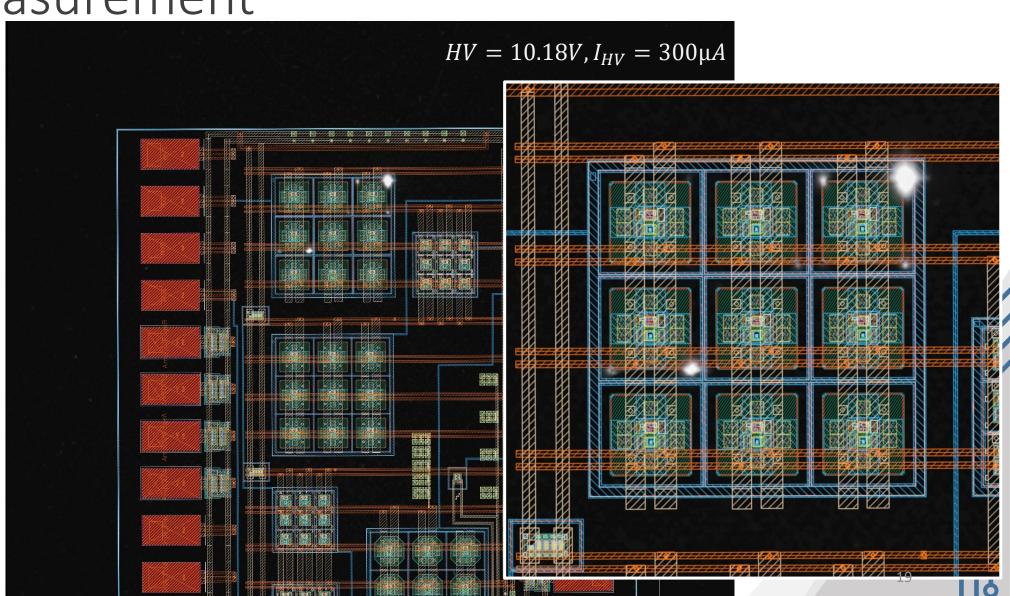


- exposure of a part of the BeBiPix
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- overlay layout





- exposure of a part of the BeBiPix
- sensor breakdown: $BDV \approx 10.1 V$
- **b** overlay layout



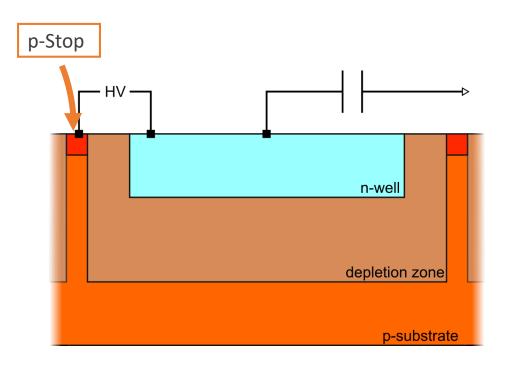
Early Breakdown

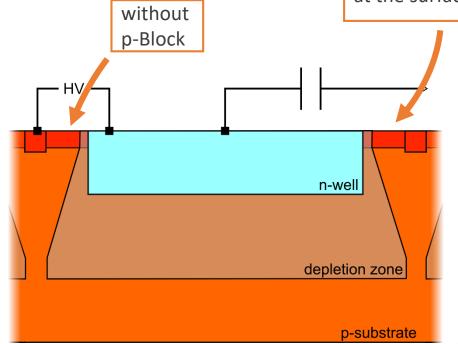
Most possible reason:

• p-Block layer was forgotten in layout

manufacturer places p-doping by default

high doping gradients results in high electric field at the surface





Summary

- combination of a BiCMOS Process with HV-MAPS is a promising concept
 - **b** simulation showed good results for the timing
- **⋄** BeBiPix has still several problems:
 - **b** early breakdown
 - poorly functioning amplifier-feedback: only slow signals visible
- next steps:
 - b use TCT-setup to investigate Signal response further