Fachhochschule
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High frequency DC/DC converters for future pixel detectors

Verbundmeeting Heidelberg

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Outline

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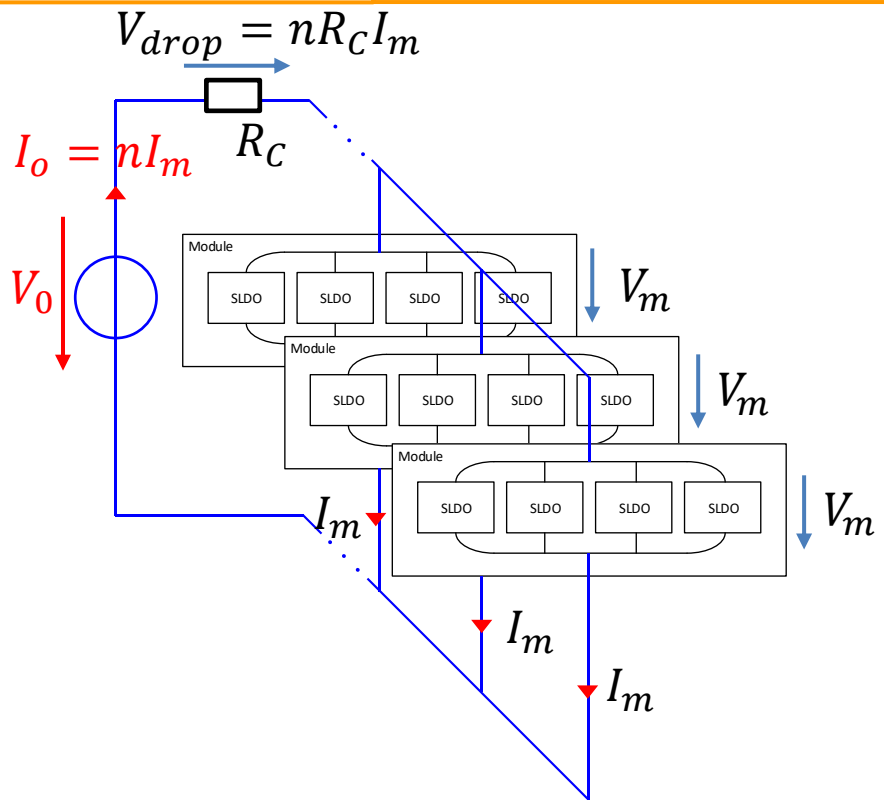
- Hybrid Converters

Introduction – New powering concepts for future pixel detectors

- Future pixel detectors aim for higher luminosity
- For the upcoming phase II upgrade of the ATLAS and CMS pixel detectors, an increased number of pixels is targeted
  - The increased number of pixels leads to a higher power consumption of the overall detector
  - At constant module voltage a higher supply current leads to higher I^2R losses
    - Target: Reduction of supply current to achieve a good overall efficiency

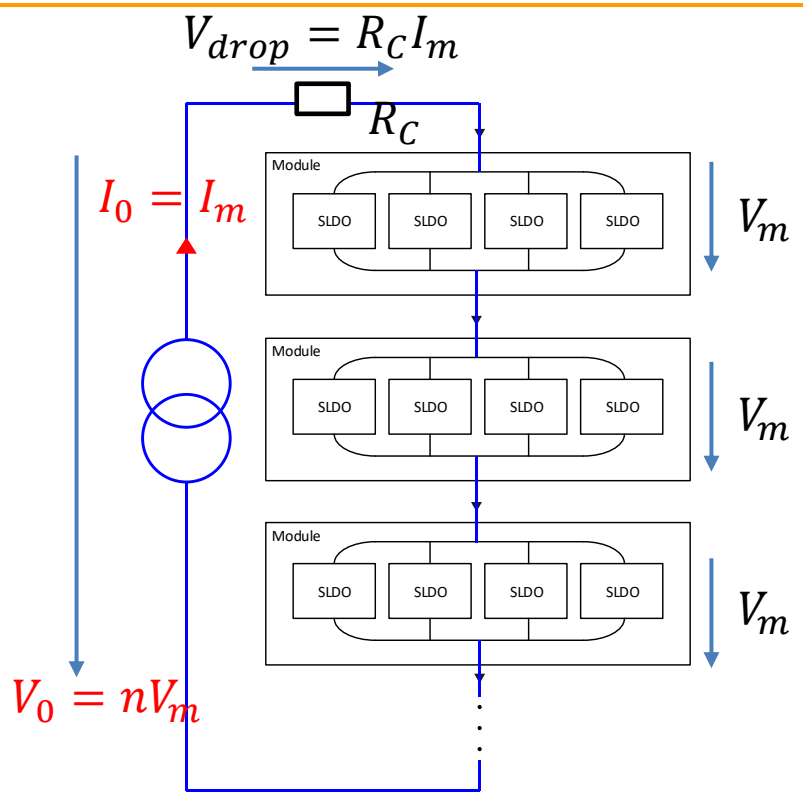
→ High interest for new innovative powering concepts

Parallel Powering vs. Serial Powering



- Modules are connected in parallel and powered by a constant voltage source
- Total supply current scales with the number of modules

$$\eta = \frac{1}{1 + n\frac{R_C I_m}{V_m}}$$



- Modules are connected in series chain and powered by a constant current source
- Total supply current is defined by maximum load current of a single module

$$\eta = \frac{1}{1 + \frac{R_C I_m}{nV_m}}$$

DC/DC converter requirements & challenges

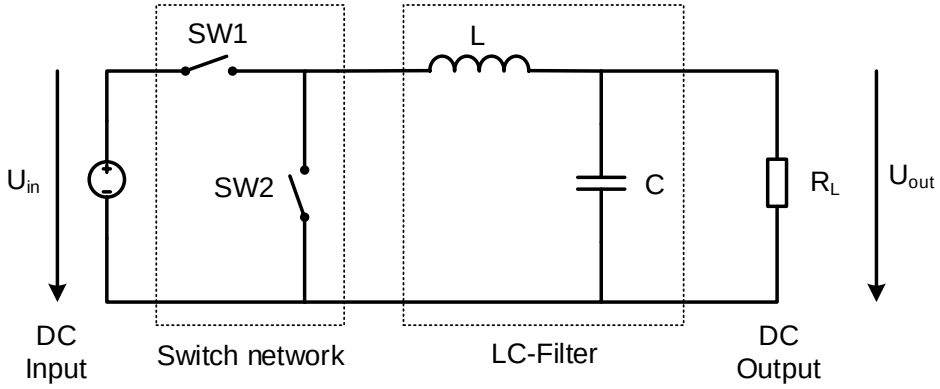
- A **total ionizing dose of up to 1 Grad** should be tolerated
  - Low voltage core transistors of a 65nm TSMC CMOS technology
- A **voltage conversion factor of 4** is targeted (input voltage is 4 times higher than module voltage)
  - For the realization of short module chains (3D sensor modules)

→ **Device Stacking necessary**

- **Space requirements:**
  - High magnetic field inside the detector: **Only bulky air coils** can be used for the inductor

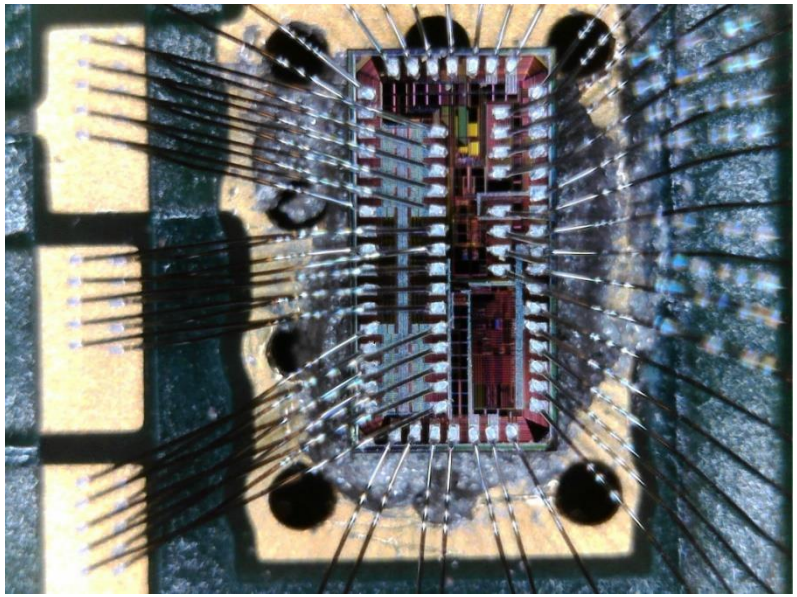
→ To meet the space requirements the inductance has to be reduced (reduced volume)

  - Operation at **high switching frequencies (Multi MHz)**



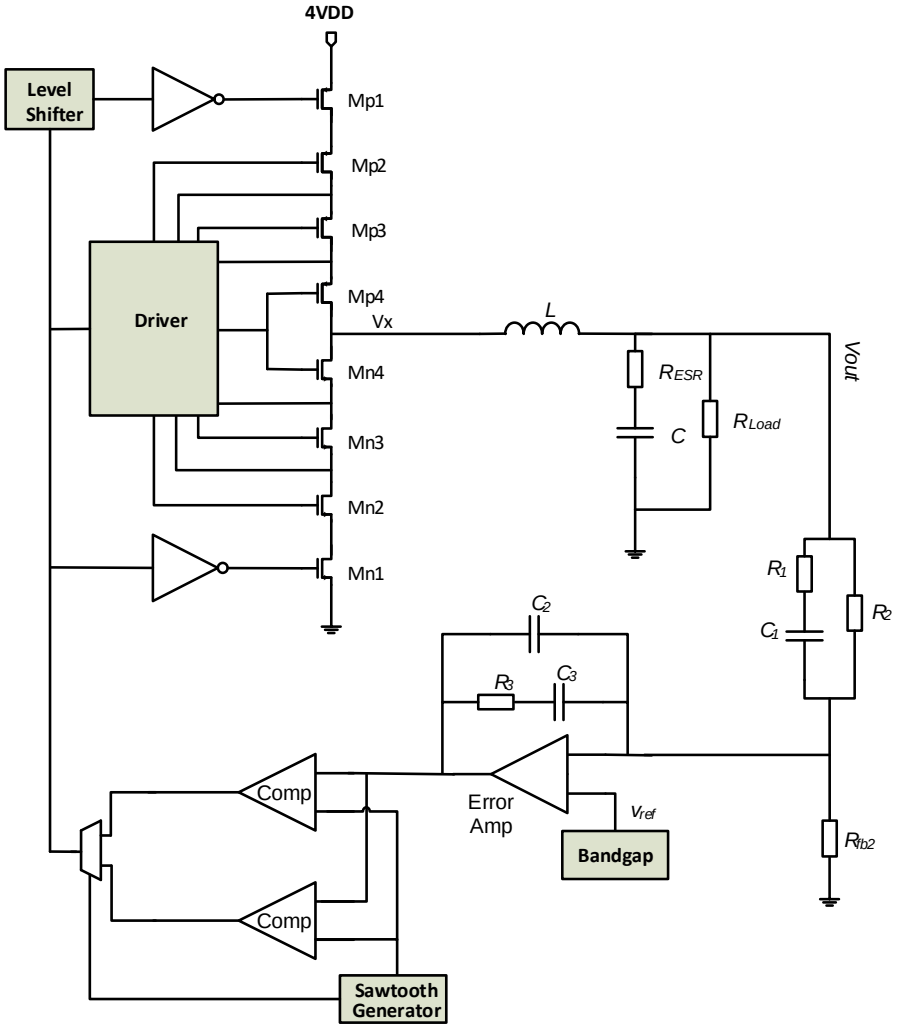
A high frequency DC/DC-converter (prototype)

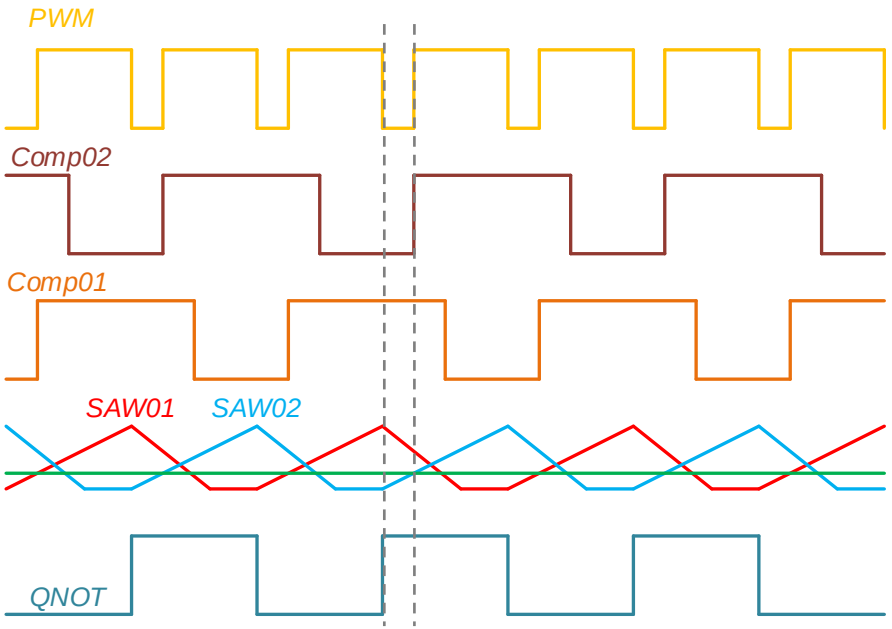
- TSMC 65nm
  - Low voltage core transistors (nominal voltage = 1.2V)
- Area: 1 x 2mm
- Switching frequency: 100MHz
- Input Voltage: 4.8V
- Output voltage: 1.2V
- Voltage conversion factor: 4
- Max. load current: 1A
- Passive components (off Chip)
  - Inductor L = 22nH
  - Capacitor C = 100nF



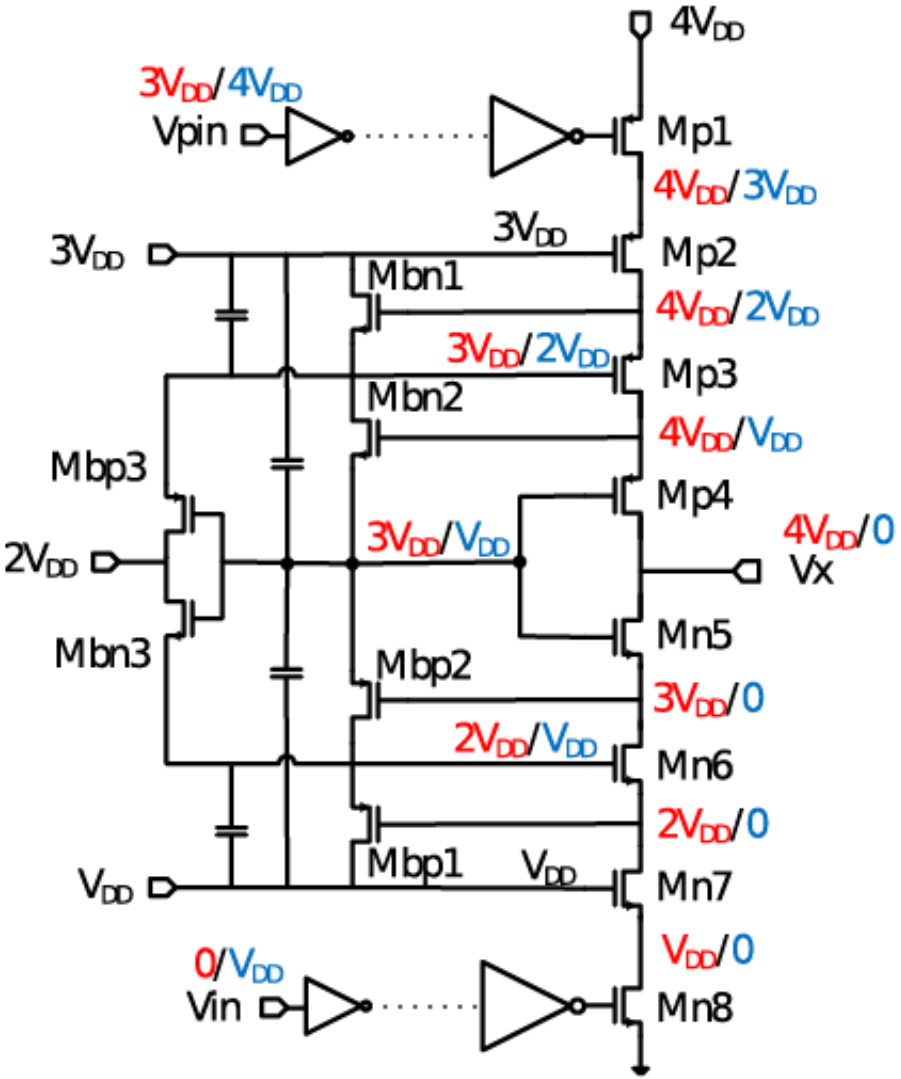
Prototype overview

- Voltage mode PWM control



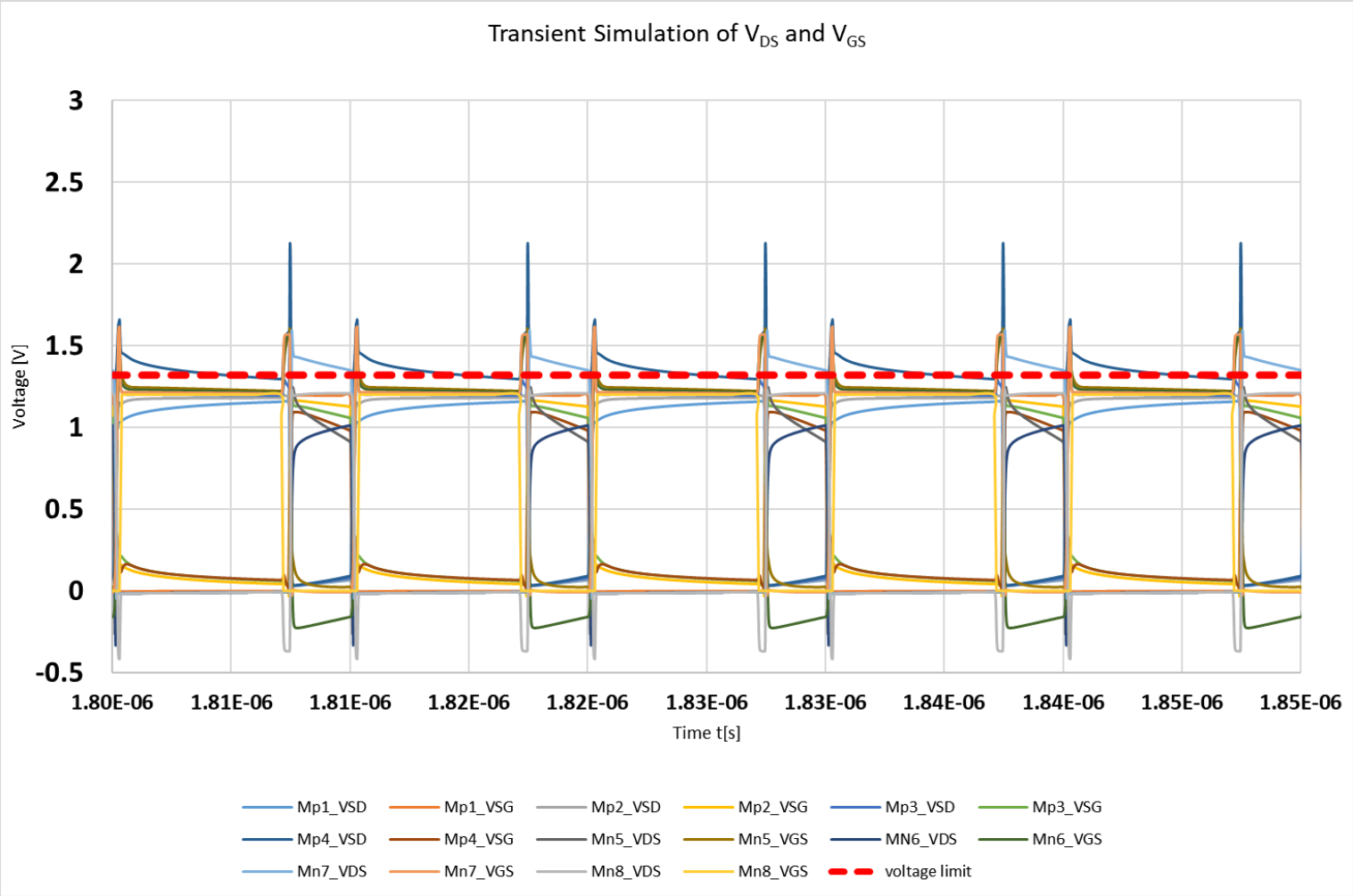


Device stacking of the switching stage

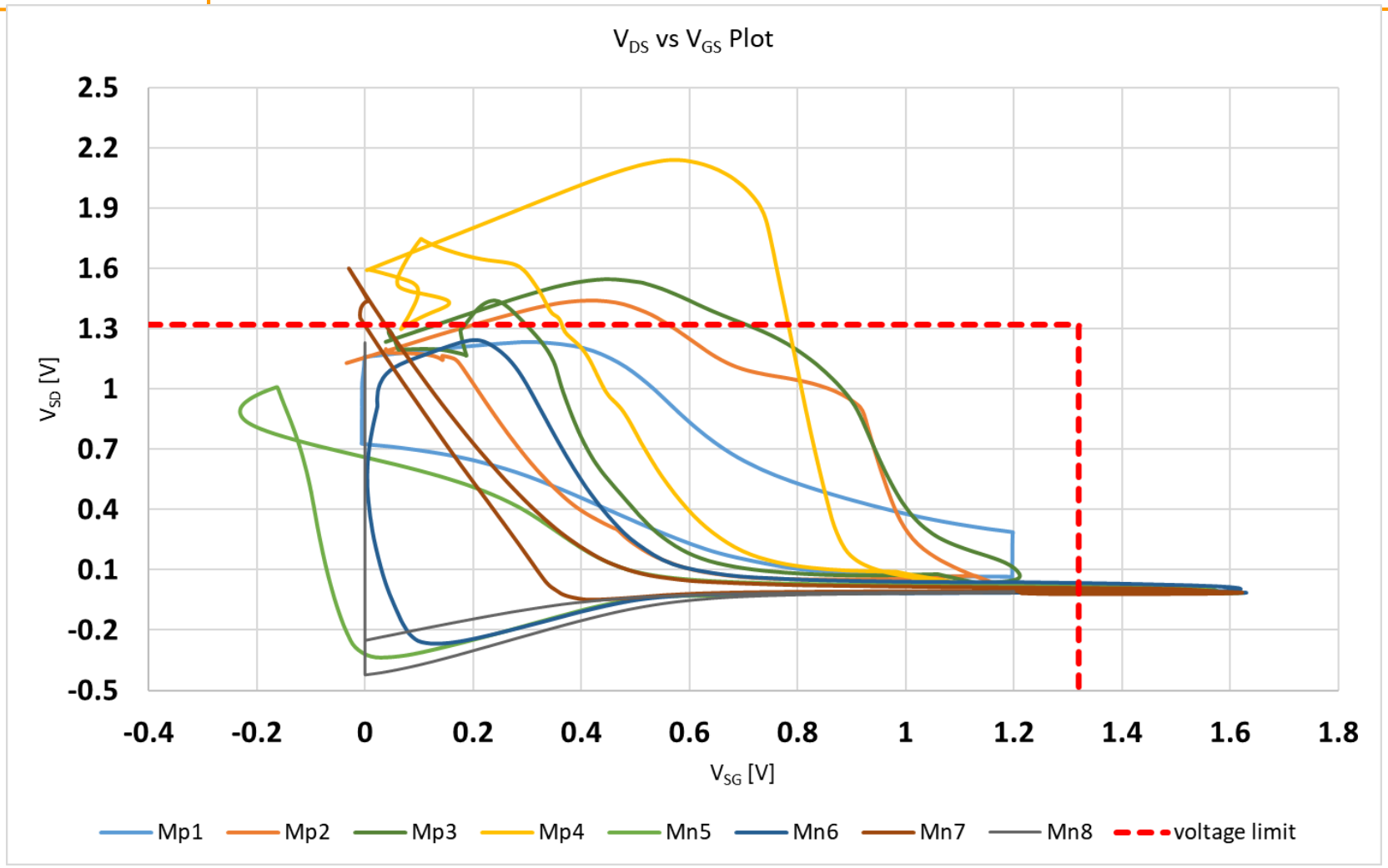


- 4 stacked PMOS and NMOS power devices
- Circuit switches between High state (red) and Low state (blue)
  - Control signals of Mp1 & Mn8 determine the state of the circuit
- Biasing network ensures safe operation of stacked transistors
  - Biasing network monitors drain potential of cascode devices and applies the required gate voltage
  - Ensures that cascode devices remain within their voltage limits
- Benefit: only two control signals necessary
- Drawback: voltage overshoots during switching moment (hot carrier effect)

Voltage overshoot during switching moment



Drain Source vs. Gate Source voltage of stacked devices



Improved Concept: J. Kampkoetter, M. Karagounis: Design and characterization of a cascode switching stage for high frequency radiation hardened DC/DC converters for the supply of future pixel detectors; Twepp 2022

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MEASUREMENT RESULTS

Sawtooth Oscillator (100MHz)

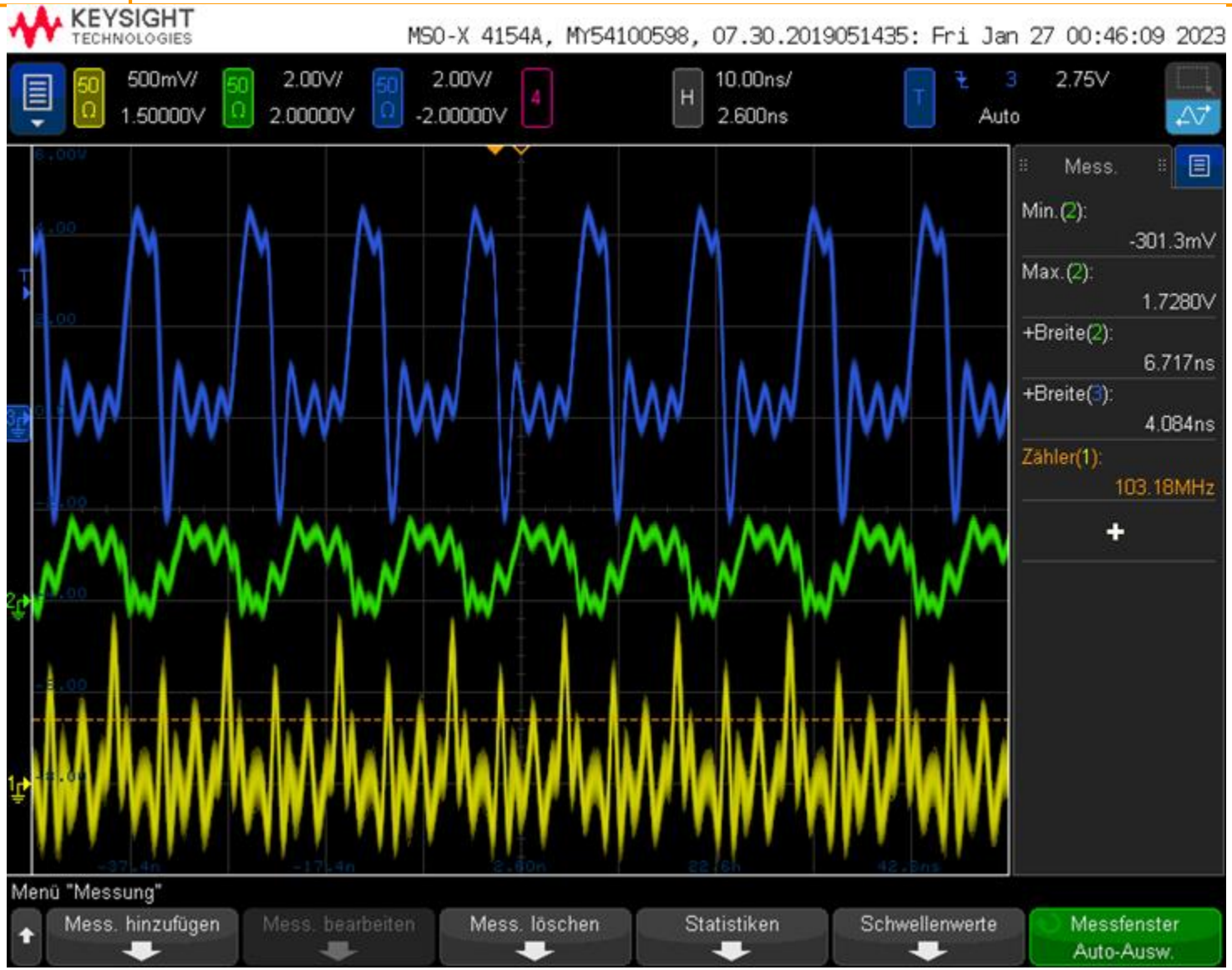
- Pulse signal becomes active as soon as ramp signal reaches its upper limit
  - Method for determining the switching frequency

Closed Loop Measurement (load current 100mA)

Vx

PWM

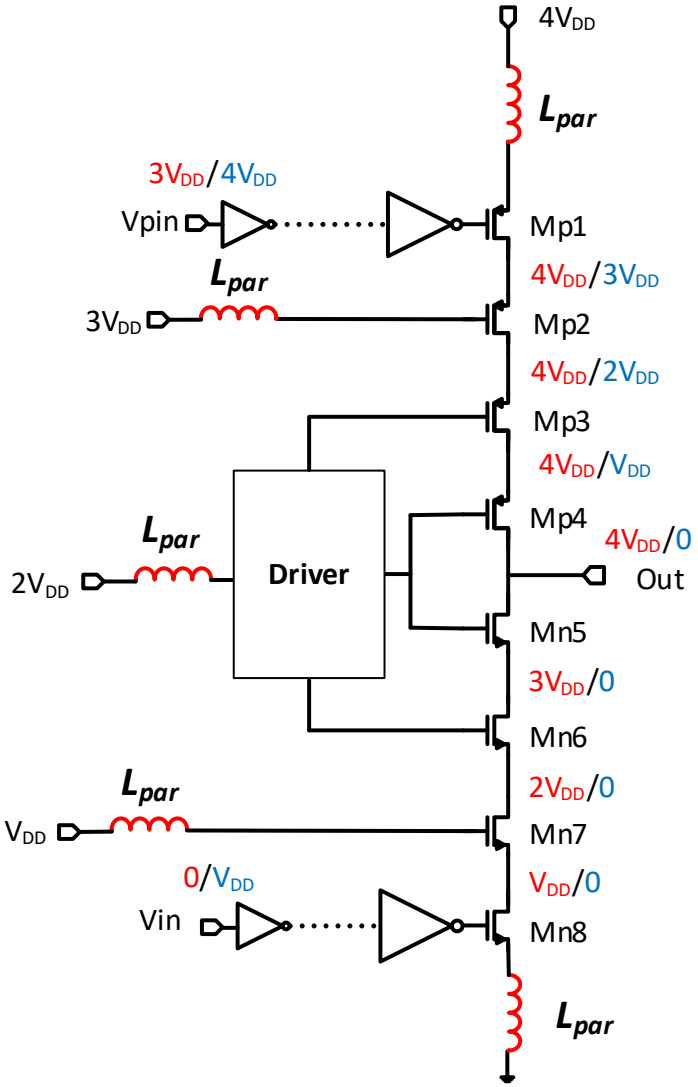
Oscillator



Parasitic effects of bond wires

- Fast switching of Mp1 and Mn8 (100 – 300ps)
  - To enable high frequencies and small duty cycles
  - Large power devices to handle high currents
- High current flow during switching action across bond wires
  - High di/dt
  - $\Delta v = L_{par} \frac{di}{dt}$
  - → Leads to increase or decrease of the supply voltages and ground bouncing
- Voltage limits of transistors can be exceeded!
- Incorrect switching behaviour!
  - Failure of whole system!

→ To avoid unwanted effects, it is necessary to take the influence of parasitic inductivities into account!!!



Measures to reduce parasitic inductances

- Adopted measures:
  - Several bond wires in parallel for critical current paths
    - Reduces total inductivity
  - Bond wires as short as possible
  - On Chip Decoupling caps for supply connectors (range of 100 – 200pF)
  - OFF-Chip Decoupling close to the chip

→ Recent measurements show that the measures are not sufficient for the entire load range!

- Potential measures for future prototypes:
  - Larger on chip decoupling caps (range of 1…4nF)
    - Drawback: Consume a large area of the chip
  - Bump Bonding
    - Reduces influence of parasitic effects by a factor of 10 compared to the use of bonding wires

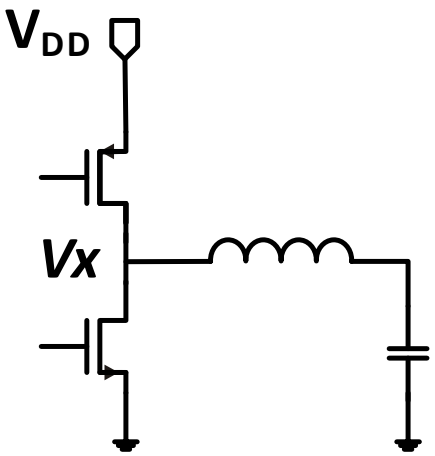
Future plans

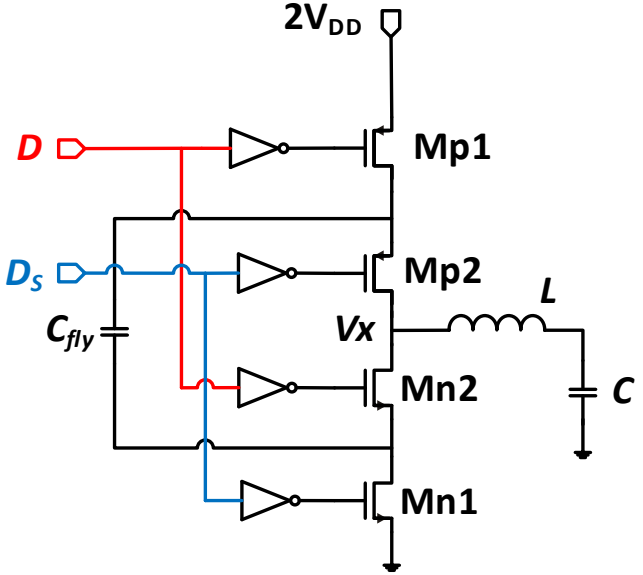
HYBRID CONVERTERS

Hybrid Converter

- Combine positive properties of capacitive and inductive switching converter
- **Goal:** Better utilization of passive components (reduction of their volume)
- Compared to conventional buck topologies hybrid converter reduce the size of magnetic components
  - Decreasing the volt second (Vs) balance product
- Compared to pure switched capacitor topologies:
  - Reduced charge sharing losses
- Wide range of different topologies: Series Parallel, N-Level Buck, Dixon …
  - Many ways to configure switches and passive components
- Multimode operation
  - Resonant (soft switching, reduces switching losses)
  - Inductive

2-Level Buck Converter (conventional) vs. 3-Level Buck Converter





- Additional Flying Capacitor
- Higher blocking voltage (2VDD)
- Up to ¼ lower current ripple at the inductor (smaller voltage drop)
  - Lower inductance or lower frequency
- 4 switching phases instead of 2: Effectively uses twice the frequency
  - Lower output voltage ripple

→ High potential for future applications

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Thank you for your attention!