Wireless Transfer

Towards a 60 GHz Multi-Gigabit system-on-chip

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OUTLINE

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- **Motivation**
- **Why is the 60 GHz band so Attractive?**
- **Technologies for 60 GHz Applications**
- **60 GHz Transceiver Building Blocks issues**
- **3-D Opportunity**
- **Preliminary timeline**
- **Summary**

OUTLINE

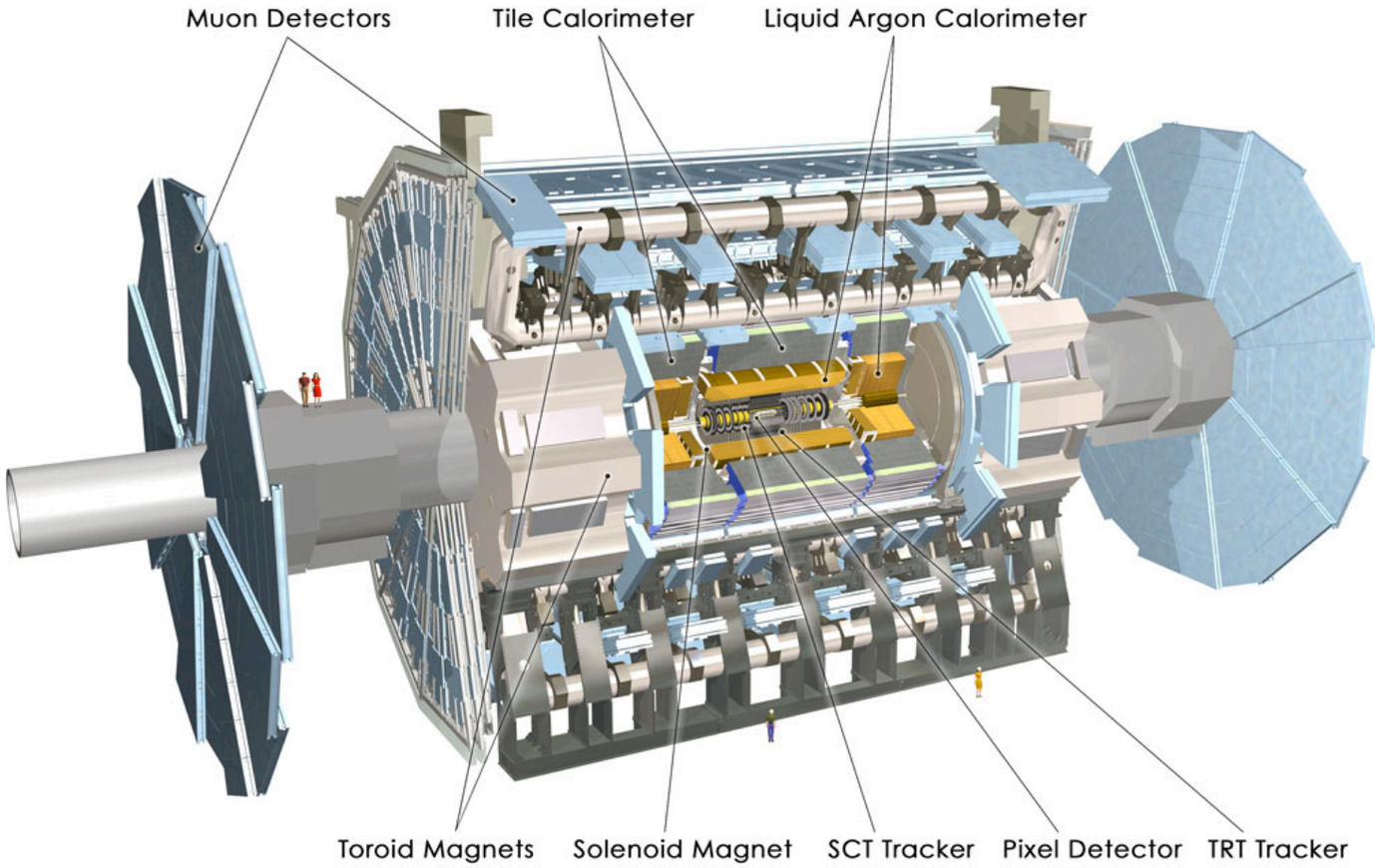
MOTIVATION

The two multi-purpose experiments ATLAS and CMS consists of several million channels and the amount of data that can be transferred from the highly granular tracking detectors is today limited by the available:

- **Bandwidth**

which again is limited by

- **Power budget**
- **Mass**
- **Space**



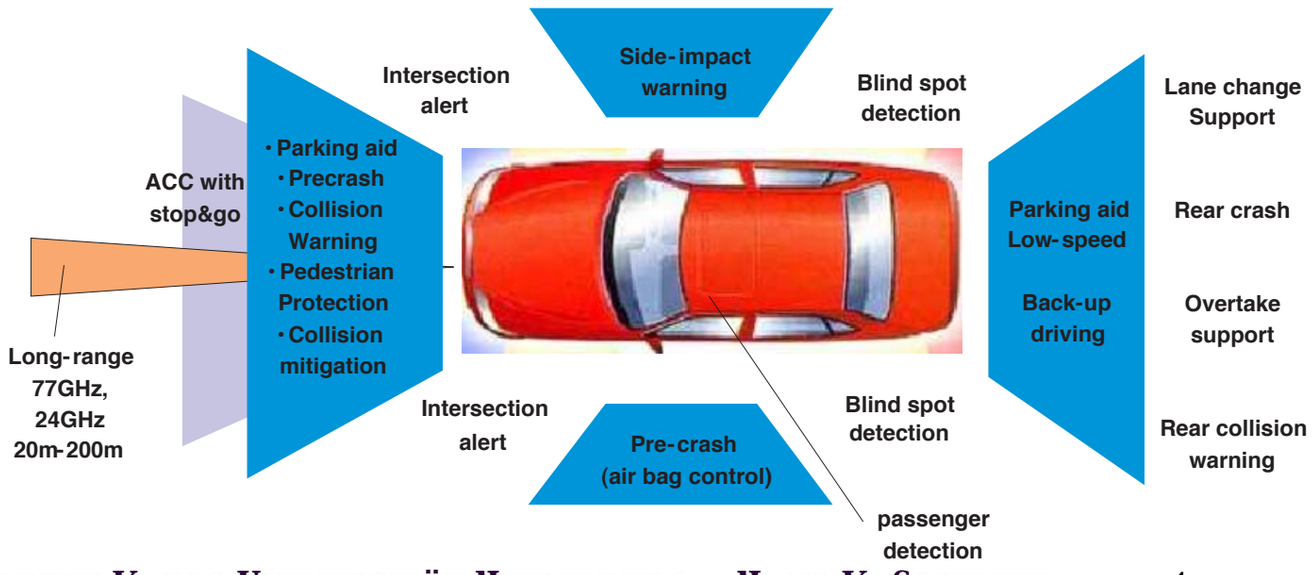
Can the 60 GHz band be the solution?

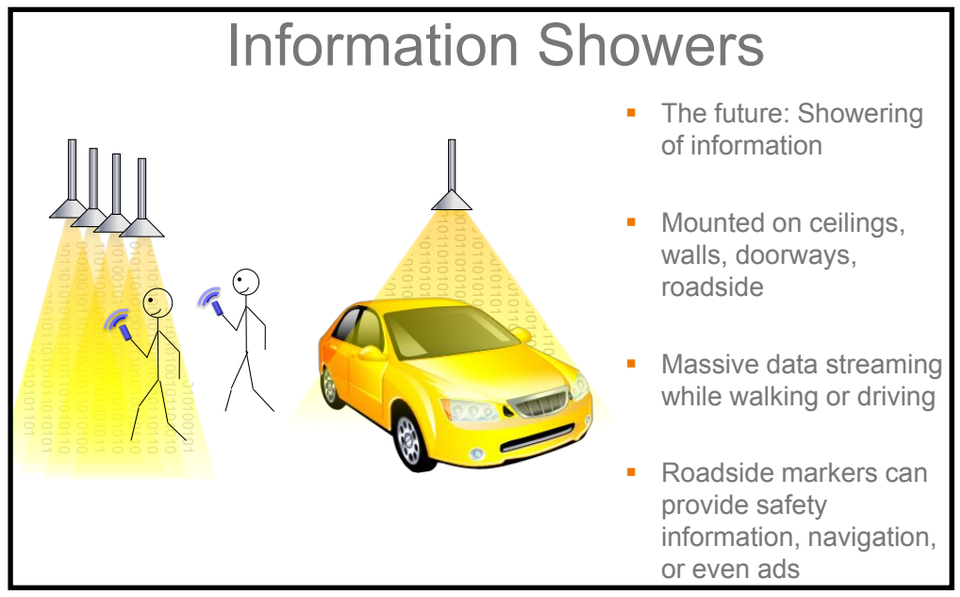
Why is The 60 GHz Band so attractive ?

In 2001, the Federal Communications Commission (FCC) allocated 7 GHz in the 57-64 GHz band for unlicensed use world wide.

The mm-wave frequency range is very attractive for various applications for a number of reasons:

- **Data rates and bandwidth are never enough**
- **Uncompressed video of high definition multimedia interface (HDMI)(2Gb/s)**
- **High speed file transfer among electronic devices and laptops**
- **Fast movie or video game down load from kiosk**
- **And now the High Energy Physics area**





MOTIVATION

A solution to this challenge could be the use of the MilliMeter Wave (MM-Wave) technology at 60 GHz

- **Offers Wireless unlicensed spectrum of 7 GHz bandwidth available world-wide.**
- **Largely unused today (low interference probability)**
- **60 GHz does not penetrate walls (security)**
- **Able to send Gigabits/s of information over local area (about 10m)**
- **Inherent atmospheric attenuation near 60 GHz, due to oxygen absorption**
- **High transmit power. 40 dBm EIRP (Effective Isotropic Radiated Power) allowed in most regions.**

MOTIVATION

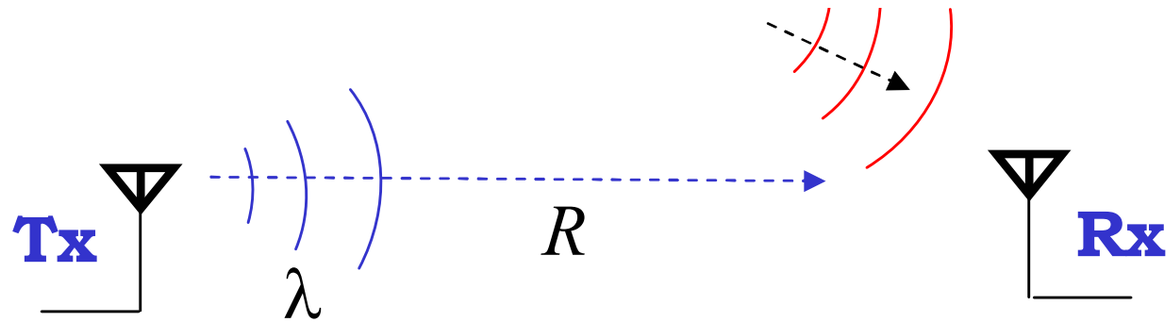
- **Traditional transceiver circuits in 60 GHz implementations exist**
- **Recent improvements in Silicon based Technologies**
- **Small component size**
- **Allow for integration of antenna(s)**
- **Flexibility of placement**
- **Do not need cables**

CHANNEL PERFORMANCE

The main challenges for a 60 GHz channel is as follows:

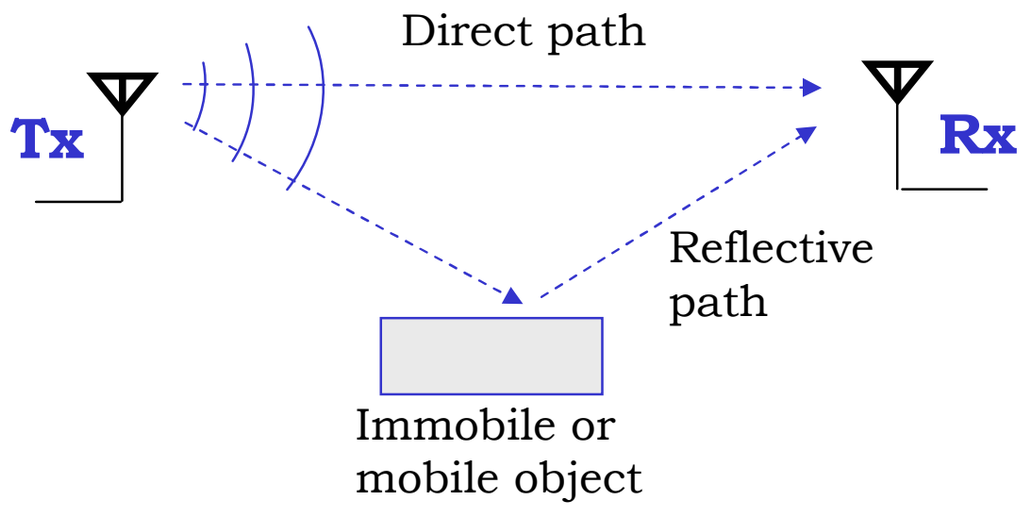
- **High loss from the Friis equation**

$$Power_{RX} = \frac{Power_{TX} \cdot Gain_{TX} \cdot C^2}{Distance \cdot Frequency}$$



Power loss in open area: $L_p = 20\log(4\pi R/\lambda)\ [dB]$

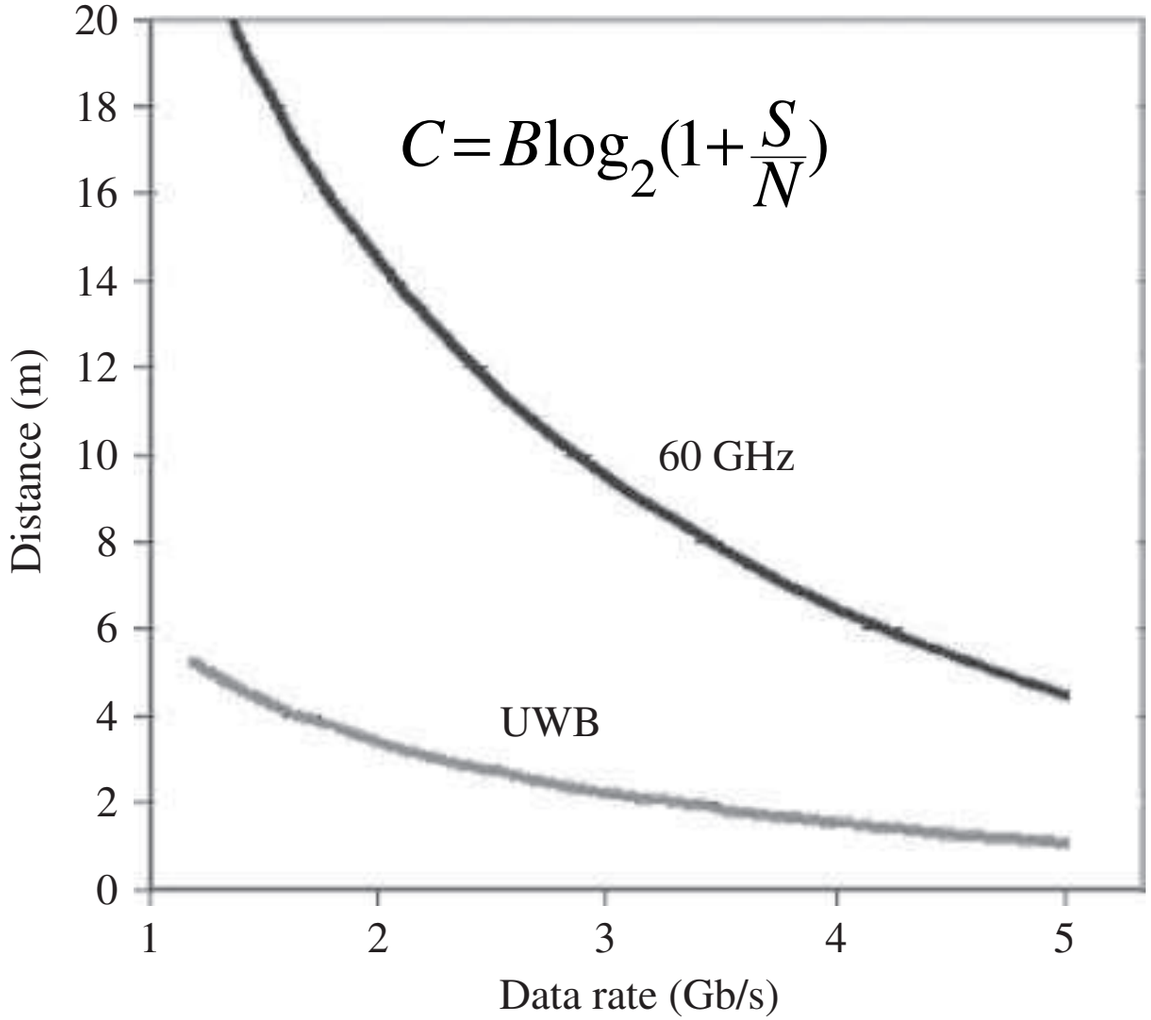
- Multipath and fading



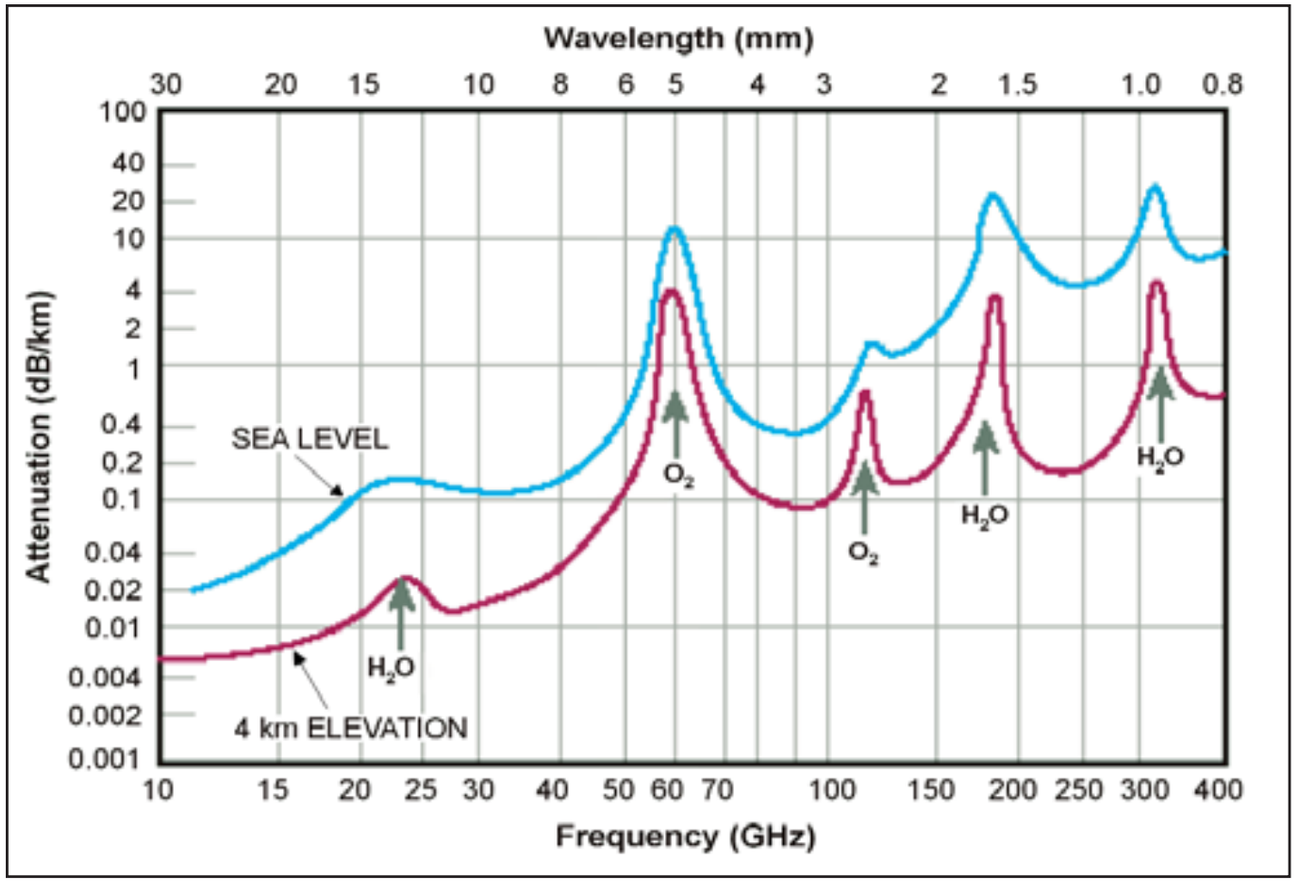
CHANNEL PERFORMANCE

To support Multi-gigabits/s data transfer, the channel need large bandwidth B and large allowable signal power S.

Shannon's theorem



Oxygen attenuation



Key Challenges for (CMOS) Millimeter-Wave Design

- **Lossy/conductive substrate → poor isolation and lower Q components**
- **High dielectric constant** $\varepsilon_r = 11.7$
- **Eddy current and skin-depth (Ohmic loss) effect.**
- **For on-chip antenna, considerable portion of the electromagnetic energy would be sucked into the substrate.**
- **Thin gate oxide and low carrier mobility constant**
- **Low breakdown voltage**
  - **Difficult to deliver high output power (low supply and break-down voltage).**
- **LNA, PA and VCO's difficult to design**
- **Benefits of using CMOS technology lies in the existing infrastructure**

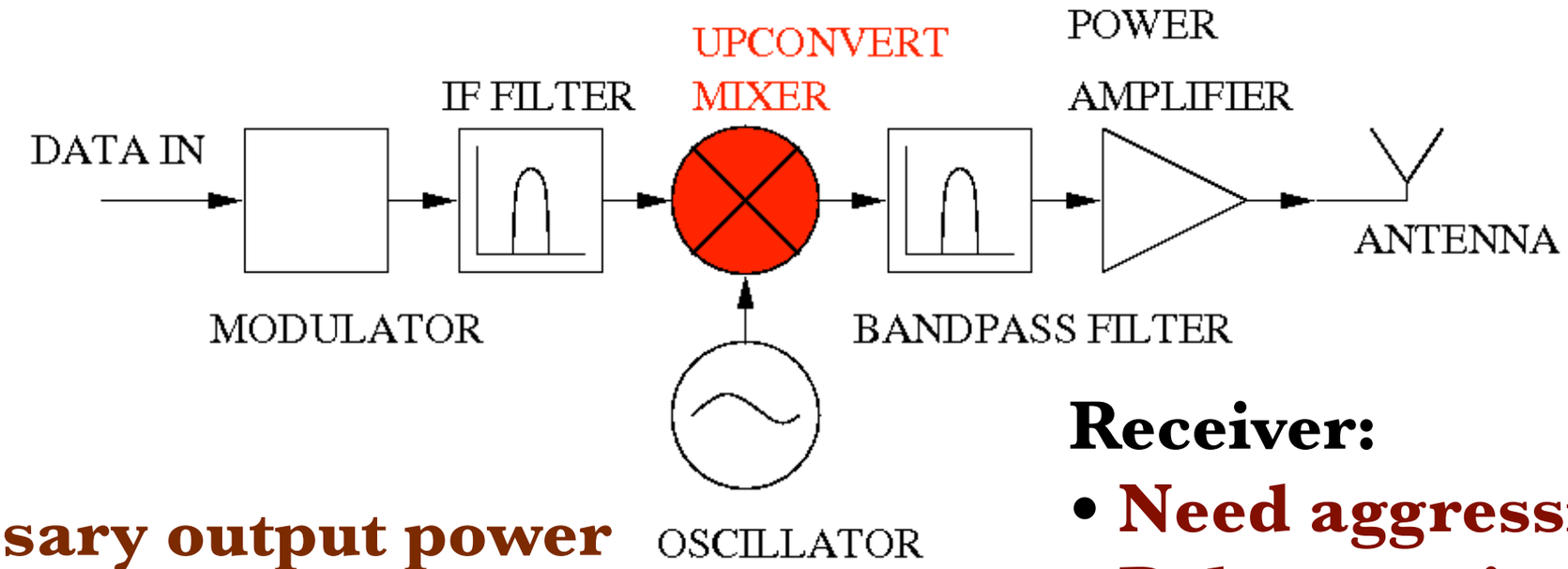
For the circuit designer, using CMOS to design millimeter wave circuits are extremely challenging

IMPORTANT ADVANTAGES SIGE HBT HAS OVER CMOS

- **For equal performance, SiGe requires less aggressive lit.(2gen.)**
- **130 nm SiGe cost less than 65 nm CMOS**
- **Higher BV at fixed performance**
- **gm/um^2 is much larger for SiGe HBTs (need big MOSFETs for high f_{max})**
- **Noise**
- **Modeling of SiGe HBTs is easier for high frequency design (first time pass)**
- **Strength: Offer advantages of both conventional silicon bipolar and silicon CMOS. Not possible for other technologies.**
- **Have built-in total dose radiation hardness (ATLAS ?)**

60 GHz Transceiver System

Transmitter



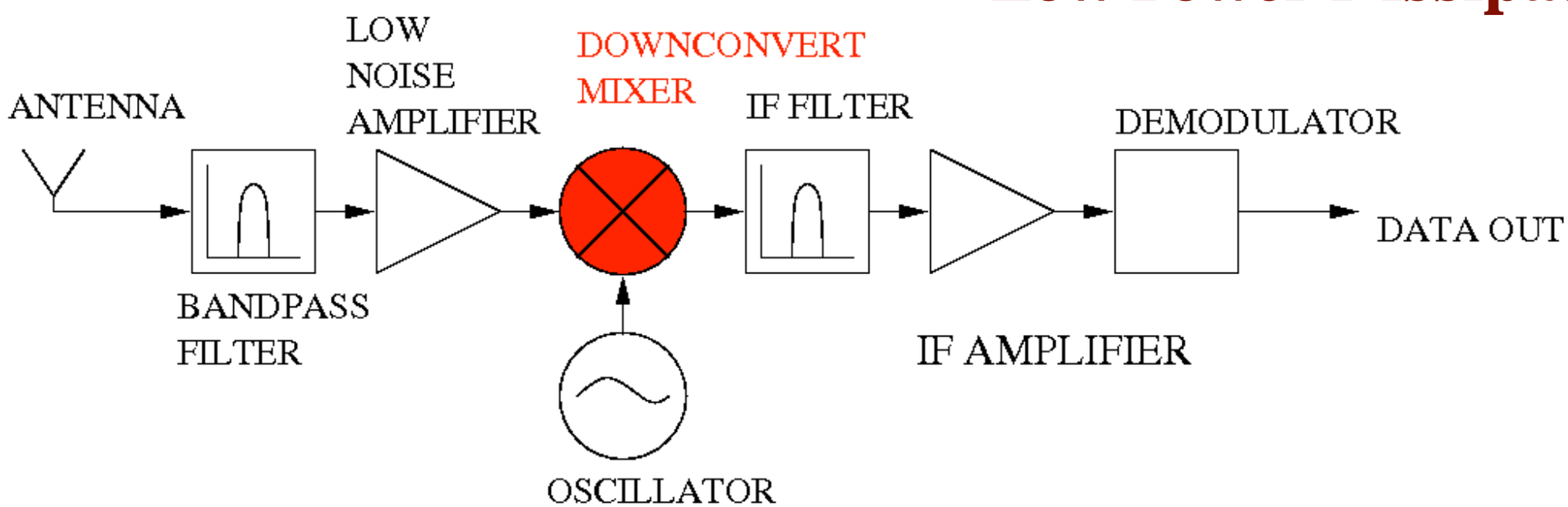
Transmitter:

- **Deliver necessary output power**
- **High power efficiency**
- **High gain and stability**

Receiver:

- **Need aggressive LNA**
- **Balance gain, linearity and NF**
- **Low Power Dissipation**

Receiver



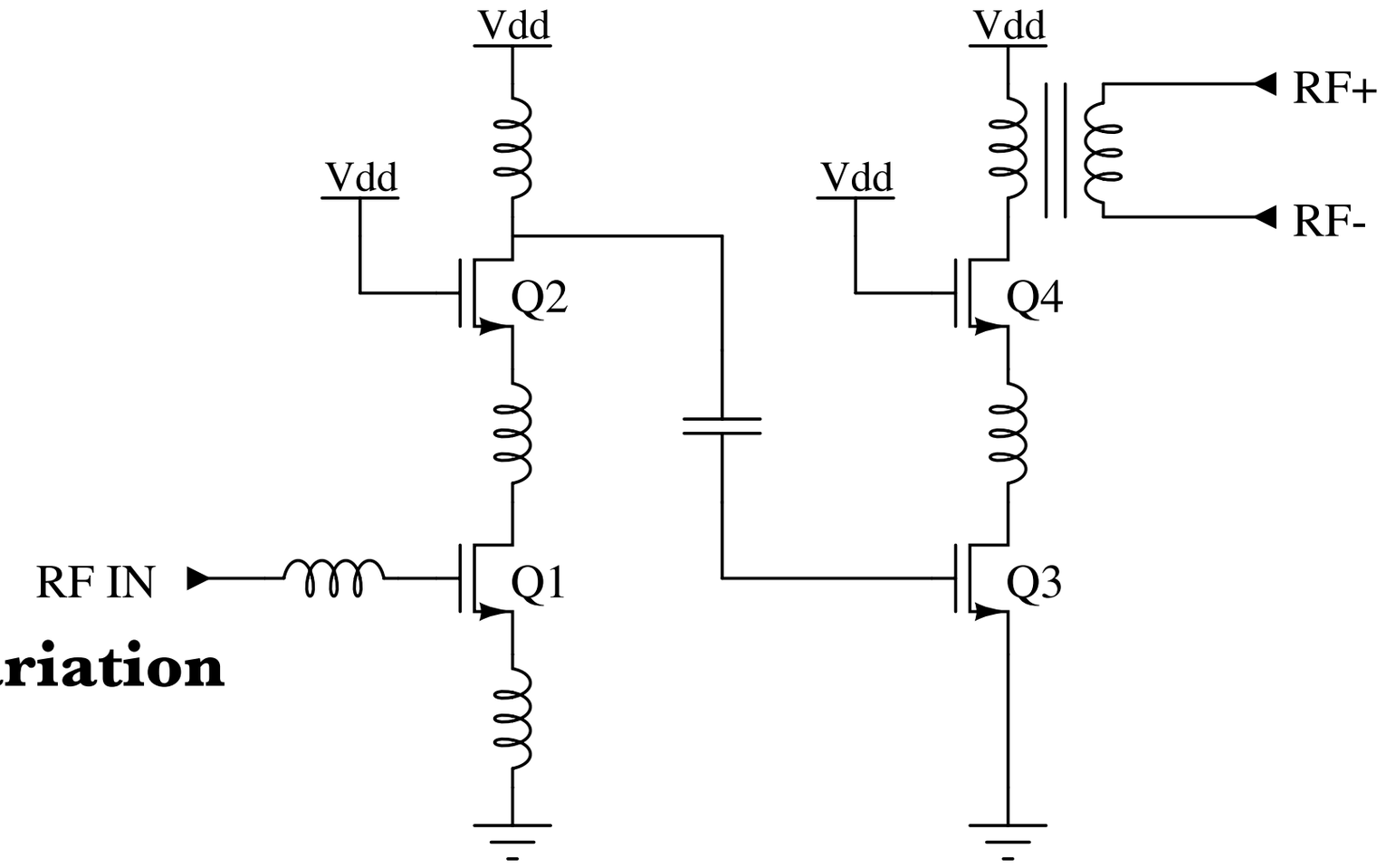
Why ON-Chip Antennas?

- **Millimeter-Wave signals have small wavelengths at 60 GHz (5mm)**
  - **Possible to integrate receive and transmit antenna(s) on-chip.**
- **High directivity is desired to improve S/N-ratio, reduce power consumption and to reduce inter-use interference.**
- **High dielectric constant in Silicon (11.7)**
- **Multiple metal layers on ICs available**
  - **Can be used to fabricate mm-wave antennas.**
- **Eliminate cable/connectors loss**
- **No need for high-frequency electrostatic discharge protection.**
- **Save PCB real estate**
- **Reduce fabrication costs**

ON-Chip antennas fabricated in standard CMOS technology with no changes to the process steps appear to suffer from a low efficiency.

Low Noise Amplifier issues

- **Power dissipation**
- **Noise Figure**
- **Linearity**
- **Stability**
- **Impedance matching**
- **Power gain**
- **Bandwidth**
- **Insensitive to process variation**



Three Fundamental differences compared to the lower frequency colleague:

1. **Transistors operate much closer to their cut-off frequency**
2. **Parasitic elements represent a much larger portion of the total impedance**
3. **Signals with small wavelengths results in distributed effects within the circuit**

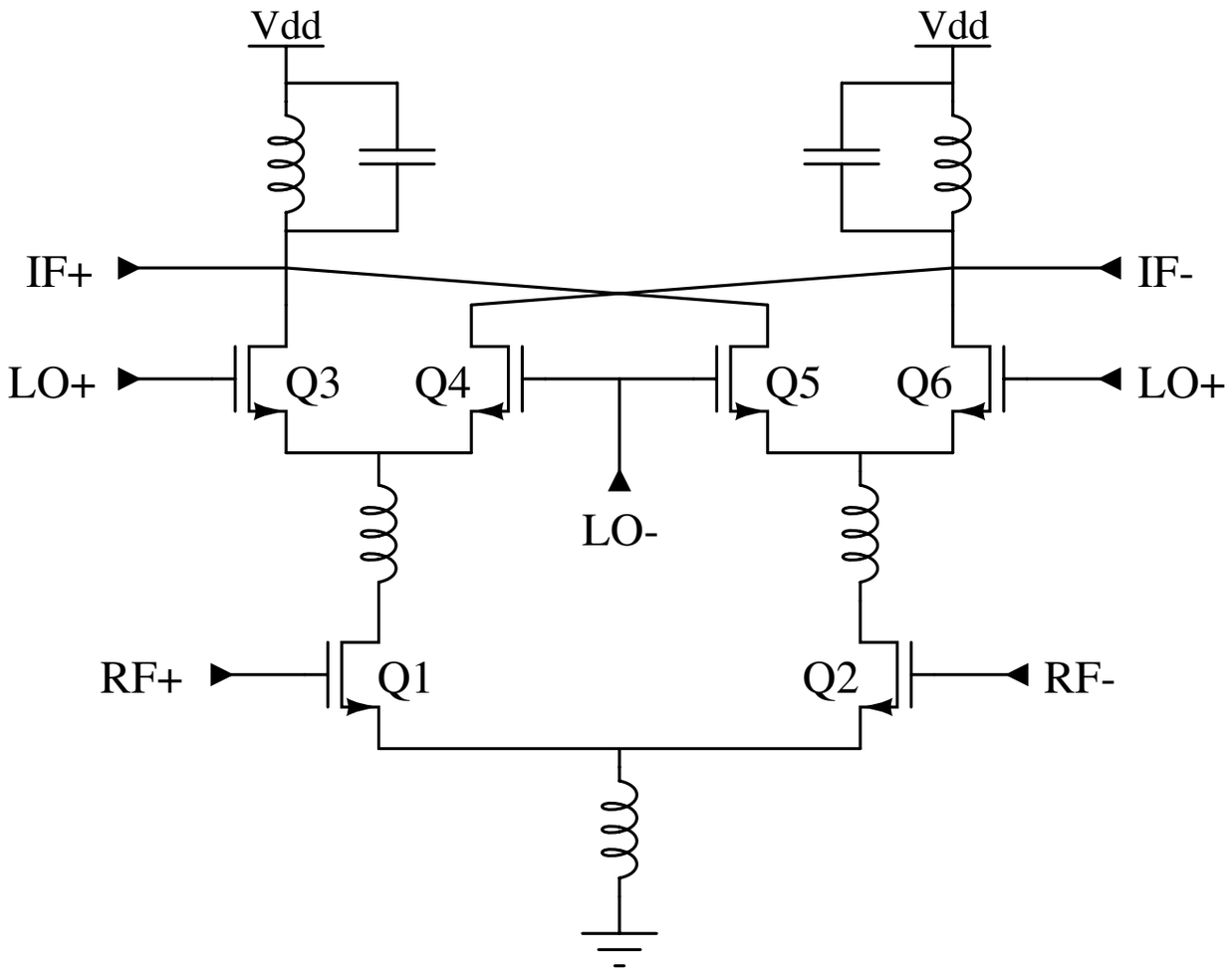
Power Amplifier issues

- **Multi-stage amplifiers**
  - **Initial stages are optimized for gain**
  - **Last stage for maximum output power**

- **Technology**
  - **Supply voltage**
  - **Substrate**
  - **Breakdown voltage**
  - **F_t**
  - **Thermal conductivity**

MIXER ISSUES

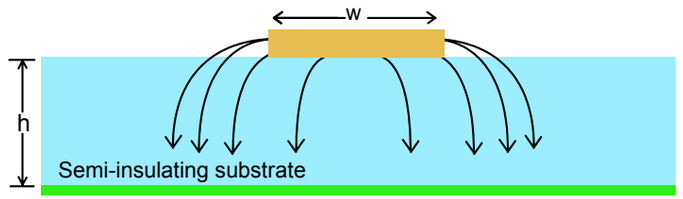
- **Double-balanced Gilbert cell for LO-RF leakage**
- **Design strategy: minimize noise, maximize linearity**
- **CM inductor for noise and headroom**
- **Middle inductors increase gain and reduce noise**
- **Interdigitated diff-pair layout sharing well**



Transmission lines and Inductance issues

Loss Mechanisms

- **Microstrip**
  - **Higher effective permittivity (eff), which leads to smaller dimensions.**
  - **Lower conductive loss than CPW and CPWG**



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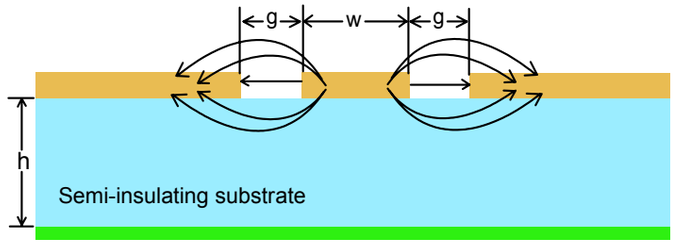
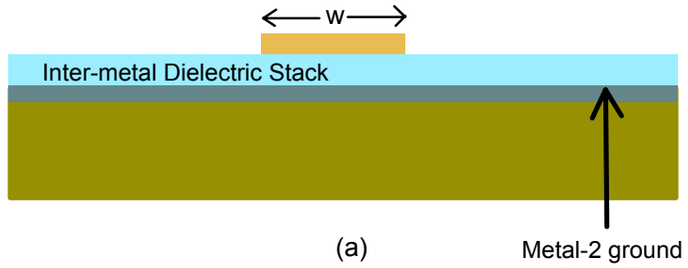


(b)

- **CPW (CoPlanar Wave)**
  - **Less electric field penetration into substrate.**
  - **Eliminates electric field penetration.**
  - **Improves isolation between adjacent lines.**
  - **Easier to realize differential topologies.**
  - **The two grounds must be forced to same potential.**



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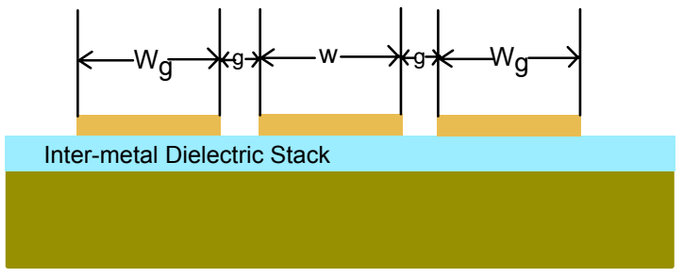


(b)

MODULATION SCHEME

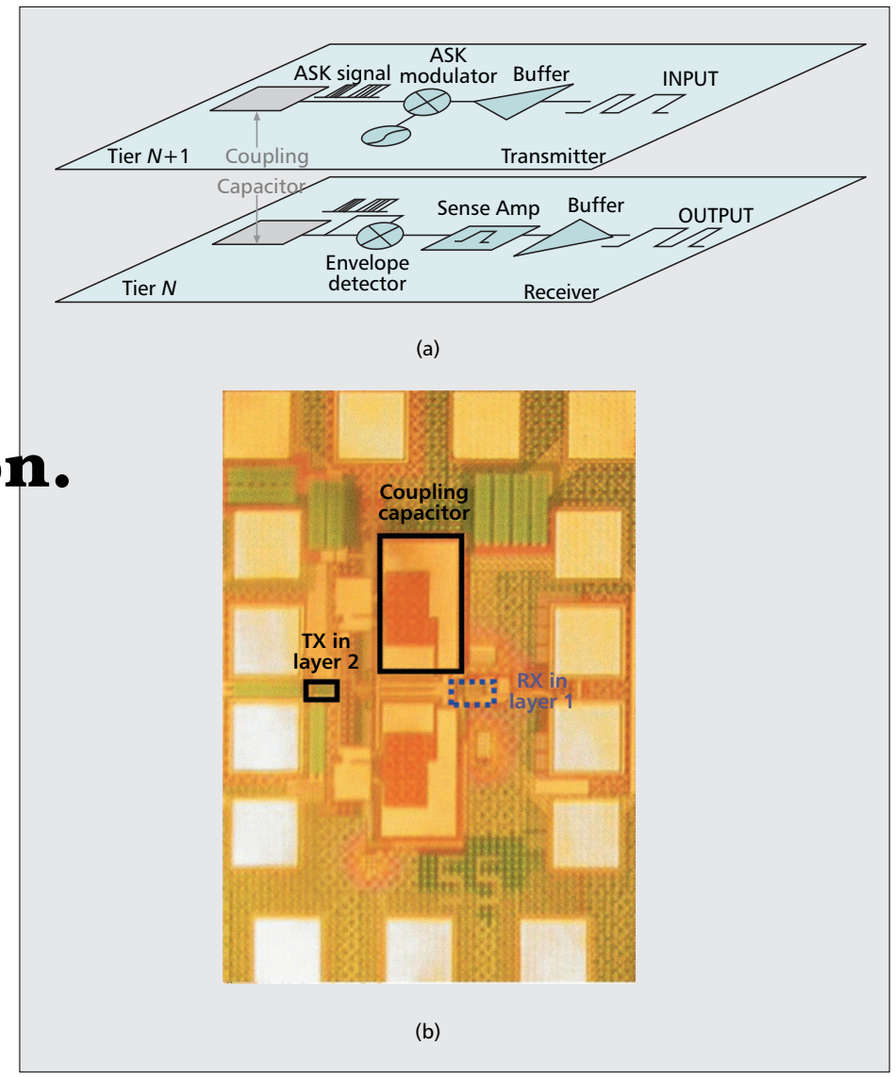
- **The purpose digital modulation is to convert an information bearing discrete-time symbol sequence into an continuous-time waveform.**
- **Key concerns are bandwidth efficiency, power efficiency and implementation complexity .**

- **Amplitude shift key modulation(ASK)**
- **Frequency shift key modulation (FSK)**
- **Binary-phase shift key (BPSK)**
- **Quadrature-Phase Shift Key (QPSK)**
- **Quadrature Amplitude Modulation (QAM)**
- **On-Off Keying (OOK)**

Modulation format	Theoretical bandwidth efficiency limits
MSK	1 bit/second/Hz
BPSK	1 bit/second/Hz
QPSK	2 bits/second/Hz
8PSK	3 bits/second/Hz
16 QAM	4 bits/second/Hz
32 QAM	5 bits/second/Hz
64 QAM	6 bits/second/Hz
256 QAM	8 bits/second/Hz

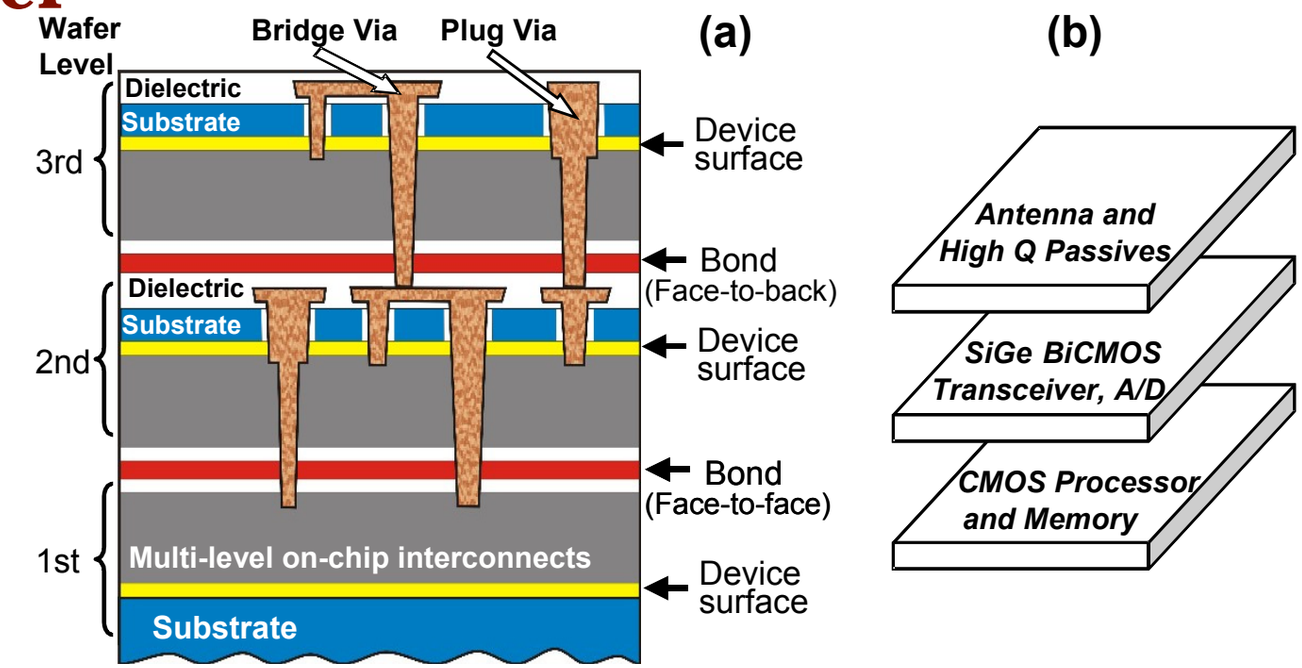
3D Chips Opens Up New Possibilities

- **RF signaling has an advantage over standard voltage signaling for inter-layer communication.**
  This due the signal is modulated on a high-frequency carrier, it does not requirer a direct connection, and capacitive or inductive coupling is enough for transmission.



WHY 3D STACKING ?

- Move from horizontal 2-D chip layouts to 3-D chip stacking.
- Increased performance - Outscaling Moores's law(More than Moore).
- Decreasing system risk.
  - E.g. Stacking a 130 nm analog die with a 45 nm digital die, rather then trying to build a 45 nm mixed signal SOC.
- Reducing cost: at some point, 3-D integration will be cheaper than shrinking further the 2-D design.
  - Moving passives onto interposer
  - Capacitors, inductors
  - potential for 20% area savings



WHY 3D STACKING ?

- **Reduce the size of the overall chip package.**
- **Boost the speed at which the data flows among the functions of the chip.**
- **Uses Through-Silicon Vias (TSV), which are vertical connection etched through the silicon wafer and filled with metal. No wires between the chips.**
- **Shortens the distance information on a chip needs to travel by 1000 times compared to a 2-D chip wire bonds that are less efficient at transferring signals off of the chip.**

Next steps

Define and specify the Chip

- Standard (antenna off-chip)
- Power consumption
- Frequency range
- Data rate
- Protocol
- Analyse test tools and instrumentation needs
- Cost
- Link budget (form factor, cost and power consumption constraints)

Preliminary Timeline

- Expect 2-3 years of development time
- VCO/PLL design has already started, planned finished 2011
- LNA and PA starts in March, planned finished end 2011
- Modulation scheme starts early 2012 and finish 2012
- First prototype planned early/middle 2013

SUMMARY

- **The 60 GHz band has very interesting features that makes it a candidate for readout of the fast-tracker.**
- **There are several challenges to integration of mm-wave systems on a silicon substrate in spite of its numerous advantages**
- **SiGe and CMOS has shown that highly integrate products are possible. SiGe HBT are chosen as the technology.**
- **3-D integration opens up new possibilities that can potentially remove the drawbacks of the 2D solution.**

Backup

Summary of the Technology Challenges

Parameter	SiGe HBT	Si BJT	Si CMOS	III-V MESFET	III-V HEMT
F_t	High	High	High	High	Best
F_{max}	High	High	High	High	High
Linearity	Better	Good	Best	-	-
Vbe (or VT) tracking	Good	Good	Poor	-	-
1/f-Noise	Good	Good	Poor	-	-
Broadband noise	High	Good	Poor	High	Best
Early voltage	Good	OK	Poor	-	-
Transconductance	Good	Good	Poor	-	-
CMOS integration	Best	Best	Better	Poor	Poor
IC Cost	OK	OK	Best	Poor	Poor