Developments in electronics for HEP

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Based on material produced in the framework of forming the DRD7 collaboration on electronics
2nd DRD7 workshop: https://indico.cern.ch/event/1318635/timetable/#20230925

Electronics in HEP

- Electronics is ubiquitous in modern HEP experiments
  - Hardware and Software are massively enabling technologies…
  - … but are becoming major cost drivers and risk factors

- Dynamic and diverse community
  - Prolific
    - Designed ~40 FE ASICs for HL-LHC
    - Developed several large data acquisition and processing systems based on state-of-the-art commercial FPGAs and processors
  - Organized
    - common frameworks for accessing technologies and tools…
    - Topical Workshop for Electronics in Particle Physics (TWEPP)
  - … but suffering from fragmented resources, becoming subcritical in several areas

- Ambitious detector projects with demanding requirements on electronics
  - Favorable, long term (10+ years) visibility and funding…
  - … widening gap between technology cycles and detector development time & complexity

- Concern that the current operating model in the community is not sustainable

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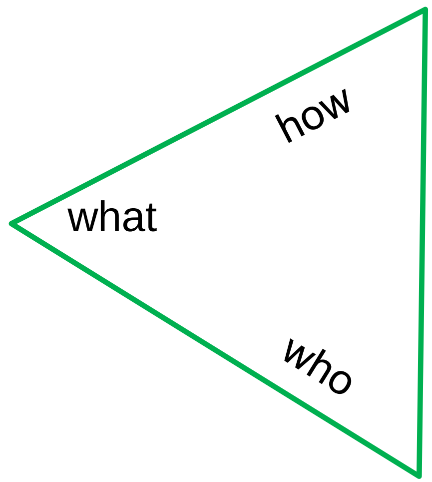
How to develop electronics in the future ?

2 Enabling technologies

1 Detector requirements



3 Available expertise

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1. Detector Requirements

- Improved granularity
  - More channels, more data
- Improved precision
  - More data
- Simultaneous space, time & energy tagging
  - More data, High accuracy timing distribution
- Low power
  - More advanced technology nodes, clever designs, efficient power distribution and conversion
- Advanced data handling
  - More intelligence, programmability and configurability
- System-level design
  - Co-optimization of sensors, electronics and algorithms
- Resistance to harsh environments

Detector Requirements > R&D Priorities

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Data density and efficiency

4D & 5D techniques

Intelligence on-detector

Backend systems and COTs

Complex imaging ASICs

Extreme environments

2. Technologies

2 Enabling technologies

1 Detector requirements

R&D Priorities

Available expertise

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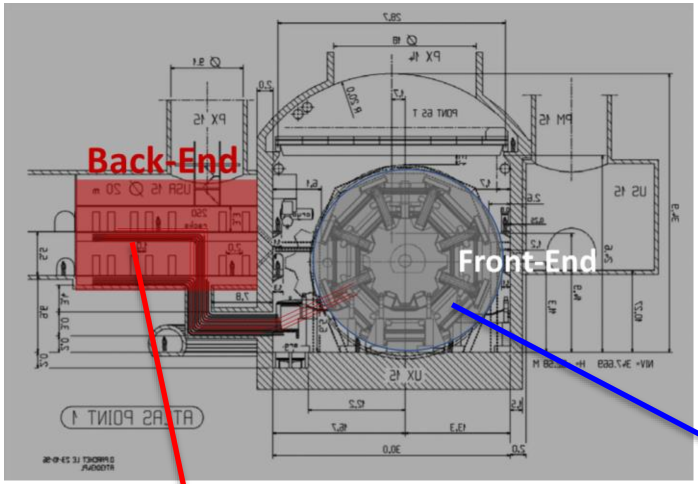
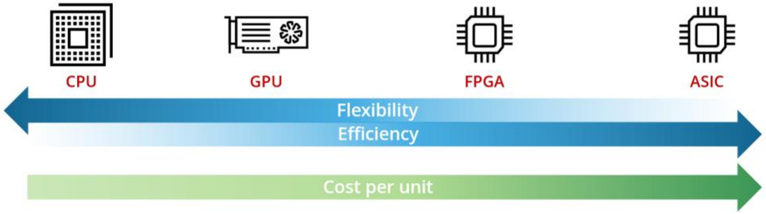
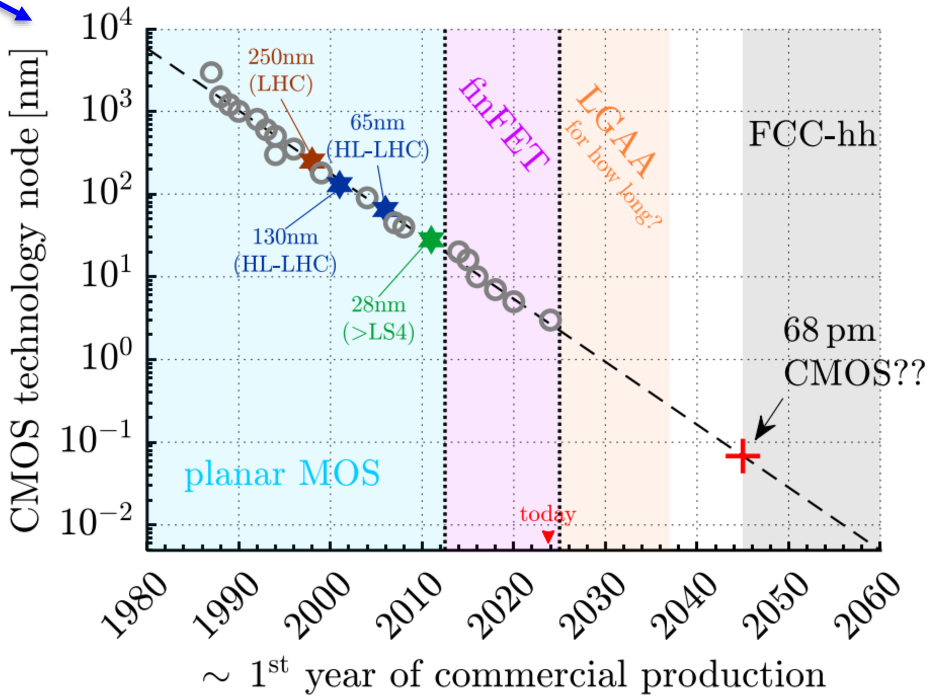
COTS or Full-Custom Technologies ?





DAQ systems increasingly COTS-based.
Economies of scale, standardization, short upgrade cycles
Exploding software effort, huge complexity and maintenance challenge

Full custom ASICs essential for Front-Ends
Optimal functionality, efficiency and rad tolerance
Complexity and cost of technology and tools are increasing and becoming unbearable



data from:
https://www.tsmc.com/english/dedicatedFoundry/technology/logic/l_3nm
https://irds.ieee.org/editions/2022/more-moore

Project Examples from DRD7 (electronics)

projects

DRD7
Letter of Intent
- 16 projects
- 64 institutes

R&D priorities

Data density and efficiency

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Complex imaging ASICs

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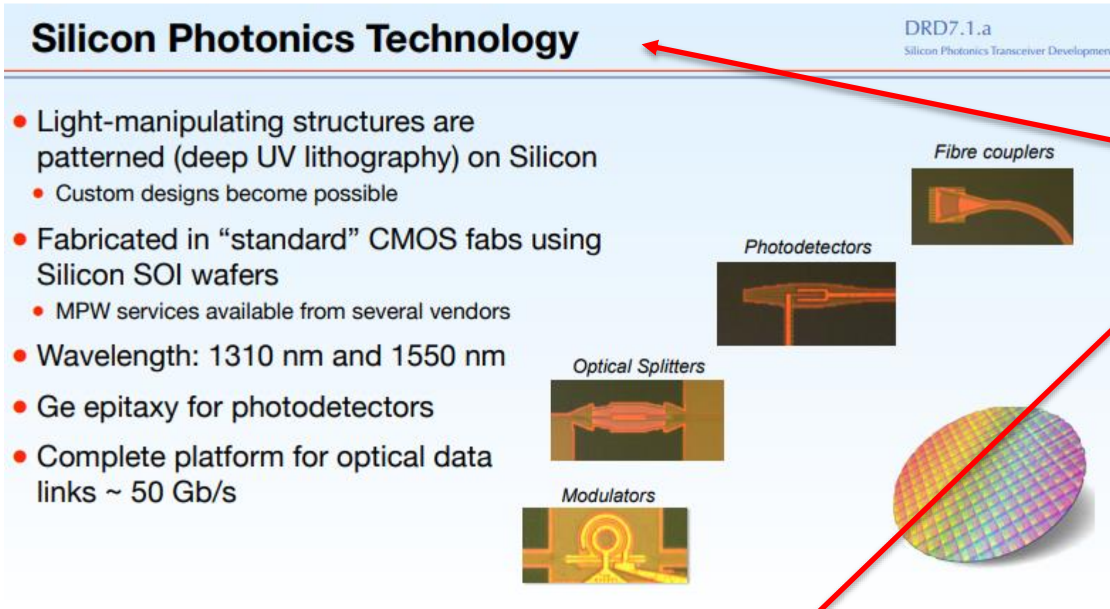
Example projects in DRD7.1

projects

R&D priorities



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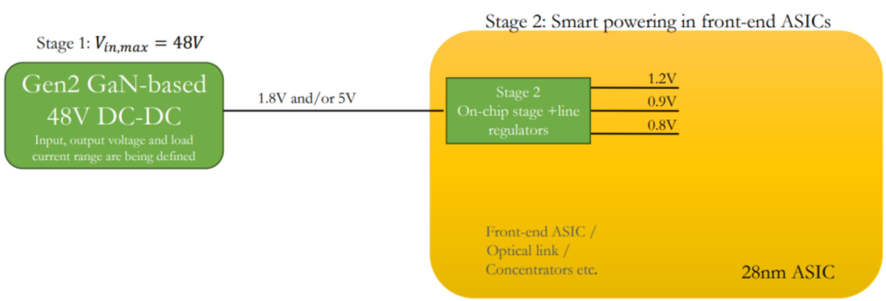
WP 7.1b: parallel power (DCDC)



Stage 1 based on HV CMOS technology and GaN power stage

Stage 2 is a fully integrated solution with all components inside the 28nm ASIC

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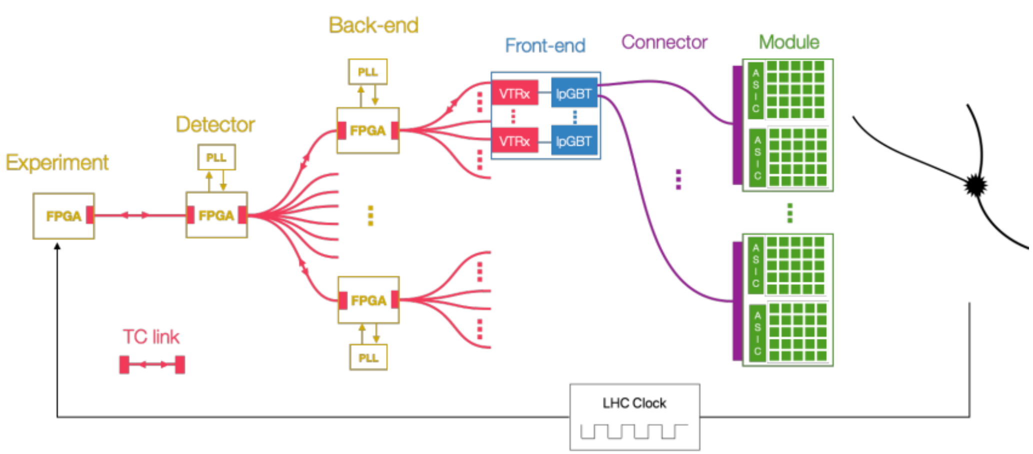
Example project in DRD7.3

DRD 7.3.b Timing measurements and distribution

First attempt to categorise and model the clock jitters, in both experiments, for a future detectors.

Already identified some clear milestones to solve:



- Define metrics and figures of merit
- Map effects to causes
- Compare implementations
- Issue recommendations

R&D priorities

Data density and efficiency

4D & 5D techniques

Intelligence on-detector

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Example project in DRD7.2

projects

R&D priorities

Data density and efficiency

4D & 5D techniques

Intelligence on-detector

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Complex imaging ASICs

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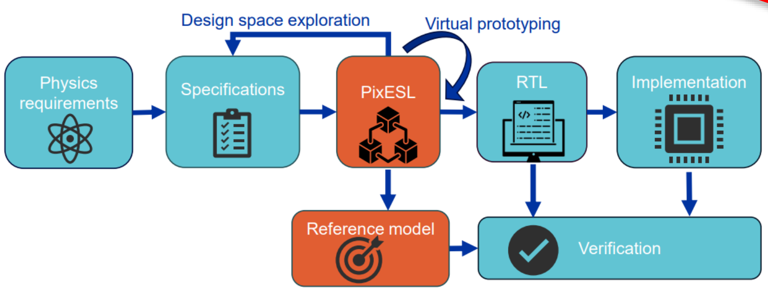
DRD 7.2.c

Detector Design Flow with PixESL

Goals

Develop a **high-level description of the system**, from front-end to back-end, to:

- Refine **specifications** and **performance evaluation** during prototyping
- Provide a **reference model** for verification
- Provide a **virtual prototyping environment** for new features development



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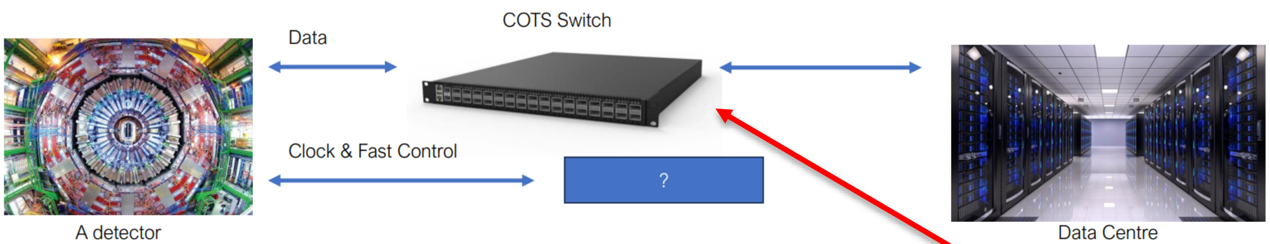
Example project in DRD7.5

projects

R&D priorities

DRD 7.5.b 

- Lower radiation levels opens the door to increasing the complexity of Front-End electronics (RISC-V based processors, RAMs and SoC in the Front-End)



⇒NEW PARADIGM: high throughput 100GbE-based data readout link can reasonably be envisaged and shall be investigated

- Data density and efficiency
- 4D & 5D techniques
- Intelligence on-detector
- **Backend systems and COTs**
- Complex imaging ASICs
- Extreme environments

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Example project in DRD7.6

projects

R&D priorities

DRD 7.6.b Common access to 3D

Strategic Goal

- Provide/facilitate the access to advanced chiplet and 3D integration technologies
- Integration of SiPh chip and optical fibers on detector module
  - Reduce development costs and production time by in-house facilities

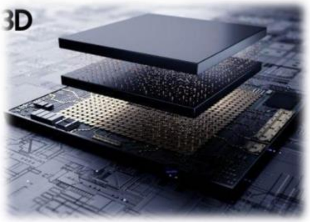
Performance Targets

- Shared competences/experiences and infrastructures/processes
- Built-up and maintain capability for wafer stacking/multi-tier, chiplet and SiPh integration

Supported Technologies

- TSV-last and redistribution layer (RDL) technologies
- Chiplet, 3D/2.5D integration, W2W, C2W and C2C bonding w/wo solder
- Integration of monolithic/hybrid PIC on detector

DRD 7.1⇔DRD 7.6



Data density and efficiency

4D & 5D techniques

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Extreme environments

Example project in DRD7.4

projects

R&D priorities

Data density and efficiency

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Motivation for the Project "7.4.a Modeling and Development of Cryogenic CMOS PDKs"

- CMOS Process Design Kits typically valid down to 233K (-40°C), although models scale relatively well down to 77K. This was verified with VDSM bulk and FDSOI technology nodes.
- Cold CMOS PDKs are fundamental for the development of complex mixed-signal ASICs allowing for innovative detector architecture and concepts, data transfer, readout and control.
- The sweet spot around LN boiling temperature (where we get the best of the MOSFET characteristics with still no saturation effects) opens promising prospects on the development of innovative readout concepts both for neutrino and dark matter detectors with noble liquids and, in general, for calorimeters and photon detectors operating at 77K.
- The growing interest on the use of CMOS for Quantum Computing and Quantum Sensing could open new opportunities for collaborative efforts with selected silicon foundries on the optimisation of solid-state sensors and CMOS processes for operation at cryogenic temperatures.

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3. Expertise

2 Enabling technologies

Maintain:

- Access
- Pace
- Expertise

1 Detector requirements

R&D Priorities

3 Available expertise

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Community and Expertise

- 64 institutes in 15 countries expressed interest to contribute to DRD7
  - Many more observing

- Maintain active community despite the complexity challenge
  - ASICs developments for HL-LHC have been first to show near-failures, but optics, FPGA, soft/firmware are close
  - Complexity trend will continue, and costs will inflate
  - Community must act and restructure to decrease risk
    - Collaborate more, on fewer projects
    - Simulate more before implementing, verify from the beginning
    - Apply system design approaches
    - Specify, develop and document with high-level synthesis tools

- Coordinate cross-community access to technologies, tools and knowledge
  - Share and re-use IP
  - Maintain existing and develop new common frameworks to access advanced technologies and share expertise
  - Develop support hubs to assist smaller teams
  - Introduce rolling reviews

Electronics R&D for HEP

Enabling technologies

Maintain:
- Access
- Expertise
- Pace

Detector requirements

R&D Priorities

DRD7
Collaboration
& Projects

Available expertise

- Common platforms
- Shared IP
- Support hubs

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References

- EPPS strategy update 2020: https://indico.cern.ch/event/957057/
- ECFA Detector R&D: https://indico.cern.ch/event/957057/
- ECFA DRD Roadmap: https://indico.cern.ch/event/957057/page/23281-the-roadmap-document
- 1st DRD7 workshop: https://indico.cern.ch/event/1214423/timetable/#20230314
- 2nd DRD7 workshop: https://indico.cern.ch/event/1318635/timetable/#20230925

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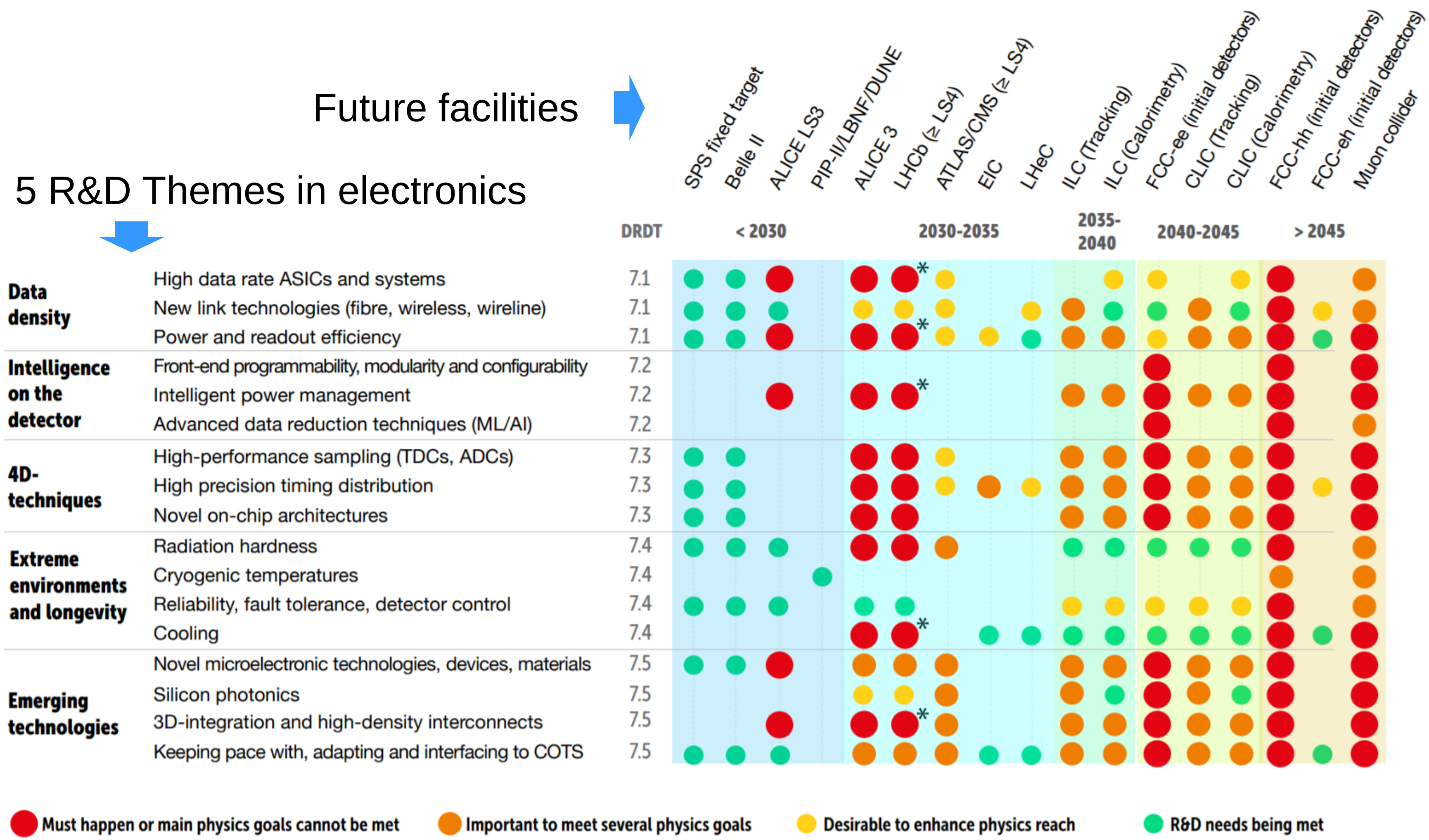
Additional material

TF7 Recommendations

a) Detector R&D Themes, Electronics



* LHCb Velo

DRD7 structure

- Collaboration Board: representatives of participating institutes
- Steering Committee: to be appointed
- Technical Committee:WG7.x conveners+steering committee

WG 7.1
Data Density & Power efficiency
Szymon Kulis
Jeffrey Prinzie
Jan Troska
Projects

WG 7.2
Intelligence On-Detector
Davide Ceresa
Francesco Crescioli
Projects

WG 7.3
4D & 5D Techniques
Sophie Baron
Marek Idzik
Adriano Lai
Projects

WG 7.4
Extreme Environments
Giulio Borghello
Oscar Francisco
Manuel Rolo
Projects

WG 7.5
Backend systems & COTS
Conor Fitzpatrick
Niko Neufeld
Projects

WG 7.6
Complex imaging ASICs & technologies
Marlon Barbero
Michele Caselle
Iain Sedgwick
Walter Snoeys
Projects

Transverse WG 7.7 Tools and Technologies
Kostas Kloukinas
Xavi Llopart
Mark Willoughby