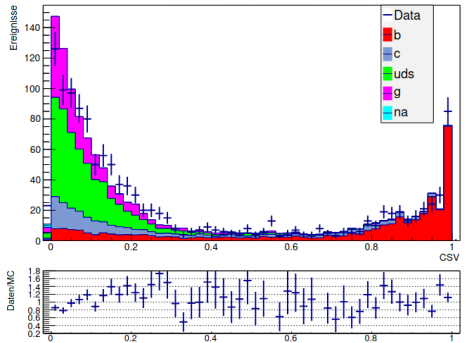
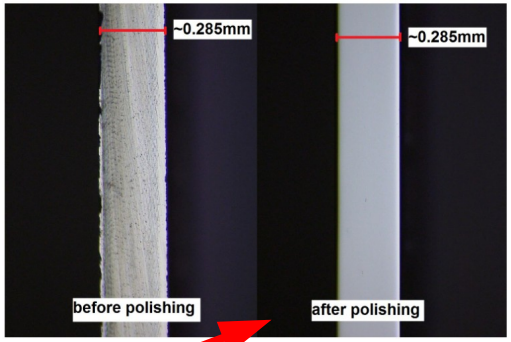
A Harbour Boat Trip

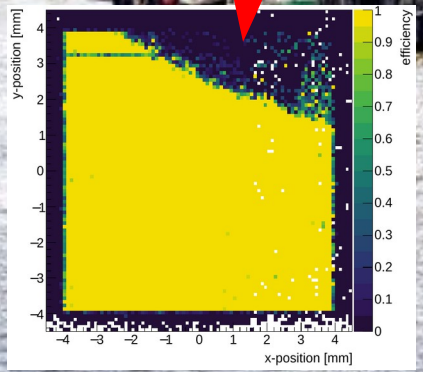
Or—as others would put it—my „journey”





This killed quite some strip sensors

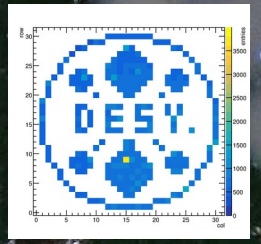
This is the only pixel sensor I damaged so far!



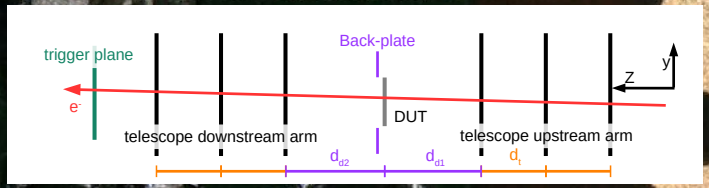
About Me

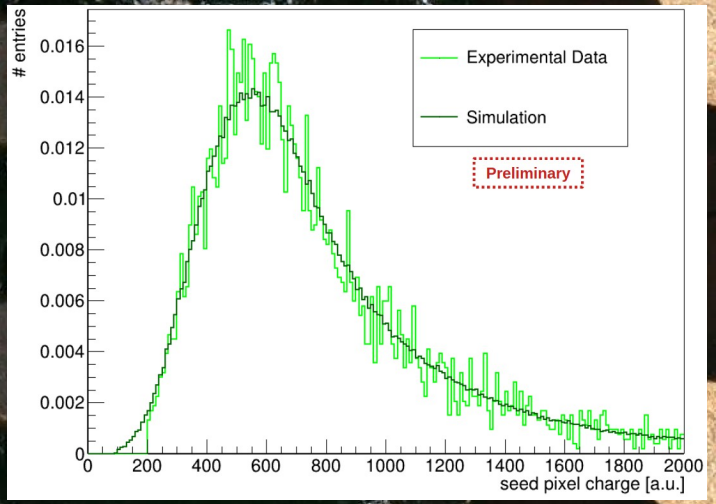
- Born in Hamburg, Finkenwerder
- Raised in Hamburg
- Bachelor thesis on b-tagging in CMS
- Master thesis about edge-TCT
- Dissertation with CMS
  Planar pixel sensors for Phase-2
- Now Postdoc at DESY Hamburg

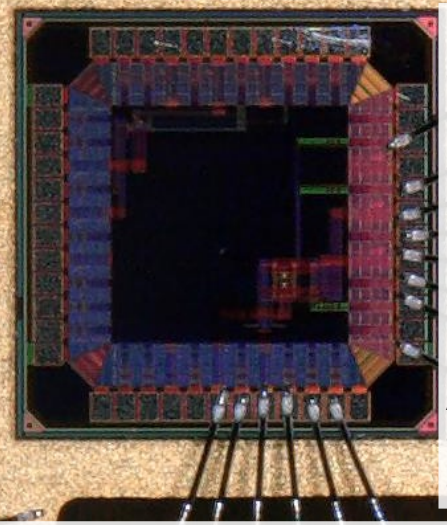
Towards a New Generation of Monolithic Active Pixel Sensors



The TANGERINE project—MAPS in a 65 nm CMOS imaging process







Project Goals

- Spatial resolution: 3 um
- Temporal resolution: 10 ns
- Thickness: < 50 um
- In-pixel charge measurement (time-over-threshold)
- Exploit/ explore capabilities for in-pixel logic

Application

- Beam-line instrumentation at DESY
- Future lepton collider/ Higgs factory

Simulation

- TCAD simulations based on generic doping profiles for detailed electric fields
- Allpix2 simulations to make predictions of sensor performance

Measurements

- First test chips investigated at DESY II, CERN PS and MAMI microtron
- Investigated charge sensitive amplifier and sensor performance
- Recorded data to **validate our simulations**. Analysis ongoing!

Something Inspiring …

From ALICE ITS3

What is this?

- This is a photograph of the mechanical mockup of an “all silicon vertex detector”.

Why would we want this?

- Significantly reduces multiple scattering effects in the tracking volume!

Key properties

- Power consumption below 20 mW/cm^2
  → air cooling possible
- High level of integration
  → data and power lines integrated on chip
- Tubes are rigid
  → significantly reduce mechanical support

Is this science fiction?

- Flexibility reached at 20 to 40 um
- Studies on wire bonding, gluing, mechanical deformations ongoing
- Bent ALPIDE chips proved operational [doi]

→ **Driving develoment of monolithic sensors**