# Latest AMD SoC-based Boards in MicroTCA.4 at DESY-

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12th MT ARD ST3 Meeting 2024 in Darmstadt 3 to 5 July, Germany



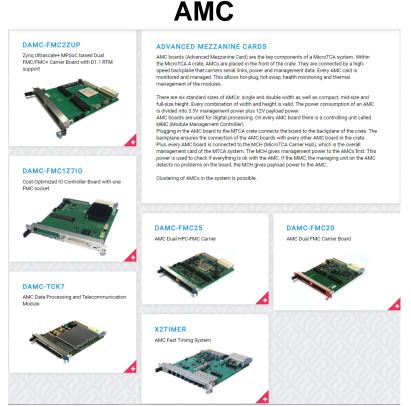


# **Licensing Strategy**

- We promote an ecosystem
- DESY has licensed almost all developments: components are available for us **and** for third parties

RTM

• Strategy: Concentrate on the application; purchase all "unexciting" infrastructure









### **FMC**



# All SoC developments of the last few years

Similarity 1: Boards are all based on DMMC-STAMP

DAMC-FMC2ZUP (Supercarrier)

Ultrascale+
MPSoC

DAMC-DS812ZUP

DAMC-MOTCTRL

DAMC-UNIZUP

(RFSoC-based)

Ultrascale+
MPSoC

Ultrascale+
MPSoC

Ultrascale+
MPSoC

Ultrascale+
MPSoC

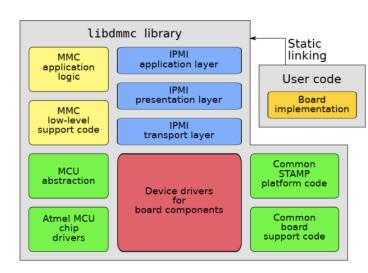
2022

2023

2024

2019 2020 2021 2022 2023 2024

DMMC-STAMP on the back of the AMC card

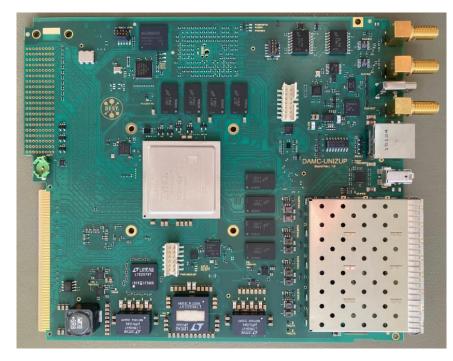


- DMMC-Stamp handles MicroTCA Management
- Complete software framework
- 95% re-use
- Compatibility with all MCHs we know of
- In-system update (from MMC and FPGA)
- Serial-over-IPMI (remote access to the FPGA and MMC UART)

DESY.

- 2024: over 1000 pieces produced
- used by 30 partners
- 100% test in the needle test adapter

## **DAMC-UNIZUP**







# INSTRUMENTATION TECHNOLOGIES

#### Inherited features:

- Quad-Core ARM Cortex-A53 @1.5 GHz, Dual-Core ARM-R5 RT @600 MHz and Mali-400 MP2 graphics
- PCIe x4 (x8 option on supported systems); Gen.3 supported
- USB type-C Alternate Mode Display Port for standalone operation (no need for additional AMC CPU Module)
- Flexible clocking scheme and front panel connector for external clock input and White Rabbit support
- Supported by all Xilinx development tools (e.g. Vivado HLx)

#### "Little Sister" of DAMC-FMC2ZUP

- Lower-cost-board with smaller FPGA: hundreds of units will be needed at Petra IV
- 14 instead of 16 layers, 0402 components, (only 0201 capacitors)

#### **Facts**

- Board inherits the technology of DAMC-FMC2ZUP
- Universal MPSoC board with high-performance RTM connectivity
- Large FPGA (in smaller package):
   Zynq Ultrascale+ ZU7CG...ZU11EG

#### New:

- 2 x 64bit wide DDR4 interfaces (in total 8GiB RAM)
- 4 integrated SFP+ slots with 16.375 Gbps (not 28 Gbps GTY)
- Connectors for "slow trigger" (RS485 for machine protection) and "fast trigger" on Front Panel
- 2 Front panel clock inputs via SMA, 1 Output



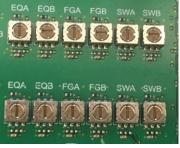
## DAMC-8SFP+

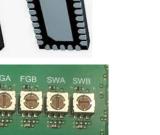
#### Fan-out of MGT Channels from DAMC-UNIZUP

- We needed to verify UNIZUPs 8 MGTs to RTM
- We designed a 8-SFP+ RTM
- Board works on all other Digital Class AMCs
- Brings 1 to 8 MGTs to RTM 12.5 Gbps: not trivial
- First use of "analog" equalizer
- Development time: 3 months
- Low-cost circuit board and components
- Manufactured in the "PCB pool" from Leiton (Berlin)
- Material: Panasonic R-1566W (Dk=0.010!!!)

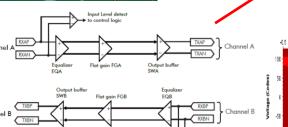


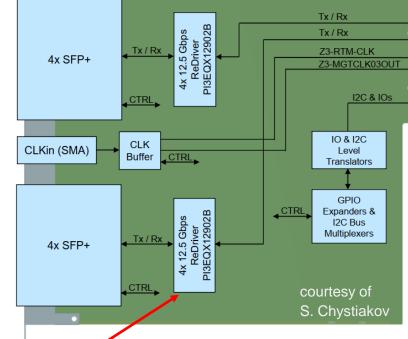


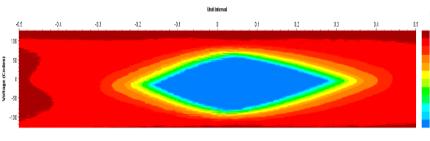












Name	TX V1	RX	Status	TX Polarity Invert	RX Polarity Invert	Bits	Errors	BER	ı
Ungrouped Links (0)									
S Link Group 0 (4)									
% Link 3	Quad_224/MGT_X0Y3/TX (xczu11_0)	Quad_224/MGT_X0Y3/RX (xczu11_0)	10.313 Gbps		✓	8.597E12	0E0	1.163E-13	
⊗ Link 2	Quad_224/MGT_X0Y2/TX (xczu11_0)	Quad_224/MGT_X0Y2/RX (xczu11_0)	10.313 Gbps	✓	✓	8.597E12	0E0	1.163E-13	
⊗ Link1	Quad_224/MGT_X0Y1/TX (xczu11_0)	Quad_224/MGT_X0Y1/RX (xczu11_0)	10.313 Gbps	✓		8.597E12	0E0	1.163E-13	
% Link 0	Quad 224/MGT X0Y0/TX (xczu11 0)	Quad 224/MGT X0Y0/RX (xczu11 0)	10.313 Gbps	<b>✓</b>		8.597E12	0F0	1.163E-13	Γ

## **MicroTCA Motion Controller Hardware**



- Board in Rev. A fully functional
- Not a single patch wire



Heterogeneous approach MPSoC (2 GB DDR4) and FPGA (4 GB DDR3)

- MPSoC:
  - Raspberry Pi in FPGA (Yocto Linux)
  - Non-real-time tasks
  - Communication with other cards
- Kintex-7: Real-time control
  - 5 SFP+-Ports (1 Gbit/s to 10 Gbit/s)
  - 3x Motor Interfaces, 2x Ring topology
  - HW-Support: CAN EtherCAT, SERCOS

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