RF Digitizer DAMC-DS5014DR based on AMD ZYNQ Ultrascale+ RFSoC Technology in MicroTCA.4 form factor

Behzad Boghrati, Burak Dursun, Michael Fenner, Cagil Gümüs, Szymon Jablonski, Johannes Zink

12th MT ARD ST3 Meeting 2024 in Darmstadt 3 to 5 July, Germany

HELMHOLTZ RESEARCH FOR GRAND CHALLENGES

DESY.

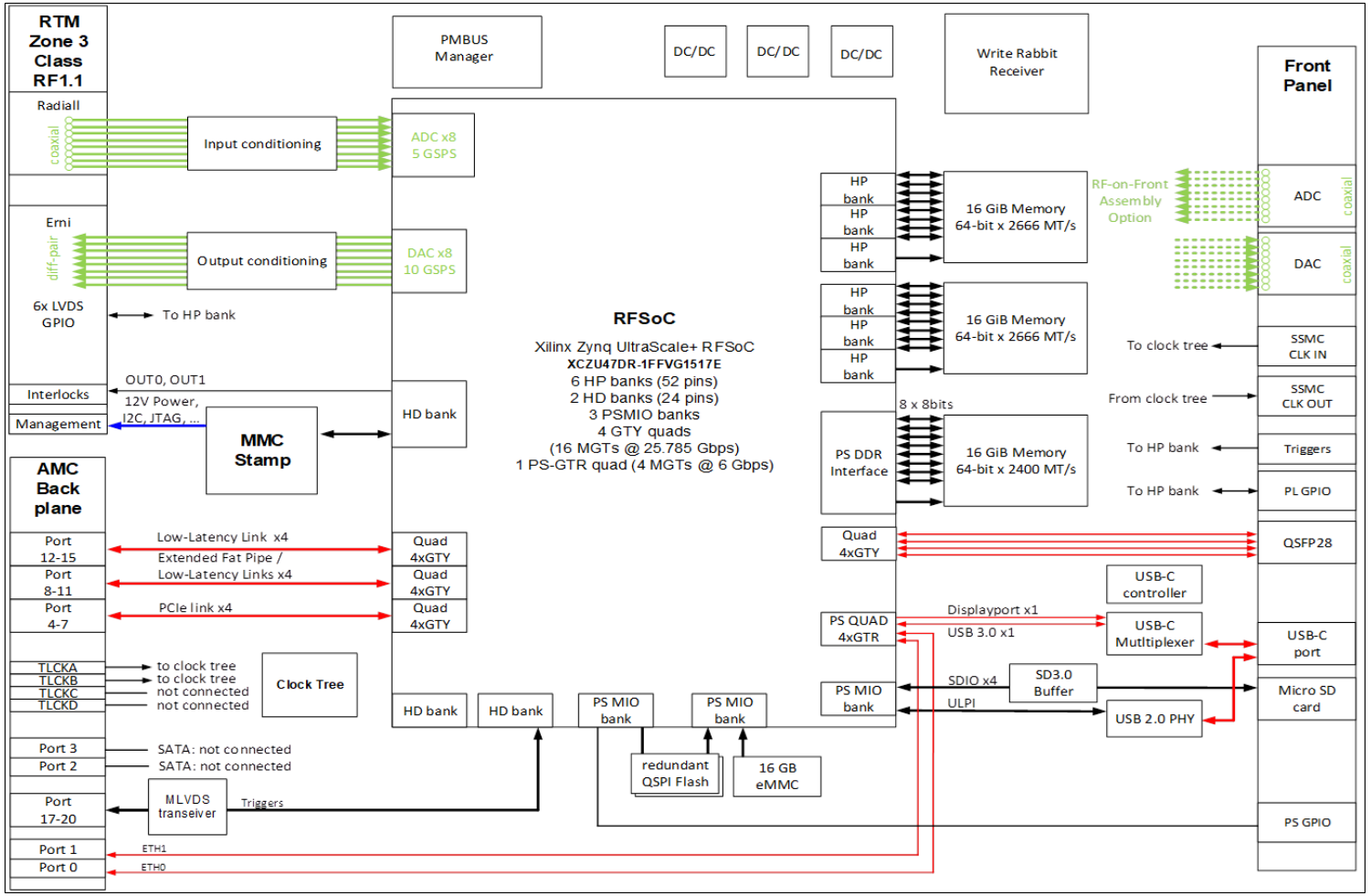
Outlines

- **Review of the DS5014DR Specifications – XCZU47DR-1FFVG1517E**
- **AC/DC Coupling – Passive Balun and Fully Differential Amplifier**
- **Clock Tree for the DS5014DR – Wideband Clock Synthesizer**
- **Zone 3 - Connectors and Class RF1.1**

DAMC-DS5014DR

General Specifications

- **ZU47DR Zynq Ultrascale+ RFSoC 3rd generation**
  - 930k logic cells, 4272 DSP slices
  - ADC 8-channels 14-bit 5 GSPS, 6 GHz analog BW
  - DAC 8-channels 14-bit 10 GSPS
- **Zone 3 RF connector compliant to new Class RF1.1**
- **Works as “CPU module”:**
  - Front panel USB type-C provides DisplayPort and USB 3
  - 16 GB (PS DDR4) + 32 GB (PL DDR4) Memory
  - Runs Yocto Linux from eMMC or SD card
- **Analog Inputs:**
  - 8x Single-ended via Zone 3 Radiall from RTM
  - 6x AC Coupling, 0.03 – 6 GHz
  - 2x DC coupling, DC – 6 GHz
- **Analog Outputs:**
  - 4x Differential via ERNI to RTM, DC coupling, DC – 2.5 GHz
  - 4x Single-ended via Radiall to RTM, AC coupling, 0.03 – 6 GHz
- **RTM, Front Panel and Backplane Clock Inputs**
- **White Rabbit endpoint capability**



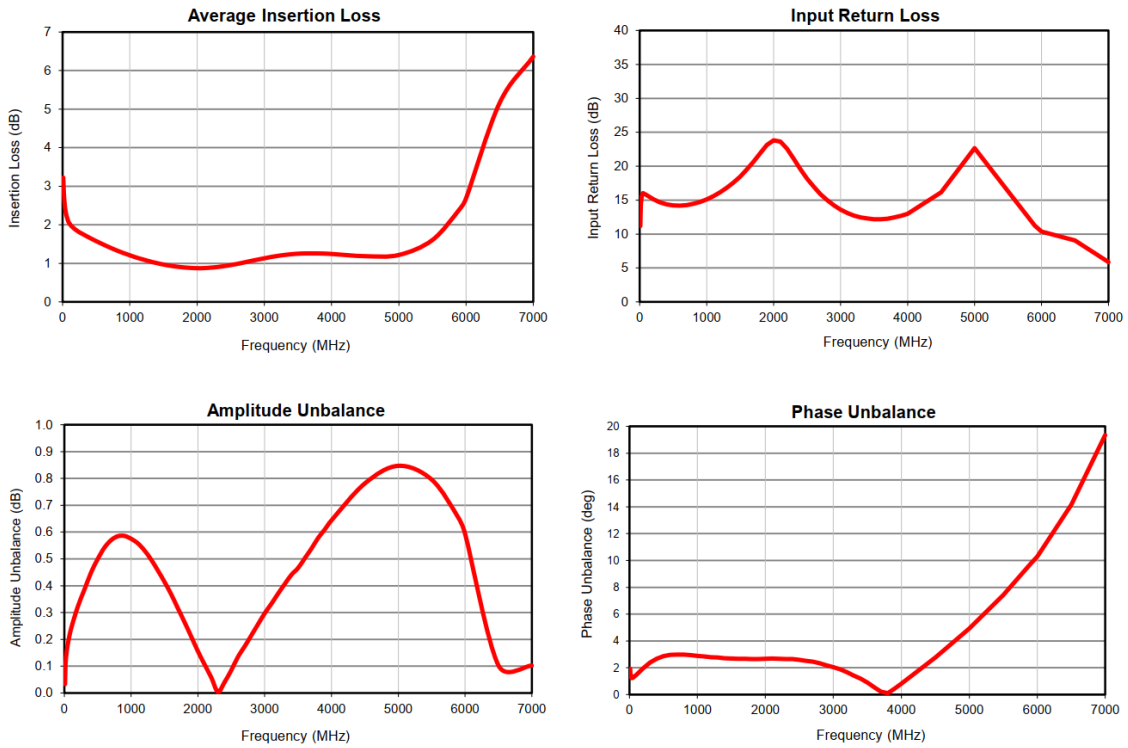
Courtesy of M. Fenner

AC Coupling - Passive Baluns

➢ **Passive Balun: TCM2-63WX+**

RF Transformer **TCM2-63WX+**

Typical Performance Data



Generic photo used for illustration purposes only

CASE STYLE: DB1627

Table 3-2: **Balun Specification Recommendations**

Specification	Typical Result
Impedance ratio	2 or 1
Bandwidth	Application specific
Insertion loss	–1 dB or better
Return loss	–15 dB or better
Common-mode rejection ratio (CMRR)	>30 dB(1)
Amplitude imbalance	<~0.5 dB
Phase imbalance	<~1.5°

Notes:

1. CMRR can be relaxed if the system is designed to avoid second harmonic distortion (HD2) by frequency planning.

DC Coupling – Fully Differential Amplifier

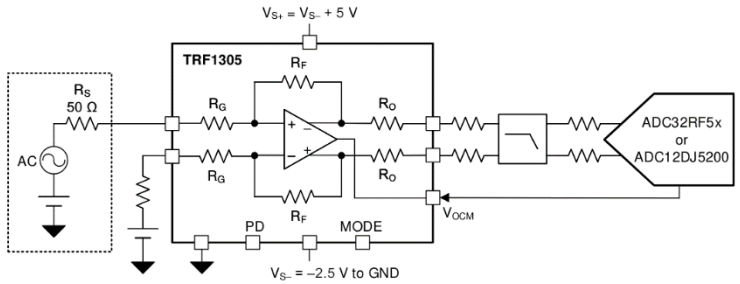
TRF1305X2

- Three performance-optimized power gain variants:

Device Information

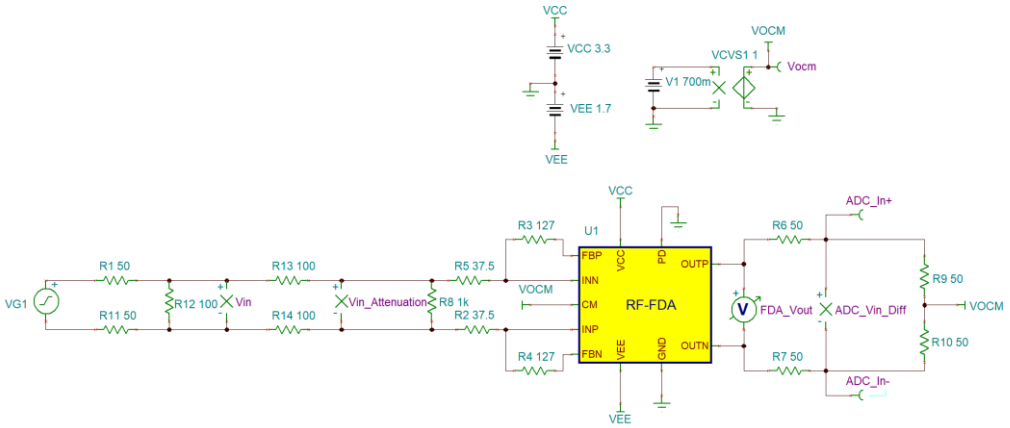
PART NUMBER(1)	D2D POWER GAIN	PACKAGE(2)
TRF1305A2 (3)	5 dB	RYP (WQFN-FCRLF, 16)
TRF1305B2	10 dB	
TRF1305C2 (3)	15 dB	

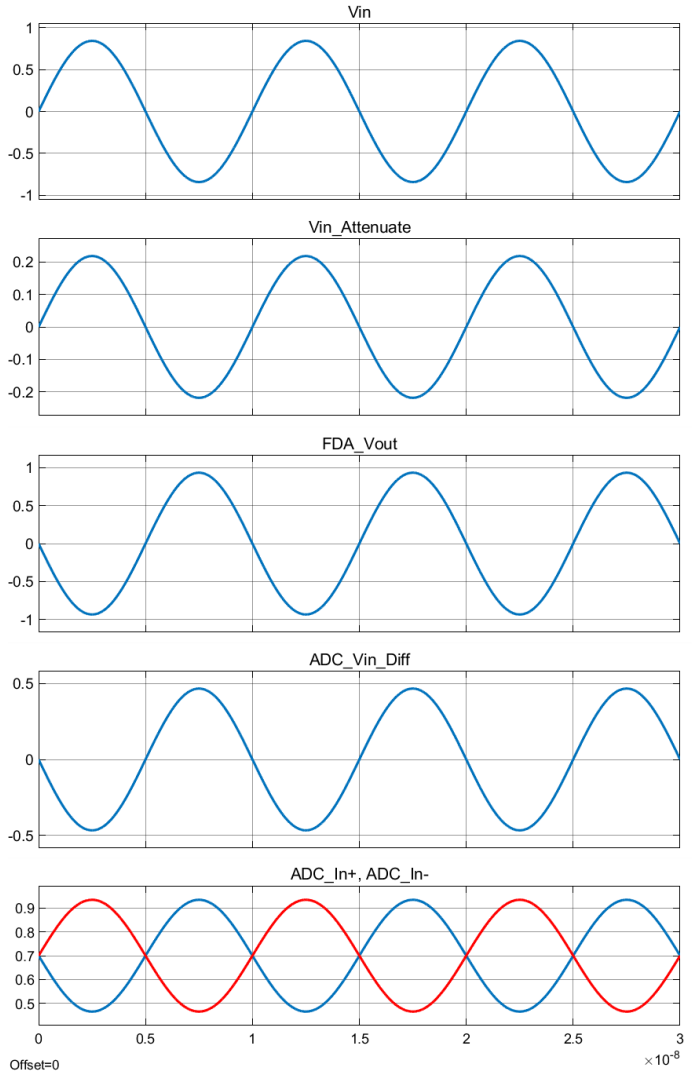
(1) See the Device Comparison Table.
(2) For more information, see Section 11.
(3) Preview information (not Production Data).



TRF1305 Driving a High-Speed ADC

- Preset gain can be reduced with external resistors
- High large-signal bandwidth:
  - TRF1305B2: 7 GHz (3-dB), 6.5 GHz (1-dB)
- Noise Figure: 10.2 dB (2 GHz), 12 dB (4 GHz)
- Slew rate: 25 kV/µs
- Flexible configurations and modes:
  - Single-ended input, differential output (S2D)
  - Differential input, differential output (D2D)
  - Single-ended output (limited performance)
  - AC- or DC-coupled input/output
  - Adjustable output common-mode voltage
  - Input common-mode range extension mode

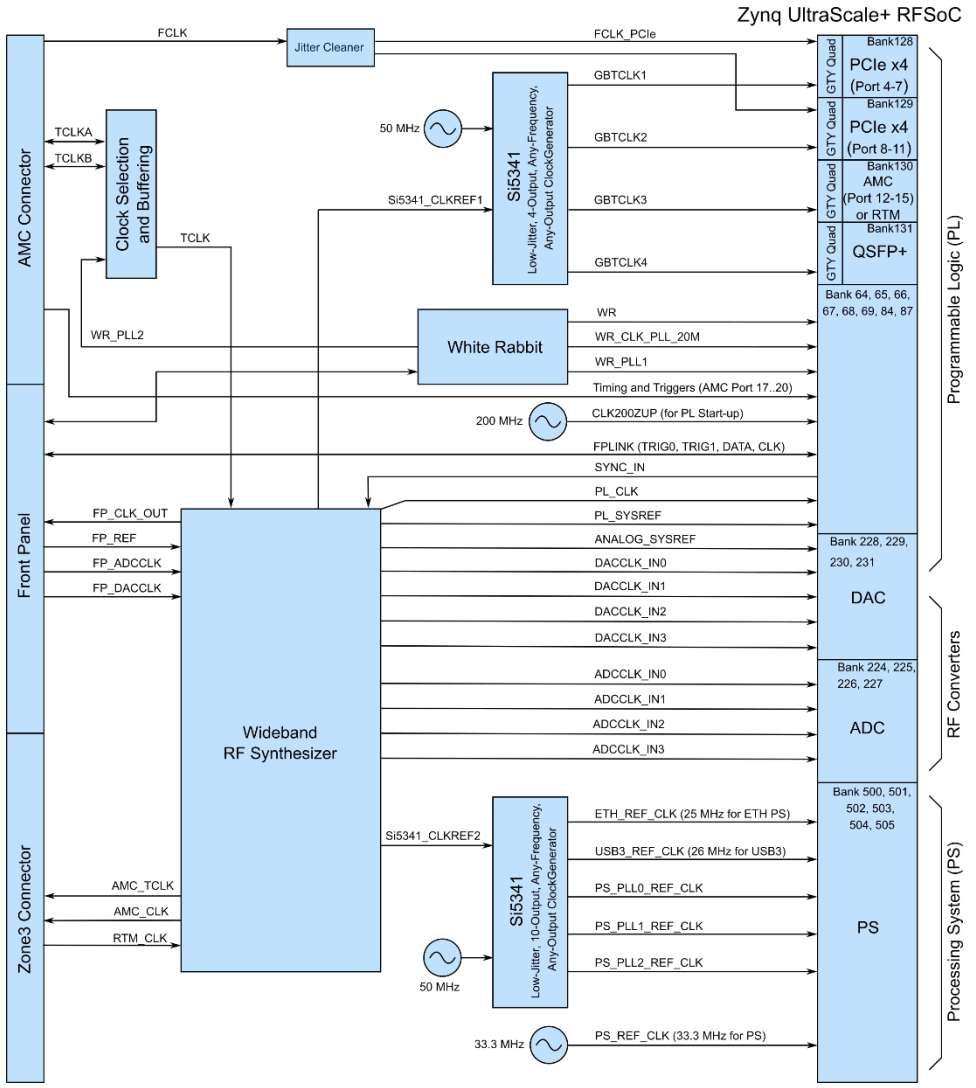




DS5014DR Clock tree and ADC/DAC converter Clocking Characteristics

ADC/DAC converter Clocking Characteristics

106				
107	Tile clock input frequency range (FIN)	102.40625 - 10000	MHz	FREF range restrictions apply when the PLL is used. The FS range restriction applies when PLL is bypassed.
108	Frequency input division ratio (R)	1	-	Possible values are 1, 2, 3, 4 Only available when using internal PLL
109	Reference input frequency (FREF = FIN/R)	102.40625 - 615	MHz	On-chip PLL activated
110	ADC Input sampling frequency (Fs)	1) 0.5 - 2.5 2) 0.5 - 5.0	GHz	1) PLL bypassed, quad ADC tile configuration 2) PLL bypassed, dual ADC tile configuration
111	DAC Input sampling frequency (Fs)	0.5 - 10.0	GHz	PLL bypassed
112	PLL output frequency (Fout)	1) 0.5 - 5.000 2) 0.5 - 6.882 3) 0.5 - 10.00	GHz	1) RF-ADC PLL output frequency range, 2) RF-DAC PLL output Low frequency range, 3) RF-DAC PLL output High frequency range.
113	Phase noise for the RF-ADC (PN_ADC)	-124, -128; -135, -143.	dBc/Hz	Offset = 100 kHz, Offset = 1 MHz, Offset = 2.5 MHz, Offset = 10 MHz.
114	Phase noise for the RF-DAC (PN_DAC)	-121, -128, -135, -144.	dBc/Hz	Offset = 100 kHz, Offset = 1 MHz, Offset = 2.5 MHz, Offset = 10 MHz.
115	Reference spur (RS)	-70	dBc	
116	Reference harmonic spur (RHS)	-70 -80	dBc	Offset from carrier <800 MHz Offset from carrier >800 MHz



Courtesy of S. Jablonski

ZONE 3 Interface

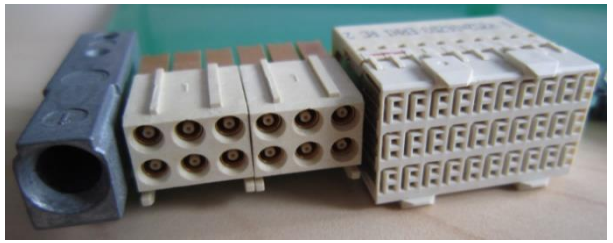
ERNI and Radiall Connectors – Johannes Zink

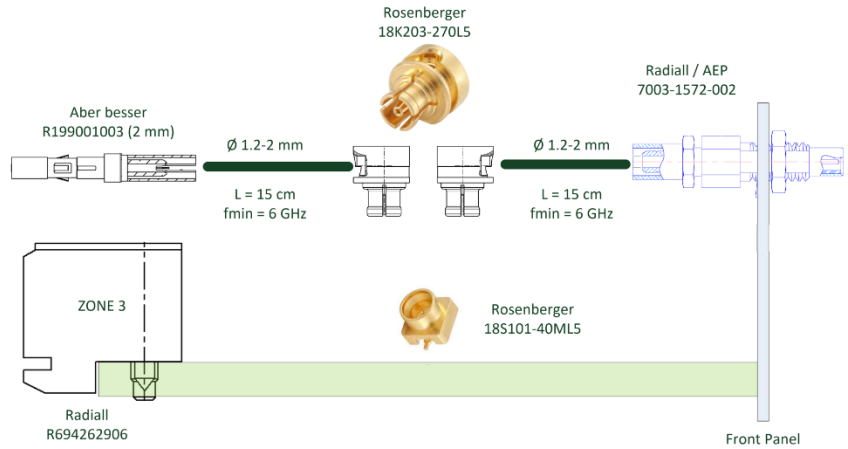
	Zone 3 Interfaces with RTM (Class RF1.1)	Pin Assignment	Pin Number	I/O	Description
208					
209	J30 ERNI Connector	PWRA1, PWRA2, PWRB1, PWRB2	1a, 2a, 1b, 2b	I	RTM supply voltage (12 V, 30 W max.)
210		PS#	1c	O	RTM present signal (connected to GND on RTM)
211		SDA, SCL	1d, 2d	I/O	I2C management interface to- RTM (level 3.3 V)
212		TCK, TDI, TDO, TMS	1e, 2e, 1f, 2f	I/O	JTAG interface to RTM
213		MGT-RX±	3a, 3b	I/O	Gigabit receiver, not implemented
214		DAC0±, DAC1±, DAC2±, DAC3±, DAC4±, DAC5±, DAC6±, DAC7±,	3a, 3b, 3e, 3f, 4c, 4d,5a, 5b, 5e, 5f, 6c, 6d, 7a, 7b, 7e, 7f	O	Differential DAC outputs, DC coupling
215		D0-CC±, D1±, D2±, D3±, D4±, D5±	3c, 3d, 4a, 4b, 4e, 4f, 5c, 5d, 6a,6b, 6e, 6f	I/O	LVDS (Vcm 1.2V, Vdiff 350mV, 100R), connected to the PL HP bank (1.8V) Note: This interface is intended to carry a differential SPI Bus with LVDS levels. A CPLD on the RTM can fan out these signals into standard SPI and I2C busses.
216		RTM-CLK±	8a, 8b	I	LVDS/LVPECL clock input from RTM to the RF synthesizer
217		RF-CLK0±, ..., RF-CLK3	10a, 10b, 8c,8d, 10c, 10d,8e, 8f	I	Not implemented
218		AMC-TCLK±	9a, 9b	O	LVDS/LVPECL clock output to RTM derived from TCLK
219		OUT0/D7±, OUT1/D8±	9c, 9d, 9e, 9f	I/O	LVDS (Vcm 1.2V, Vdiff 350mV, 100R) trigger, interlock or user IO connected to the PL HP bank (1.8V)
220		AMC-CLK±	10e, 10f	O	LVDS/LVPECL output clock to RTM from RF synthesizer
221					
222					
223	J31 Radiall Connector	DAC-OUT0, DAC-OUT1, DAC-OUT2, DAC-OUT3	1a, 1b, 2a, 2b	O	Single-ended DAC outputs, AC coupling
224		ADC-IN6, ADC-IN7	3a, 3b	I	Single-ended ADC inputs, AC coupling
225					
226					
227	J32 Radiall Connector	ADC-IN0, ADC-IN1, ADC-IN2, ADC-IN3, ADC-IN4, ADC-IN5	1a, 1b, 2a, 2b, 3a, 3b	I	Single-ended ADC inputs, AC coupling

		Digital Clock IO	Digital Fixed IO	Digital Clock Input	Digital User IO		Differential DACs			MTCA.4 Management	
J30		10	9	8	7	6	5	4	3	2	1
-	F	AMC-CLK-	OUT1-/D8-	RF-CLK3-	DAC7-	D5-	DAC4-	D2-	DAC1-	TMS	TDO
+	e	AMC-CLK+	OUT1+/D8+	RF-CLK3+	DAC7+	D5+	DAC4+	D2+	DAC1+	TD1	TCK
-	d	RF-CLK2-	OUT0-/D7-	RF-CLK1-	D6-	DAC5-	D3-	DAC2-	D0-CC-	SCL	SDA
+	c	RF-CLK2+	OUT0+/D7+	RF-CLK1+	D6+	DAC5+	D3+	DAC2+	D0-CC+	MP	PS#
-	b	RF-CLK0-	AMC-TCLK-	RTM-CLK-	DAC6-	D4-	DAC3-	D1-	DAC0-	PWRB2	PWRB1
+	a	RF-CLK0+	AMC-TCLK+	RTM-CLK+	DAC6+	D4+	DAC3+	D1+	DAC0+	PWRA2	PWRA1
		Single Ended Analog Signals									
J31		3	2	1							
	B	ADC-IN7	DAC-OUT1	DAC-OUT3							
	A	ADC-IN6	DAC-OUT0	DAC-OUT2							
J32		3	2	1							
	B	ADC-IN1	ADC-IN3	ADC-IN5							
	A	ADC-IN0	ADC-IN2	ADC-IN4							

Courtesy of J. Zink

Zone 3 – Class RF1.1 pin assignment J30, J31, and J32 Connector, AMC side View.





Backup Slides

ZU47DR General Specification

FPGA Resources	Parameter	Value	Scale	Condition
Part Number	XCZU47DR-1FFVG1517E			
	ADC Tile Configuration	Dual		14-bit RF-ADC with DDC
	Number of ADC Tiles	4		
	Number of ADC Channels	8		
	ADC Max Rate	5	GSPS	
	DAC Tile Configuration	Dual		14-bit RF-DAC with DUC
	Number of DAC Tiles	4		
	Number of DAC Channels	8	-	
	DAC Max Rate	8.92 (9.85)	GSPS	
	Number of DDCs per RF-ADC	1	-	
	Analog Bandwidth	6	GHz	
	Decimation / Interpolation	1x, 2x, 3x, 4x, 5x, 6x, 8x, 10x, 12x, 16x, 20x, 24x, 40x	-	
	System Logic Cells	930	k	
	CLB LUTs	425	k	
	Max. Dist. RAM	13	Mb	
	Total Block RAM	38	Mb	
	UltraRAM	22.5	Mb	
	DSP Slices	4272	-	
	GTY Transceivers	16	-	
	PCIe Gen3 x16	-	-	
	PCIeGen3 x16/Gen4 x8 / CCIX	2	-	
	150G Interlaken	1	-	
	et MAC/PCS w/RS-FEC	2	-	
	System Monitor	2	-	
	Speed Grades	-1E	-	
	PSIO	214	-	
	HDIO	48	-	
	HPIO	299	-	
	GTR	4	-	
	GTY	16	-	
	Package Footprint	FFVG1517	-	
	Package size	40 x 40	mm^2	