An open source FPGA firmware framework (FWK) by DESY

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INTRODUCTION: What is FWK? Why use our FPGA framework?

- The development of modern FPGA firmware involves the integration of software/hardware CPUs, hardware description languages **(HDL)** modules, high-level synthesis **(HLS)** entities, and embedded Linux or bare-metal applications. This procedure is difficult and complex because it can involve modulus, tools from various vendors and hierarchical designs from different manufacturers.
- The procedure is further complicated by the requirement for long-term maintenance and repeatability for designs that may include several developers from research institutes like Deutsches Elektronen-Synchrotron (DESY).
- At DESY to address these challenges of FPGAs, we have created an open-source **FPGA firmware framework (FWK)** that simplifies development, promotes teamwork, and lowers complexity to address these issues.
- The initial iteration of the firmware framework was created in 2013 for MTCA.4 systems at EuXFEL [1]. Figure 1 depicts the initial idea of the FWK.
- FWK also generates documentation and address maps necessary for high-level software frameworks like ChimeraTK [2]. This work presents an overview and the idea of the FWK and its ongoing developments.
- The generation of address space descriptions is one of the challenging aspects of FPGA design. This framework simplifies this aspect by collecting address space information and creating address space trees. Our solution for tackling this challenge is **DesyRDL** which is an open-source tool that generates outputs for an address space defined by one or many SystemRDL [3] input files.
- FWK also supports custom Embedded Linux developments by introducing the **Yocto build** method [4] and publishing generic Yocto package feeds for various embedded FPGA architectures.

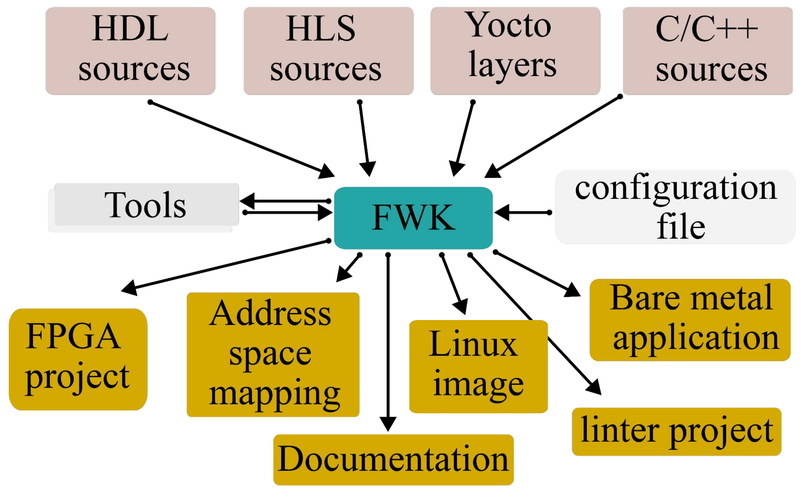

Figure 1: FWK concept and overall technology support

CONFIGURATION FILES: Tcl scripts

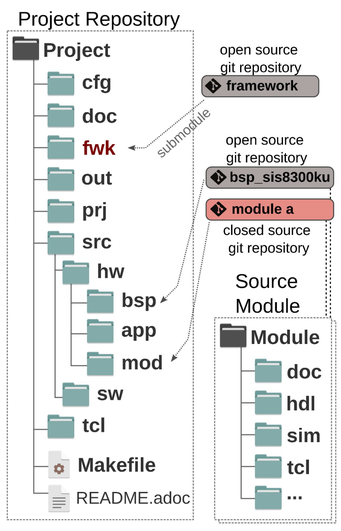

Figure 2: FWK project structure.

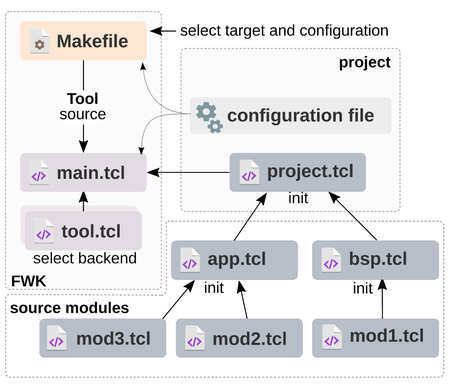

Figure 3: FWK Tcl scripts flow.

- The structure of scripts follows the hooks concept, ensuring that each module's functionality seamlessly integrates into the framework.
- The key folders include configurations, sources, build outputs, documentation, and scripts, with specific hardware, software, and Linux components subfolders. (Figure 2)
- Each project and source module must have a separate Tcl file for executing the creation and build procedures (Figure 3)

GENERAL STRUCTURE: FWK major components

- In the firmware framework, there are four major components:
  1) Framework module 2) Source modules 3) Main project 4) Vendor tools
- The framework is a set of scripts, functions, and procedures that combine all the input files needed to create a build system. The generated files are added to the project and become an integral part.
- Hardware/software source modules which are the blocks of functionality can be decoupled and abstracted from the rest of the project. Therefore, each module can have its own address space and can be shared among various projects. In FWK, a module code is structured as HDL, HLS, C/C++, or Yocto layers. The main project contains all the modules which bind together to produce outputs.
- All the supported components and tools are presented in Figure 4. For each project, a configuration file is required for defining the interface and variable sets including the project name, used technology, and hardware/software system configurations.

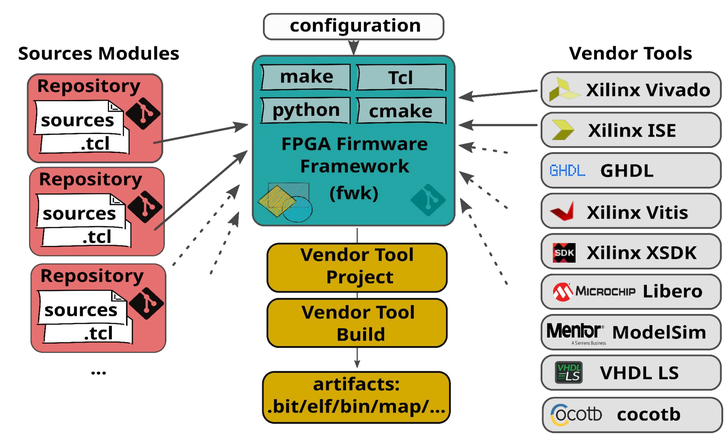

Figure 4: FPGA firmware framework major components.

ADDRESS SPACE: DesyRDL

- Address space description and generation are essential aspects of FPGA design and DesyRDL is our solution for address space management.
- Input files for DesyRDL are prepared by the FWK and are based on SystemRDL input files, which convert all address space formats to SystemRDL style.
- The address space backend translates the Tcl-based address tree into an actual address space description in a form understood by high-level software frameworks like ChimeraTK or bare-metal applications.
- This tool also generates documentation files, register-transfer level (RTL) files such as VHDL, or register models and abstractions used in the design verification.
- These address trees can be accessed by various managers, including embedded CPUs, over Ethernet, using direct memory access (DMA), or PCIe.
- Address space management procedures are depicted in Figure 5 and Figure 6.
- Available at: **https://pypi.org/project/desyrdl/**

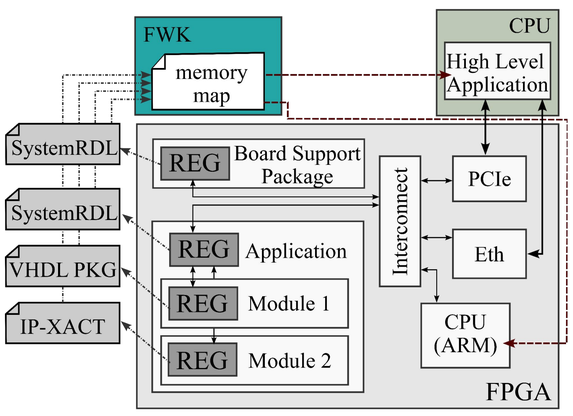

Figure 5: Collecting and compiling of address space by FWK.

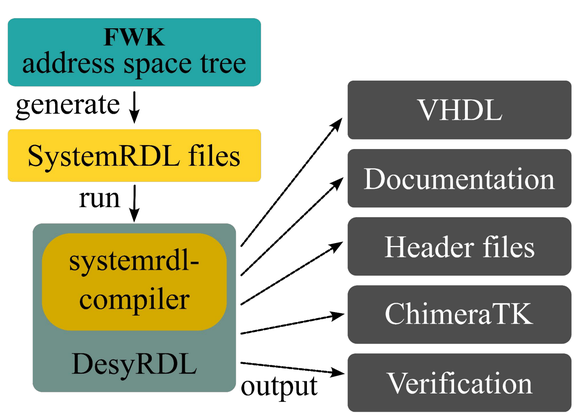

Figure 6: Generation of artifacts by DesyRDL tool.

CONTRIBUTION & COLLABORATION

- FWK is written and supported by many scientists and engineers in various research centers and universities (DESY, TUHH, Brookhaven National Laboratory, Synchrotron SOLEIL, MYRRHA, etc.)
- You can find numerous example designs for SoCs, MPSoCs, and FPGA systems on our web pages.

- FWK reference paper:
  - **THE DESY OPEN SOURCE FPGA FRAMEWORK [5]**
- FWK home webpage (We are open to your contribution!):
  - **https://gitlab.desy.de/fpgafw/fwk**
- FWK Documentation:
  - **https://fpgafw.pages.desy.de/docs-pub/fwk/index.html**

FWK
FPGA firmware framework

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HELMHOLTZ RESEARCH FOR GRAND CHALLENGES

MSK. Maschine Strahlkontrollen

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MTARD

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