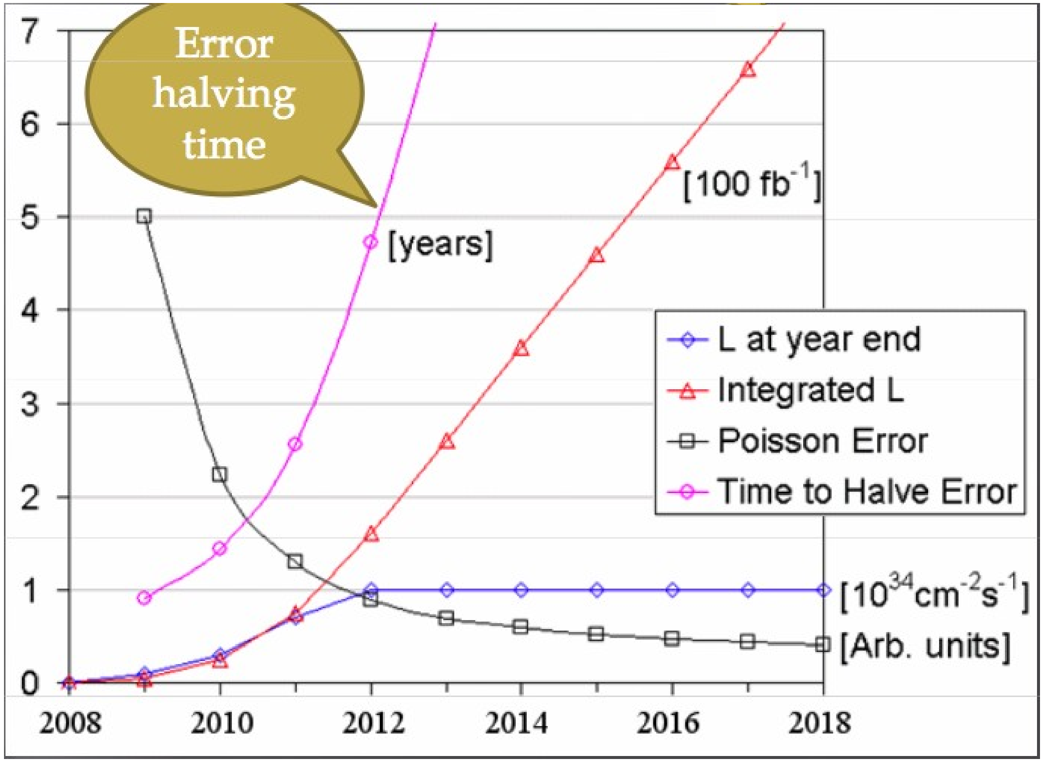
ATLAS Upgrade

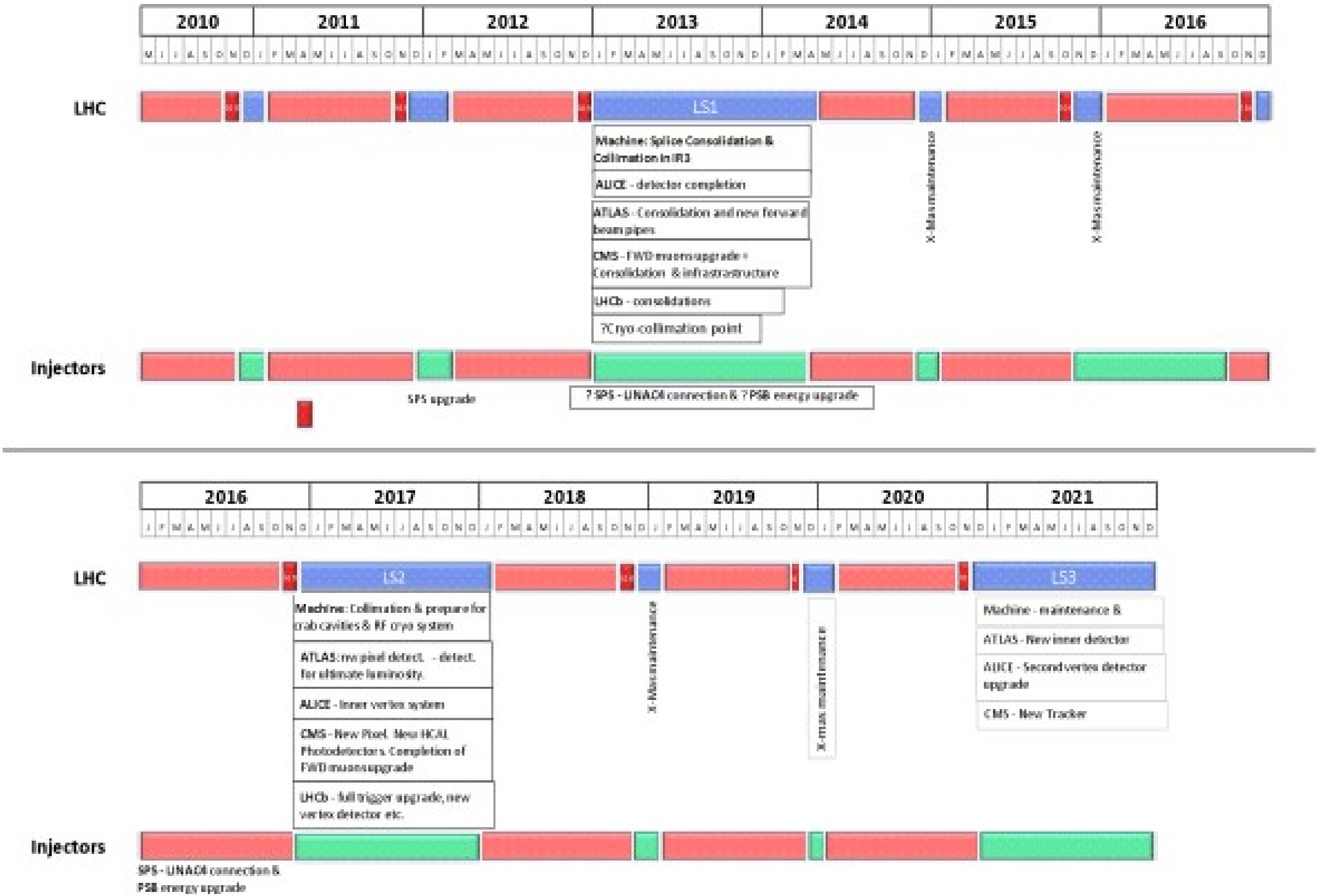
Daniel Muenstermann

Why Upgrades?

- LHC has a design luminosity of 10^{34} cm^{-2} s^{-1} and shall collect 730 fb^{-1}
- With unprecedented energy and luminosity, LHC is a 'discovery machine' for the Higgs, SUSY-particles, …
- After each discovery, measurements with more statistics must follow...
  - Why not use a well-understood detector and the existing collider?
- Higher statistics needs 'long^2' at constant luminosity
  - → **more** luminosity
  - → **s**LHC/HL-LHC



Updated LHC schedule



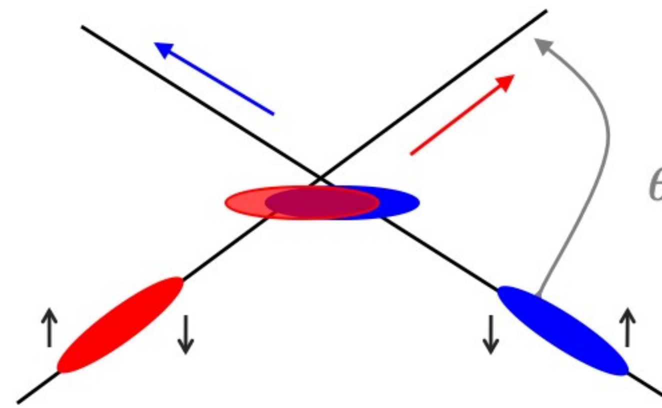
Upgrading: step by step...

2009	Start of LHC
	Run 1: 7 TeV centre of mass energy, luminosity ramping up to few 10^{33} cm^{-2} s^{-1}, few fb^{-1} delivered
2013/14	LHC shut-down to prepare machine for design energy and nominal luminosity ATLAS Phase-0 upgrade
	Run 2: Ramp up luminosity to nominal (10^{34} cm^{-2} s^{-1}), ~50 to 100 fb^{-1}
2017 or 18	Injector and LHC Phase-I upgrades to go to ultimate luminosity
	Run 3: Ramp up luminosity to 2.2 x nominal, reaching ~100 fb^{-1} / year accumulate few hundred fb^{-1}
~2021/22	Phase-II: High-luminosity LHC. New focussing magnets and CRAB cavities for very high luminosity with levelling
	Run 4: Collect data until > 3000 fb^{-1}
2030	ILC, High energy LHC, ... ?

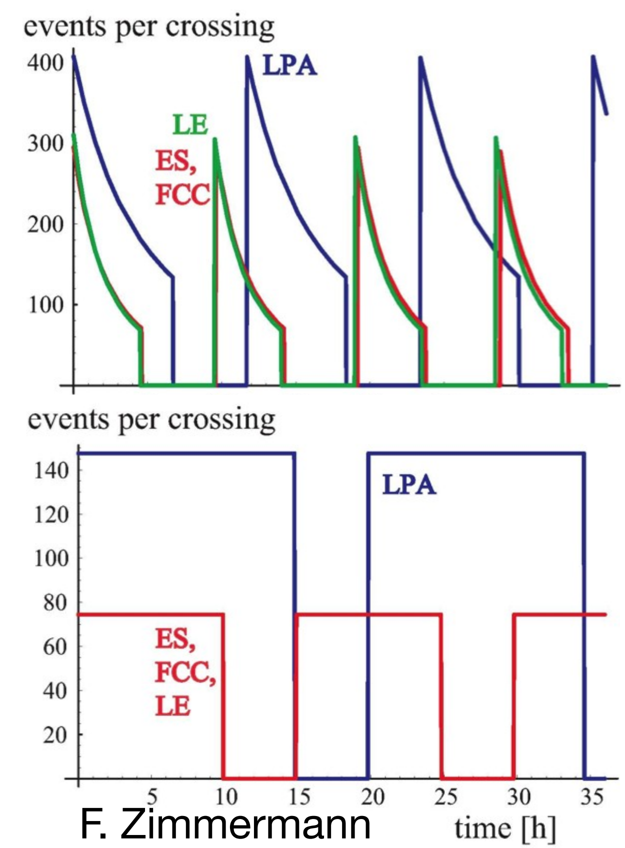
N. Hessey

How could sLHC fluences be reached?

- Accelerator-wise, there are several ways to reach luminosities beyond 10^{34} cm^{-2} s^{-1}
- Most favoured by the experiments: Full Crab Crossing (FCC) with 25 ns bunch spacing
  - no changes of the 40 MHz collision frequency
  - still up to 300 pile-up events per bunch crossing!



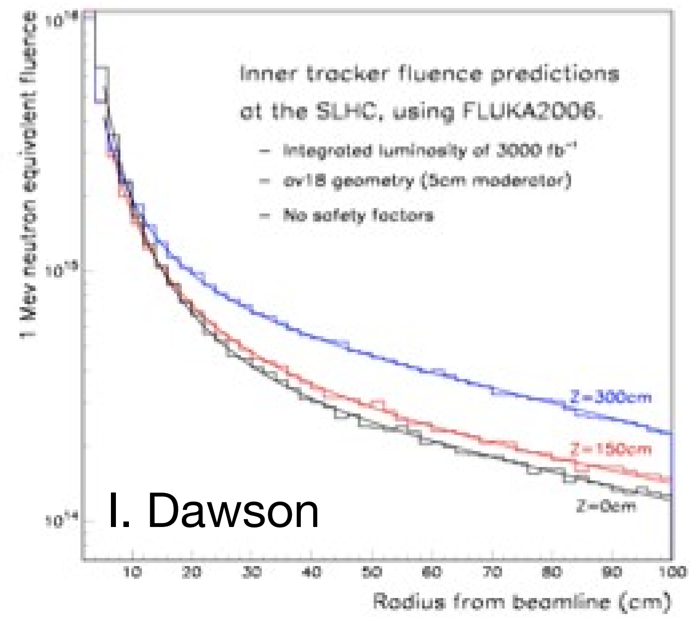
- Luminosity levelling might reduce this number to around 100 pile-up events per bunch crossing
- Consequences:
  - ➔ higher data rates
  - ➔ higher occupancy
  - ➔ more radiation damage
- Detector upgrades are necessary due to all items:
  - improved TDAQ
  - finer granularity to limit occupancy
  - more rad-hard sensors and electronics

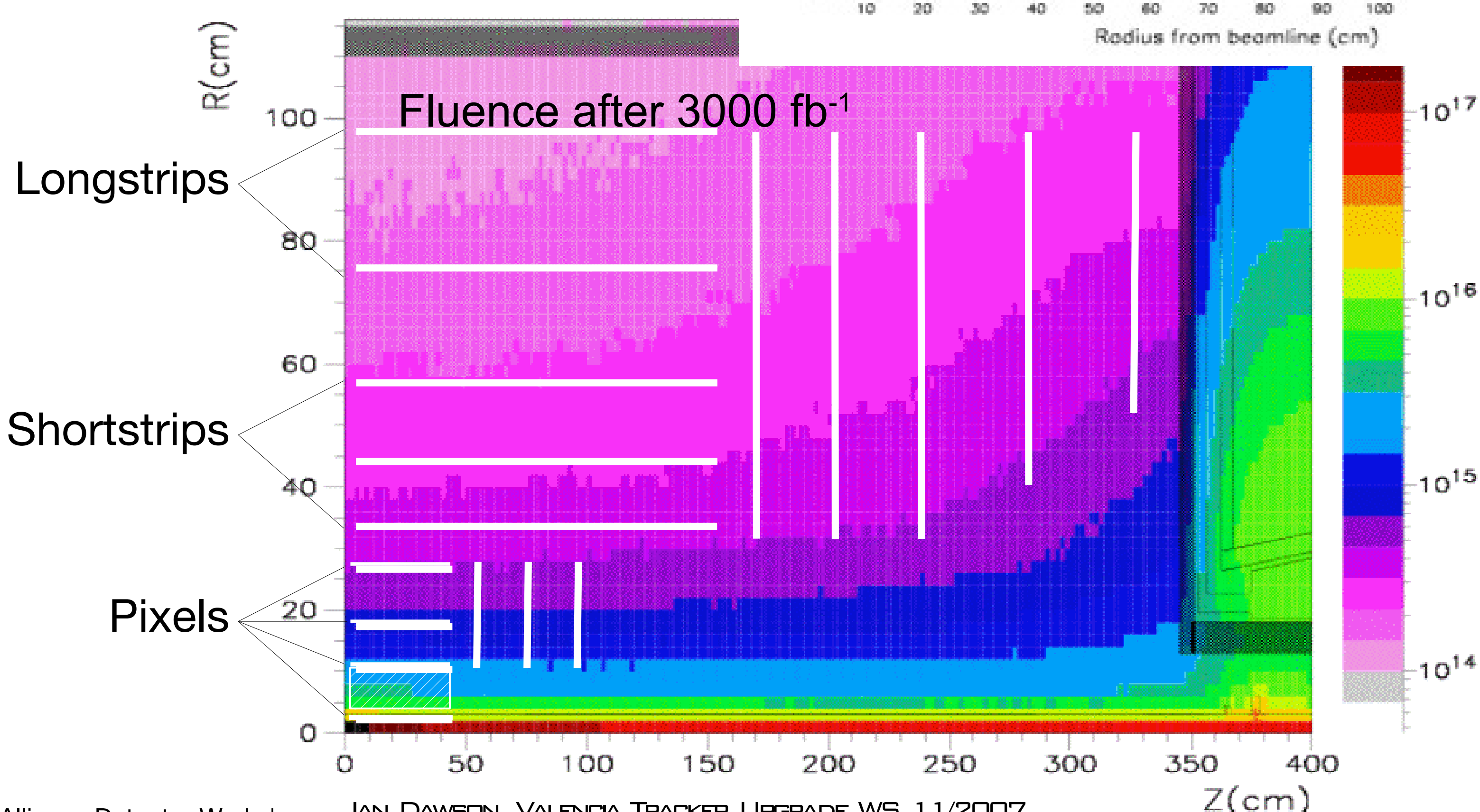


F. Zimmermann

Fluences at sLHC

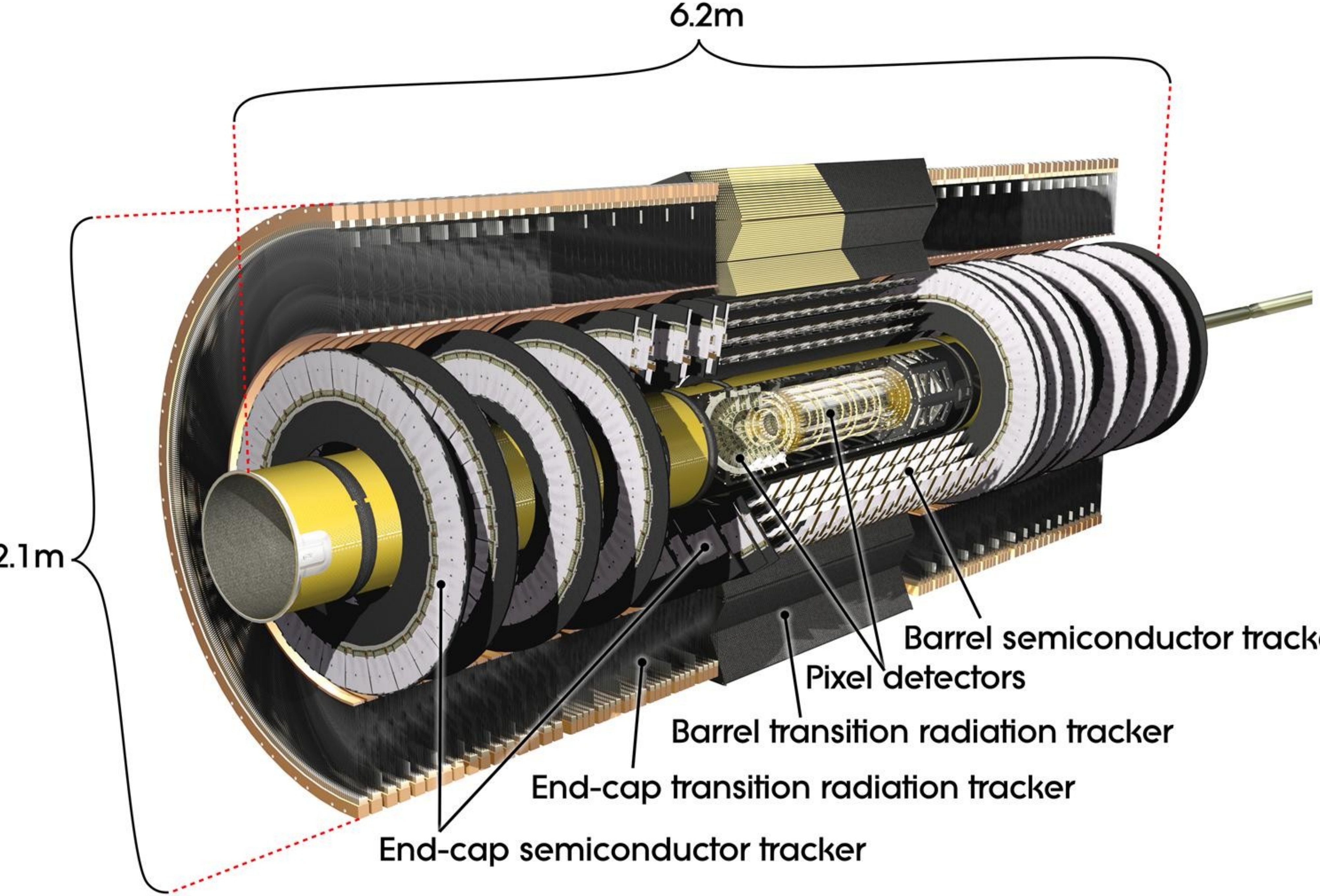
- integrated luminosity for sLHC: 3000 fb^{-1}
- including a safety factor of 2 to account for all uncertainties this yields the following fluences:
  - $2 \cdot 10^{16}$ n_{eq} cm^{-2} at 3.7 cm radius
  - up to 10^{15} n_{eq} cm^{-2} at 30 cm radius
  - > 10^{14} n_{eq} cm^{-2} at the outer tracker radius



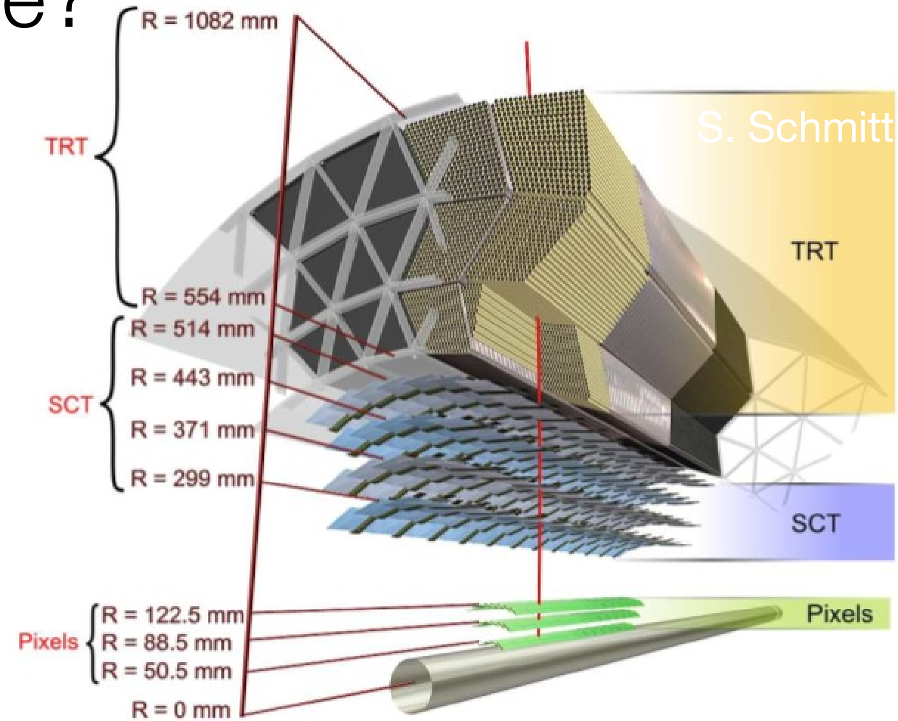


Ian Dawson, Valencia Tracker Upgrade WS 11/2007

Current ATLAS Tracker...



What/How/When to upgrade?



- Main challenges:
  - occupancy
  - radiation damage
  - data rate/trigger rate
- Components needing upgrades:
  - TRT
    - occupancy-limited beyond about $2 \cdot 10^{34}$ cm^{-2} s^{-1}
      → replace by all-silicon inner tracker
  - SCT
    - radiation damage limited (p-in-n sensors collect holes → n-in-p to collect e$^-$)
    - occupancy limited (long strips → replace inner layers by short strips)
  - Pixel
    - radiation damage limited (?) for innermost layers → sensor R&D
    - data rate limited (inefficiency expected in b-layer above $3 \cdot 10^{34}$ cm^{-2} s^{-1})
      → replace with new readout chip
- Current tracker able to cope with “ultimate” LHC, but requires complete replacement for sLHC
- Upgrades leading to physics improvements could be done before!

Upgrading: ATLAS

2009 — Start of LHC

Run 1: 7 TeV centre of mass energy, luminosity ramping up to few 10^{33} cm^{-2} s^{-1}, few fb^{-1} delivered

2013/14 — LHC shut-down to prepare machine for design energy and nominal luminosity ATLAS Phase-0 upgrade

nSQP, IBL

Run 2: Ramp up luminosity to nominal (10^{34} cm^{-2} s^{-1}), ~50 to 100 fb^{-1}

2017 or 18 — Injector and LHC Phase-I upgrades to go to ultimate luminosity

new Pixel??

Run 3: Ramp up luminosity to 2.2 x nominal, reaching ~100 fb^{-1} / year accumulate few hundred fb^{-1}

~2021/22 — Phase-II: High-luminosity LHC. New focussing magnets and CRAB cavities for very high luminosity with levelling

full Tracker replacement

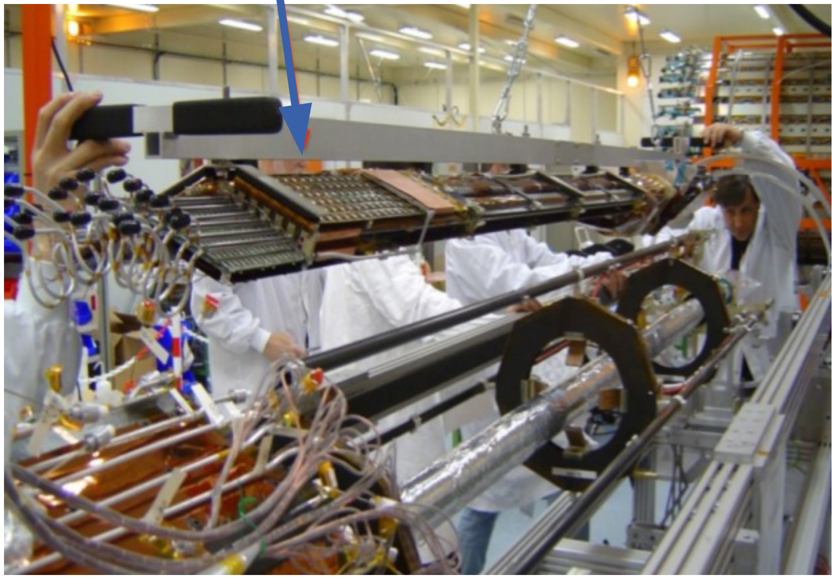
Run 4: Collect data until > 3000 fb^{-1}

2030 — ILC, High energy LHC, ... ?

N. Hessey

Anticipating failures: the nSQP project

- The Service Quarter Panels are located adjacent to the pixel detector and house the so-called Optoboards where the transition from LVDS to optical data transmission is made

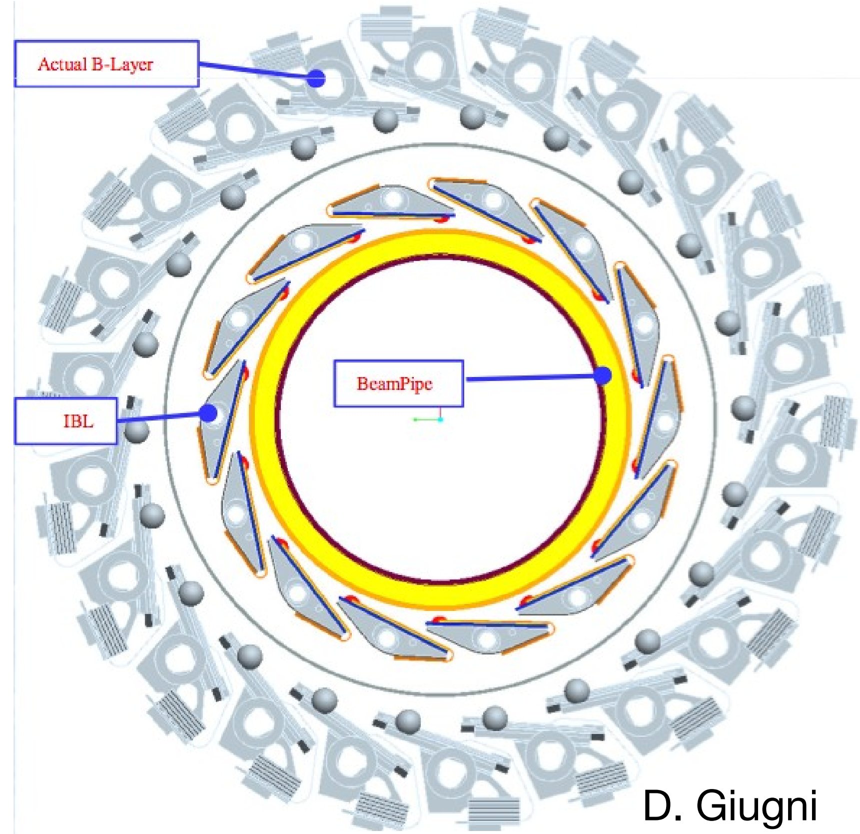


- VCSEL lasers identical to those used in the Optoboards exhibited series failures in off-detector positions
  - multiple causes assumed: humidity, ESD, …
  - up to now no on-detector (Optoboard) failures!
- Optoboards are currently in an position inacessible during maintenance shutdowns
  - move them outside of the ID endplate
  - bridge the distance by LVDS

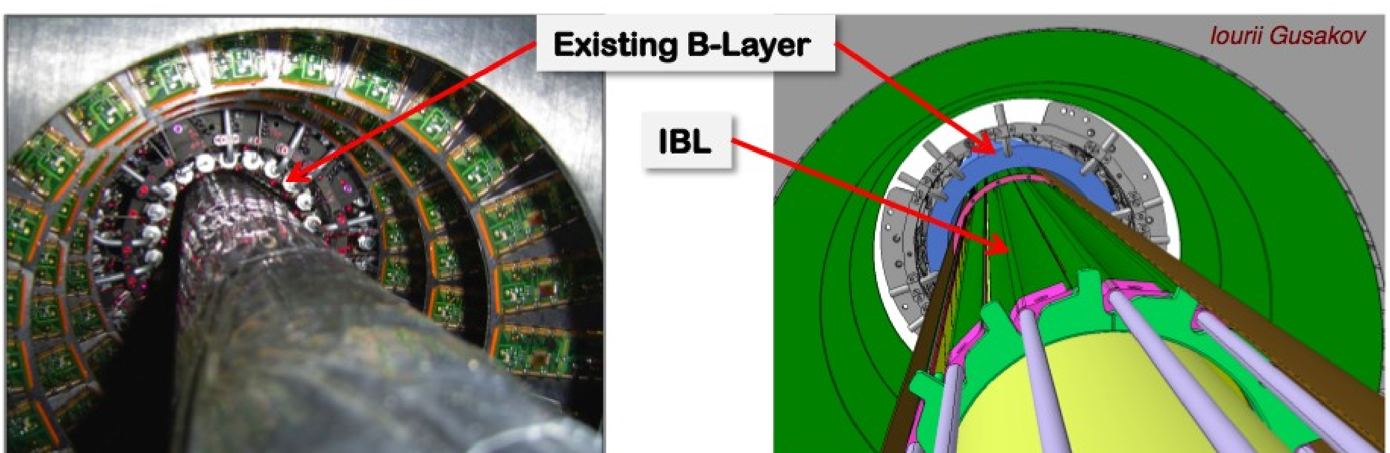
→ new Service Quarter Panel project
  - replace Optoboards by E-boards
  - qualify rad-hard LVDS driver ICs
  - re-build Service Quarter Panels as there will be no time to recycle the old structures and cables

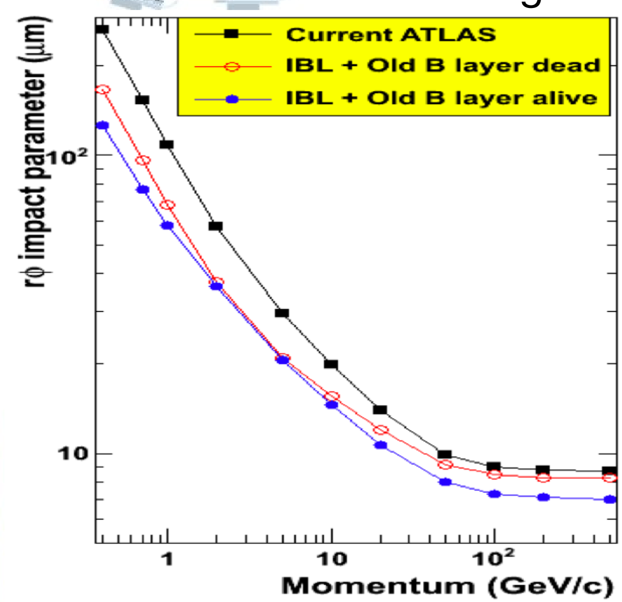
A 4th pixel layer: IBL

- Idea:
  - exchange beampipe with thinner one
  - use additional space for a 4th pixel layer: Insertable B-Layer (IBL)
- The IBL fulfills several functions:
  - improved determination of secondary vertices → better b-tagging
  - 'hot spare' stand-in for a possibly deteriorating b-layer
  - 4th pixel hit → improved tracking cuts
- (New) timescale: be ready for installation in 2013



D. Giugni



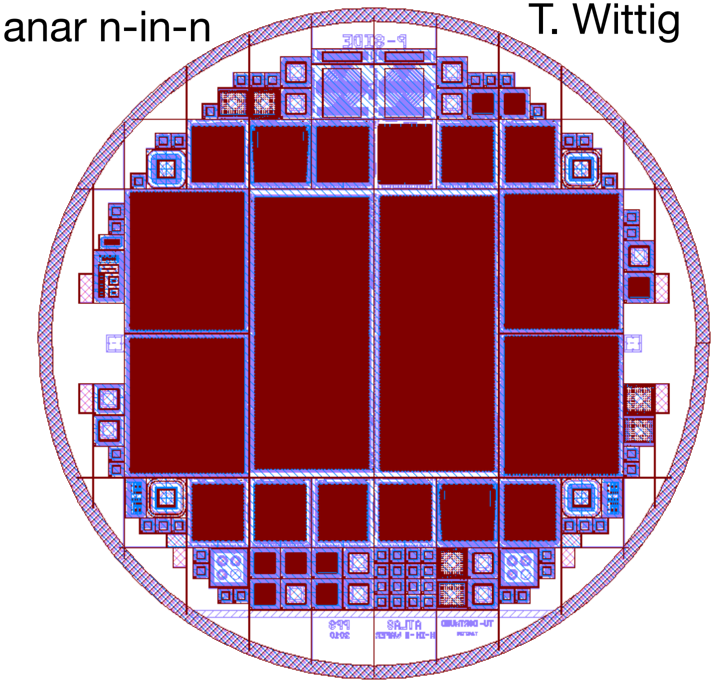


IBL Sensor qualification

- IBL requirements:
  - qualification fluence: $5 \cdot 10^{15}\ n_{eq}\ cm^{-2}$
  - qualification dose: 200 MRad
- Due to the very aggressive time schedule for installation in 2013, only two sensor options are able to comply with the production plan
  - planar n-in-n
  - 3D DDTC
- IBL-type sensors from these technologies have been manufactured
- An extensive test programme with FE-I4 assemblies has started
  - FE-I4 flip-chipping
  - irradiations
  - test-beam comparison
- Based on these results, the IBL sensor will be chosen in mid-2011

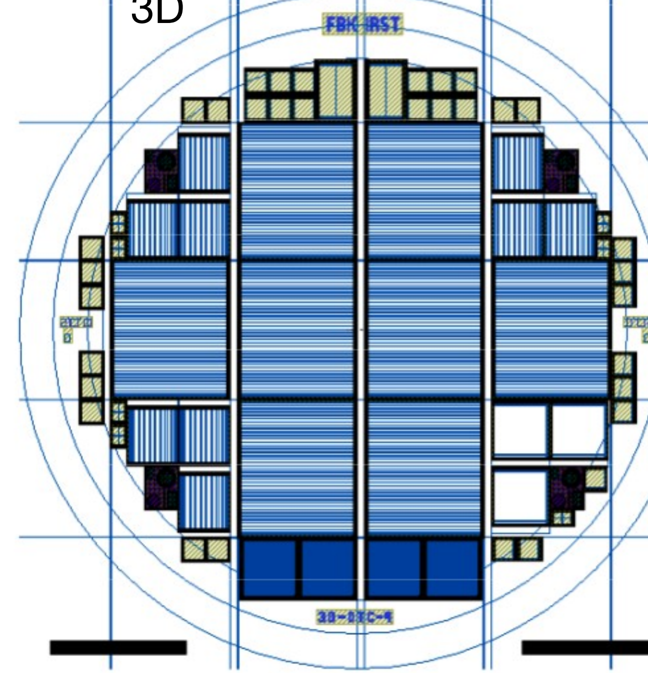
planar n-in-n

T. Wittig



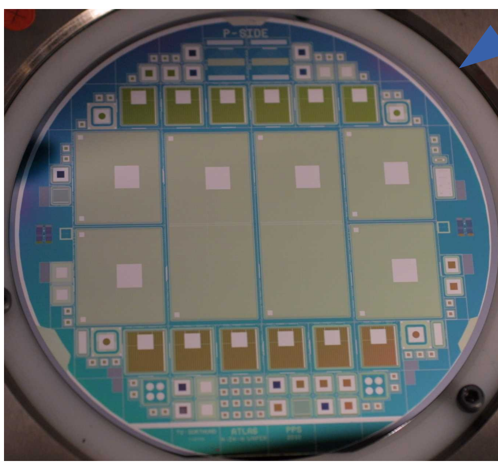
3D

C. da Via

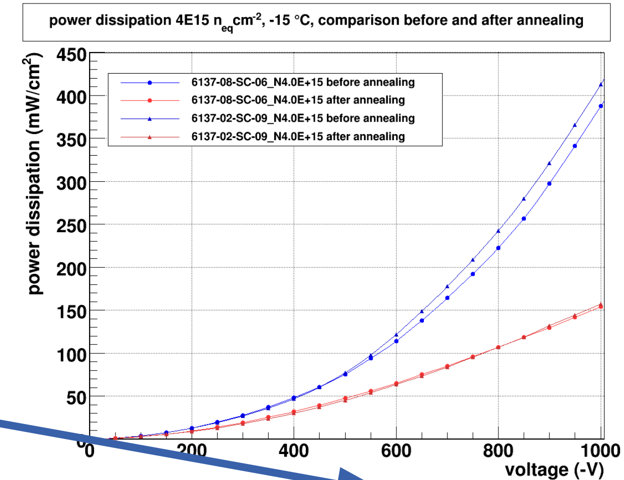


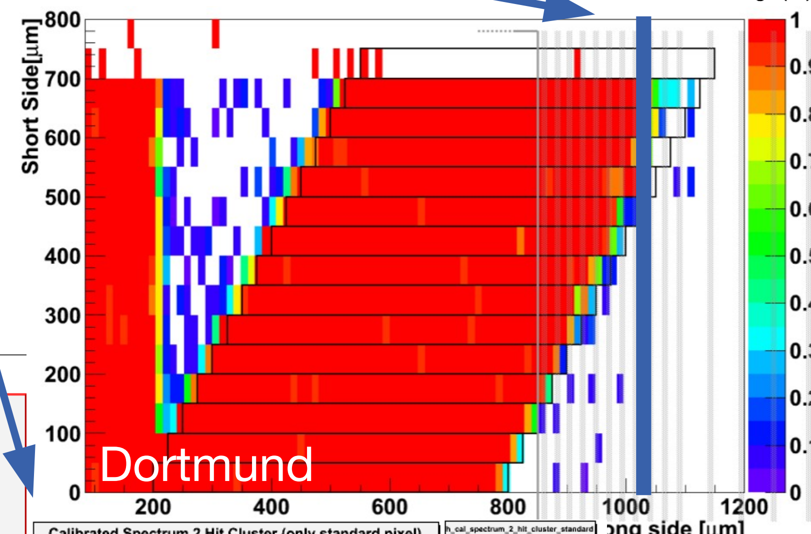
Planar Sensors for IBL

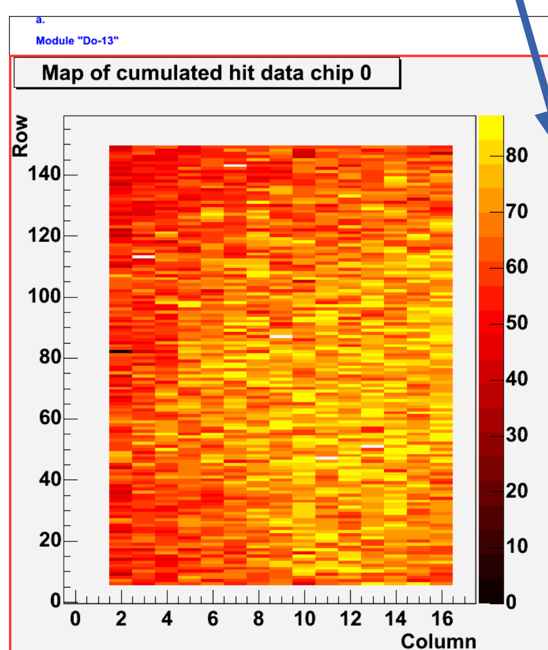
- IBL specifications to qualify:
  - ✔ Power dissipation < 200 mW/cm²
  - ✔ Leakage current < 100 nA/pixel
  - ✔ Inactive edges < 450 µm (actually ~250 µm)
  - ✔ Operation possible with -15°C on sensor
  - ✔ Thickness between 150 and 250 µm

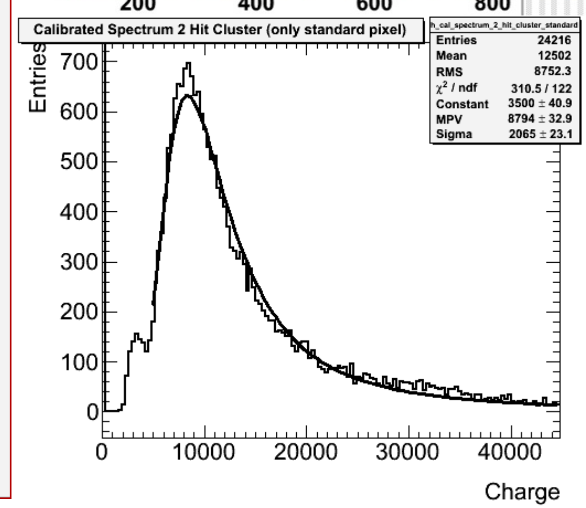


thickness	wafers ordered	wafers received
250um	12	18
225um	6	11
200um	6	10
175um	6	11
150um	6	8



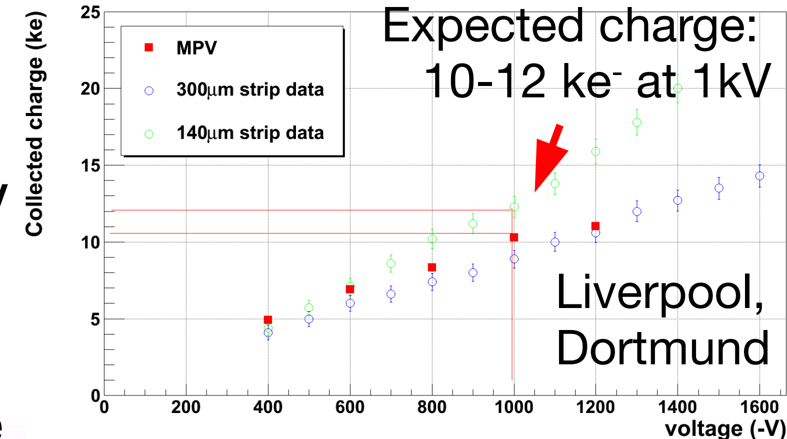


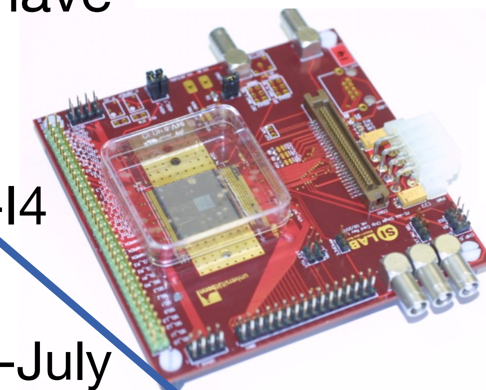




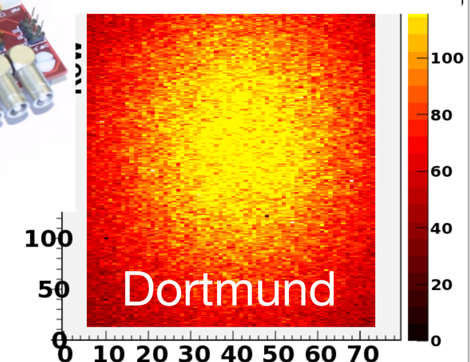
Planar Sensors for IBL

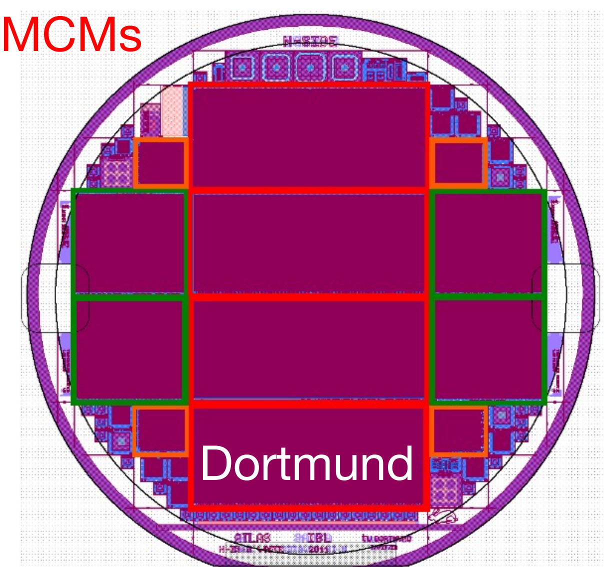
- Planar sensors have been shown to yield more than 10 ke$^-$ after $5 \cdot 10^{15}$ n_{eq}/cm^2 at 1 kV
  - should be sufficient for good hit efficiency with FE-I4 which will be demonstrated soon
- Several IBL sensor qualification wafers have been produced very successfully
  - high yield, ~200-250 µm inactive edge
  - thresholds below 3 ke$^-$ possible with FE-I4
- Planar IBL (pre-)production ongoing
  - delivery of > 50 wafers expected by mid-July
  - wafer design has already been submitted
    - 4 FE-I4 2x1 MCMs
    - 4 FE-I4 SCs
    - 4 FE-I3 SCs



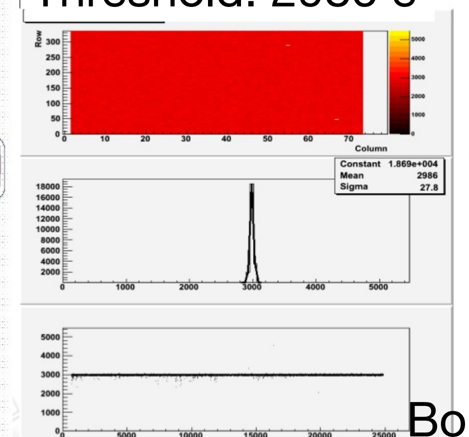


FE-I4 module with Sr-90 source

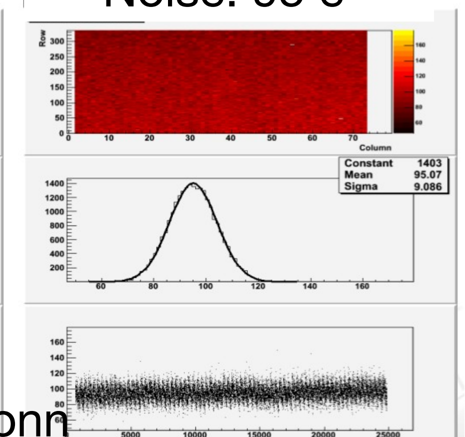




Threshold: 2986 e$^-$



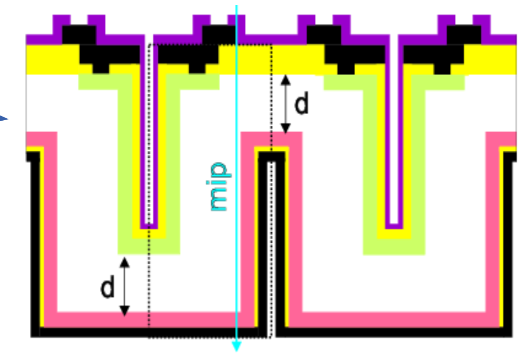
Noise: 95 e$^-$

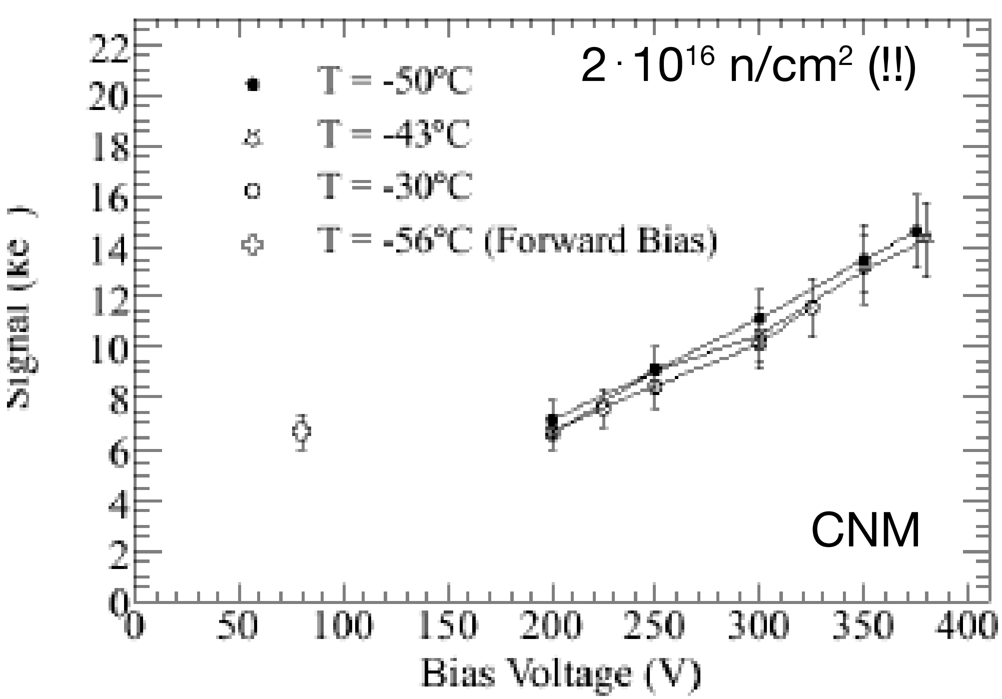


ATLAS Upgrade

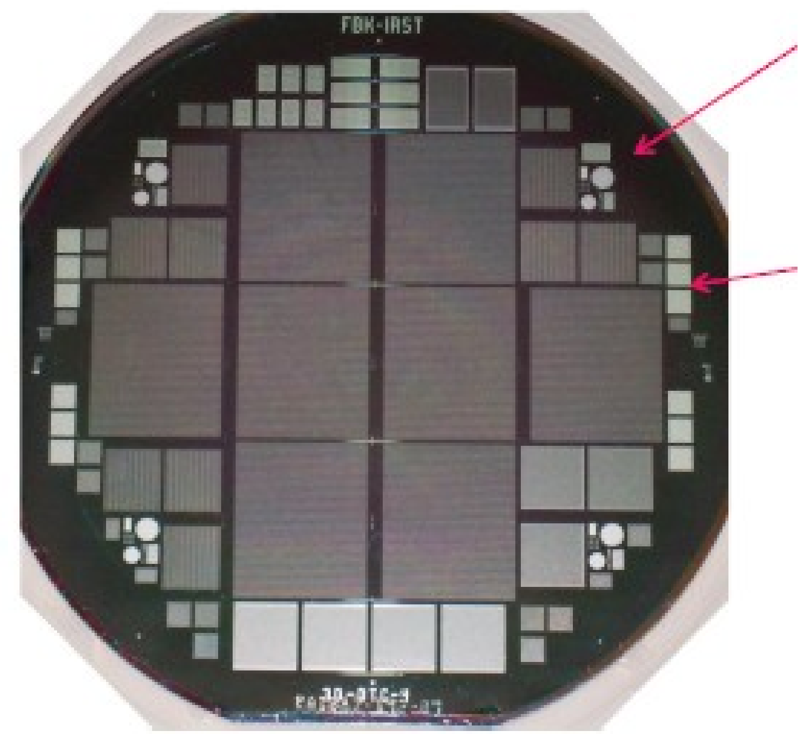
3D sensors for IBL

- For Fast-Track IBL 3D chose double-side 3D to reduce complexity
- Will be fabricated with 200 microns guard fences and a thickness of 230 microns.
- Double sided with deep column proved good radiation hardness performance with moderate bias voltage (120-150V at $5 \cdot 10^{15}$ n/cm^2) and power dissipation of 34 mW/cm^2 at $5 \cdot 10^{15}$ n/cm^2 at -10°C





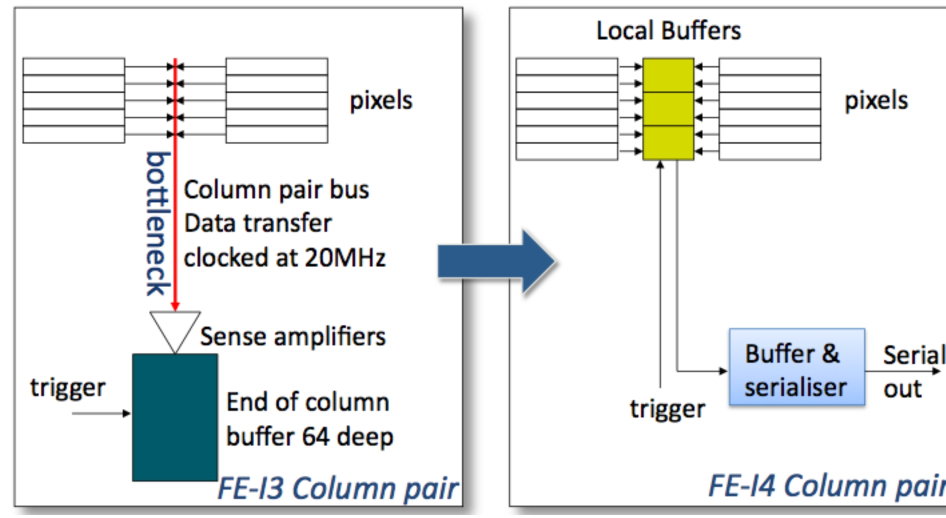
Completed FBK-wafer

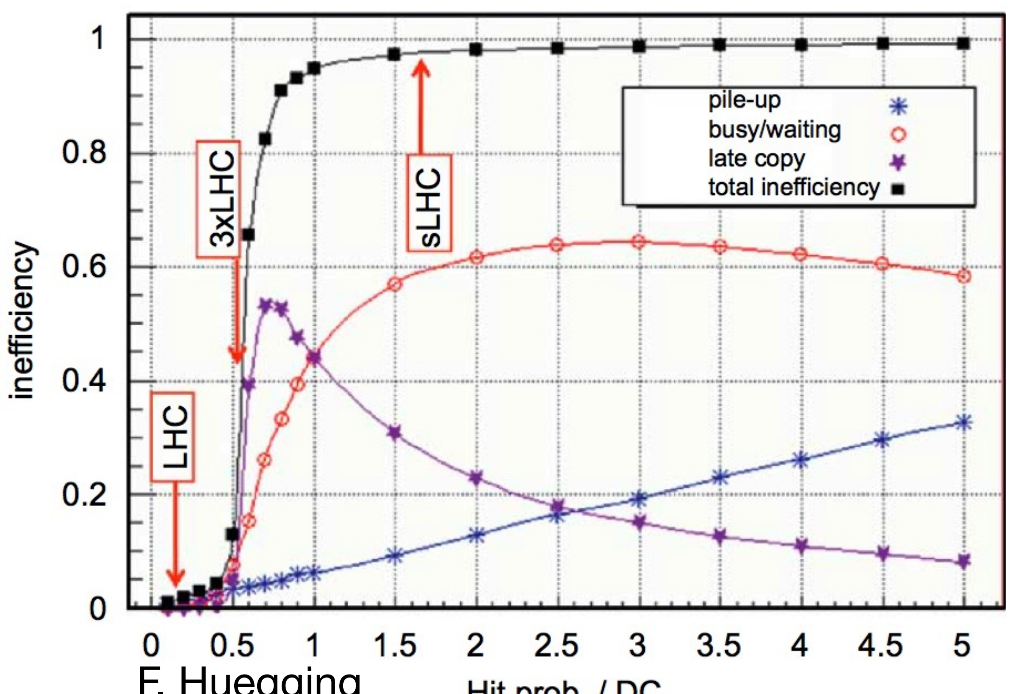


IBL electronics: FE-I4

- FE-I3 inefficient beyond $3 \cdot 10^{34}$ cm^{-2} s^{-1} due to congested DC-bus
- FE-I4 assets:
  - local memory cells (no bus activity except for readout
  - larger active fraction
  - higher data rate
  - more radiation hard (130 nm)
- Works quite well
- FE-I4B submission in summer

G. Darbo



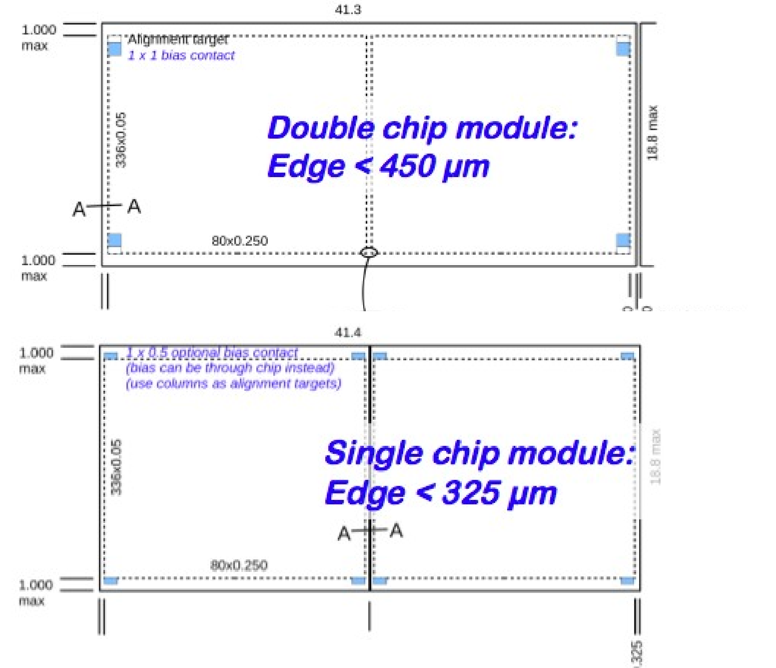


F. Huegging

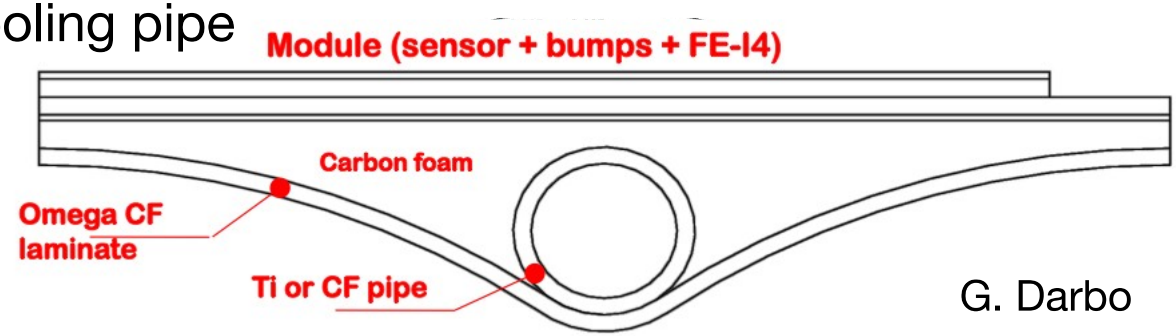
	FE-I3	FE-I4
Pixel size [μm^2]	50x400	50x250
Pixel array	18x160	80x336
Chip size [mm^2]	7.6x10.8	20.2x19.0
Active fraction	74%	89%
Analog current [μA/pix]	26	10
Digital current [μA/pix]	17	10
Analog Voltage [V]	1.6	1.5
Digital Voltage [V]	2.0	1.2
Pseudo-LVDS out [Mb/s]	40	160

IBL staves

- very little space → low-profile stave
- X/X_0 very important → lightweight stave
  - carbon foam
  - no shingling, but flat arrangement of detector modules
    - 3D : SingleChip modules (1 FE-I4 per sensor)
    - Planar: 'slim edges' (<450 µm inactive edge): MultiChip modules (2 FE-I4 per sensor)
  - Baseline: single Titanium cooling pipe
  - CO_2 cooling



M. Garcia-Sciveres

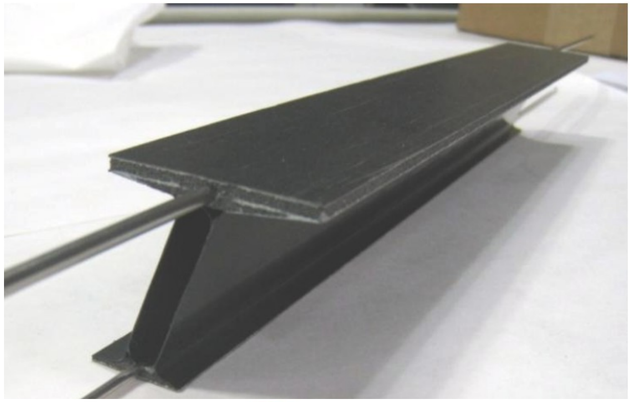


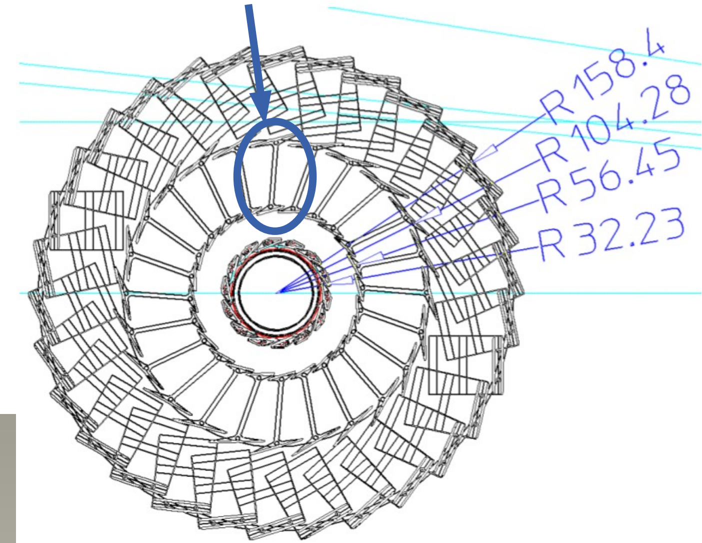
G. Darbo

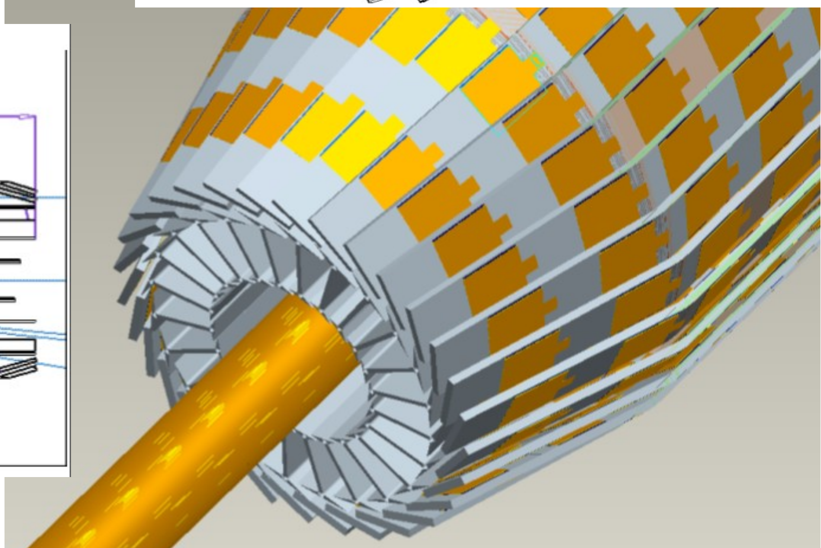
D. Giugni

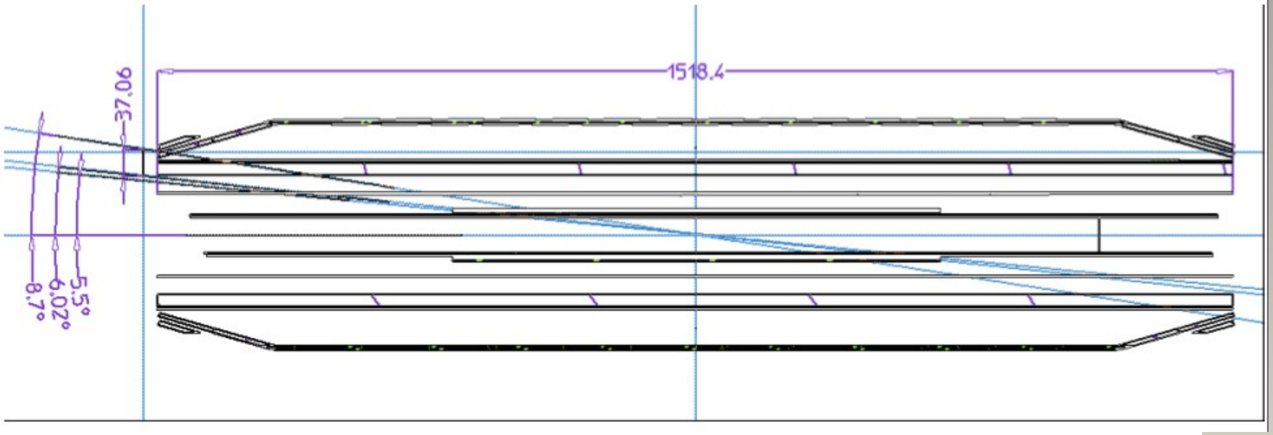
2017: A case study

- The delay of the second long shutdown to 2017 would grant the opportunity to build and install a new Pixel detector which could offer
  - improved physics capabilities: lower X/X0, better b-tagging, granularity, …
  - replacement of already aged detector
- Design would rely on FE-I4 chip and already existing options for cooling and mechanics drastically reducing the cost
- Case study to explore the feasibility and performance improvements is currently underway



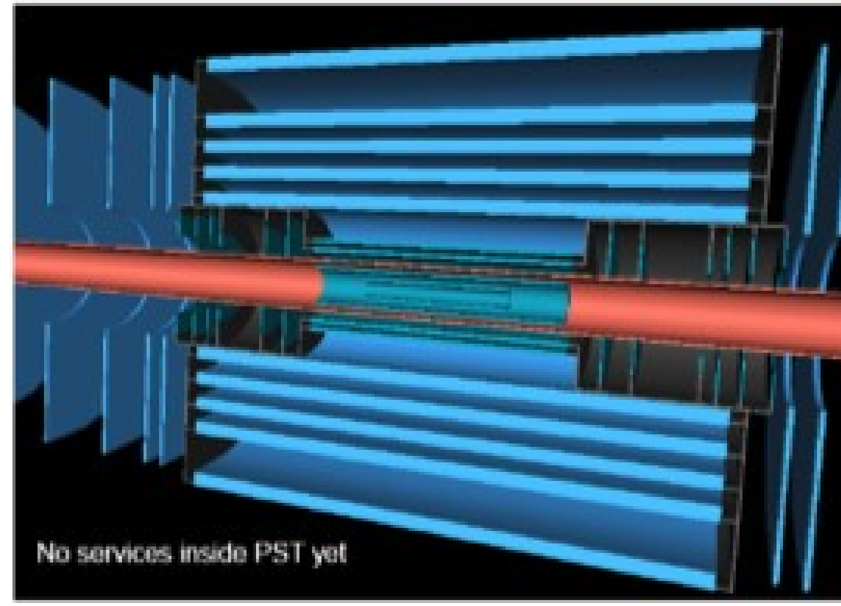


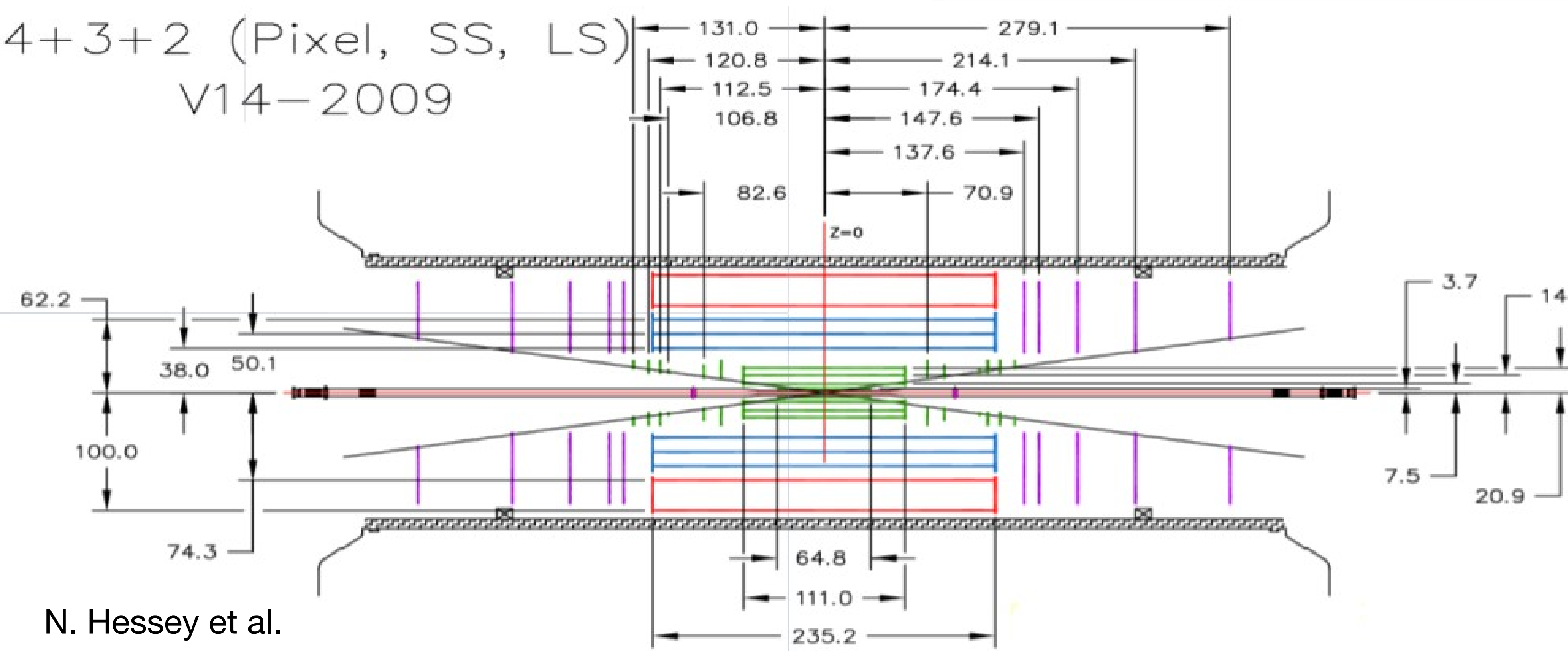




Upgrades for sLHC/HL-LHC

- All-silicon tracker:
  - 2 longstrip-layers
  - 2-3 shortstrip-layers
  - 4-5 pixel-layers
- Dedicated Track-Trigger-layers being discussed





N. Hessey et al.

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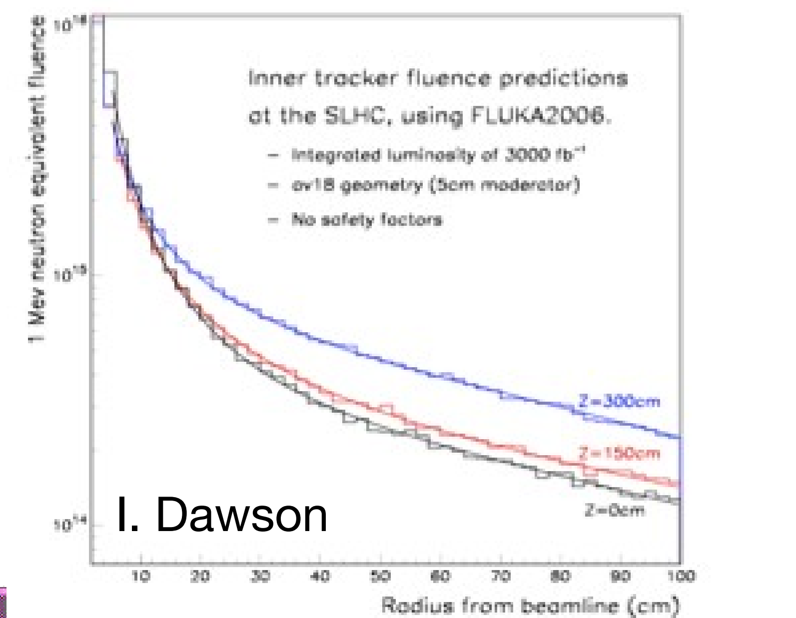
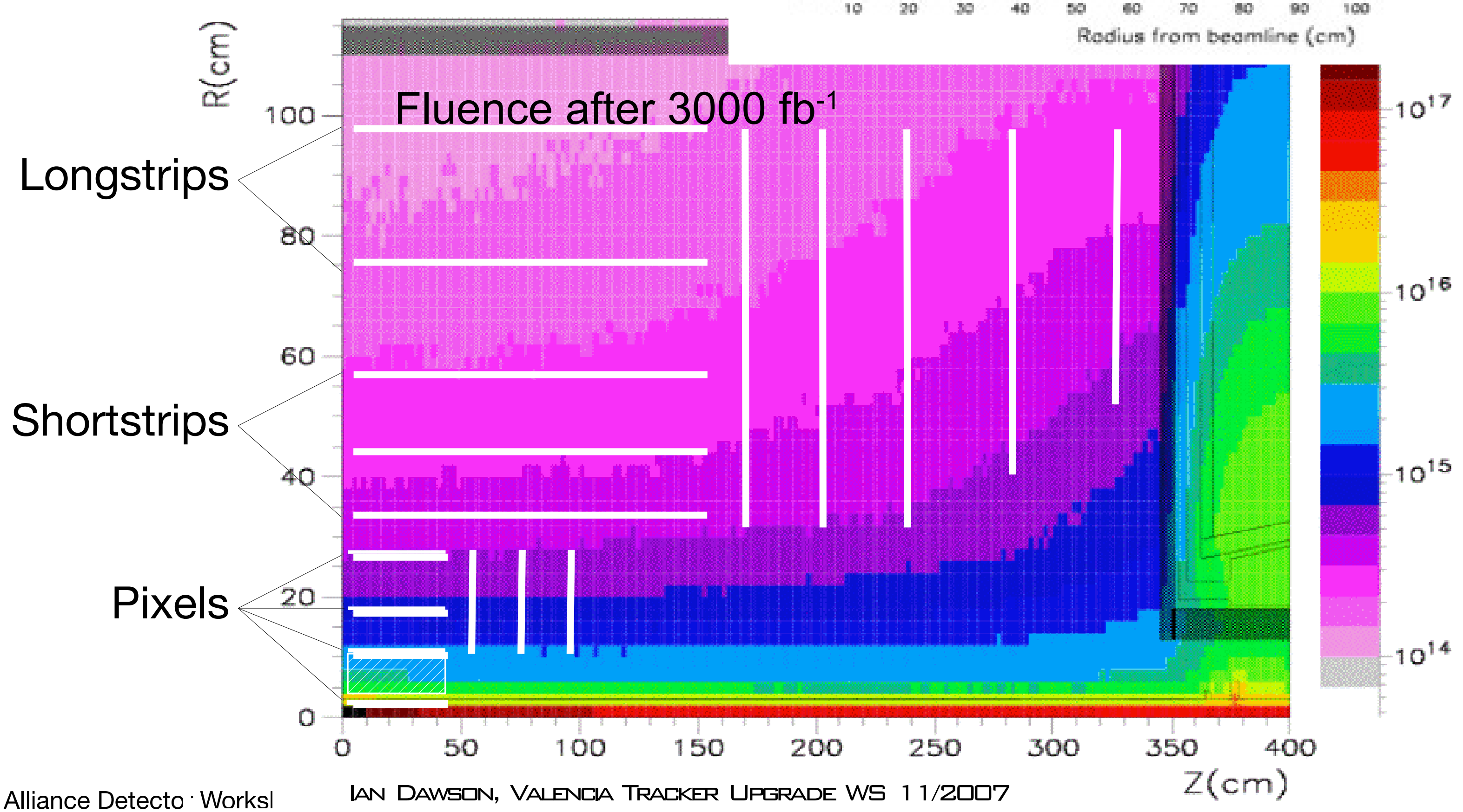
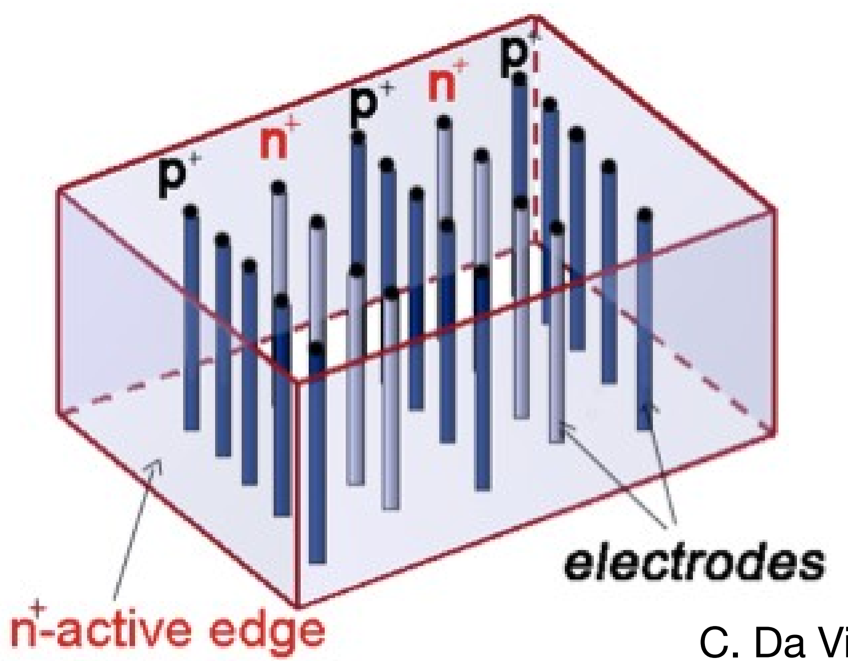


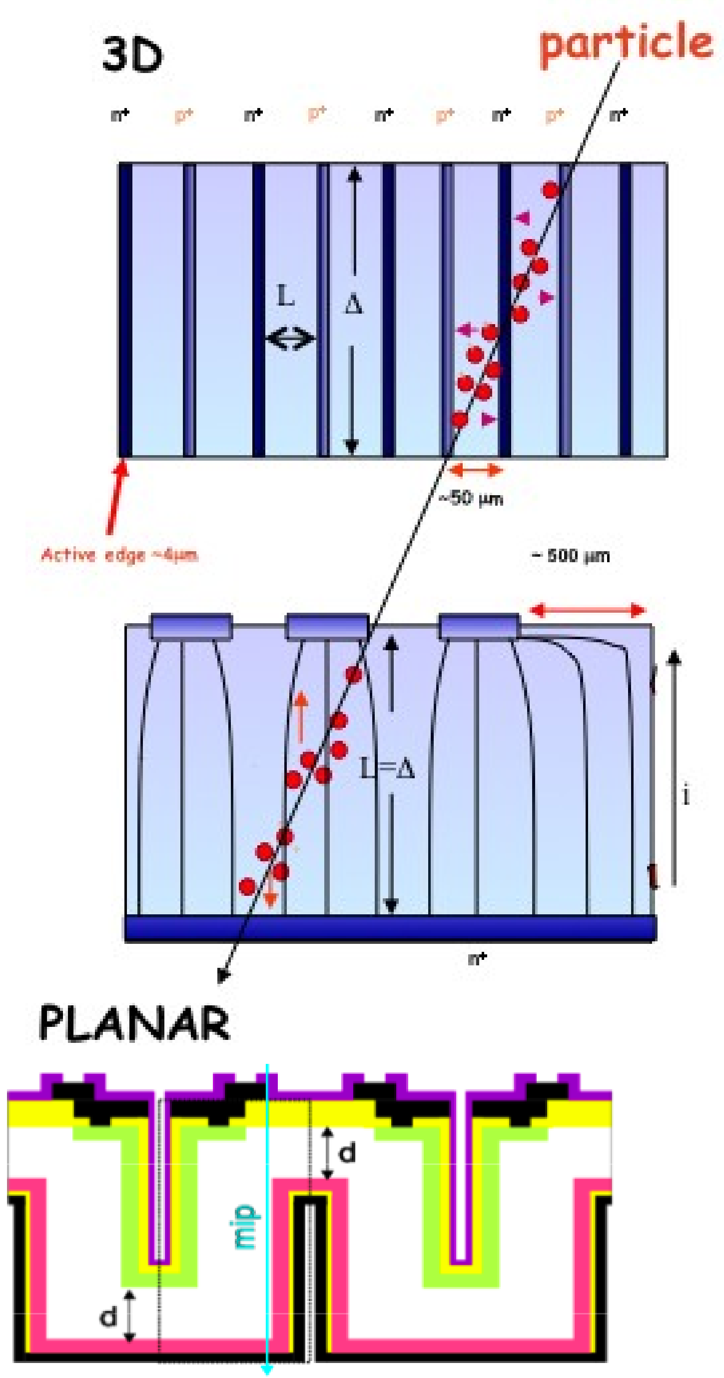


Ian Dawson, Valencia Tracker Upgrade WS 11/2007

Innermost sensors: 3D

- Main cause for the decrease of collected charge above 10^{15} n_{eq} cm^{-2}: trapping
- Possible amendment: Shorter drift distances
  → 3D-electrodes realised with DRIE-etching
- Several manufacturing methods and facilities established:
  - Double-sided Double-Type Columns (DDTC)
  - Full-3D with active edges

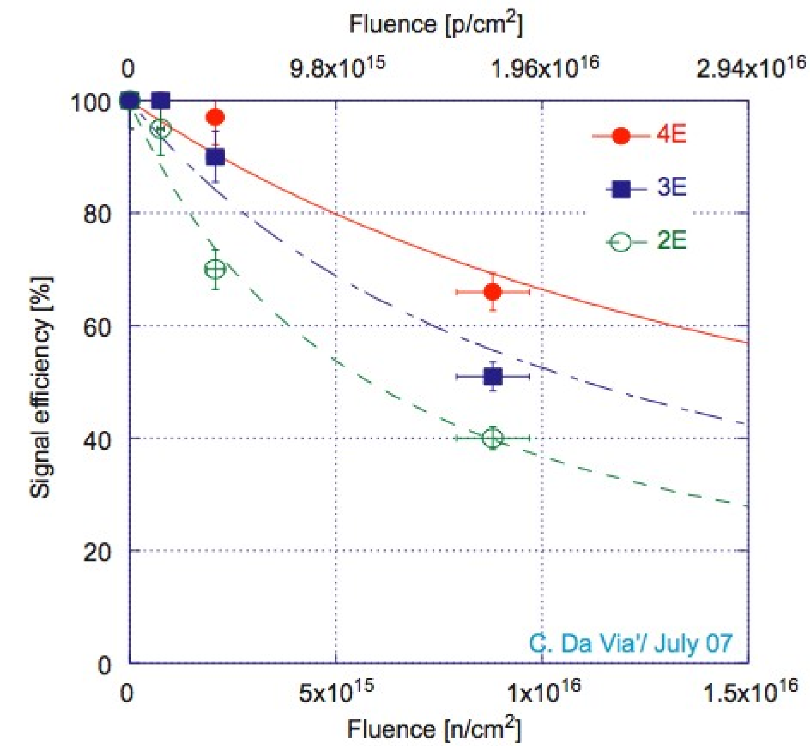


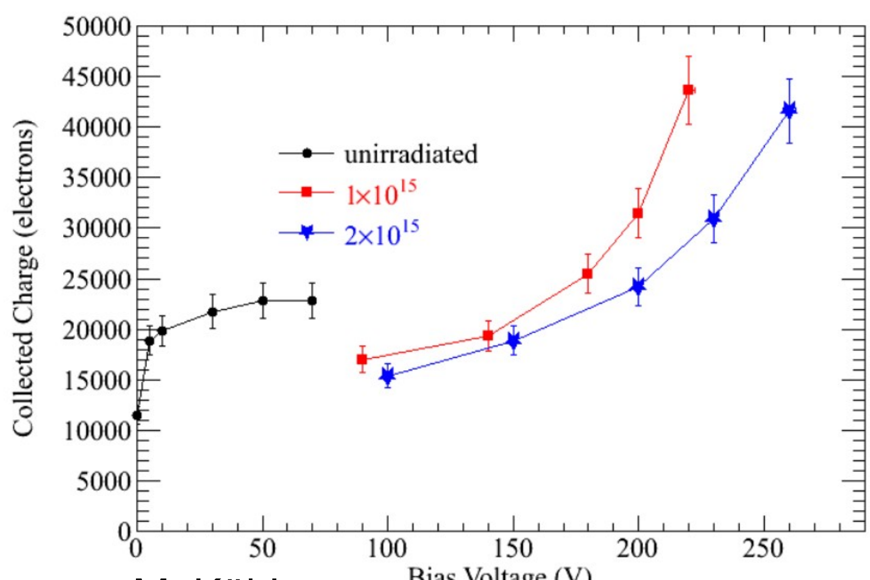


C. Da Via

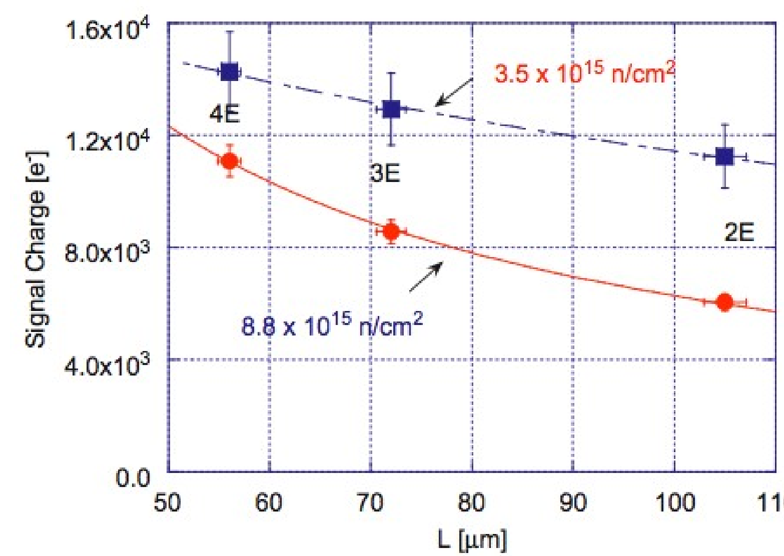
Innermost sensors: 3D

- Instead of 250 μm drift length only 55 to 105 μm
  → less trapping, better CCE
- Charge amplification observed
  → apparently general phenomenon of highly irradiated silicon
- Challenges:
  - production yield
  - capacitance
    → noise, threshold





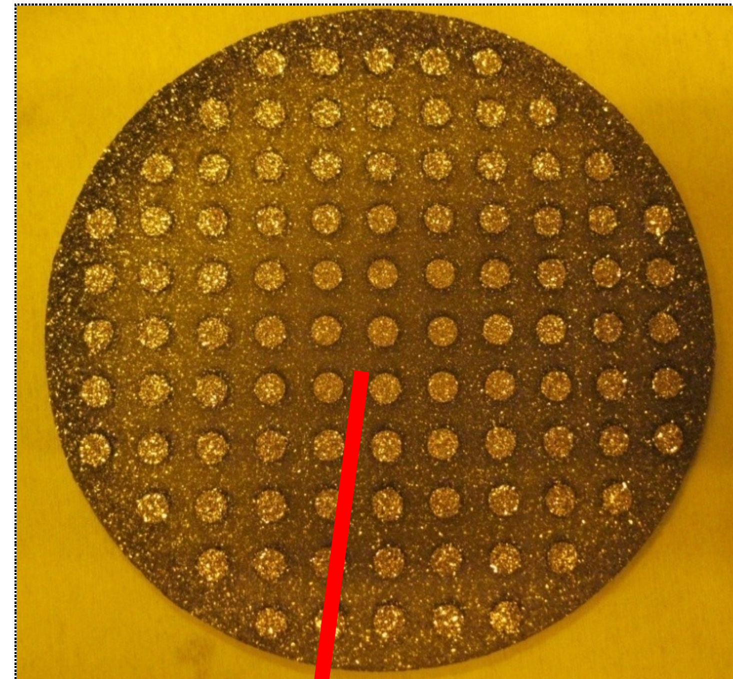
M. Köhler

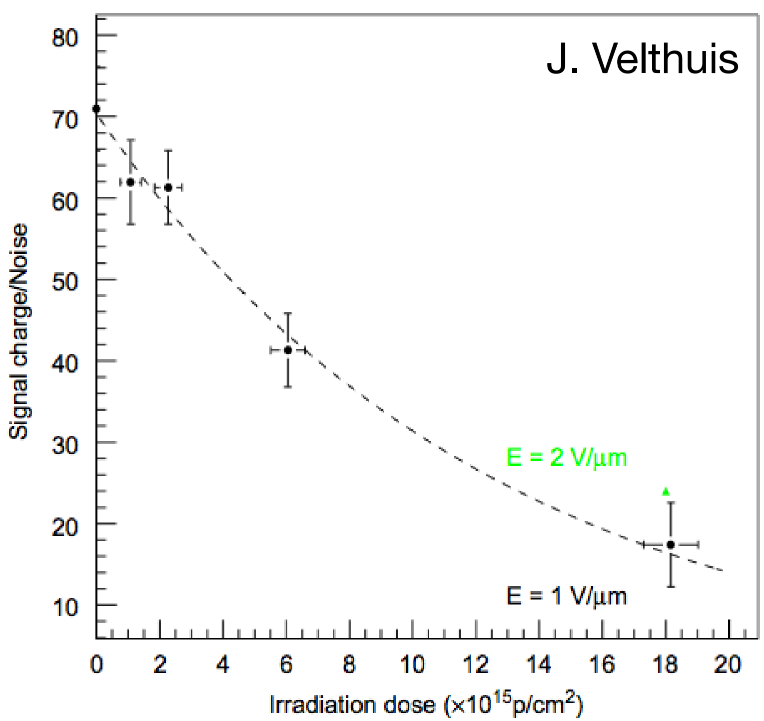


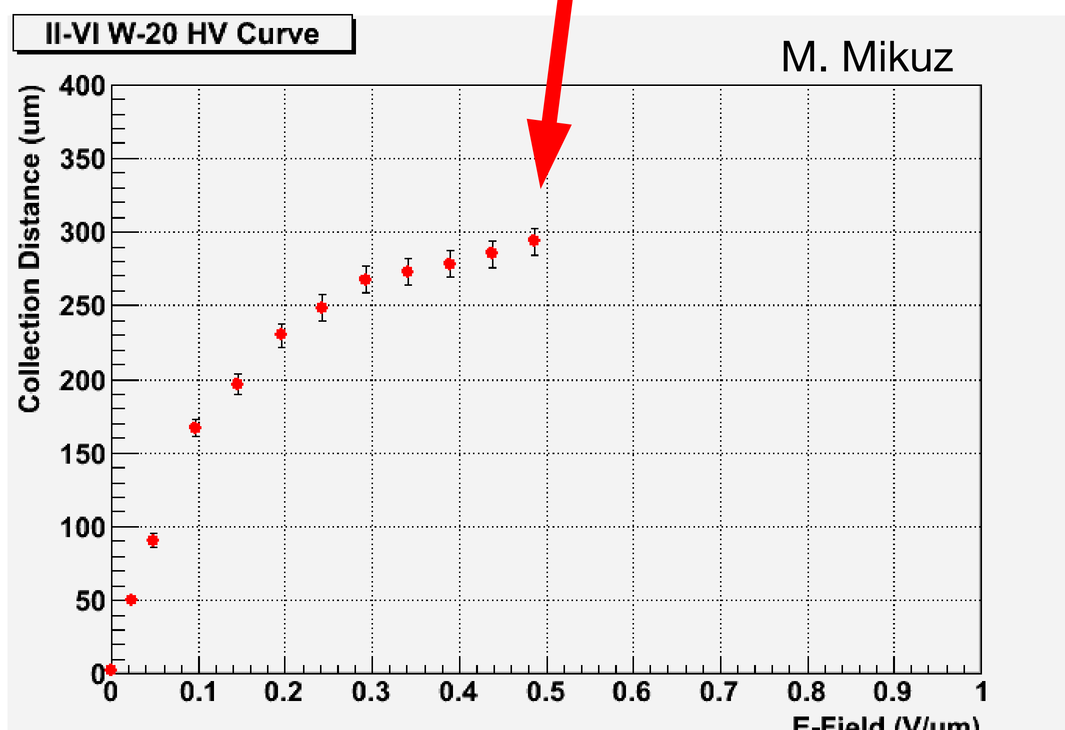
ATLAS Upgrade

Innermost sensors: Diamond

- virtually no leakage current, even decreasing after irradiation
  → no cooling required
- low capacitance → low noise
- large CCD pCVD material being tested
- but: trapping exists, S/N decreasing with fluence
- diamond used already for several BCMs, CMS Pixel Luminosity Telescope

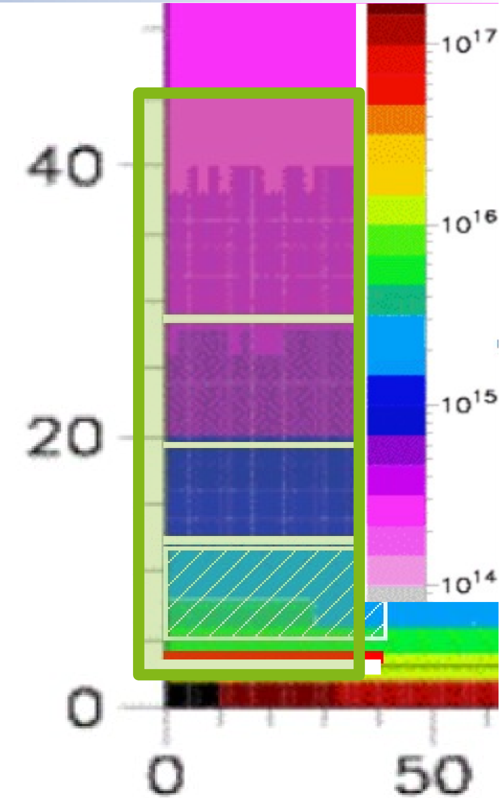


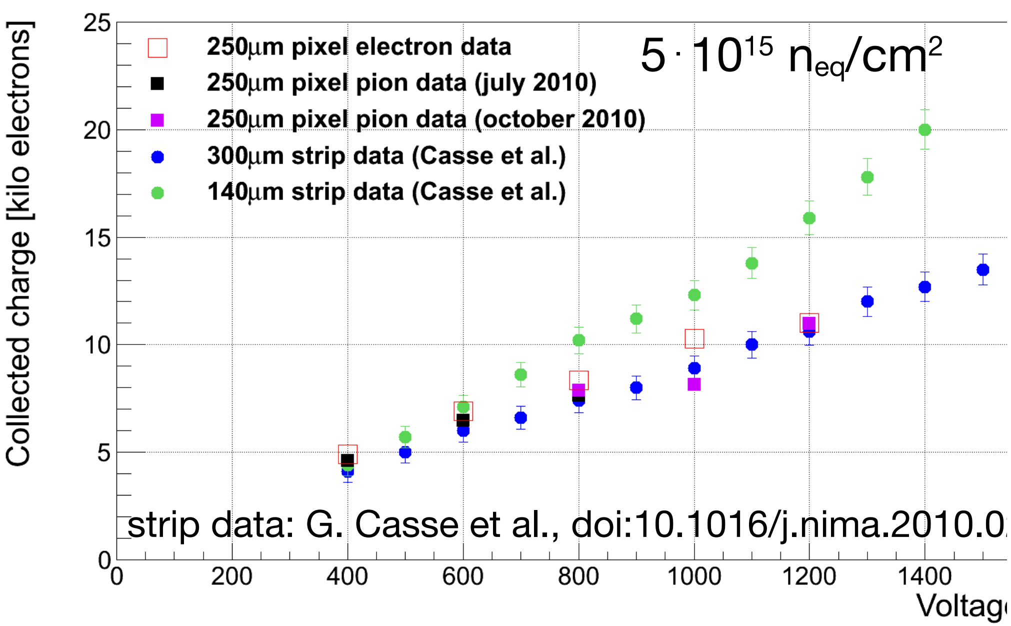


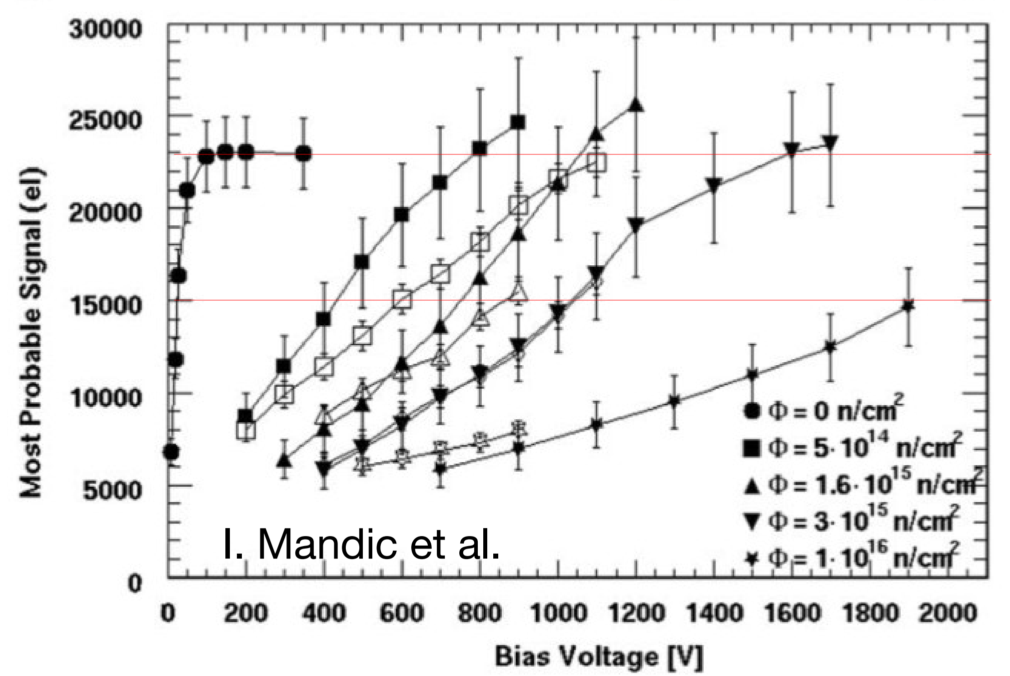


Planar sensor results

- With sufficient cooling, very high bias voltages are possible (up to 2 kV!)
- Charge amplification at high voltages/fields observed
- Usage of planar sensors in
  - all but innermost pixel layer appears to be qualified (similar to IBL!)
  - innermost layer feasible but needs further study:
    - stability of charge amplification
    - handling of very high bias voltages







ATLAS Upgrade

Cost efficient pixel sensors for large radii

- pixel sensors offer improved spatial resolution and reduced occupancy
- only one detector layer needed per space-point (two with stereo-angle for strips)
- since ATLAS production, large advances in cost efficiency:

Item	ATLAS Production	Costing goal 2008	Current best estimate for large volumes
Sensor	~ 55 CHF/cm²	~ 50 CHF/cm²	< 25 CHF/cm²
Readout chip	~ 150 CHF/cm²	< 50 CHF/cm²	< 30 CHF/cm²
Bump-bonding	~ 190 CHF/cm²	< 50 CHF/cm²	< 30 CHF/cm²
Sum	~ 400 CHF/cm²	< 150 CHF/cm²	< 85 CHF/cm²

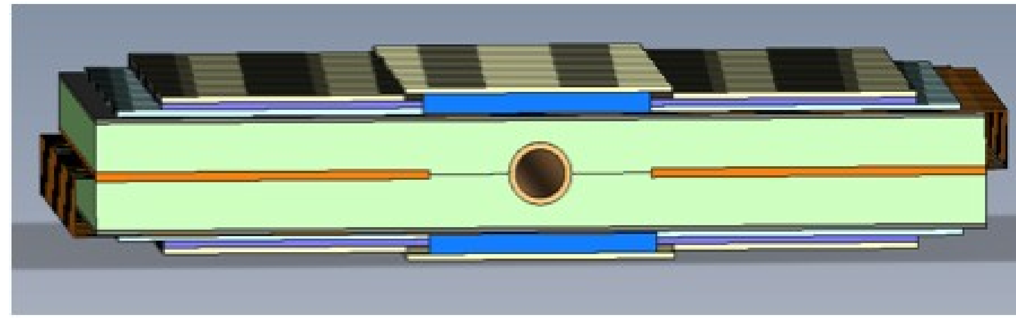
- current cost estimate may still decrease significantly
  - single-sided n-in-p sensors ought to be even cheaper than strip sensors (better yield)
  - industrial bump-bonding (C4NP) might become available for 50 µm pitch
  - large-scale FE-I4.2 production might be with cheaper vendor

➔ cost efficiency important aspect for SLHC

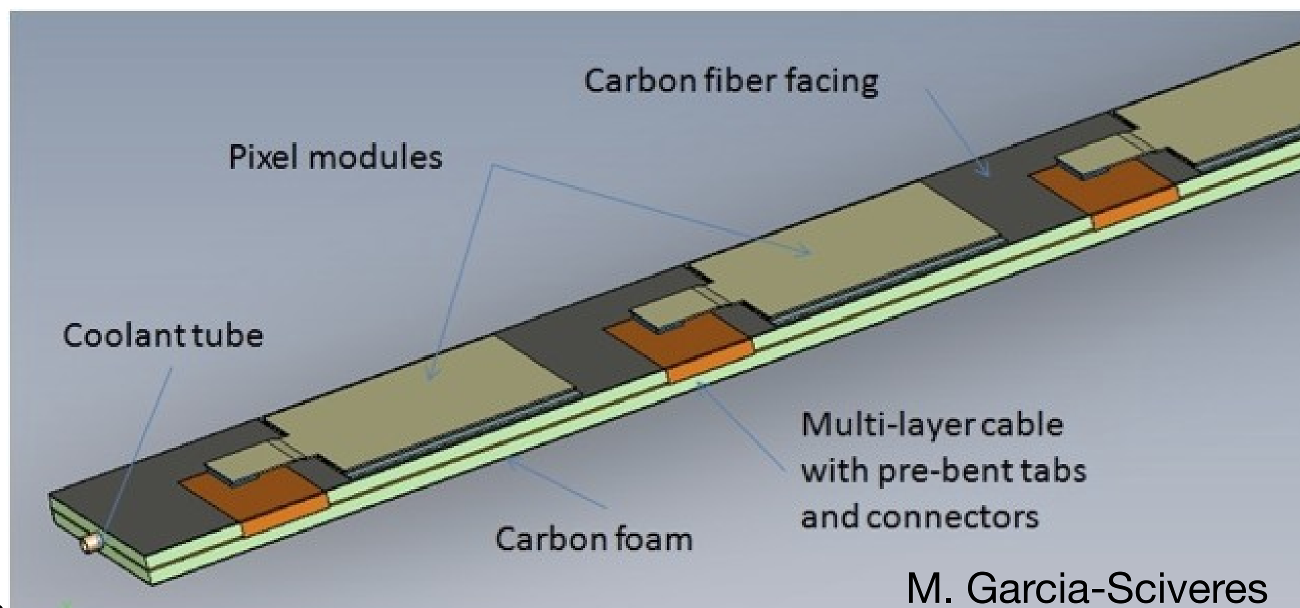
➔ making good progress towards competitive pricing

Pixels prototyping

- Efforts currently focused on outer pixel layers (need longest production time)
- Basic concept:
  - double-sided staves
  - carbon foam
  - flex inside of stave
  - 2x2 MultiChip-Modules

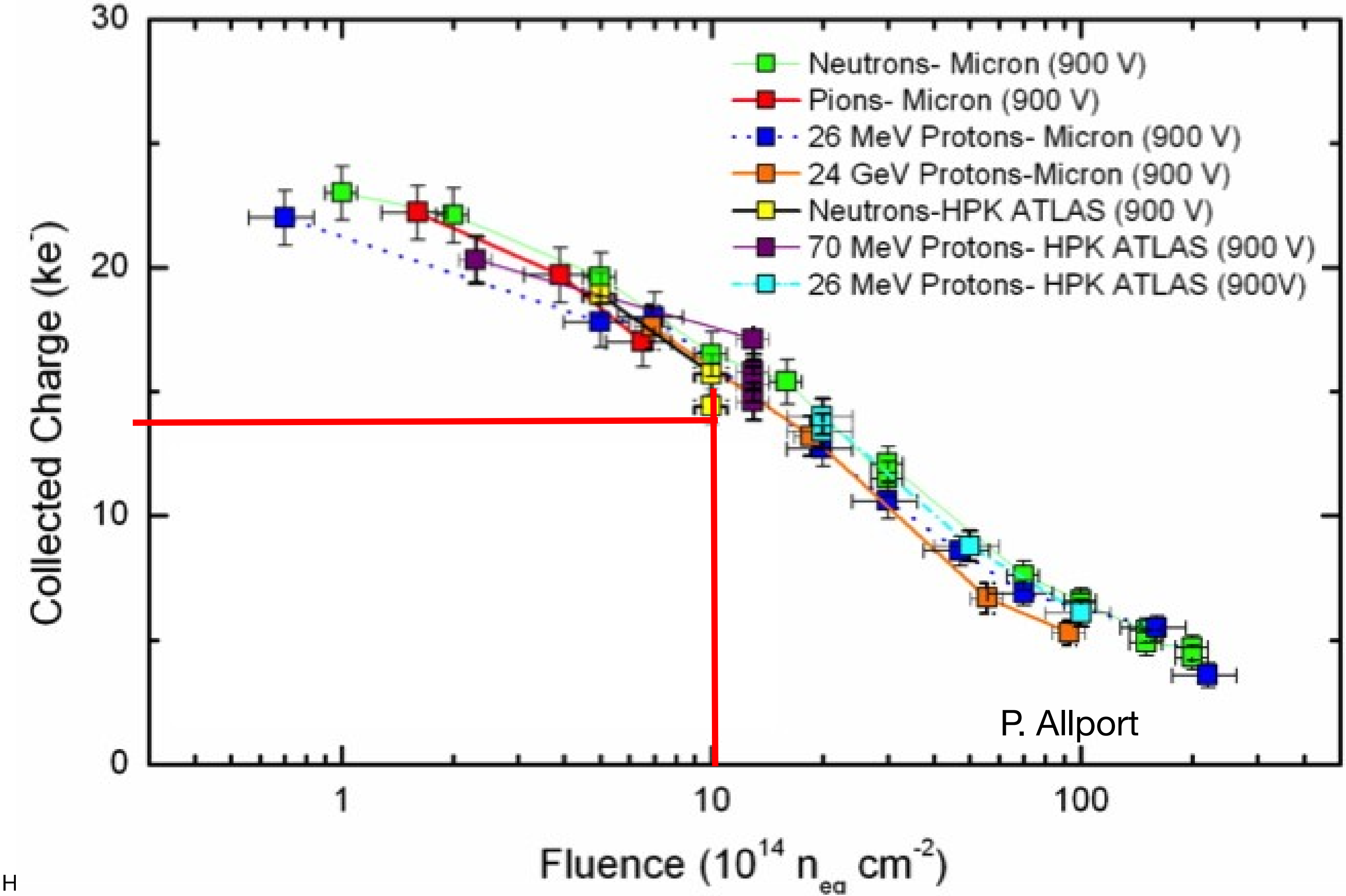


- Extensive prototyping programme starting (Stave 2010)
- Many 'real' components soon available:
  - 2x (2x1) MC-sensors that can serve as 2x2 MC-sensor prototypes
  - FE-I4
- Cost reduction an important topic for pixels at large radii
  - low-cost bump-bonding



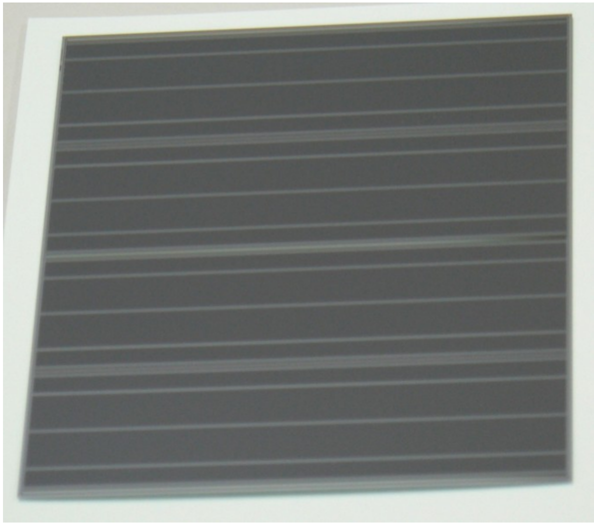
Strip sensors: Collected charge with n-in-p strips

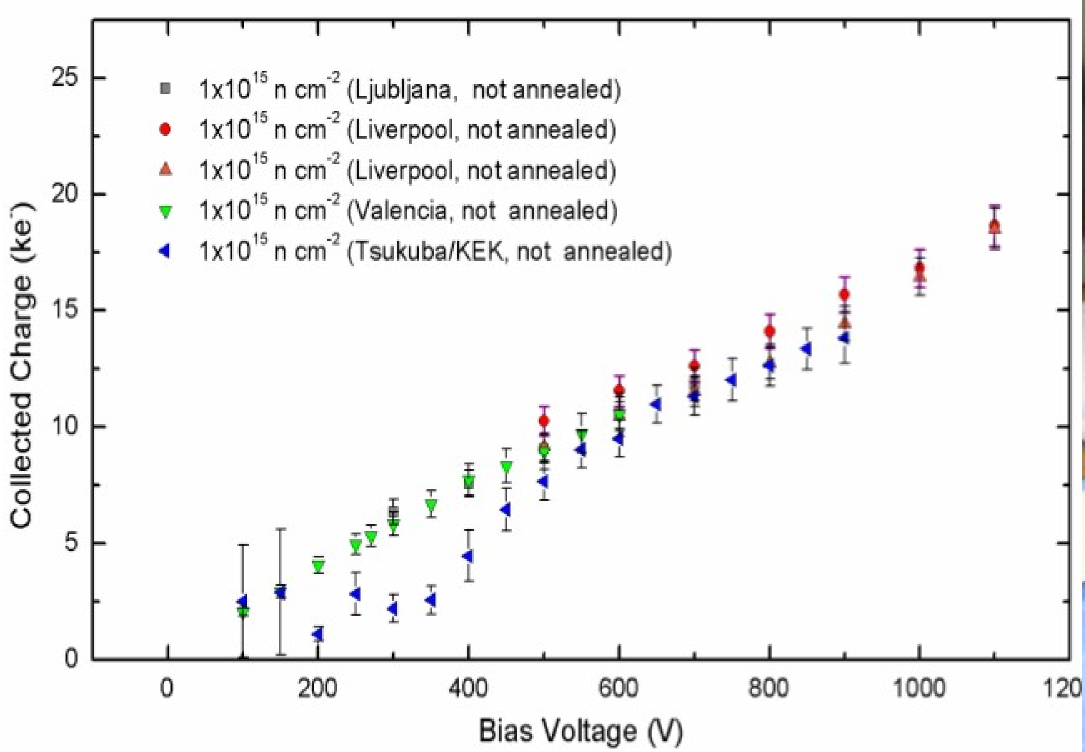
- collected charge > 14000 e^- at 10^{15} n_{eq} cm^{-2} and 900V bias voltage
  - well sufficient for all envisaged strip regions
- sensor self heating due to leakage current → sufficient operation temperature

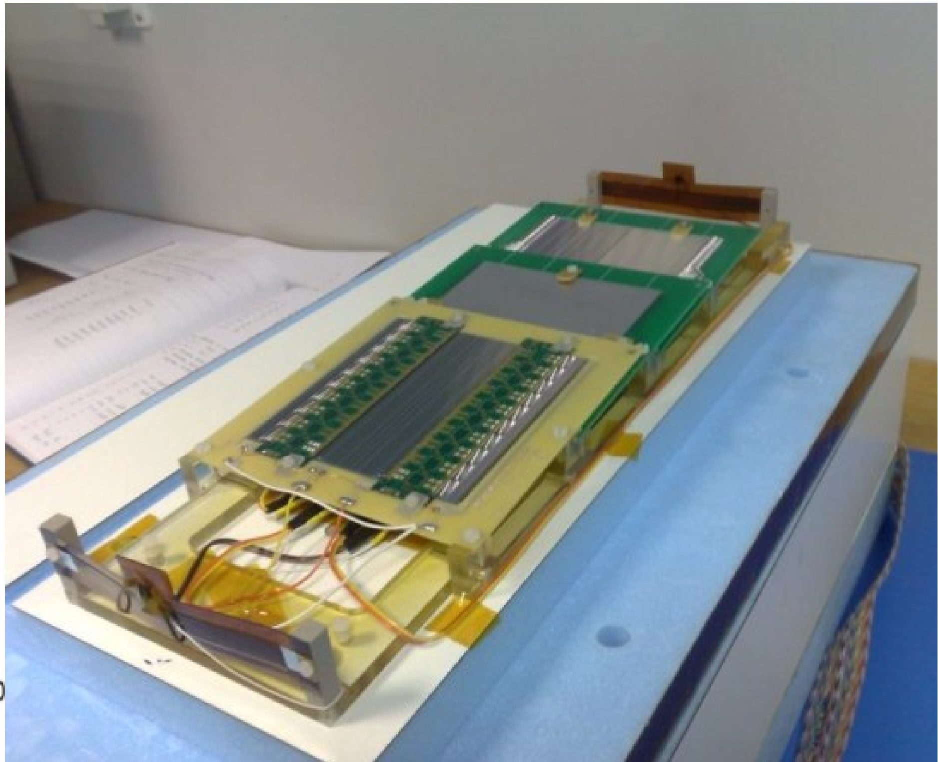


Strip prototyping

- n-in-p sensors in full size available (ATLAS07)
- Breakdown voltage > 1000 V
- Radiation hardness verified up to 10^{15} n_{eq} cm^{-2}
- Full-size sensor irradiations accomplished
  - sensors
  - modules

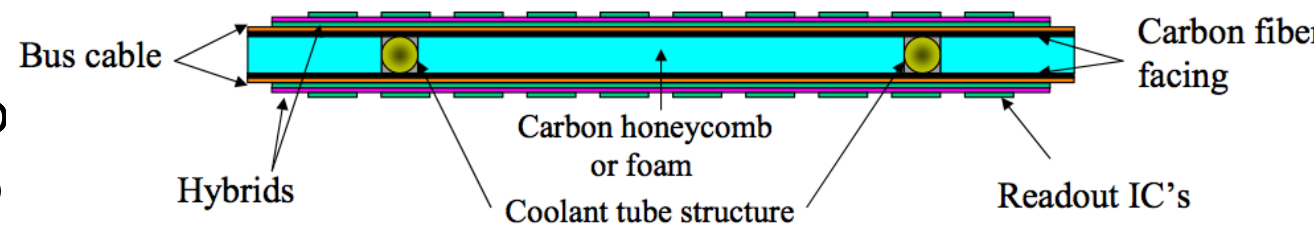


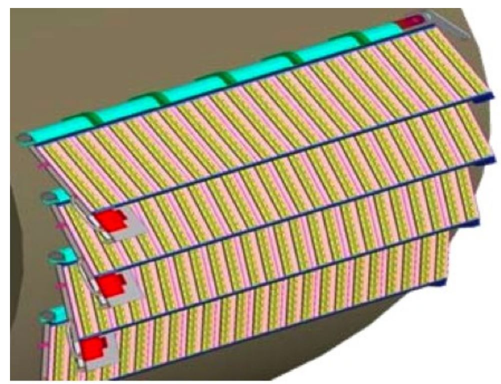


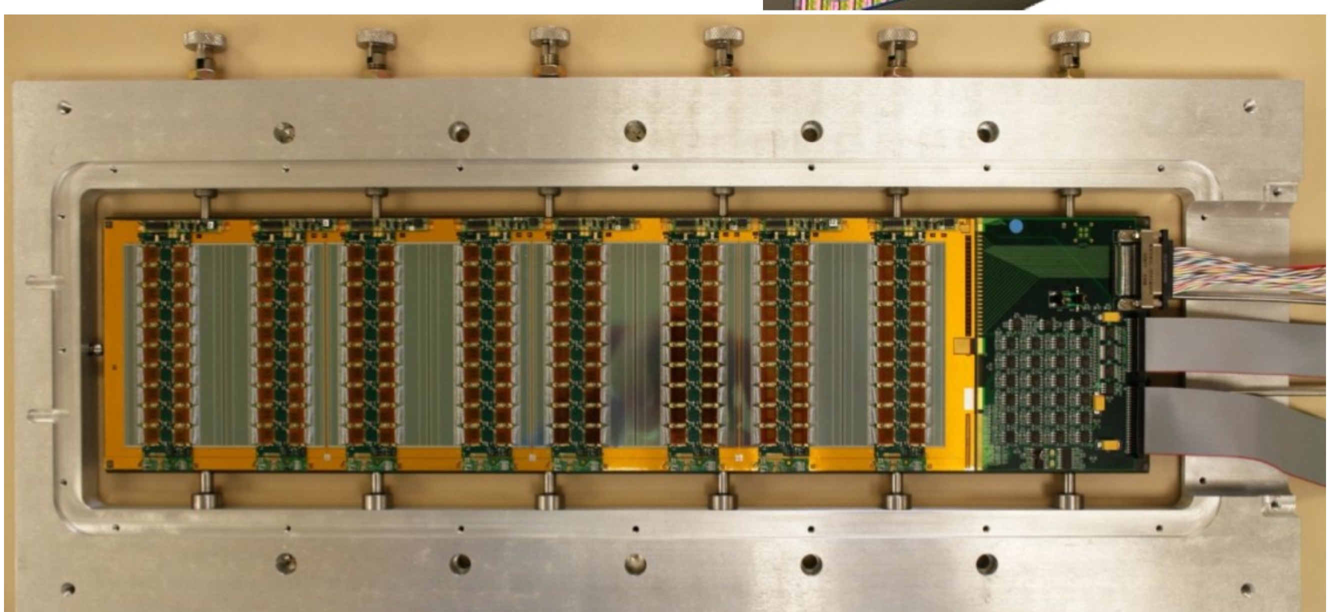


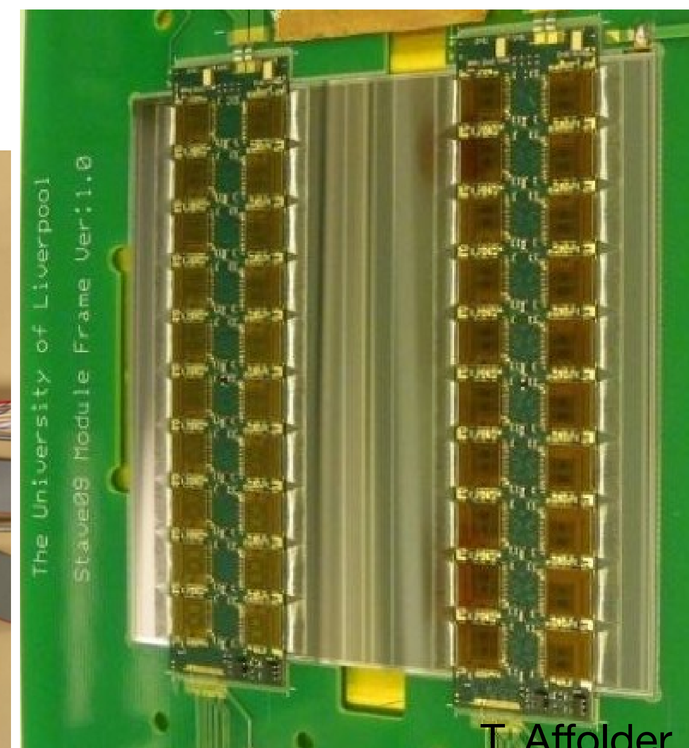
Strip prototyping: staves

- Extensive stave prototyping programme exists (stave06 … stave09)
- Focus on short strip part – extensive experience with current (long strip) SCT
- Baseline: Stave concep
  - Hybrid glued to senso
  - Sensor glued to stave
- Readout chip:
  - ABCN25 (128 channels) → ABCN13 (256 ch)









T. Affolder

Summary

- Upgrade plans for ATLAS have been impacted by recent shifts of LHC schedule:
  - nSQP and IBL now both planned for 2013 shutdown
  - sLHC/HL-LHC-Upgrade planned for 2022 shutdown
  - case study for a possible new pixel detector in 2017 underway
- IBL has adopted “fast track” schedule: ambitious but possible
  - sensor qualification currently underway with irradiations and test beams
  - planar and 3D DDTC sensors to be qualified, sensor choide mid-2011
- R&D and prototyping for SLHC upgrade continues
  - several sensor types under study for innermost layer(s)
  - prototypes with n-in-p planar sensors for outer pixel and strips underway
  - new management structure to better coordinate efforts (USC)
  - next ATLAS Upgrade week will be held in 10 days in Oxford