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PHYSICS AT THE TERA SCALE
Helmholtz-Alliance

Electronics Developments - VLDT Bonn

H. Krüger

Overview

- Short Update on Recent Chip Developments
  - ATLAS Pixel front-end FE-I4
  - **ATLAS DCS (Uni Wuppertal)**
  - Gaseous Pixel Detectors Timepix2
  - DEPFET Pixels
  - **PixCap (sensor capacitance measurement)**

- Chip Design Tutorial

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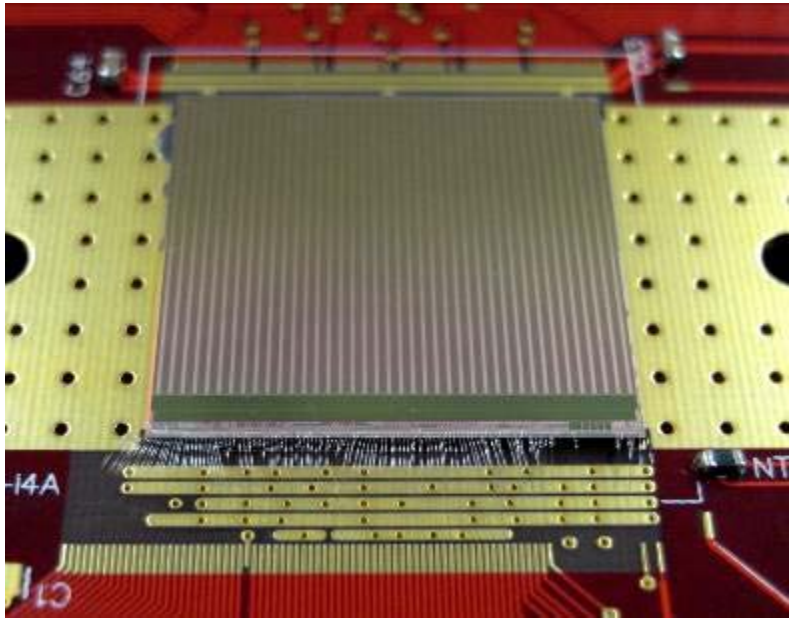
Chip Design for the ATLAS Pixel Detector

ATLAS Pixel: FE-I4

- IBL requirements
  - Occupancy
  - Rad. hardness
- 50µ x 250µ pixel size
- Pixel region buffer architecture
- IBM 130nm



	FE-I3	FE-I4
Pixel Size [µm²]	50×400	50×250
Pixel Array	18×160	80×336
Chip Size [mm²]	7.6×10.8	20.2×19.0
Active Fraction	74 %	89 %
Analog Current [µA/pix]	26	10
Digital Current [µA/pix]	17	10
Analog Voltage [V]	1.6	1.4
Digital Voltage [V]	2	1.2
LVDS out [Mb/s]	40	160

½ current pixel size!

largest in HEP to date

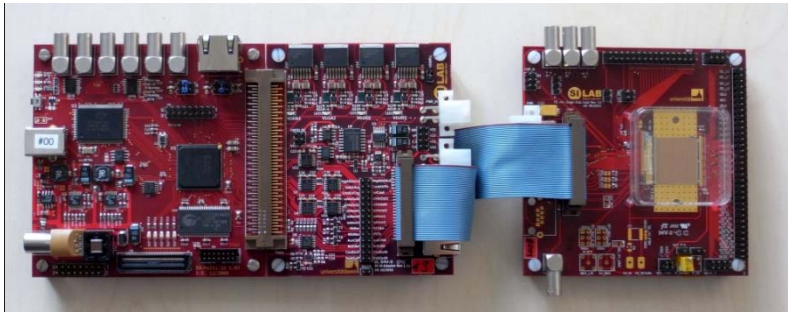
analog / digital power

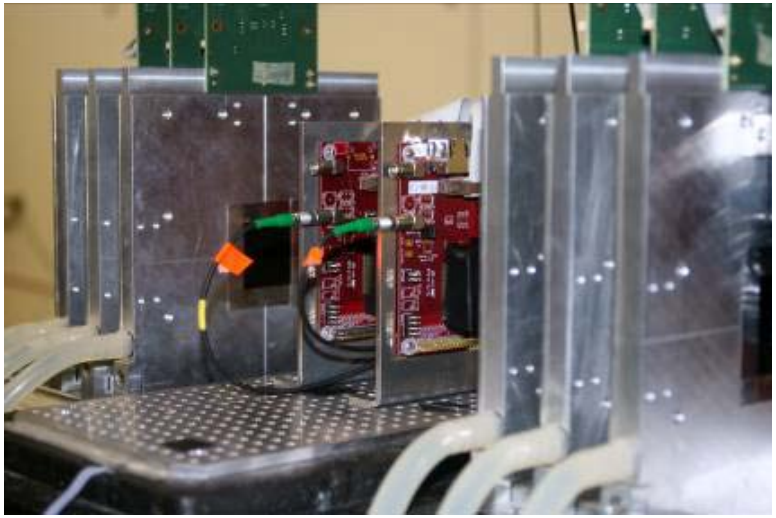
tuned for IBL occupancy

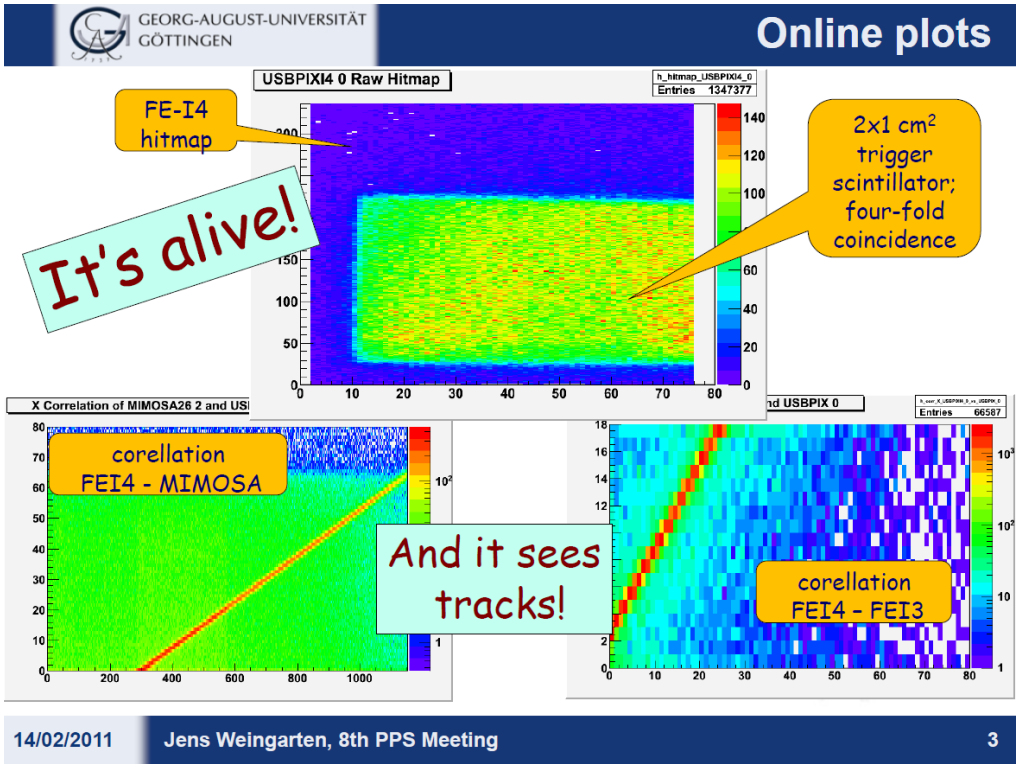
- Full scale engineering prototype: FE-I4A
- Submitted August 2010
- Wafer shipping October 2010
- Successful beam test in Feb 2011

IBL Test Beam Feb 2011 @ DESY

- USBpix test system with FE-I3 and FE-I4 module opertated in the EUDET Telescope
- 4 GeV electron beam @ DESY







ATLAS Pixel: Status & Outlook

- FE-I4 successfully submitted in 2010 (LBNL, Bonn, NIKHEF, Genua), meets all specs.
- Sensor characterization with FE-I4 (Göttingen, Dortmund): 3D, new planar sensor, Diamond …
- USBpix read-out system for lab and test beam measurements used by more than 20 groups including Göttingen, Heidelberg and MPI Munich (~40 systems distributed)
- FE-I4 re-design (minor modifications only) planned for June/July
  ➔ production version for the IBL construction

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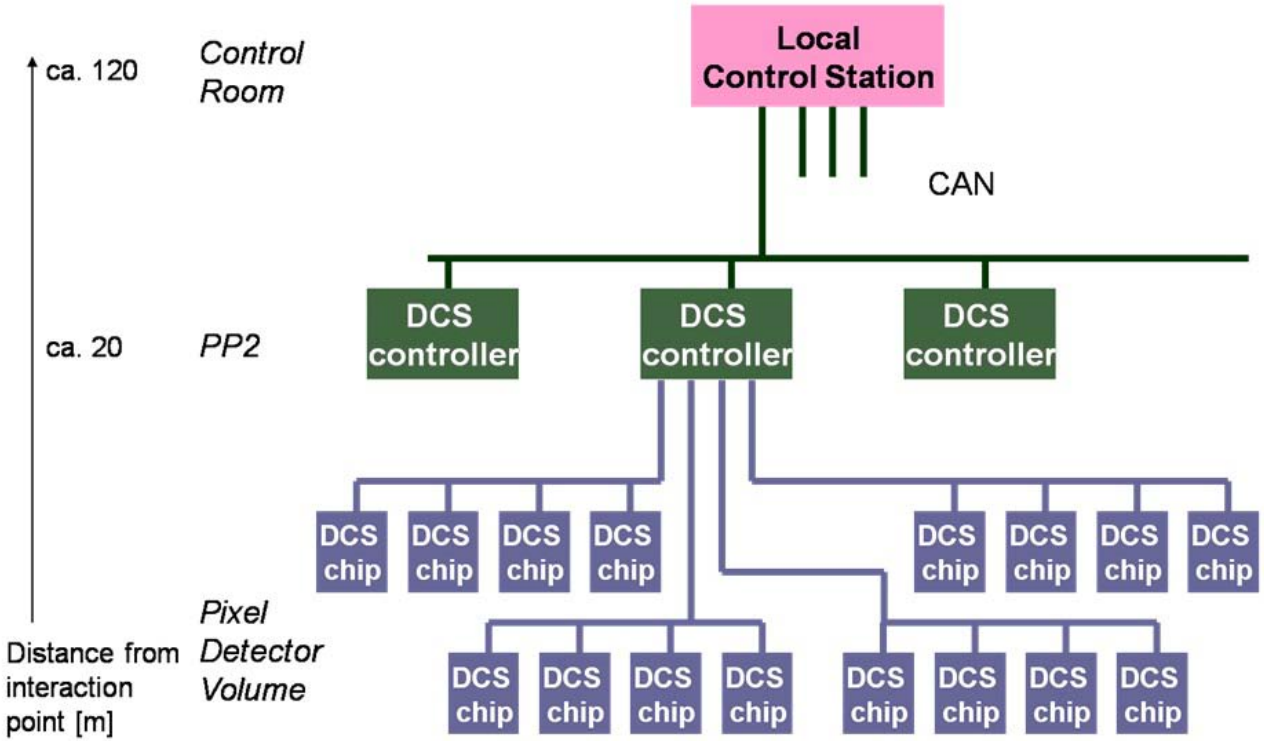
ATLAS Detector Control System (Uni Wuppertal)

ATLAS Detector Control System

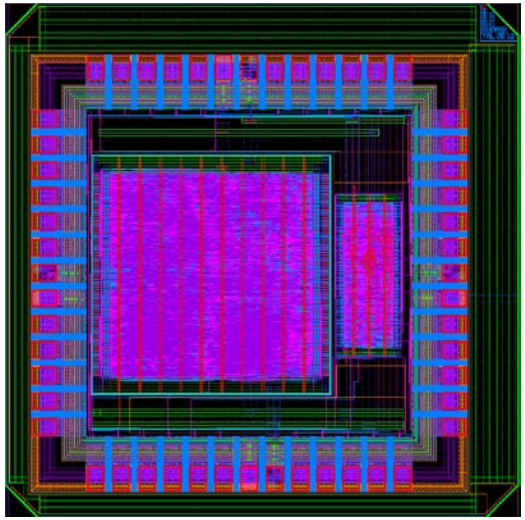
- Implementation of a DCS network for future ATLAS Pixel detector upgrades based on custom made chips
  - development by Wuppertal University
  - integration on the end of stave and PP2



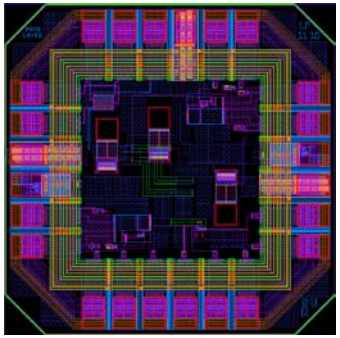
Universität Wuppertal

Current Chip Developments for ATLAS DCS @ Wuppertal

- COntrol & FEEdback: CoFee1
  - First design in IBM 130 nm by Wuppertal
  - Digital design (2mm x 2 mm) includes DCS Controller and DCS Chip
  - Currently being tested



- Physical layer chip
  - Second design in 130nm
  - Full custom layout (1mm x 1 mm)
    - Diff. driver for CAN bus
    - DAC test structure
    - Clock generator
  - Submitted Nov 2010, shipping expected soon



Support of the VLDT Bonn for Wuppertal

- Installation of Cadence tools and design kits in Wuppertal
- Visits of Wuppertal chip designers in Bonn
- Support during all phases of the design
- Wire bonding of the test structures
- Wuppertal resources actively involved in the design effort:
  3 physicists + 1 engineer
- Up to now 3 chip submissions (1x AMS 0.35µ, 2 x IBM 130nm)
- New submissions planned

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Chip Design for the Gaseous Detectors

See Klaus' talk tomorrow

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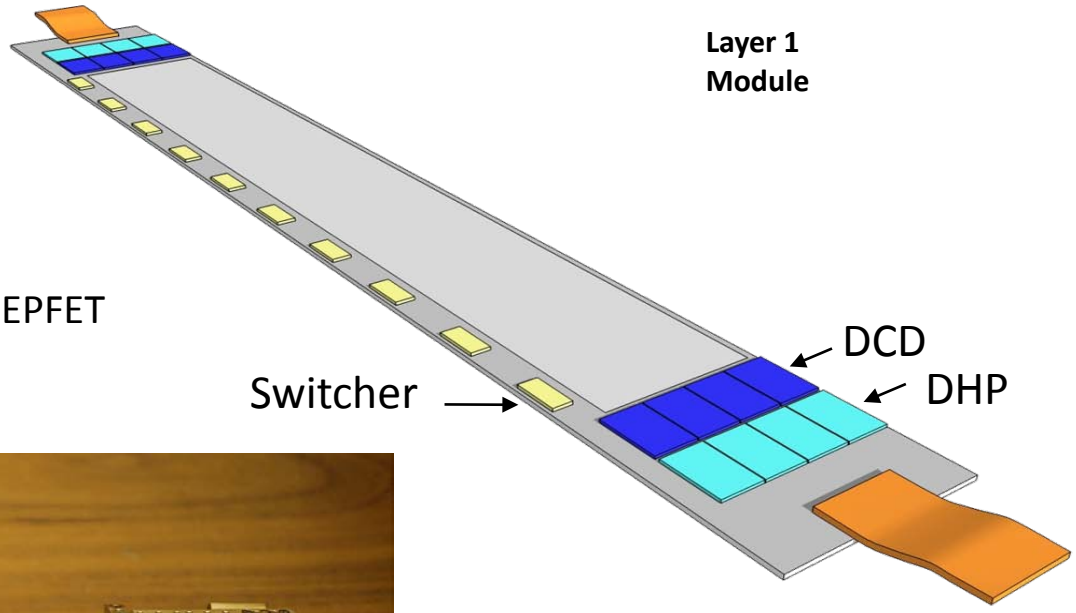
Chip Design for DEPFET Pixel Detectors

DEPFET Vertex Detector for BELLE 2

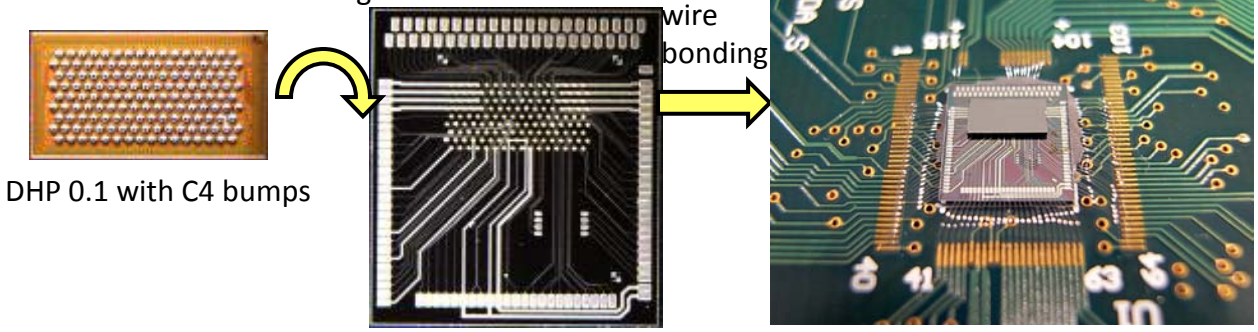
- two layers of pixel modules (r = 14 mm and 22 mm)
- active pixel area thinned to 75 µm
  - low mass design
- surrounding (non-thinned) frame
  - mechanical support
  - mounting and routing for the ASICs
- ASICs bump bonded directly onto the DEPFET substrate

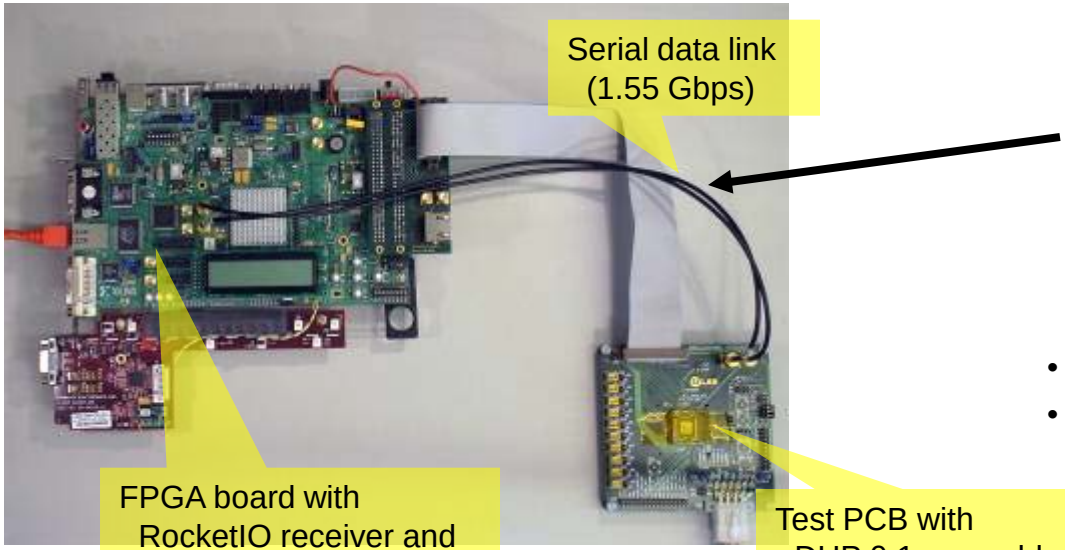


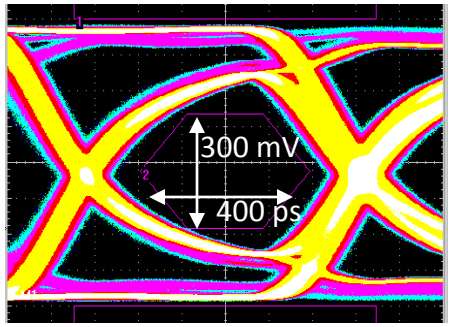
PXD mockup

DHP 0.1 Test Chip

- DHP 0.1 (IBM 90nm)
  - half size chip (32 ch.)
  - C4 bump bonds
  - digital data processing
  - Gbit link
  - submitted Feb 2010
  - shipped July 2010
- Test system (Gigabit link support)





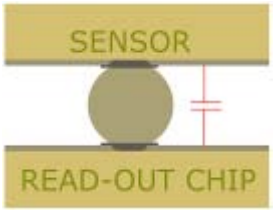


- 1.55 GHz 8b/10b random data
- DHP chip → WB adapter → 5 cm PCB → SMA → 40cm coaxial cable → SMA → Xilinx RocketIO

PixCap – A chip to precisely measure the load and inter-pixel capacitance of pixel sensors

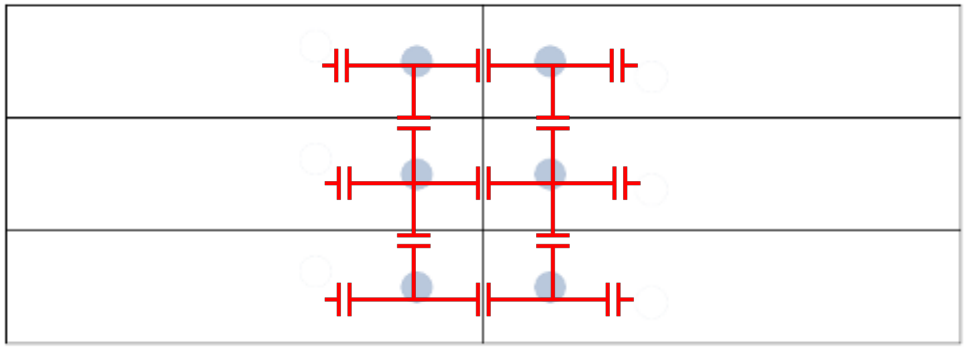
Motivation

- LHC upgrade developments introduce new sensor materials and concepts (3D sensors, Diamond …)
- in order to predict their performance and to optimize the front-end electronics, sensor specifications have to be known (leakage current, pixel capacitance)



cross section of a bump bond connection in a hybrid pixel assembly

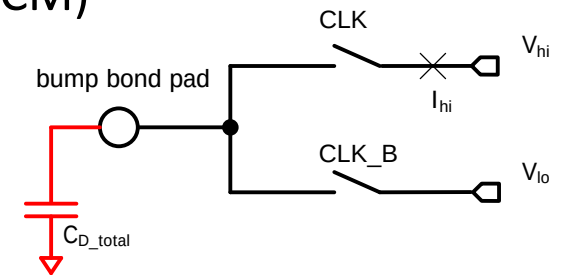
- Several kinds of capacitances can be defined:
  - between sensor and read-out chip
  - capacitance to back plane
  - inter-pixel capacitances



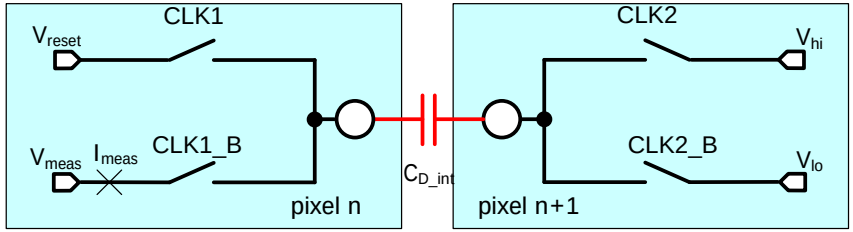
pixel bump pad layout (FE-I4)

Measurement Concept

- charge based capacitance measurement (CBCM)
  - simple measurement: $C_D = I_{hi} / (\Delta U \cdot f_{CLK})$
  - (sub) fF resolution



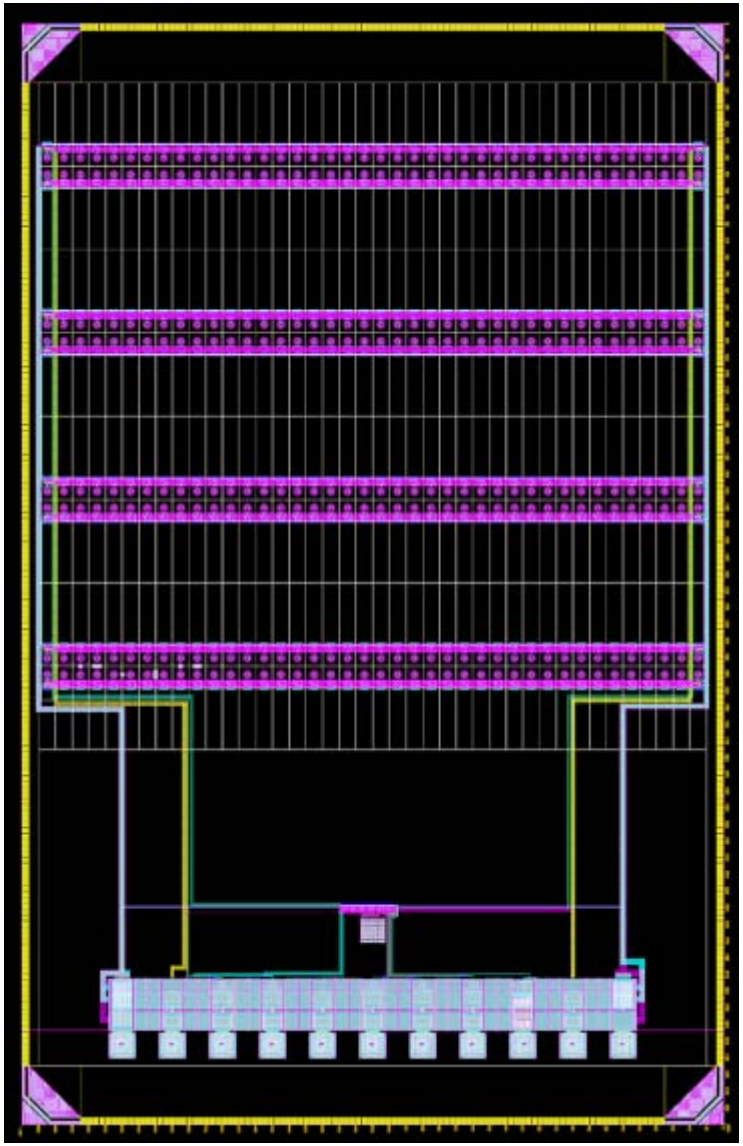
measurement of total pixel capacitance



measurement of inter-pixel capacitance

- measurement principle originally proposed for precise measurement of on-chip parasitic capacitances B. McGaughy, A Simple Method for On-Chip, Sub-Femto Farad Interconnect Capacitance Measurement, IEEE Electronic Device Letters, VOL. 18, NO. 1, Jan 1997

Implementation



- bump-bond pad layout for 250x50 µm pixels (ATLAS FE-I4)
- Physical size: 3.3 x 2.1 mm
- Number of channels: 320 (40x8)
- 11 wire bonding pins
- Implemented test circuits
- Technology: L-Foundry 150 nm
- MPW 6 metals + thick metal (top)
- designer: M. Havranek (PhD student)

Pixel Sensor Characterization

- 150 nm LFoundry CMOS technology
  - available via Europractice or MPW service directly through the vendor
  - 850 EUR / mm^2 (cheap! IBM 130nm is three times more expansive)
- Currently the design will fit the ATLAS FE-I4 sensor layout
- Design is not explicitly radiation hardened (leakage current), will be addressed in next chip iteration, if necessary
- Test chip back in April 2011
- Need to place fine pitch solder bumps (difficult on single dies ➔ IZM)

- Feedback from interested **Alliance members** welcome for future modifications:
  - **users**: input of application specific parameters (pixel pitch..), implementation done by VLDT
  - **developers**: participation in chip design (adaption of existing design blocks), good “first time” project

Chip Design Tutorial

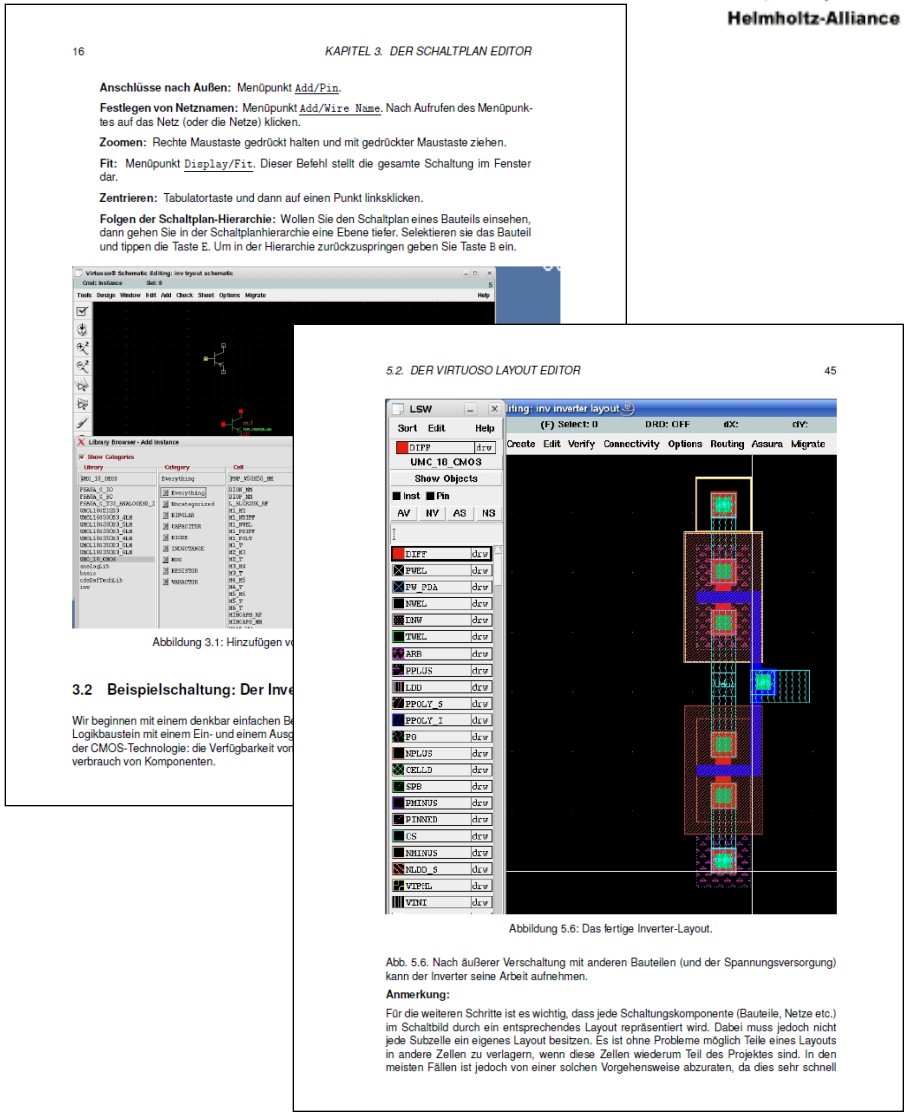
- Initially developed to give students a first introduction to the tools (Cadence) and methods of integrated chip design
- Used in internships (Bonn Cologne Graduate School, BCGS) and advanced electronic lecture exercise
- Guides through the various phases of a full custom design flow
- uses UMC 180nm design kit + special library with a few predefined elements
- Very easy level, only few prerequisites needed
- Not mend to train a person to become a chip designer
- up to now only available in German

Structure of the Chip Design Tutorial

1. Introduction
   - Analog & digital circuit
2. Component Libraries
   - Cadence library manager
3. Schematic Entry
   - Creating instances
   - Defining design parameters
4. Simulation
   - DC, AC and transient analysis
   - parametric analysis
5. Layout
   - Virtuoso Layout Editor
   - DRC (design rule check)
   - LVS (layout versus schematic)

Usage of the Script

- The script should be used in front of a Cadence workstation
- Every step is explained and snapshots from the Cadence tool windows are shown
- Usually two students share a Cadence workstation (4 stations available in our student lab) and one chip designer is available on-call during the exercise
- Time needed to work through the script (57 pages): 15-30 h



16 KAPITEL 3. DER SCHALTPLAN EDITOR

Anschlüsse nach Außen: Menüpunkt Add/Pin.

Festlegen von Netznamen: Menüpunkt Add/Wire Name. Nach Aufrufen des Menüpunktes auf das Netz (oder die Netze) klicken.

Zoomen: Rechte Maustaste gedrückt halten und mit gedrückter Maustaste ziehen.

Fit: Menüpunkt Display/Fit. Dieser Befehl stellt die gesamte Schaltung im Fenster dar.

Zentrieren: Tabulatortaste und dann auf einen Punkt linksklicken.

Folgen der Schaltplan-Hierarchie: Wollen Sie den Schaltplan eines Bauteils einsehen, dann gehen Sie in der Schaltplanhierarchie eine Ebene tiefer. Selektieren sie das Bauteil und tippen die Taste E. Um in der Hierarchie zurückzuspringen geben Sie Taste B ein.

Abbildung 3.1: Hinzufügen v

3.2 Beispielschaltung: Der Inve

Wir beginnen mit einem denkbar einfachen B
Logikbaustein mit einem Ein- und einem Ausg
der CMOS-Technologie: die Verfügbarkeit vor
verbrauch von Komponenten.

5.2. DER VIRTUOSO LAYOUT EDITOR 45

Abbildung 5.6: Das fertige Inverter-Layout.

Abb. 5.6. Nach äußerer Verschaltung mit anderen Bauteilen (und der Spannungsversorgung) kann der Inverter seine Arbeit aufnehmen.

Anmerkung:

Für die weiteren Schritte ist es wichtig, dass jede Schaltungskomponente (Bauteile, Netze etc.) im Schaltbild durch ein entsprechendes Layout repräsentiert wird. Dabei muss jedoch nicht jede Subzelle ein eigenes Layout besitzen. Es ist ohne Probleme möglich Teile eines Layouts in andere Zellen zu verlagern, wenn diese Zellen wiederum Teil des Projektes sind. In den meisten Fällen ist jedoch von einer solchen Vorgehensweise abzuraten, da dies sehr schnell

Tutorial @ VLDT

- Original idea: Provide the script to interested individuals within the Alliance and enable remote access to the Cadence workstations at VLDT Heidelberg (after appropriate NDA signing)

- Just recently Cadence tightened their access policy for academic users (no more remote access to the Cadence tools for non-institute members)

- Now: Alliance members wishing to attend the tutorial will be invited to come to Bonn or Heidelberg (after individual appointment)

- Questionnaire received up to now feedback of 4-5 interested people/groups

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Thank you!