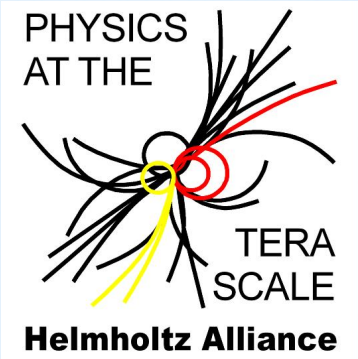
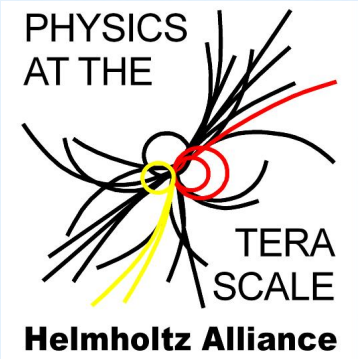
The VLDT Node Heidelberg – Current Status / Projects / Results Ideas for a Future beyond 2012



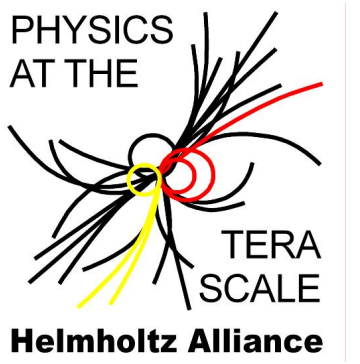
Karlheinz Meier
Kirchhoff-Institut für Physik
Heidelberg University

HGF Alliance Detector Workshop
March 2011, DESY

Infrastructure



HGF Alliance Laboratory for Detector Technologies (VLDT)



- Ensure a visible, efficient and sustained contribution of German groups to the future projects ILC and sLHC
- Develop, provide and maintain infrastructures and make them available to the Alliance
- Three branches, electronics system development, sensor development and general detector test facilities
- Central nodes of the VLDT are DESY, the University of Bonn and the University of Heidelberg. Additional infrastructure is made available to the Alliance by Aachen, Hamburg and Karlsruhe

Infrastructure available in Heidelberg (partly funded by Alliance)

- Test Lab Equipment (clean rooms, high performance measurement devices)
- Assembly facilities (bonders, BGA placers, somponent placers, soldering)
- Well maintained and up-to-date S/W CAE Tools, ASICs, FPGAs and PCBs
- Instrumentation Tutorials (Testing, Bonding, Packaging)
- Software Support (Layout, Simulation)
- Chip Submission Support (MPW, Engineering Runs, Full Runs)
- Submission Readiness Reviews
- ASIC Designer Style Guides

AMI SEMICONDUCTOR

Mentor Graphics

austriamicrosystems
a leap ahead in analog

XILINX®

IBM

ALTERA®

tsmc®

cadence

SYNOPSYS®

Proposed Infrastructure for Rapid PCB Prototyping :

Workflow : Dispensing – Mounting – Soldering

Engineer Support for external users available

Total Investment : 90 k€

Proposed cost sharing :

45 k€ remaining HGF funds
45 k€ EU project funds

Extract from recently updated CADENCE Terms of Use (from EUROPRACTICE, march 4, 2011)

Cadence: Installation protection and license statement - Action Required

The Cadence tools are kept confidential and only accessed by bona-fide staff and students of your organisation who need to access the Cadence tools for their legitimate studies, duties and research.

A bona fide employee is an individual who performs work for, and subject to the control of, the employer

....

Your organisation:

Keeps accurate records of all persons who have been given access the Cadence tools. These records should be kept for a minimum of 5 years and include the person's full name, system user name, email address, dates granted access and their status within your organisation

....

Implements access control mechanisms on the installed Cadence tools to prevent casual access by other users of your computer network who are not authorized to access the Cadence tools

Way out as stated in proposal :

„The Alliance will support members from partner institutions for short and longer visits at the sites. In this way a transfer of knowledge in addition to the utilisation of the central facilities will be made possible. It is encouraged that scientists trained at the central facilities take their knowledge home to continue work. Emphasis is placed on the training of young researchers, students and postdocs, in these high technology areas. Through the backbone activities the Alliance has reserved funds to enable these activities“

To be complemented by conceptual courses (no access to restricted software. Local access given to those really involved in a project. VLDT Heidelberg would provide support for local installation with dedicated toolset. Minor additional financing (O(10k€)) required for installation.

Staff Situation (VLDT funded)

2 positions assigned to Heidelberg node, 1 to be sustained

Intermediate financing of ASIC support engineers :

Ralph Achenbach : Selection, purchase, installation, documentation and long term support of new test equipment

Marcus Dorn : Installation, maintenance and long term support of CAE tools

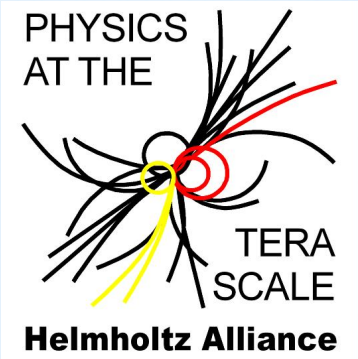
(Final) positions filled 2010 :

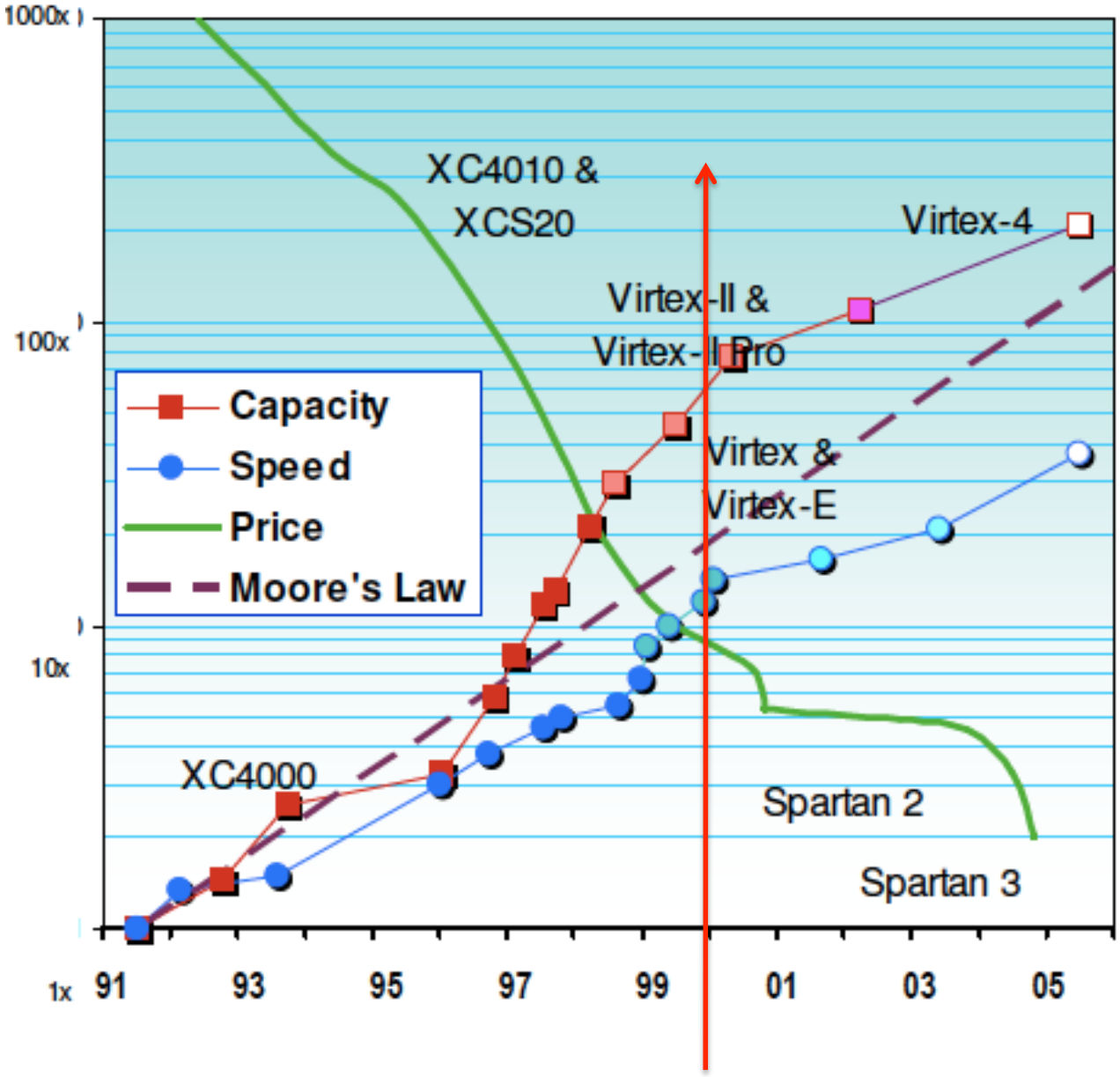
Andreas Grübl : physicist, permanent employment, sustained position, future head of electronics workshop (starting 2014)

Gvidas Sidlauskas : engineer, project support, installation and support of new deep-submicron technologies (TSMC 65nm)

Recent development : GS will leave may 2011 (family reasons), position offered to Victor Andrei, ATLAS Level-1 Upgrade, FPGA support)

Running Projects





The Rise of Field Programmable Gate Arrays

Logic x 200

Speed x 40

Lower Power x 50

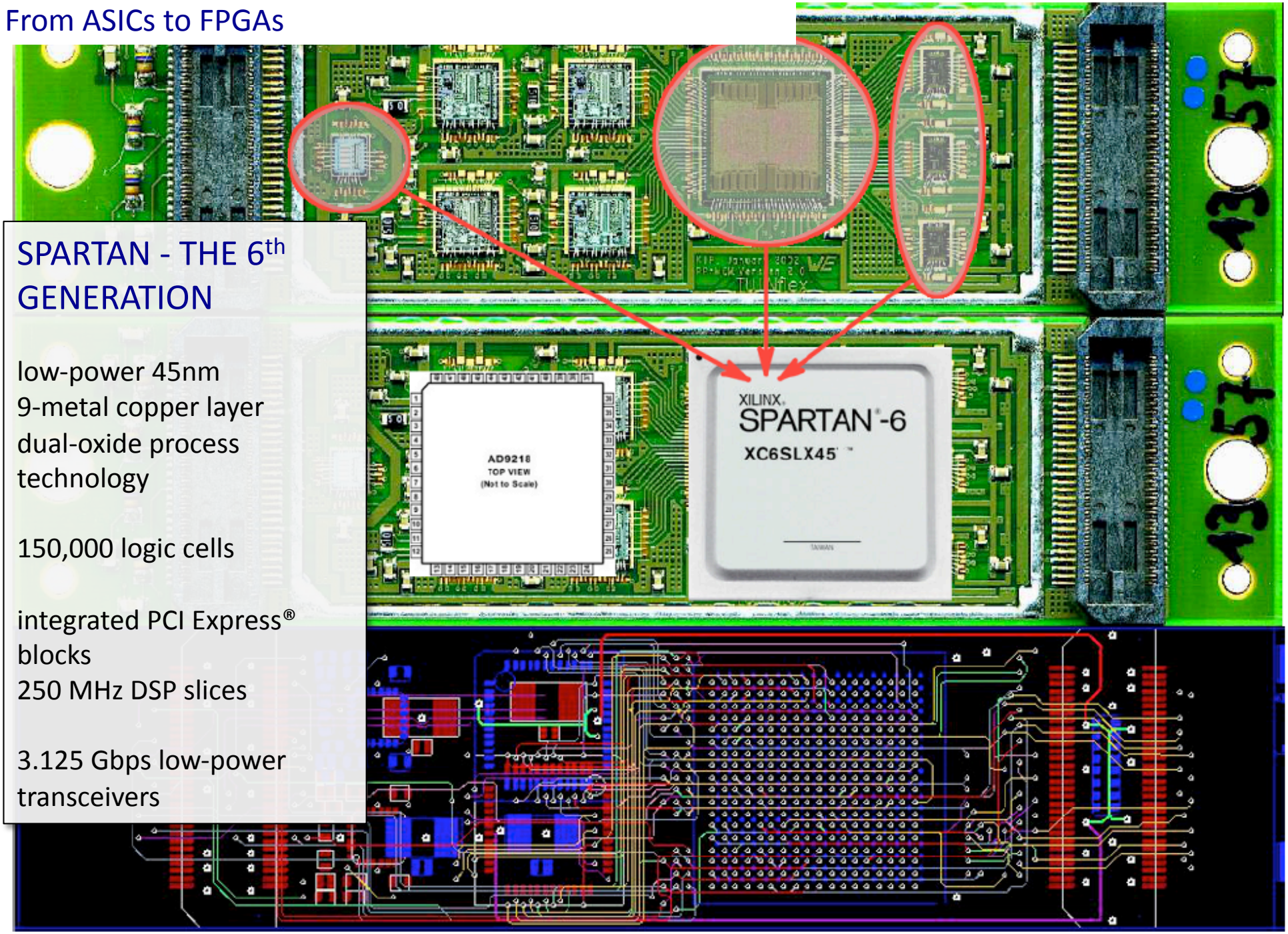
Lower Cost x 500

S. Trimberger (XILINX)

many LHC (frontend) technology decisions

Easy access to „custom digital design“ for university groups without expensive equipment

ATLAS – Level-1 Calorimeter Trigger Upgrade (Heidelberg)
From ASICs to FPGAs



SPARTAN - THE 6th GENERATION

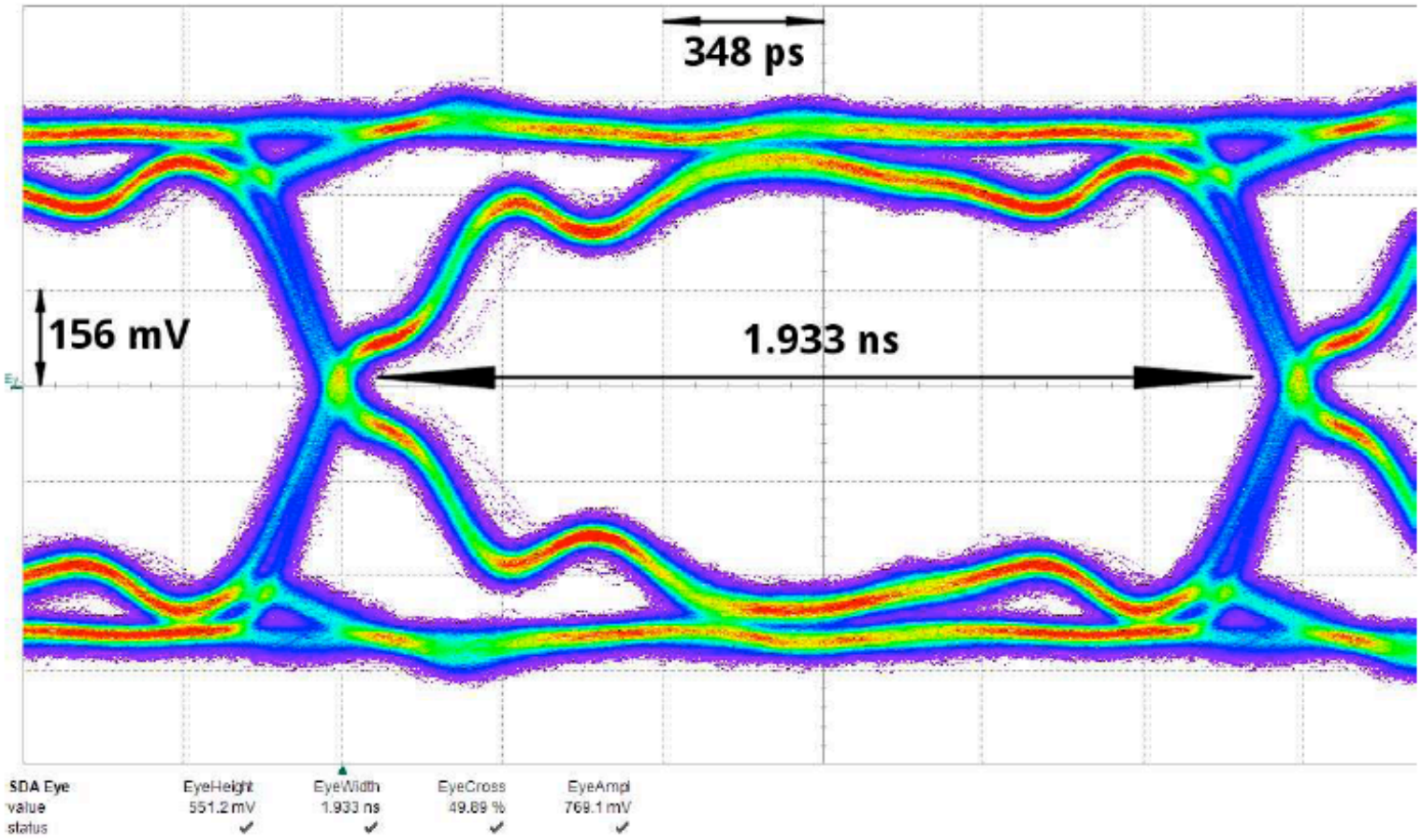
low-power 45nm
9-metal copper layer
dual-oxide process
technology

150,000 logic cells

integrated PCI Express®
blocks
250 MHz DSP slices

3.125 Gbps low-power
transceivers

480 Mbits/s LVDS link driven by Spartan-6 FPGA

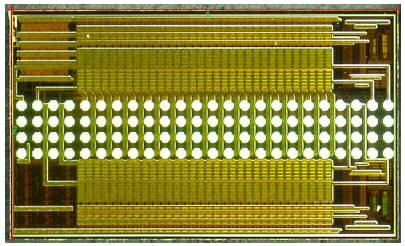


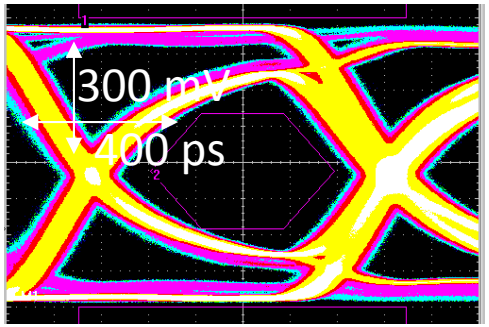
Implemented using Spartan-6 output serialiser blocks (OSERDES2).

TWEPP 2010 : Andrei Khomich (Heidelberg)

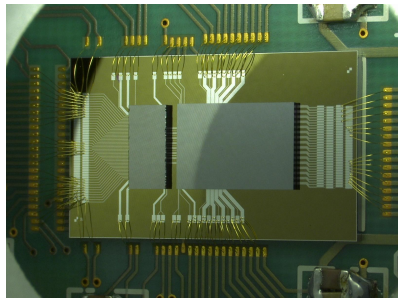
Belle DEPFET Vertex Detector
Complete Electronics Chain (Barcelona, Bonn, Heidelberg)

Data handling processor DHP 0.1 (IBM 90nm)
C4 bump bonds, full data processing, Gbit link,
Analog blocks (U Barcelona)





Switcher : radiation-hard
switching of on-detector 20 V
signals



DEPFET Current Digitiser (DCD)
256 channels, 10-bit, 10 MHz ADCs, 65 400 MHz Links

TWEPP 2010 : Jochen Knopf (Heidelberg)

Silicon Photomultiplier Readout Systems Heidelberg

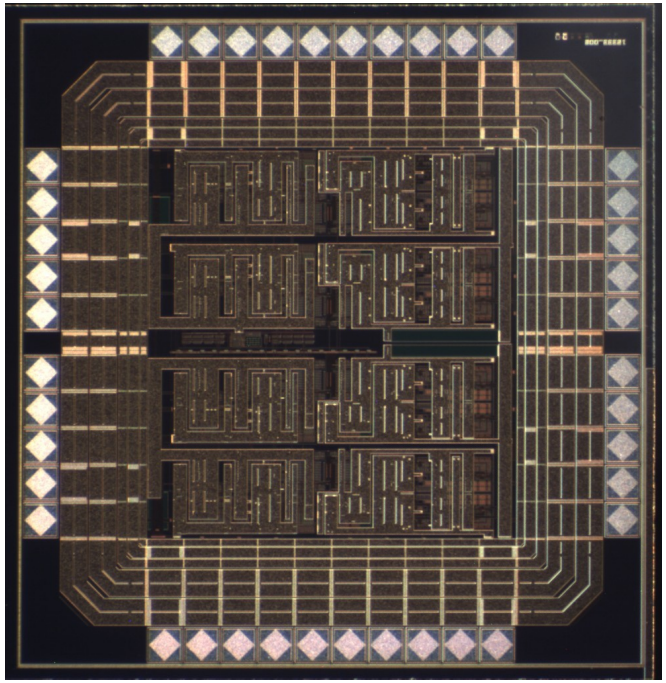
CALICE

KLauS: Charge Readout Chip

[Kanäle für Ladungsauslese von SiPMs]

AMS 350nm CMOS technology; 4 channels;
SPI interface controlled by FPGA; Bias DAC tunable;
high Signal/Noise Ratio [>10, 40 fC signal charge];
fast trigger available [pixel signal jitter < 1ns];
large dynamic range up to 150pC

Upgrade version to be part of SPIROC III
S. Callier et. al, IEEE NSS/MIC, 2009;
0.1109/NSSMIC.2009.5401891



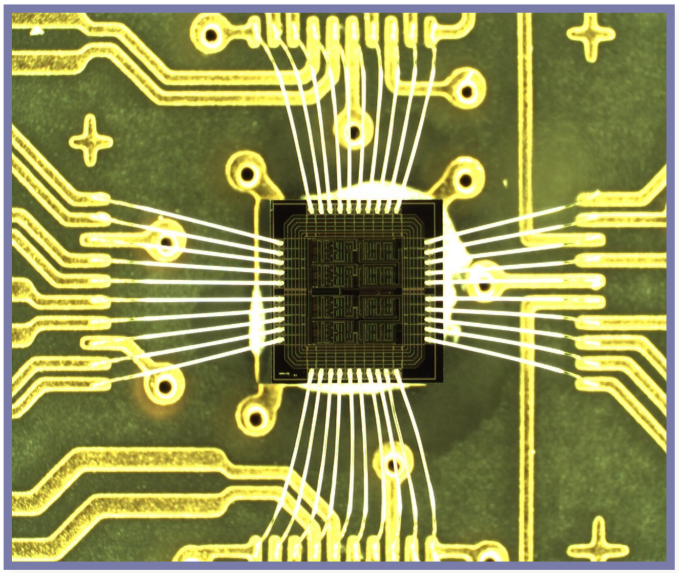
PET and ToF

STiC: SiPM Timing Chip

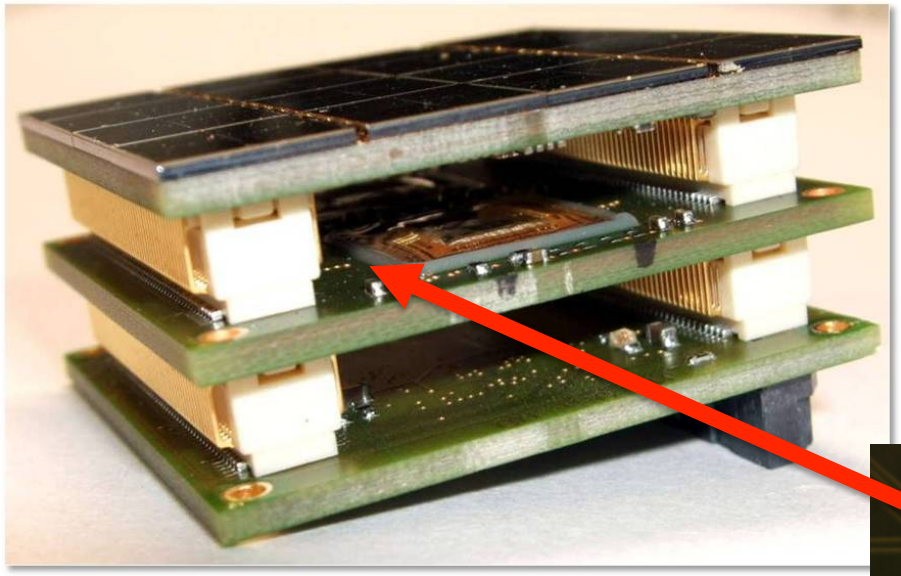
[Fast Discrimination for ToF]

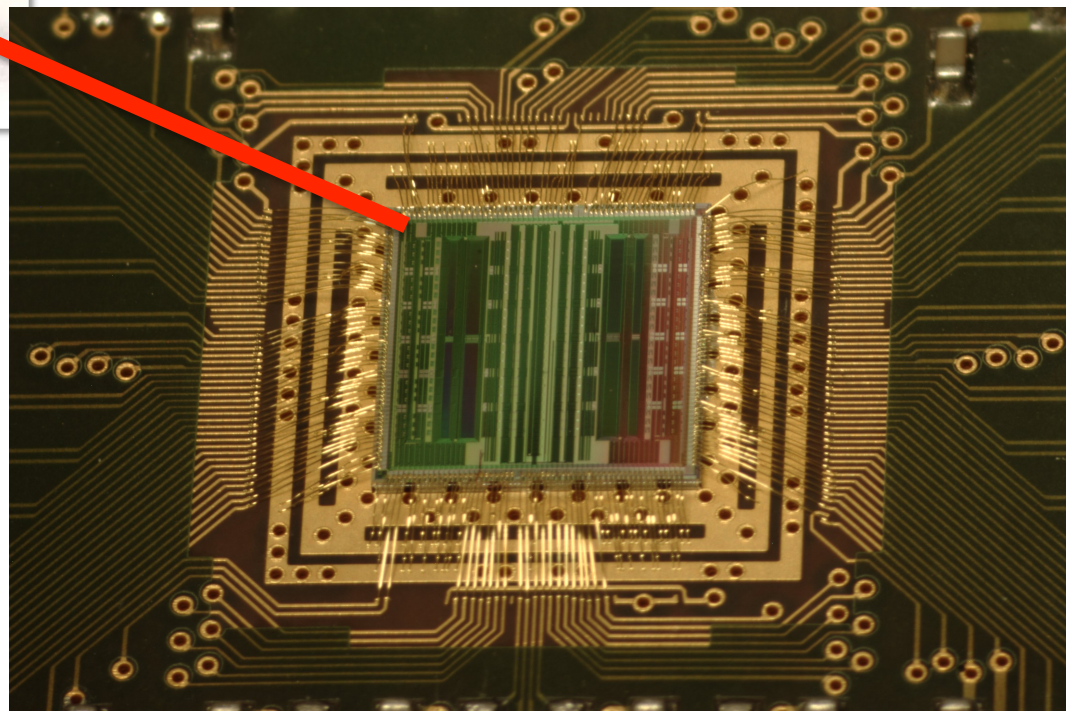
AMS 350nm CMOS , 4 channels;
Leading edge & Constant fraction Trigger;
Bias DAC tunable ~ 1 V; power < 10mW/ch
Pixel jitter ~300 ps, time of flight capability

W. Shen et. al, IEEE NSS/MIC,
2009; 10.1109/NSSMIC.2009.5401693



Readout of APD Array for PET-MR (Heidelberg)

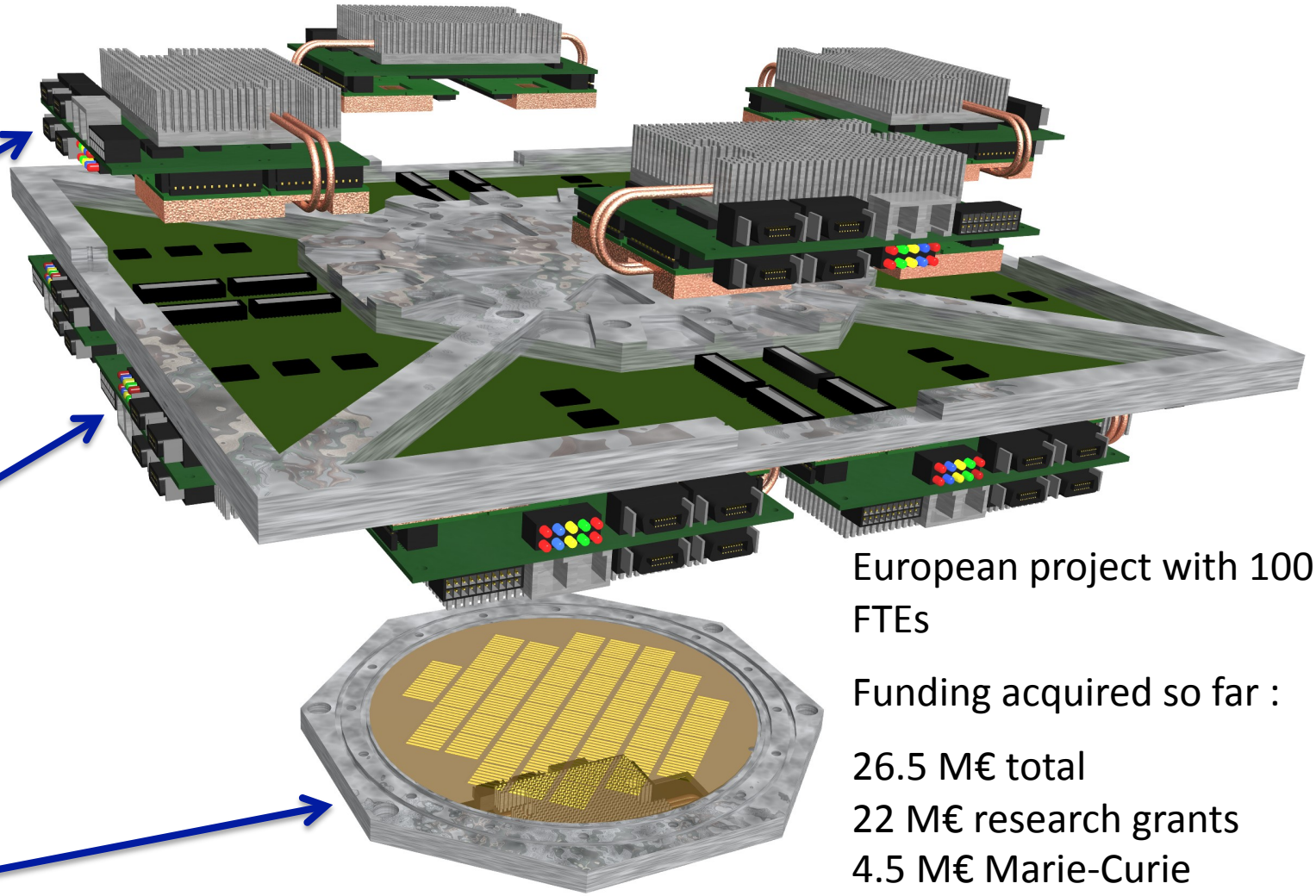




40 Channel Readout Chip

- fast low-noise differential amplifiers
- O(100µV noise)
- timestamping with 50ps binwidth
- integrator
- > 9Bit ADC

Non von-Neumann Computing
up to 200.000 electronic neurons, 50.000.000 electronic synapses
Data volume of 1 Terabits/s transferred from wafer



Control and Communication FPGAs

Control and Communication Board with digital communication ASICs

Post-Processed Neural Network Wafer (8 inch)

European project with 100 FTEs

Funding acquired so far :

26.5 M€ total
22 M€ research grants
4.5 M€ Marie-Curie

Substantial investment into Heidelberg infrastructure

TSMC 65nm CMOS Technology (towards deep(er)-submicron)

The currently used 180nm process was introduced in 1999. Since then, substantial progress has been made in semiconductor technology.

The new process offers:

- more that 10 times higher device density for all digital components
- higher clock frequencies/ faster data transmission
- low power consumption
- more routing capacitance due to 9 metal layers

Since all modern processes are optimized for digital designs, there will be some challenges for analog circuits, for example:

- significant gate tunneling
- increased leakage currents
- device mismatch
- low supply voltage

Little is published, knowledge is very restricted, need to find our ourselves !

65nm Prototype Chip (TSMC)

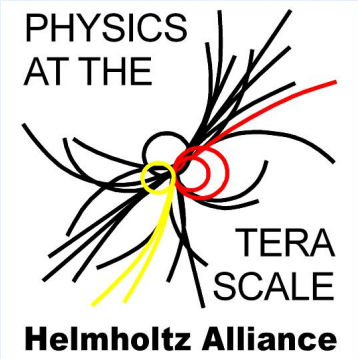
1.8mm x 1.8mm MiniASIC produced through IMEC

The content of the prototype chip will be:

- **32-bit CPU, a first version of a very compact embedded processor**
  - provides reasonable complexity to test the digital design flow for the new process

-**Analog circuits that allow for quantitative analysis of process characteristics :**
  - capacitive storage cells
  - floating gate memory cells
  - full custom SRAM
  - operational amplifiers
  - DACs

Future



Running an expensive ASIC Lab for one application (like Terascale physics) is not such a good idea :

-Limited scope (front-ends, data transmission, trigger)
-Not in all cases „academically sufficient“ (PhD theses, high impact publications, visibility
-Limited external grant support

Open to other fields and share infrastructure investments

Service activities

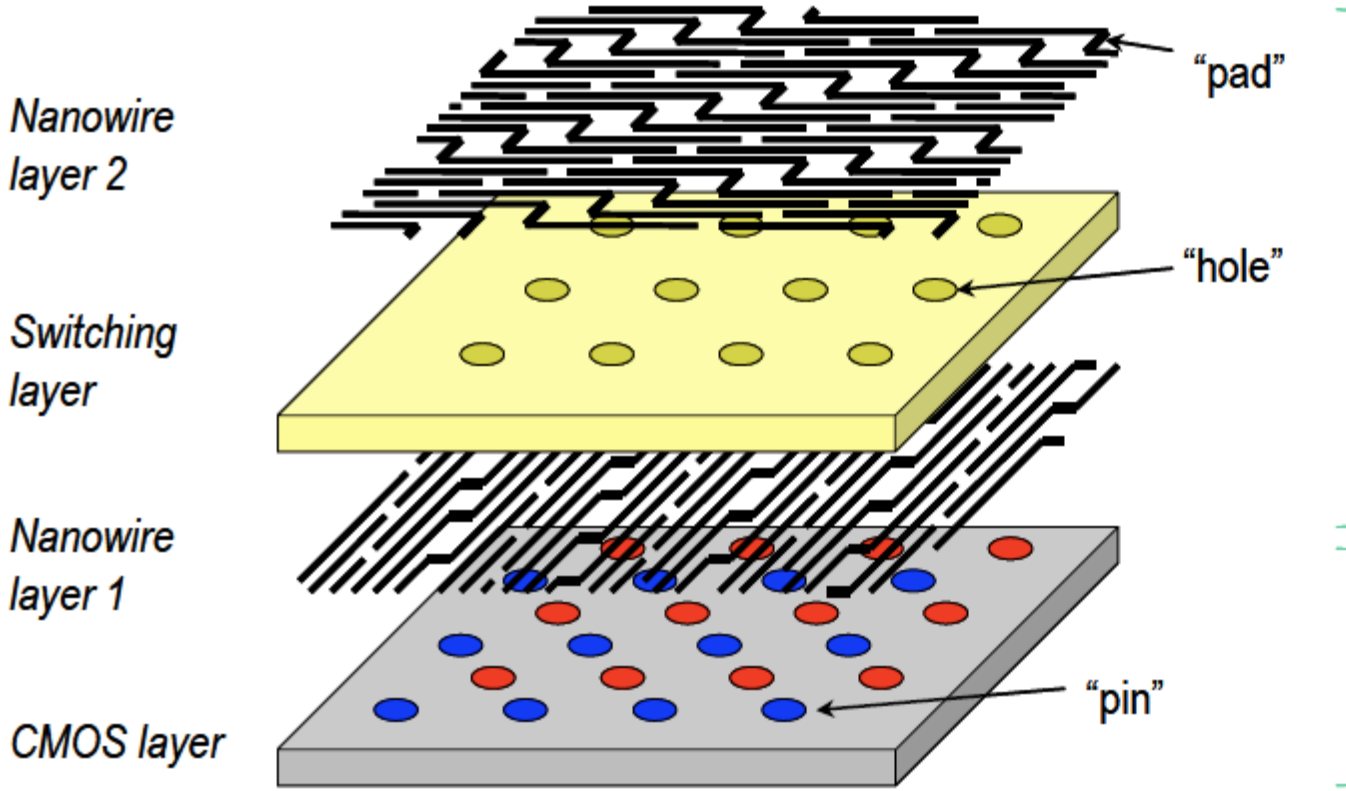
-Established cooperations : XFEL, medical imaging
-Not fully explored cooperations : FAIR, astrophysics

Stand-alone basic research activities

Novel computing paradigms, deep-submicron, nanoscale components. May well lead to future HEP applications

Will attract other sources of funding (EU, Industry)

HP FPNI : Field Programmable Nanowire Interconnect



@ 0.1 F_{CMOS} = 100x CMOS

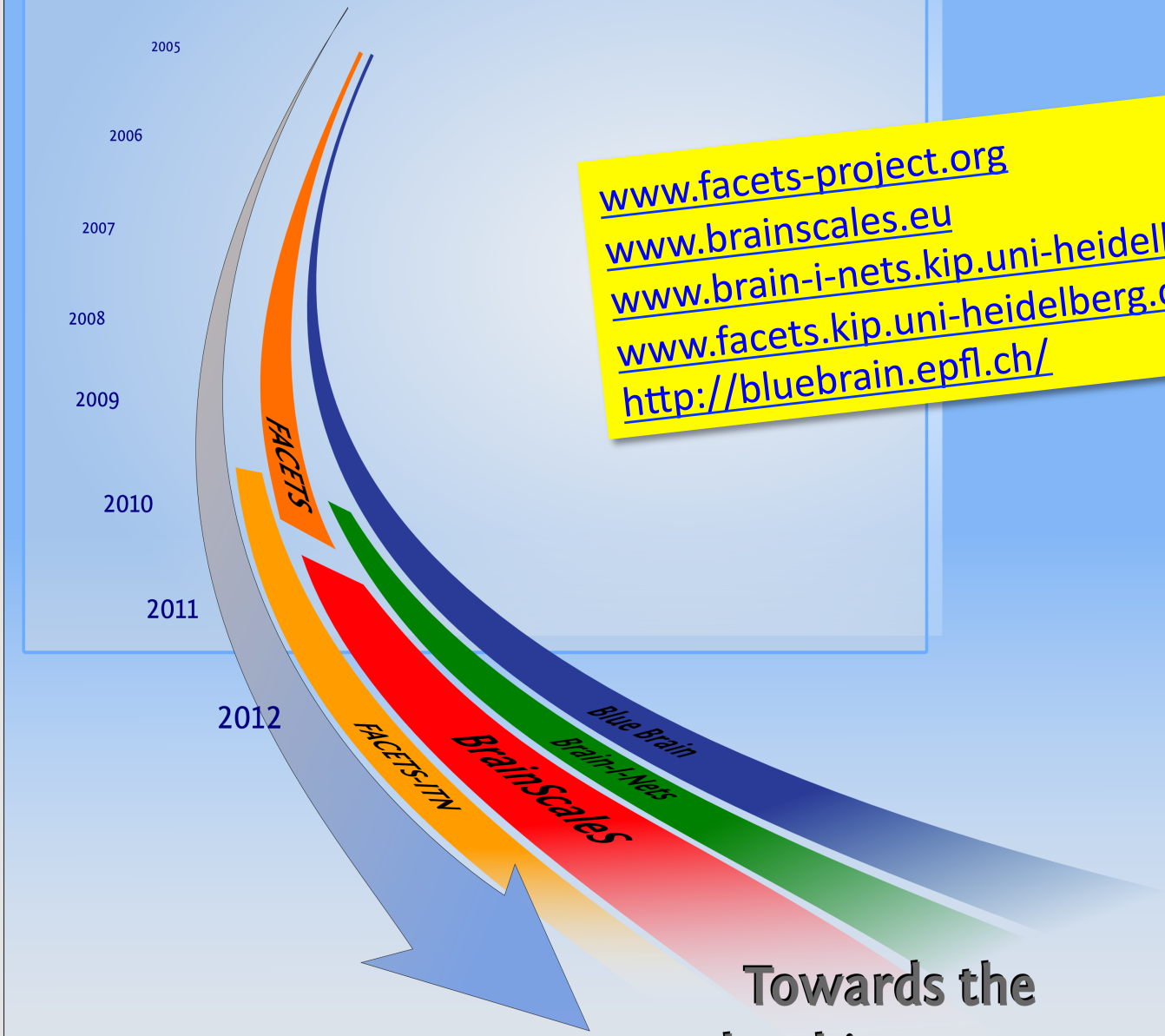
crosspoint memory

CMOS logic

Nano redundancy → defect tolerance
Small size, high yield → low cost
Low energy

G. Snider et al, IEEE Trans. Nano (2007)

CMOS – Nanoelectronics Integration



www.facets-project.org
www.brainscales.eu
www.brain-i-nets.kip.uni-heidelberg.de/
www.facets.kip.uni-heidelberg.de/ITN
http://bluebrain.epfl.ch/

Towards the FET Flagship Programme

FET FLAGSHIPS

Running an expensive ASIC Lab for one application (like Terascale physics) is not such a good idea :

-Limited scope (front-ends, data transmission, trigger)
-Not in all cases „academically sufficient“ (PhD theses, high impact publications, visibility
-Limited external grant support

Open to other fields and share infrastructure investments

Service activities

-Established cooperations : XFEL, medical imaging
-Not fully explored cooperations : FAIR, astrophysics

Stand-alone basic research activities

Novel computing paradigms, deep-submicron, nanoscale components. May well lead to future HEP applications

Will attract other sources of funding (EU, Industry)