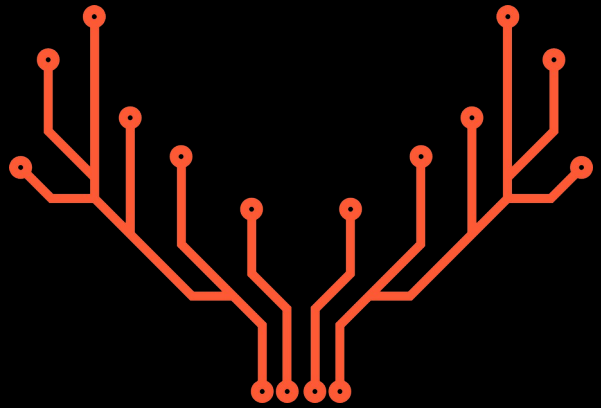
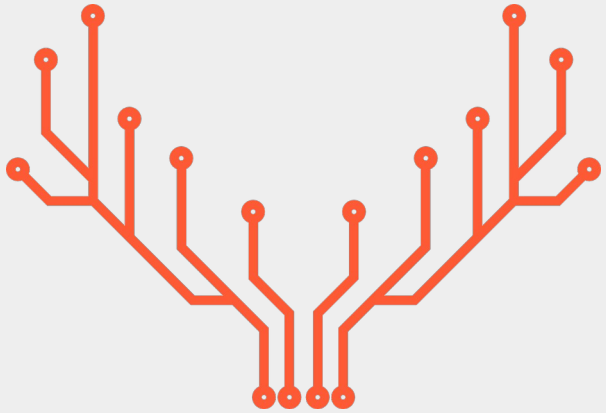


https://gitlab.cern.ch/caribou

Caribou*

A versatile data acquisition system for silicon detector prototypes



Simon Spannagel, DESY FH-ATLAS
for the Caribou Developers & Users @ DESY

Joint DESY/UHH perspectives in detector research
01 June 2023

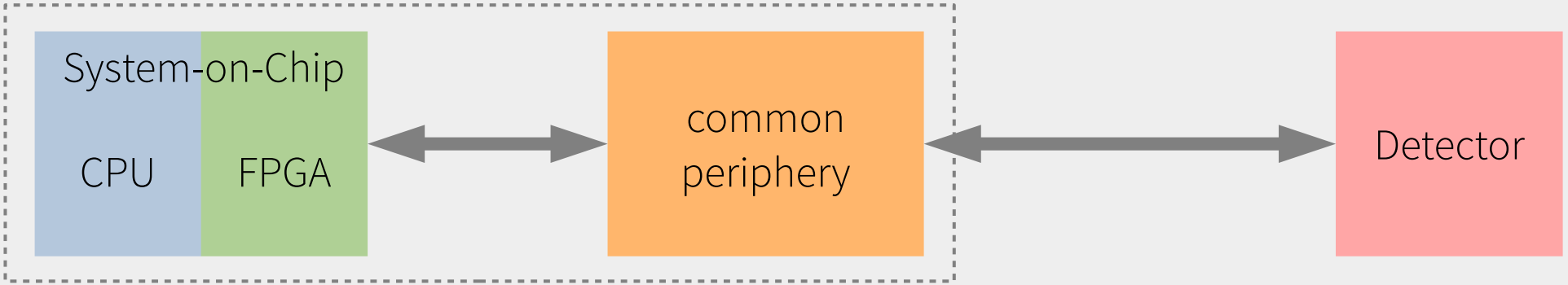
** species of deer with circumpolar distribution, native to Northern Europe, Siberia, and North America*

Motivation

- Many different silicon detector technologies under investigation
  Tangerine, ECFA DRD3, CLICdp study, ATLAS ITk prototypes, RD50…
  - Similar concept: readout, control, powering for most silicon pixel detectors
  - Differences in voltage levels, number of channels (data/voltage) or protocols
- Often development of new detector-specific DAQ for every prototype
  - Time-consuming process: developing & debugging HW/FW/SW
  - No innovative functionality compared to other systems
- A versatile DAQ system can significantly reduce time for development
  - Few changes/FW modules to write, large parts of system well tested
  - Cheaper than many systems designed from scratch

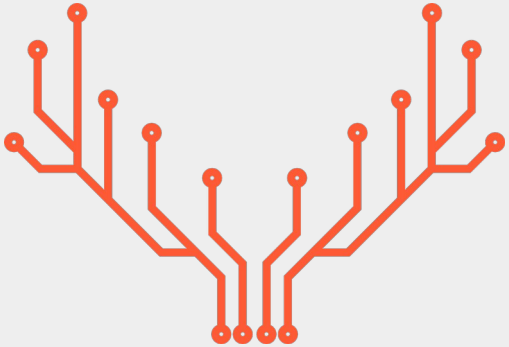
Data Acquisition for Generic Detector R&D

- Generic R&D requires flexible DAQ system, minimal effort for supporting new prototypes



- Using System-on-Chip devices to combine
  - Programmable logic (PL) – FPGA fabric for detector control, data handling
  - Processing system (PS) – CPU for data acquisition, user interface, full Linux system
- Custom-designed board with commonly used periphery components:
  voltage regulators, ADCs, LVDS connections, pulse generators, clock generator, TLU interface

The **Caribou** Data Acquisition System



- Open source hardware, firmware and software for laboratory and beam tests

- Goal: Provide a versatile DAQ system which
  - minimizes device integration effort
  - reduces time to get first data from a new detector

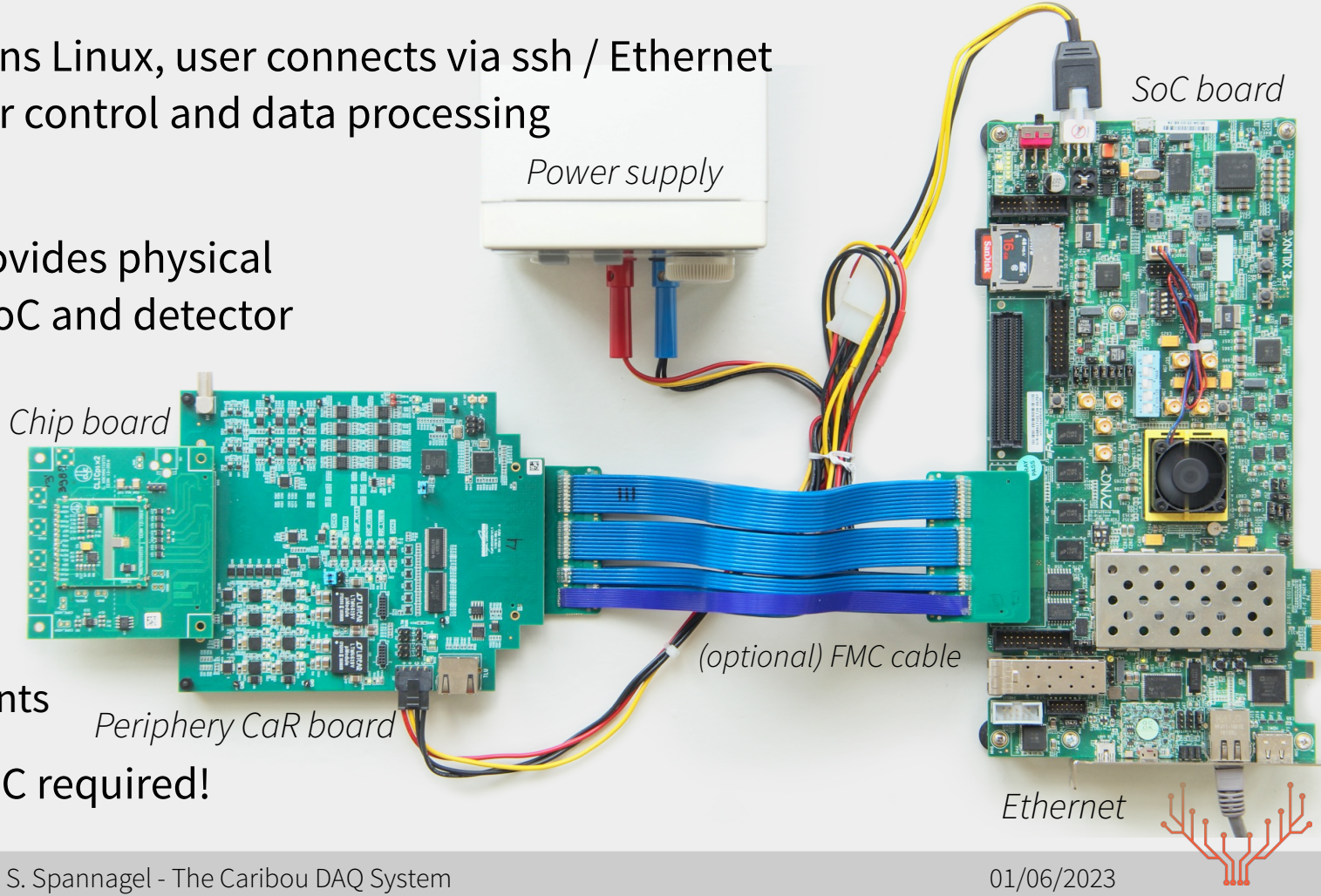
FH-FEA
FH-ATLAS

- Developed & maintained by collective effort from:

Brookhaven National Laboratory
Oak Ridge National Laboratory
Carleton University
CERN
Université de Genève

System Overview

- **SoC PS** processor runs Linux, user connects via ssh / Ethernet
  SoC PL runs detector control and data processing
- **Periphery board** provides physical interface between SoC and detector
- Application-specific **chip board:**
  - Detector
  - Passive components
- No additional DAQ PC required!

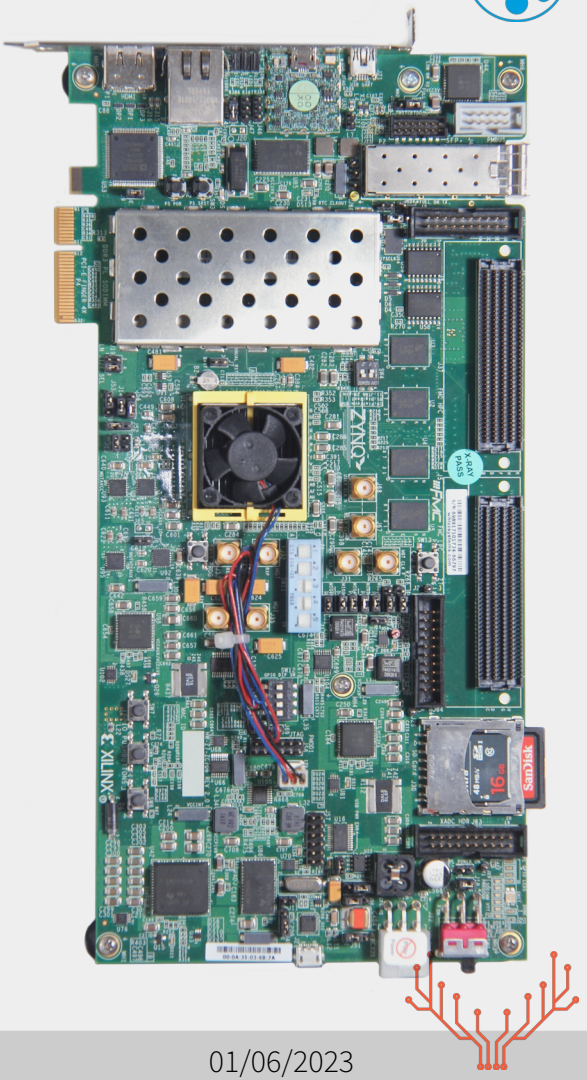


The Hardware: SoC Evaluation Board

- Based on Intel Xilinx Zynq series

- PS (embedded ARM CPU) runs full Linux operating system
  - Standalone machine, connect to via Ethernet (ssh)
  - Runs DAQ software (Peary)
  - Allows to run data analysis (quality monitoring) locally

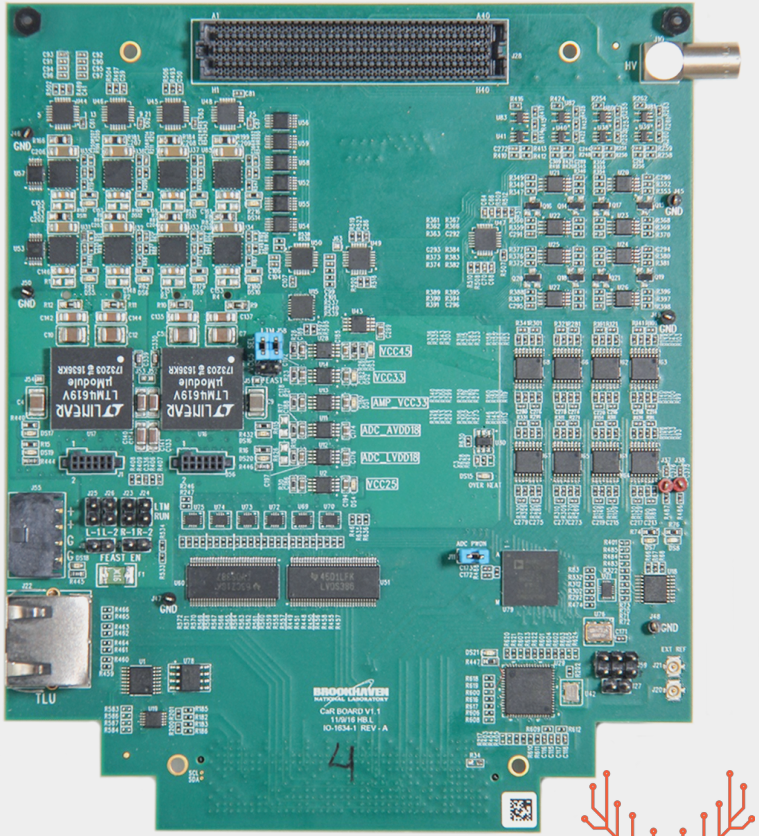
- PL runs custom firmware blocks for data processing, detector control
  - Interface between FPGA fabric and CPU available
  - Firmware for signalling & lower layers of communication protocols
  - Possibility to (pre)process data in hardware



The Hardware: Control and Readout Board

- Provides physical interface from the FPGA/SoC to the detector chip
  - Commonly used components such as voltage & current sources, clock generators, biases…

8 adjustable power supplies with monitoring (0.8 – 3.6 V, 3A)
32 adjustable voltage references (0 – 4 V)
8 adjustable current references (0 – 1 mA)
8 voltage inputs to slow (50 kSPS) 12-bit ADC (0 – 4 V)
16 analog inputs to fast (65 MSPS) 14-bit ADC (0 – 1 V)
4 programmable injection pulsers
8 full-duplex high-speed GTx links (<12 Gb/s)
17 LVDS links (bidirectional)
10/14 output and input links, adjustable level (0.8 – 3.6 V)
Programmable clock generator,
External inputs for HV, clock reference, trigger

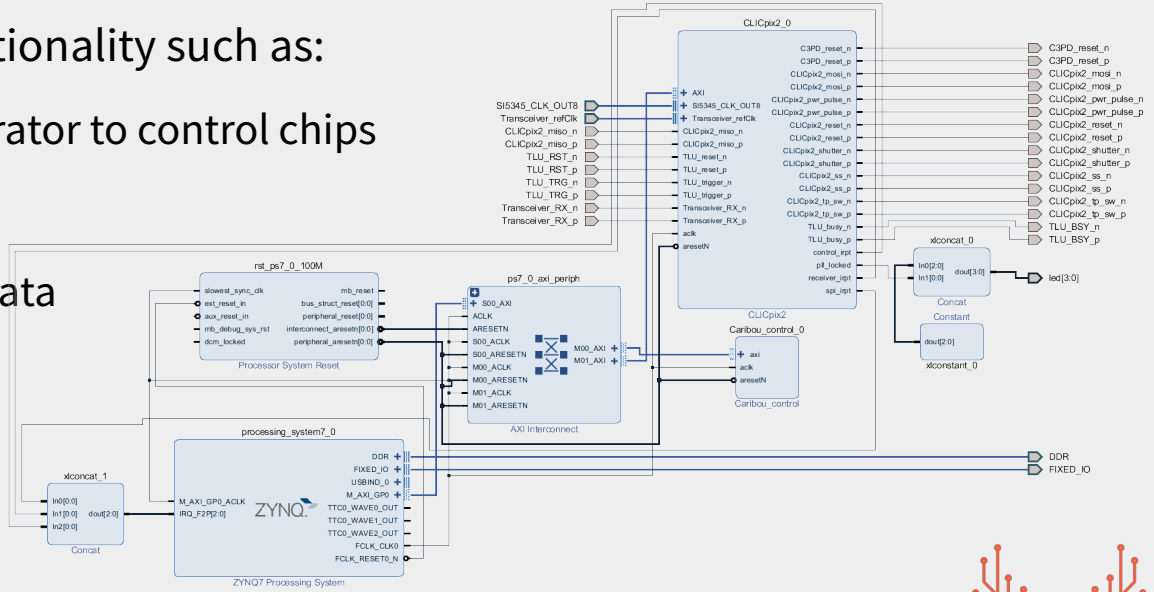


The Firmware

- Based on combination of **custom Caribou modules** and **standard Xilinx IP cores**
  - Provides an interface between CPU (SW) and a detector (HW)
  - Modules are connected to CPU through AXI bus, direct mapping of registers

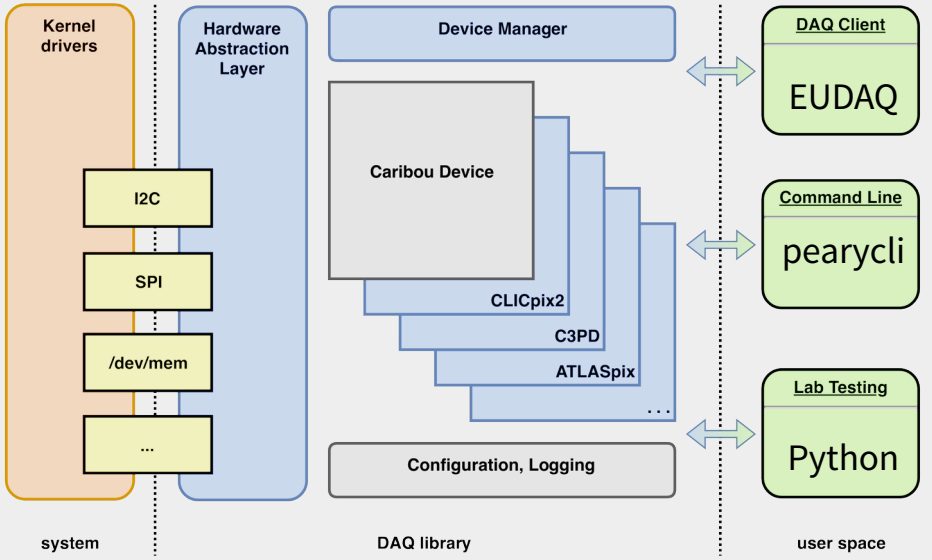
- **Caribou modules** provide common functionality such as:
  - Highly-configurable pattern/wave generator to control chips
  - Time-stamping for different signals
  - Generic ring buffer for timestamp and data

- Adding new detector-specific modules for data transfer, detector control



The Software Stack

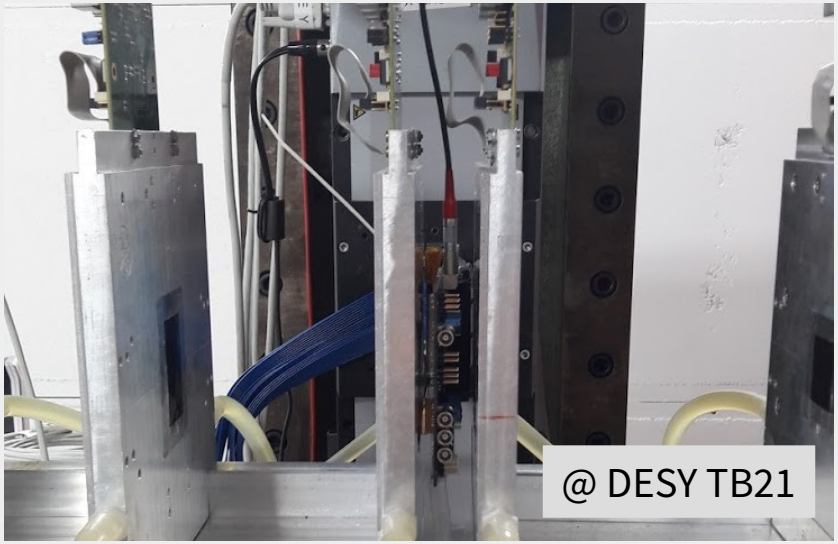
- **Custom Yocto-based Linux distribution**
  - Industry-standard OpenEmbedded build system for embedded devices
  - Custom Yocto layers (**meta-caribou**) with our software
- **Peary* DAQ Software**
  - Hardware Abstraction Layer (HAL)
  - Functions to control CaR board
  - Device management
- Various user interfaces available
  - Command line interface (CLI)
  - Client interface for integration with other systems
  - Python interface for scripting



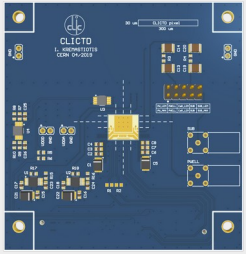
* *subspecies of caribou found in the High Arctic islands of Nunavut and the Northwest Territories in Canada*

Example: Integration at DESY-II Testbeam Facility

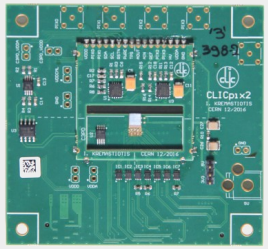
- **Hardware**
  Periphery board comes with interface for trigger logic
- **Firmware** supports different triggering modes,
  - flexible synchronization with reference devices (beam telescopes, trigger scintillators, …)
- **Software**
  Integrated with DAQ Control System
  - Works for all prototypes!
  - Direct integration with analysis software
- Successfully operated at
  - CERN SPS with CLICdp Timepix3 Telescope, ACONITE Telescope …
  - DESY with DATURA Telescope, Timepix3, TLU, …



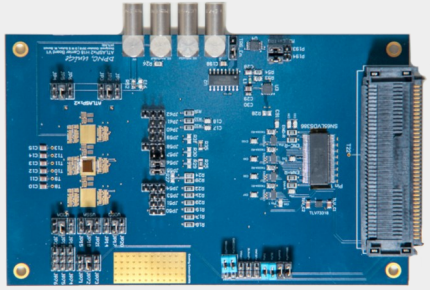
Supporting Many Devices



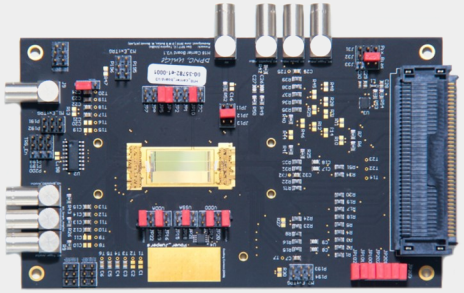
CLICTD



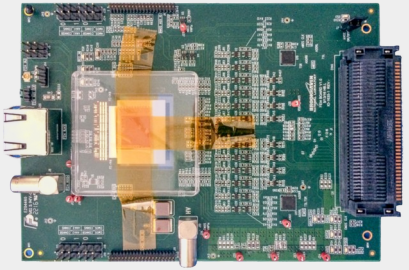
CLICpix2, C3PD



ATLASPix2

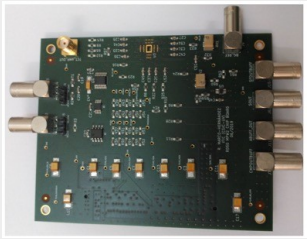


ATLASPix



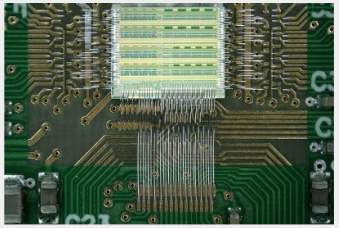
H35Demo/FEI4

RD50-MPW1

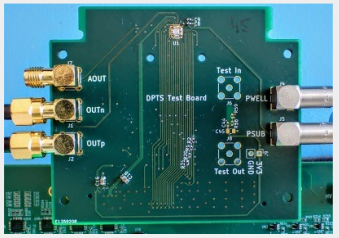


RD50-MPW2

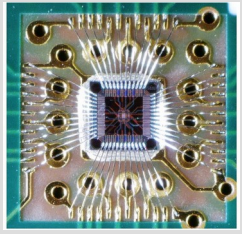
RD50-MPW3



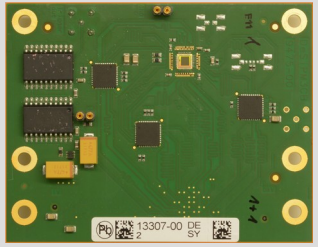
FASTPIX



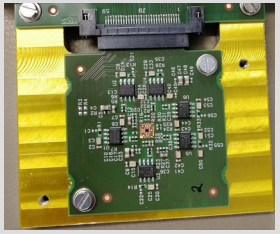
DPTS (65nm)



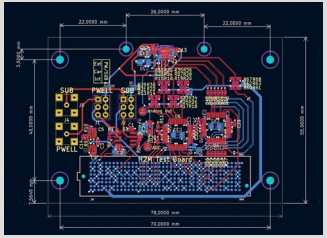
APTS (65nm)



dSiPM

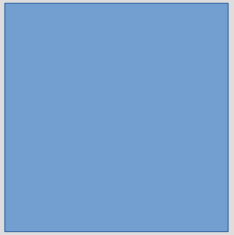


Tangerine MLR1



Tangerine H2M

CoRDIA



Tangerine DI/DII

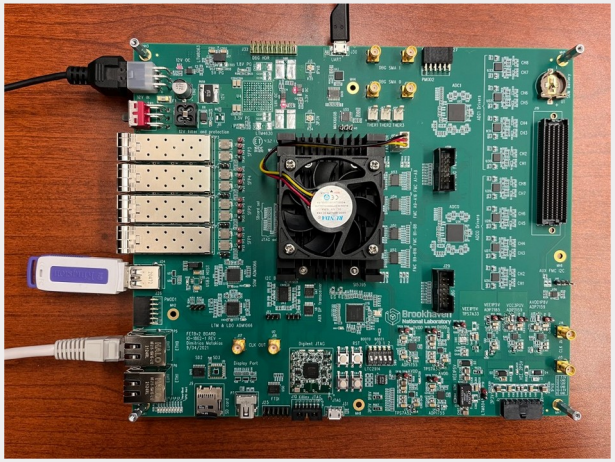
The Next Generation: Caribou 2.0

- Next version of system already currently under development
  - System-on-Module (SoM) platform based on Zynq UltraScale+
  - Replace evaluation board + Carboard with a single custom carrier board

  → Reduced cost and improved performance
  → Making system independent of evaluation board supply

Enclustra Mercury+ XU1 SoM

- Ongoing hardware design effort by Carleton University / BNL / ORNL
  - Pre-prototype carrier board from BNL with full digital design ready
  - Analog resources & design features currently being iterated
  - Carboard 2.0 design in progress, analog/power circuits well progressed



Pre-prototype for Caribou 2.0 @ BNL
Digital design only

- Aiming for first prototypes by Q3 2023

Summary & Outlook

- Caribou is a **versatile DAQ system** for silicon detectors
  - Reduce required design/production effort for DAQ systems of new prototypes
  - Provide flexible, prototype-independent integration to external systems

- Immensely profiting from Caribou v1.4 on Campus Bahrenfeld
  - **Six DESY prototypes by different groups**, integrated, minimal effort on DAQ building
  - Has show to be efficient approach to provide flexible DAQ for early-stage detector prototypes

- **Next-generation Caribou 2.0 in development**
  - Integrated System-on-Module approach, base board currently under design
  - Continued DESY involvement in:
    common FW module development, OS stack support, Peary software development


DESY.