

Master-Colloquium

Implementation of a Multi-Timepix3 Readout

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(tmblock@uni-bonn.de)

AG Desch

28.03.2023

Detector Projects

Beam
Telescope/Tracker

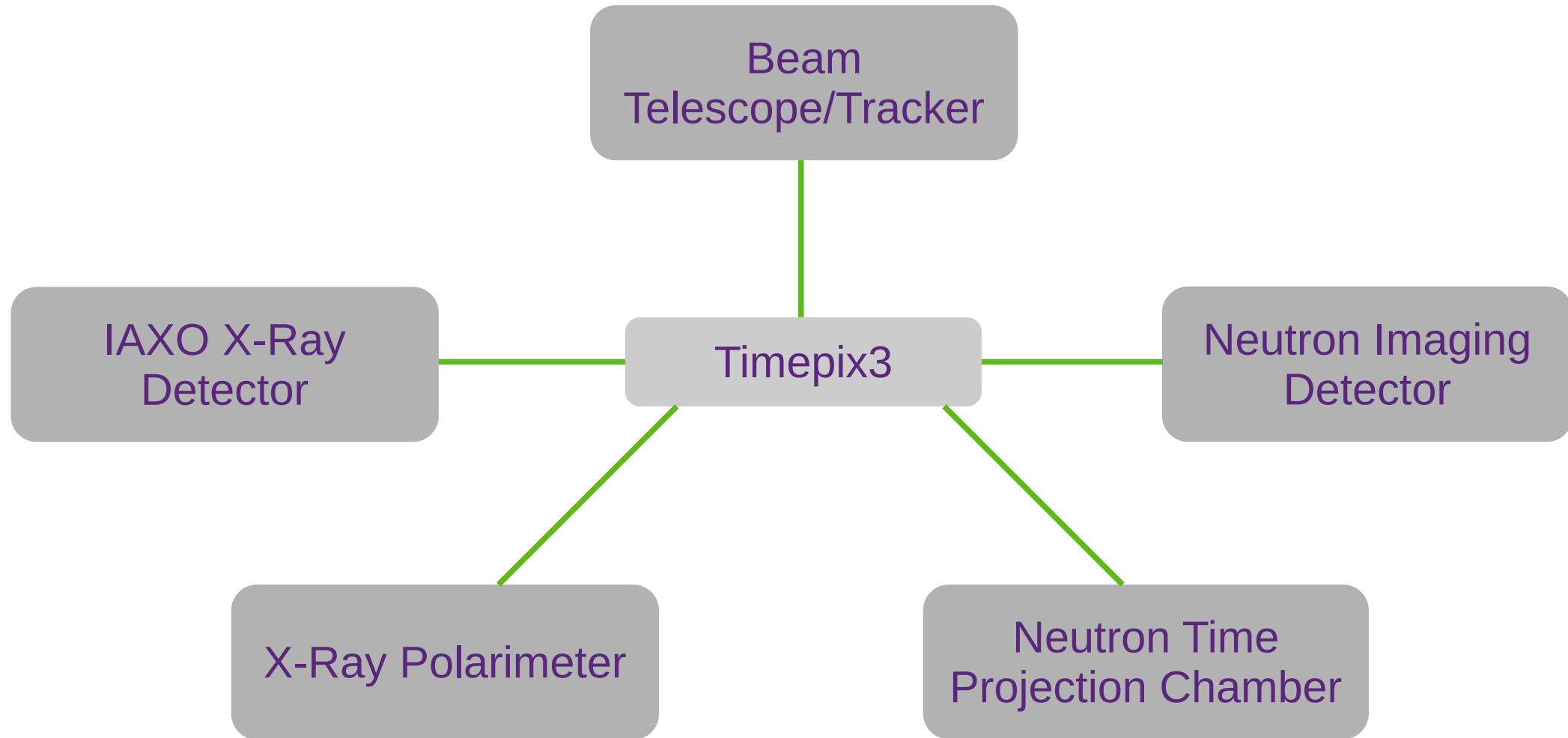
IAXO X-Ray
Detector

Neutron Imaging
Detector

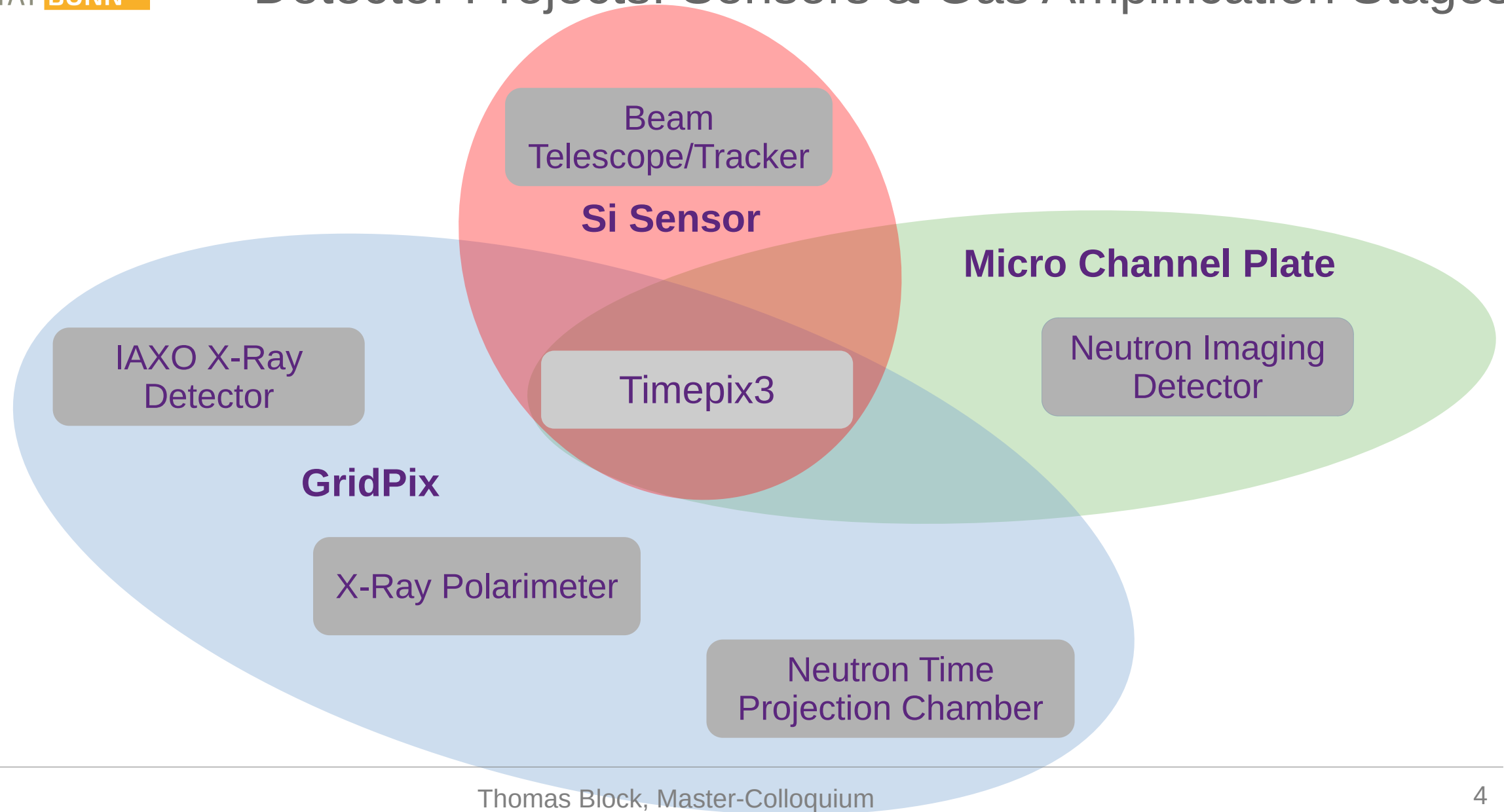
X-Ray Polarimeter

Neutron Time
Projection Chamber

Detector Projects: Readout

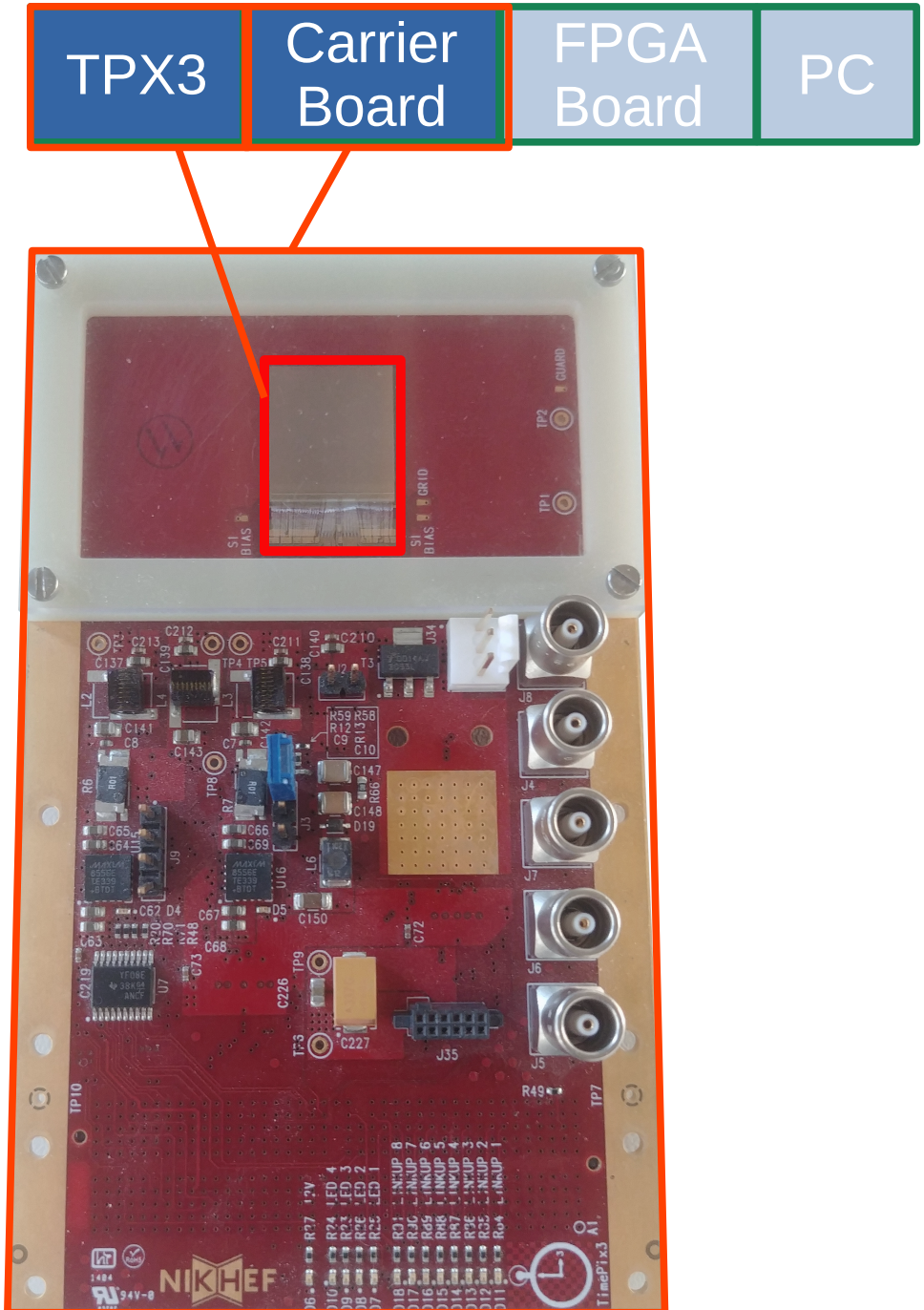


Detector Projects: Sensors & Gas Amplification Stages



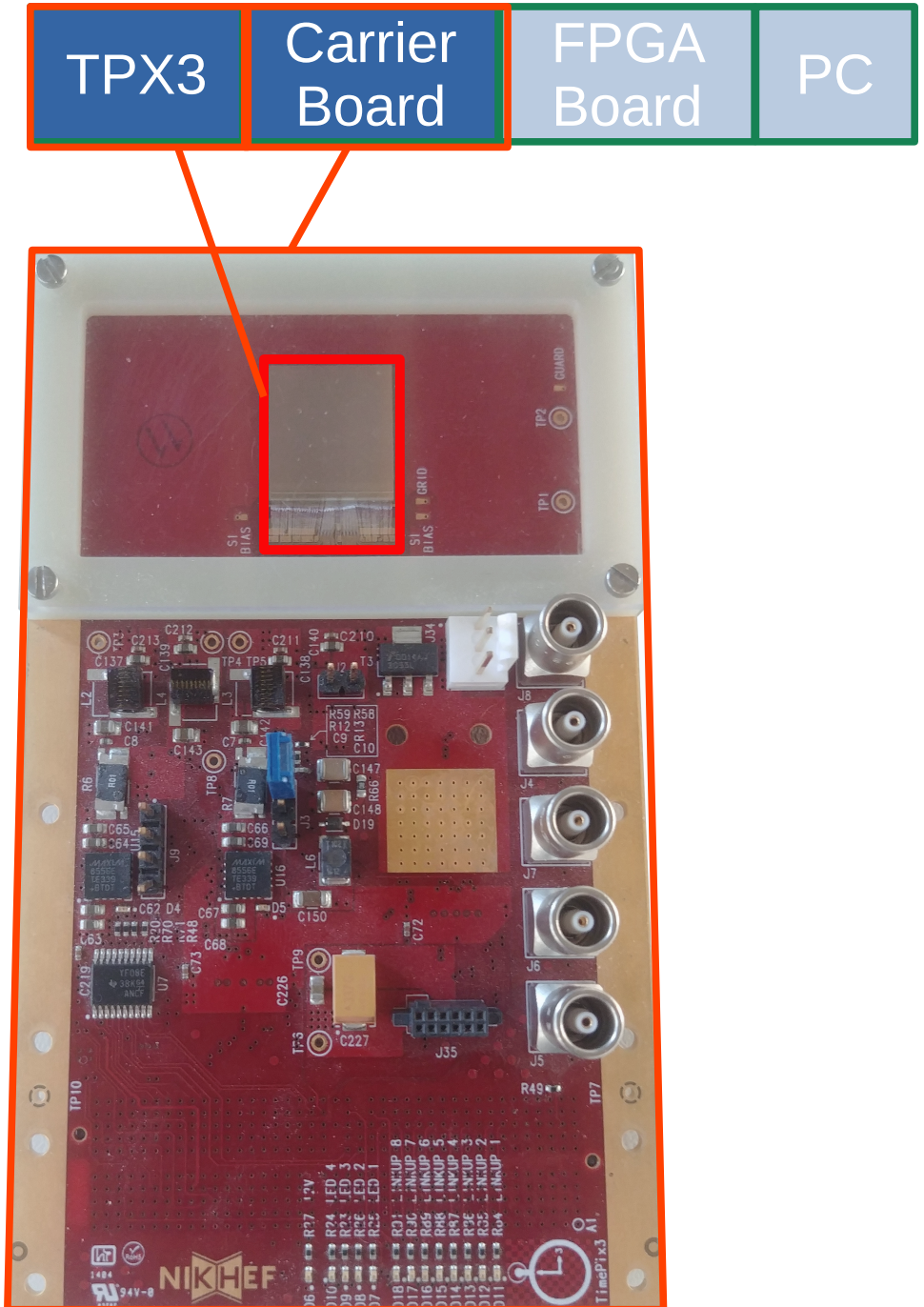
Timepix3 ASIC

Developed by	Medipix Collaboration
# Pixels	256 x 256
Pixel size	(55 x 55) μm^2
Timing resolution	1.56 ns (@ 640 MHz)
Acquisition modes	ToT & ToA ToA only Hit Counter & iToT
Readout modes	Data driven Sequential (both zero-suppressed)
Data links	8
Output bandwidth	Max. 5.12 Gbit s ⁻¹



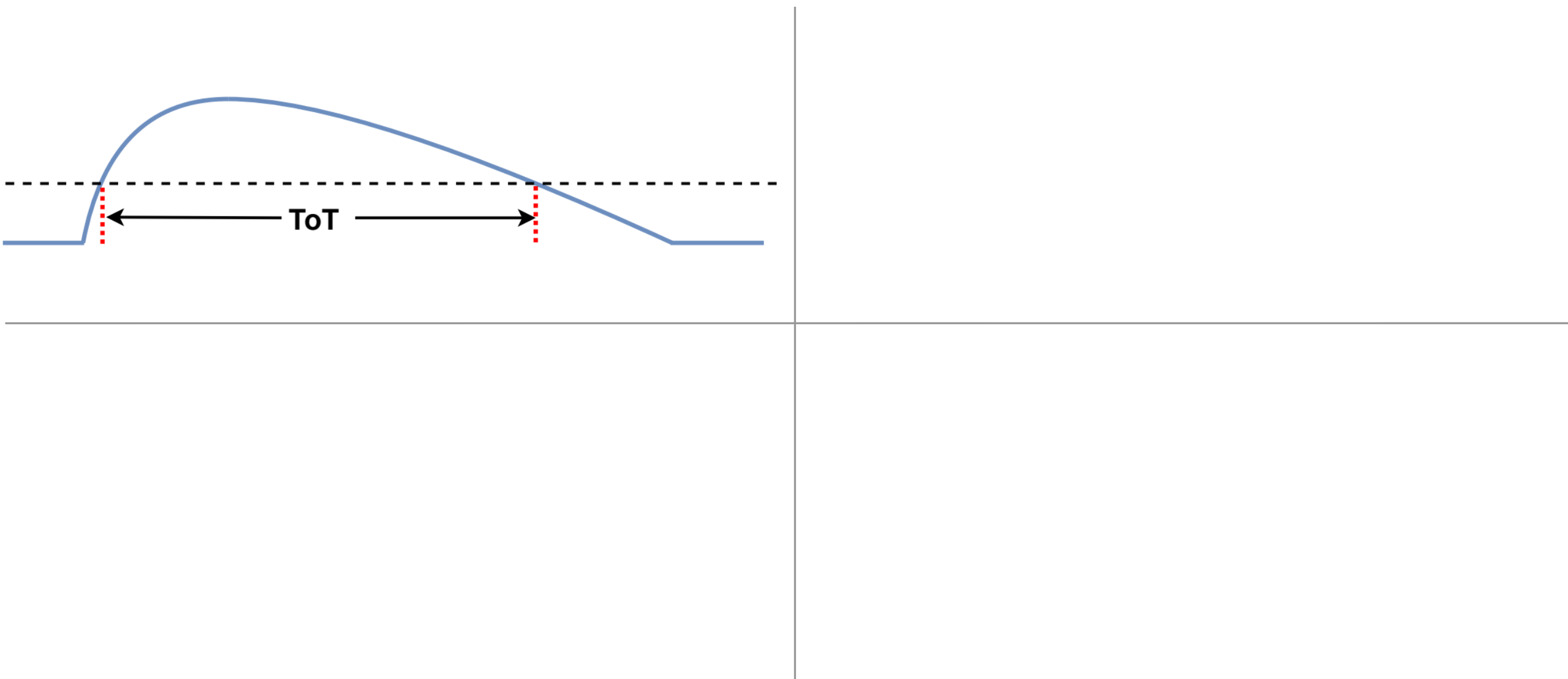
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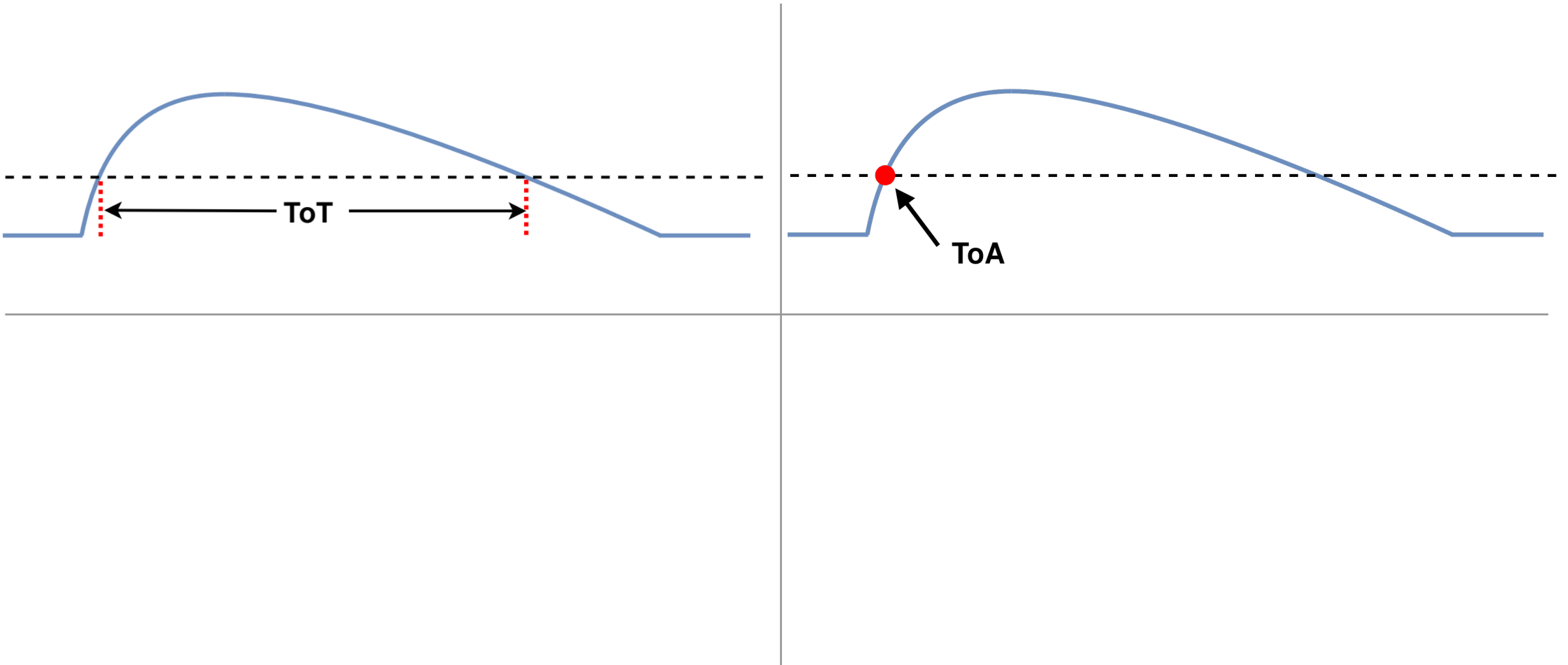


Timepix3 ASIC – Acquisition Modes

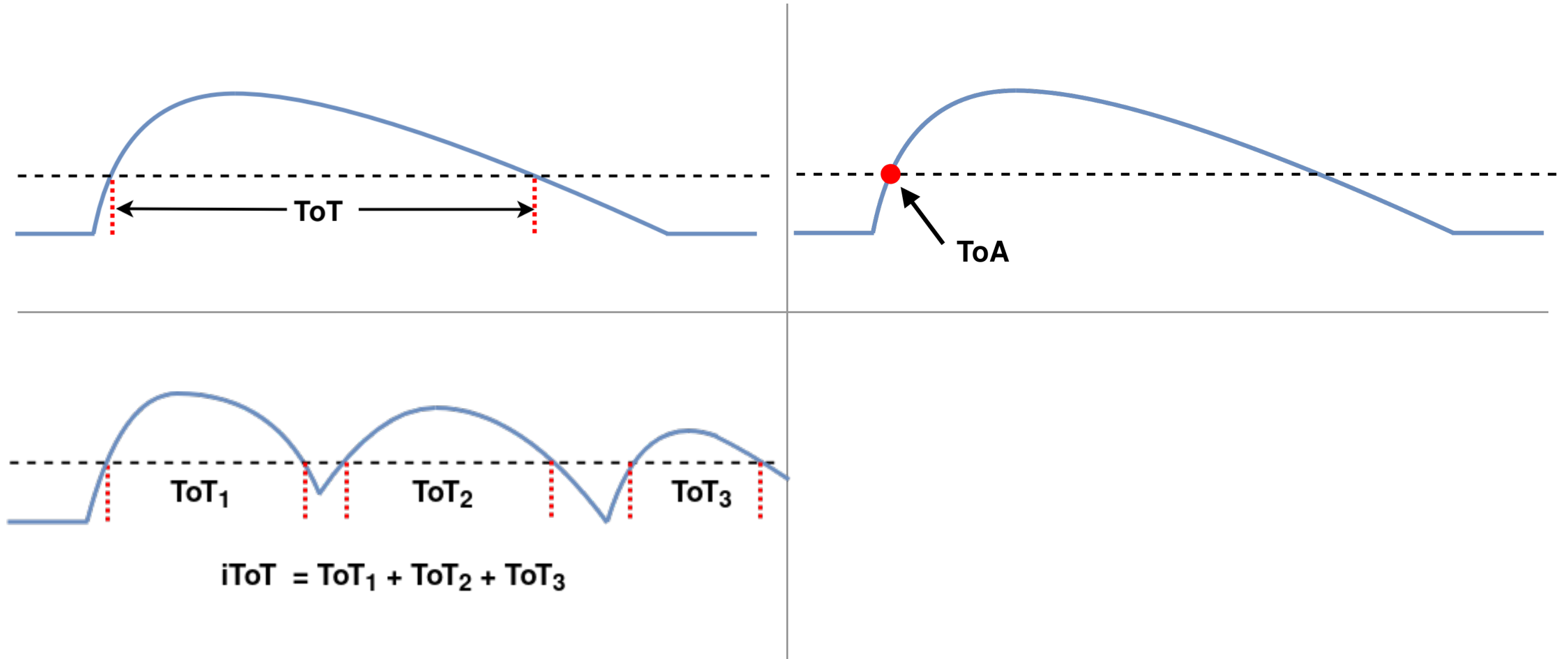
Timepix3 ASIC – Acquisition Modes



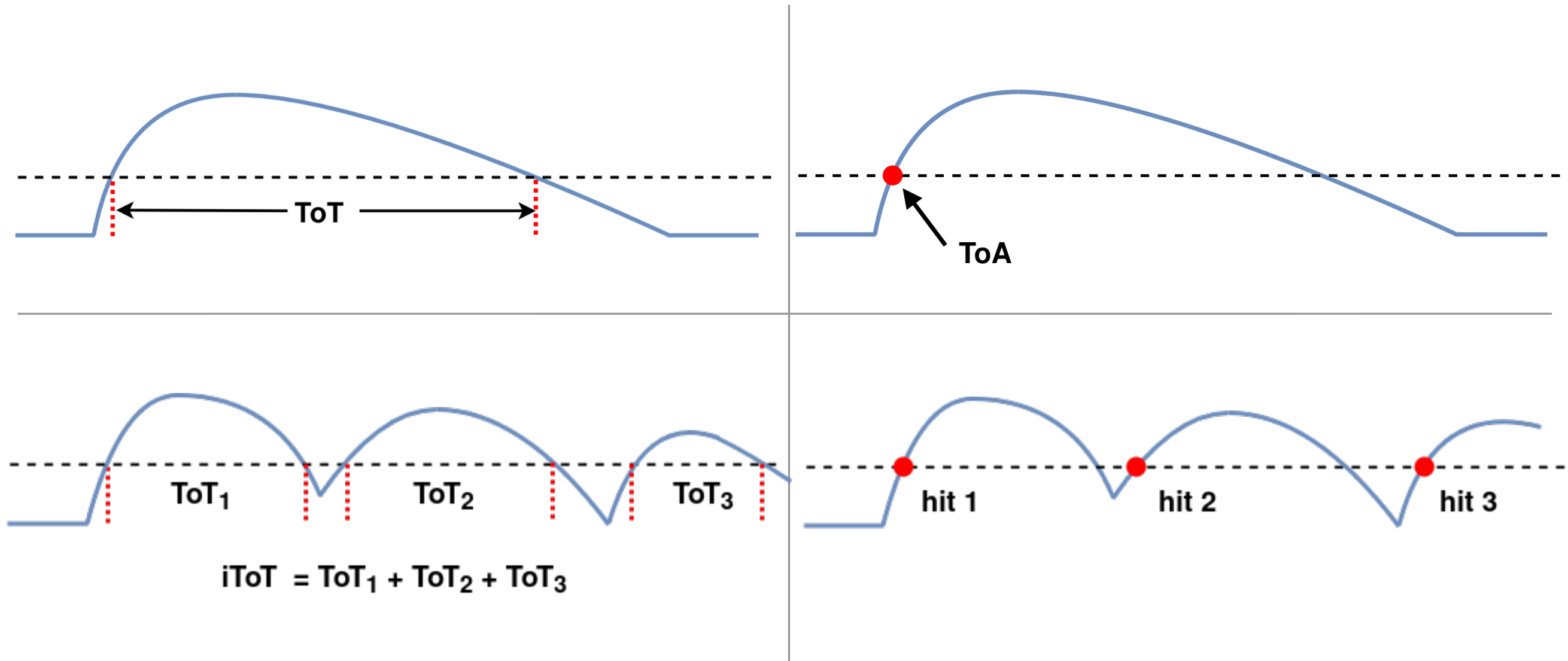
Timepix3 ASIC – Acquisition Modes



Timepix3 ASIC – Acquisition Modes

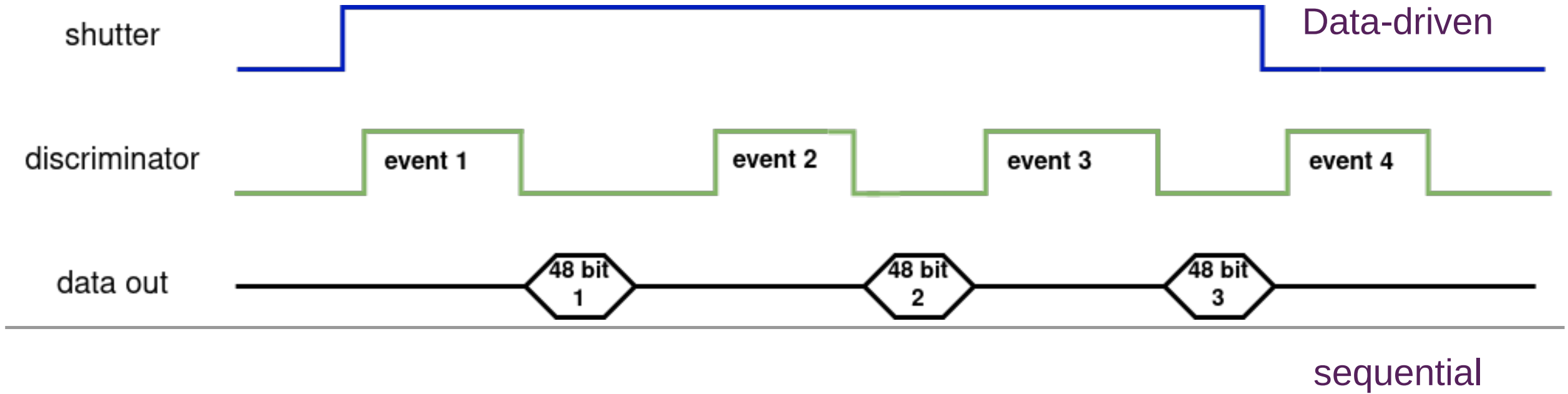


Timepix3 ASIC – Acquisition Modes

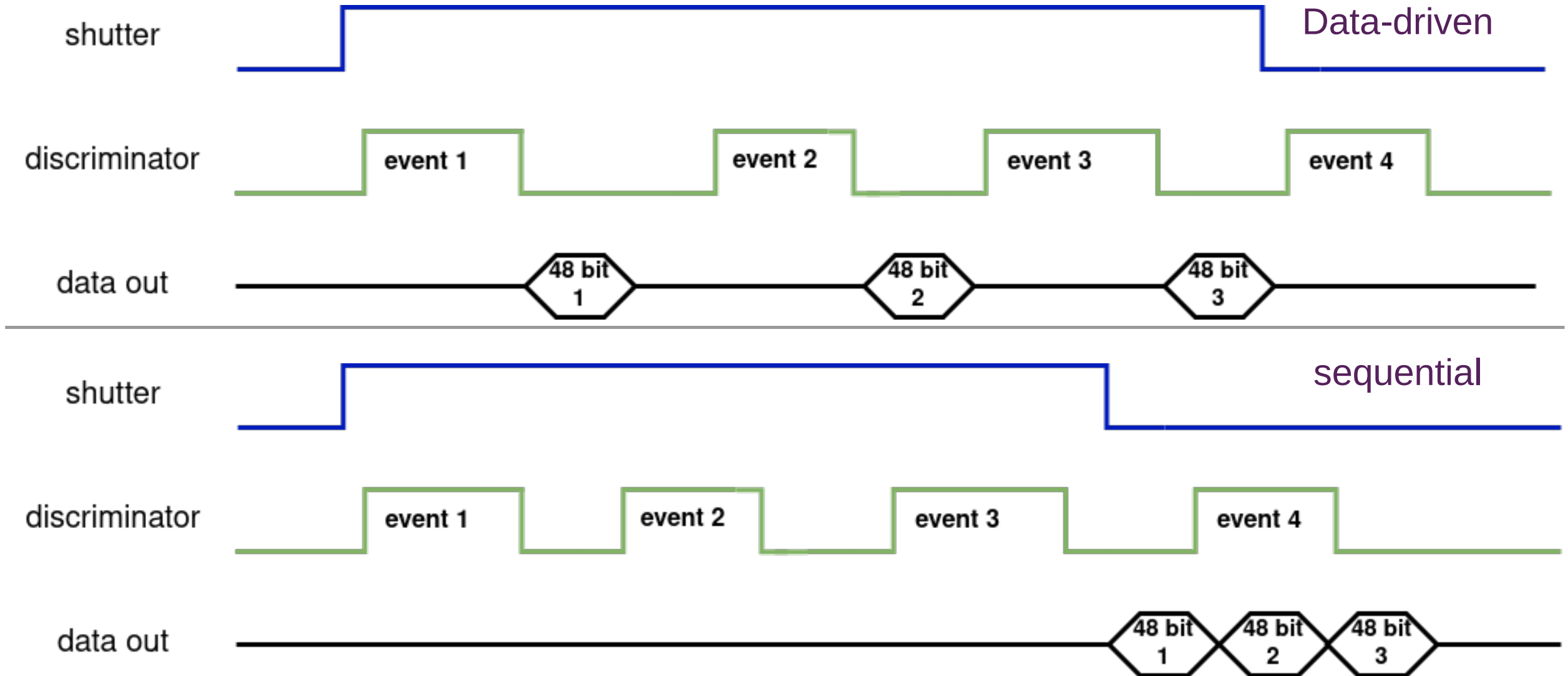


Timepix3 ASIC – Readout Modes

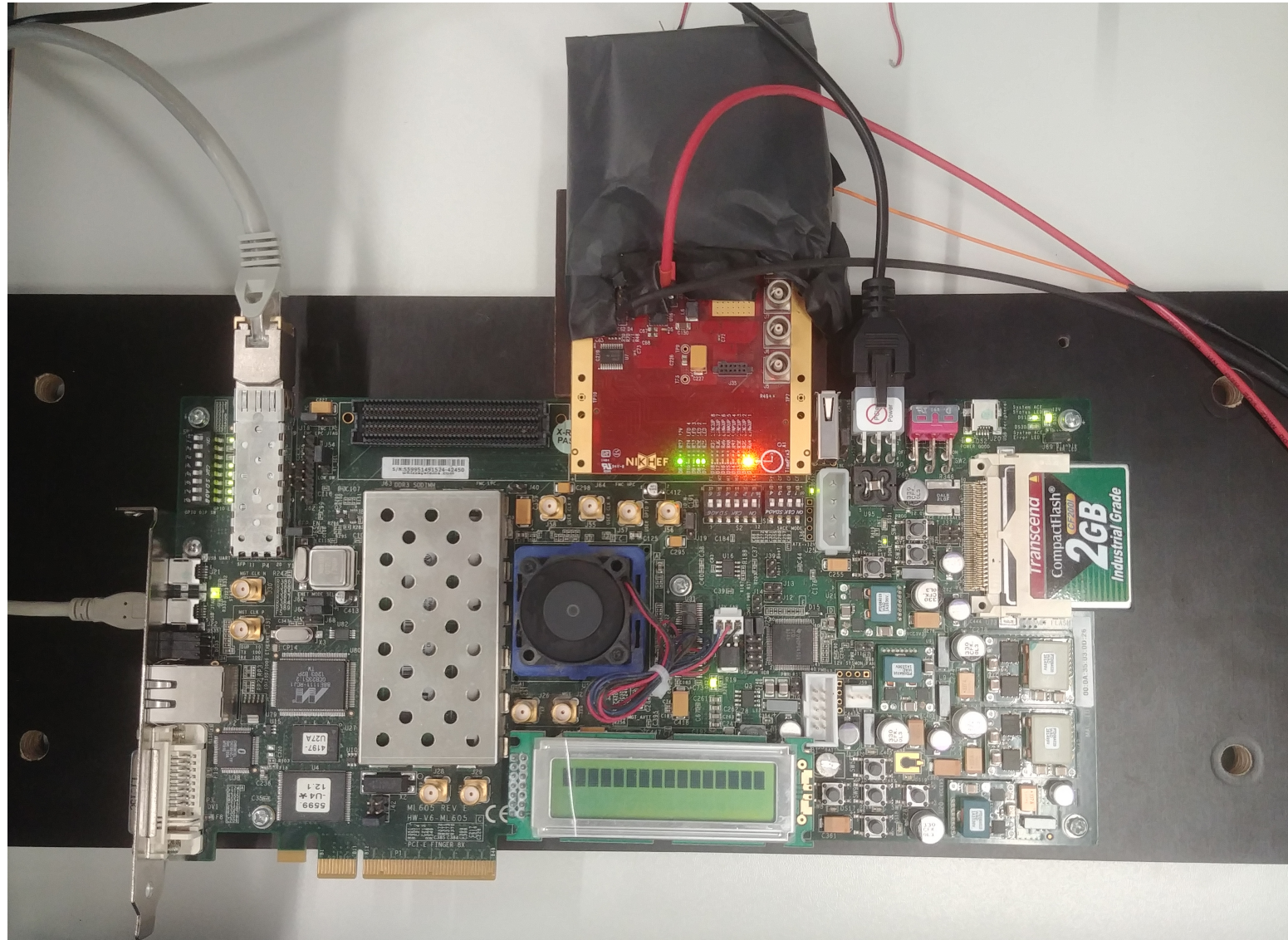
Timepix3 ASIC – Readout Modes



Timepix3 ASIC – Readout Modes



Setup



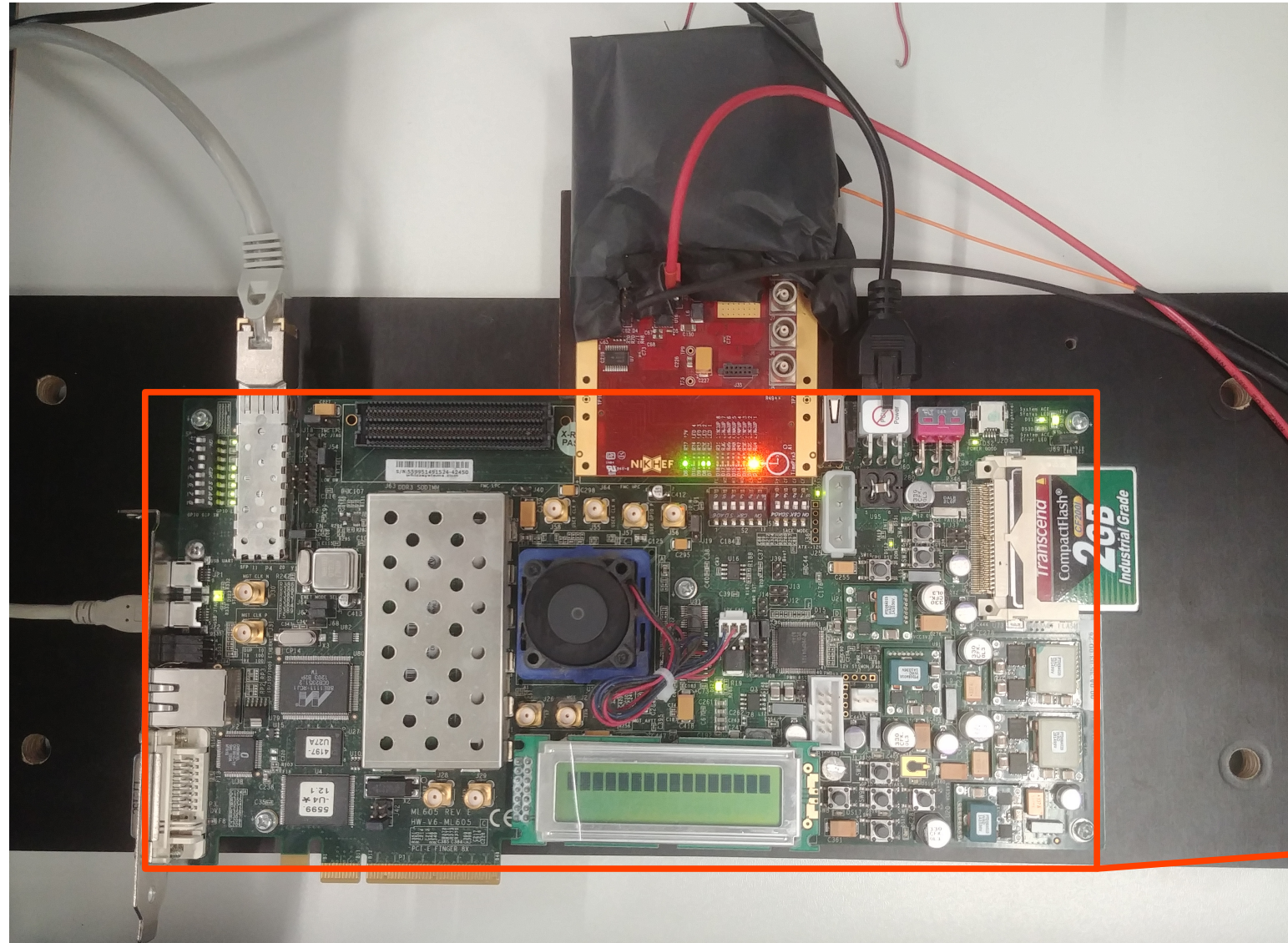
Setup

TPX3

Carrier
Board

FPGA
Board

PC



ML605

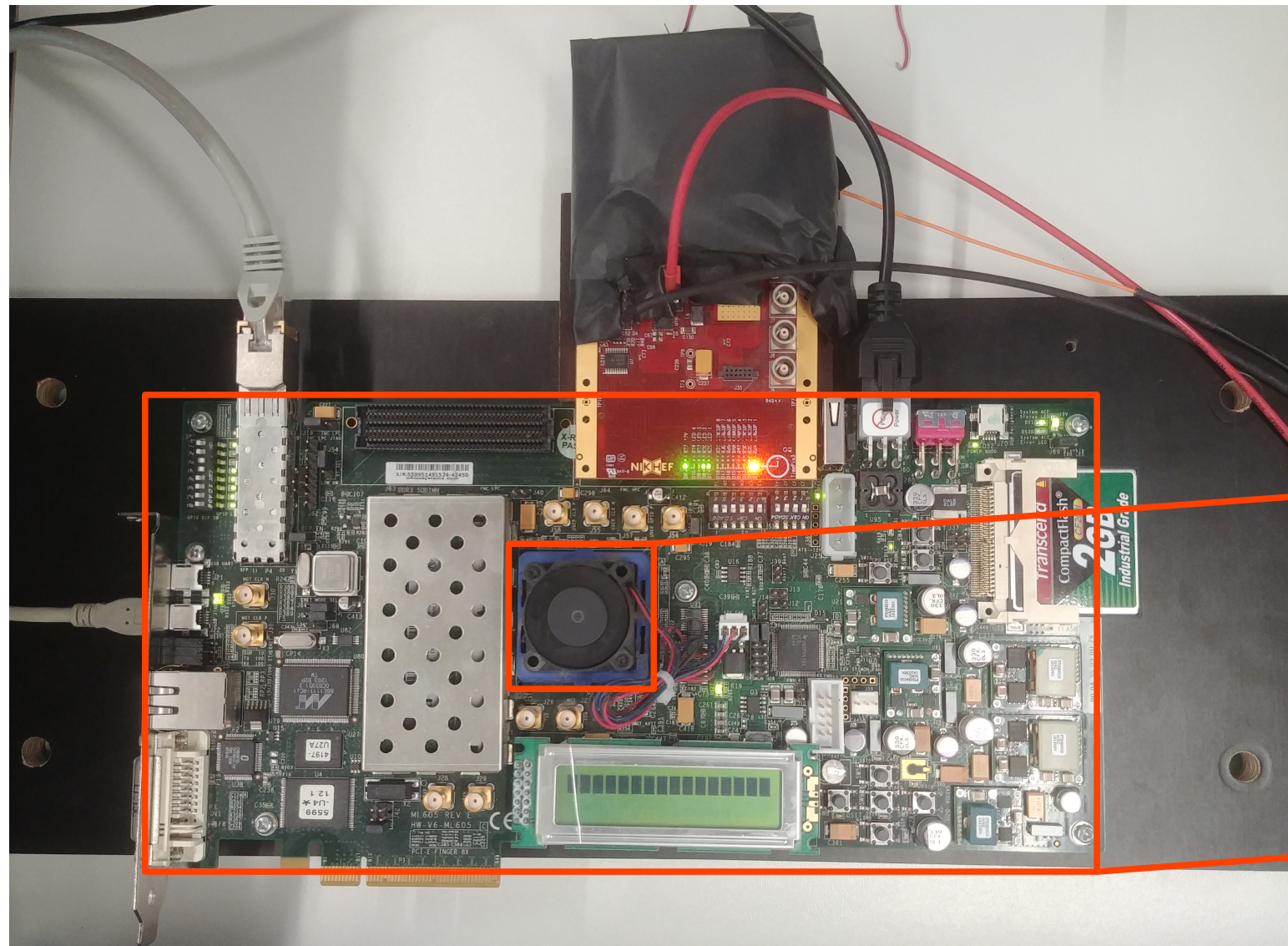
Setup

TPX3

Carrier
Board

FPGA
Board

PC

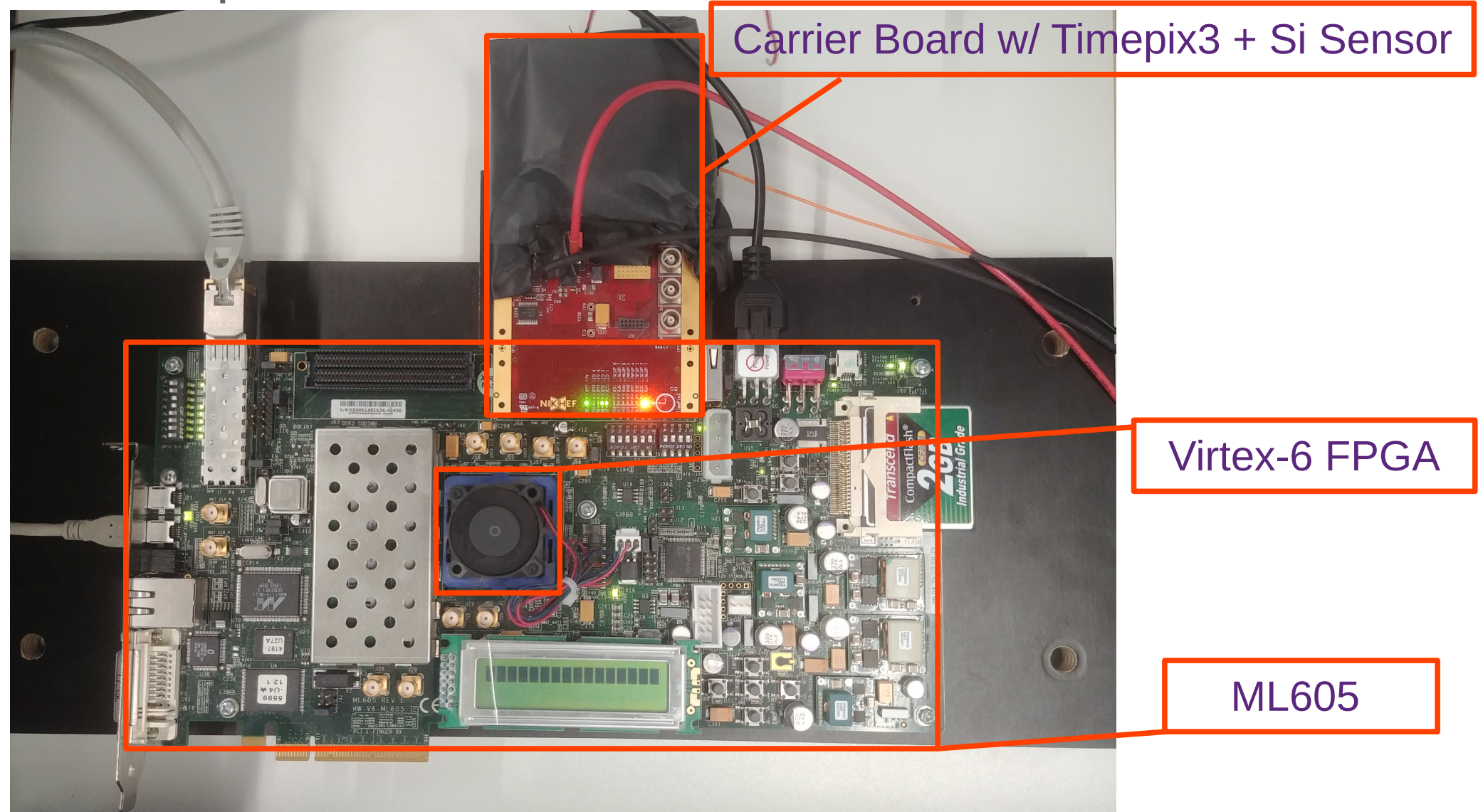


Virtex-6 FPGA

ML605

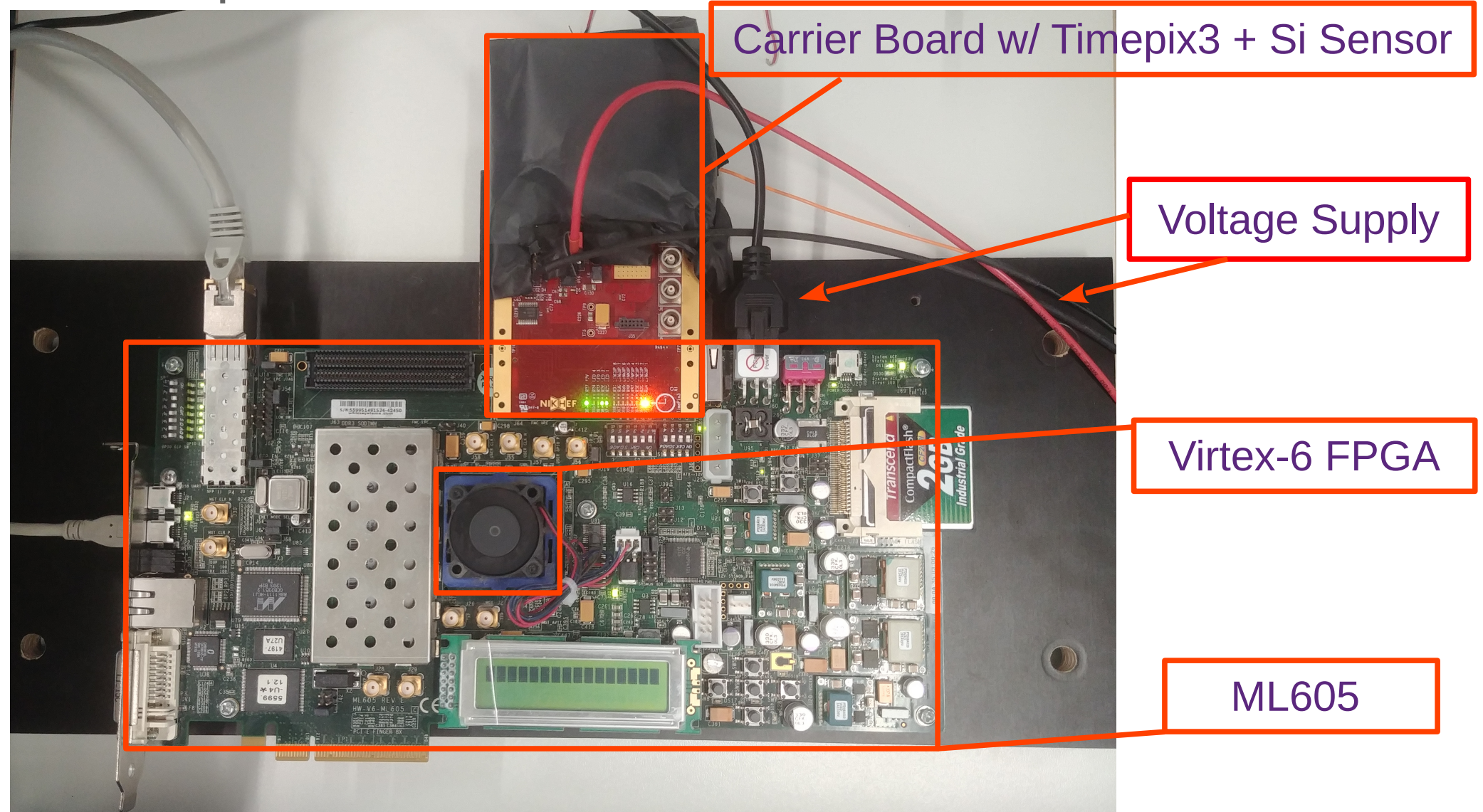
Setup

TPX3	Carrier Board	FPGA Board	PC
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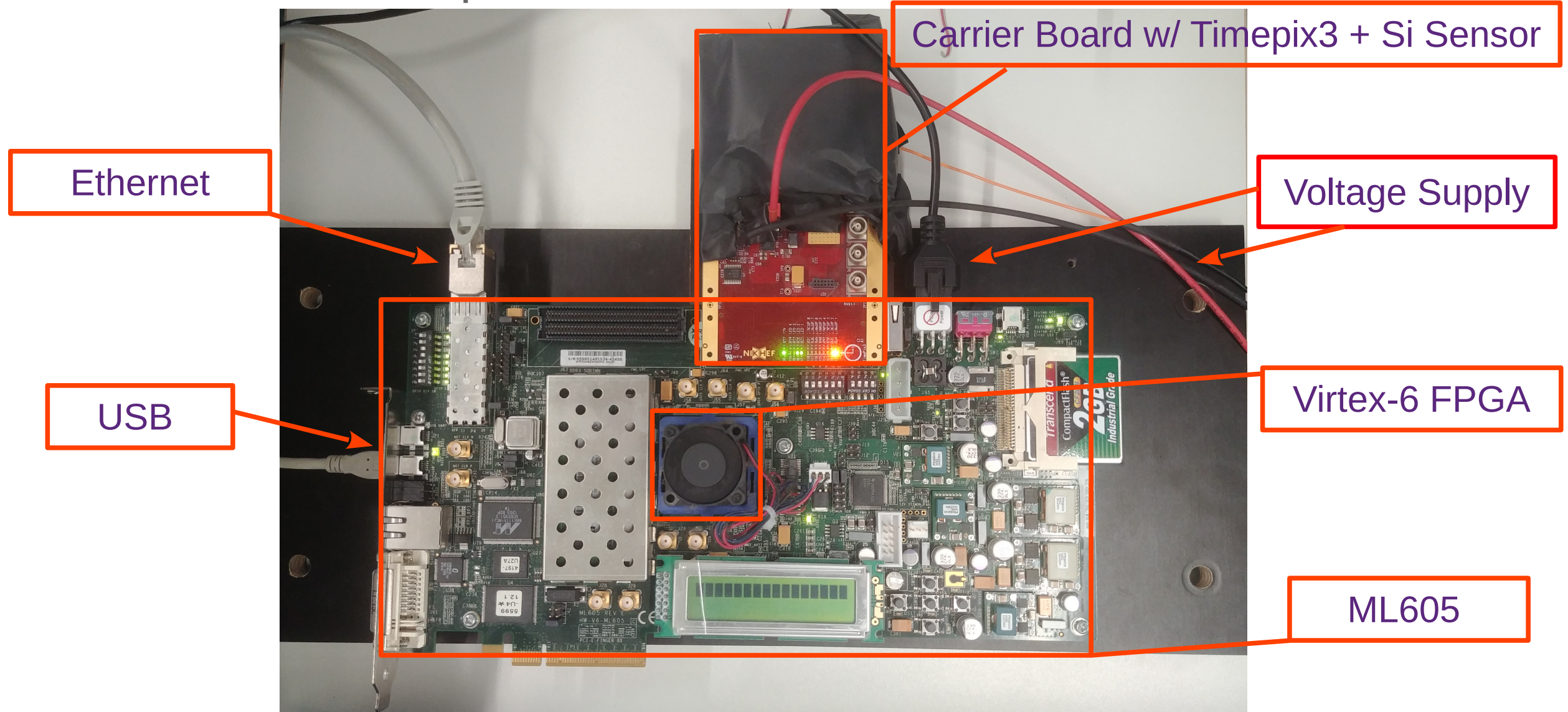
Setup

TPX3	Carrier Board	FPGA Board	PC
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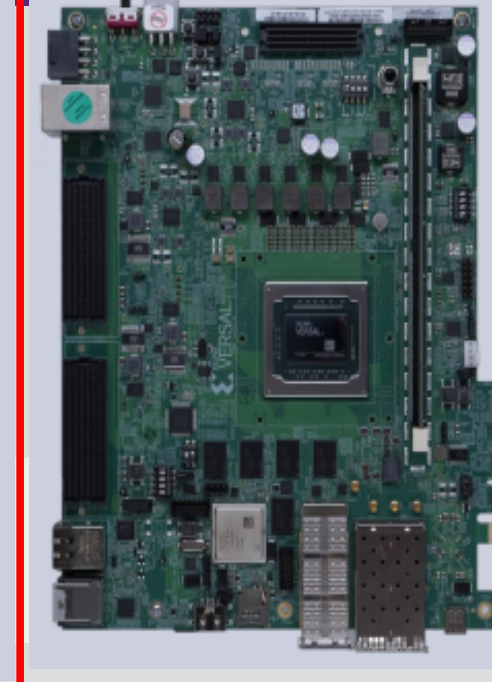


Setup

TPX3	Carrier Board	FPGA Board	PC
------	---------------	------------	----



FPGA & Board support

Board	MIMAS A7	SRSv6	ML605	VCK190
Picture				
Status				
FPGA	Artix-7	Virtex-6	Virtex-6	Versal Prime (AI)
I/O Links and Rate	2 links x 320 Mbps	8 links x 320 Mbps	8 links x 320 Mbps	> 8 links x 640 Mbps

Firmware written in Verilog

Software written in Python

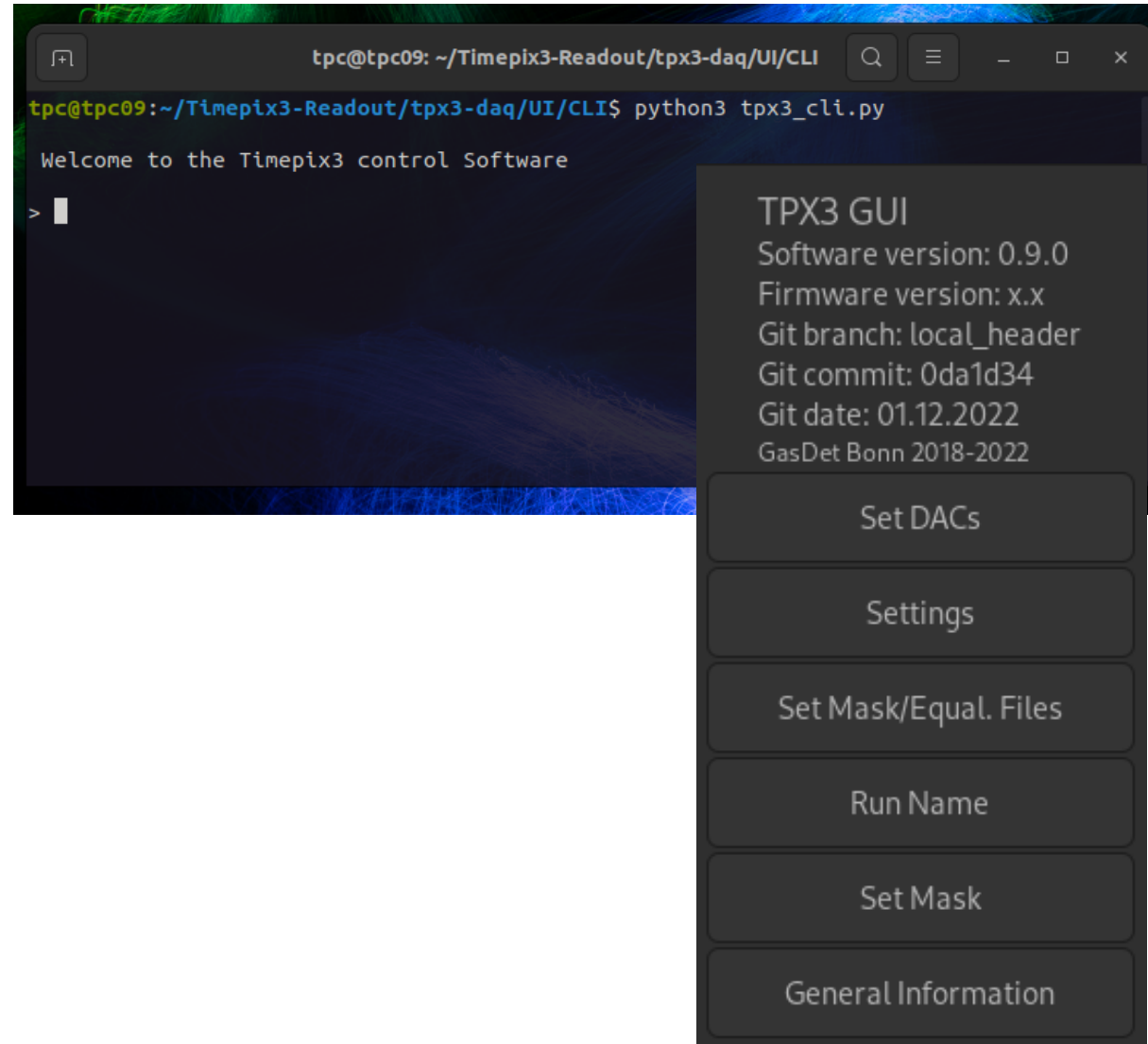
Based on basil-framework
(github.com/SiLab-Bonn/basil)

Graphical User Interface
(GUI) and Command Line
Interface (CLI)

Data stored in HDF5 files

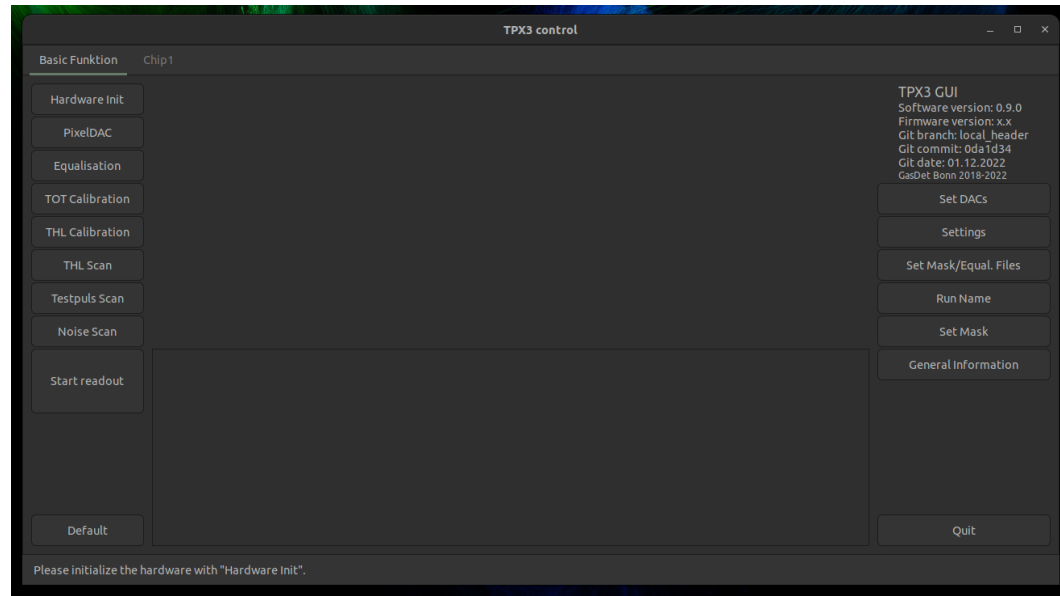
Settings stored in YAML files

Fully open source (GPL-3.0)



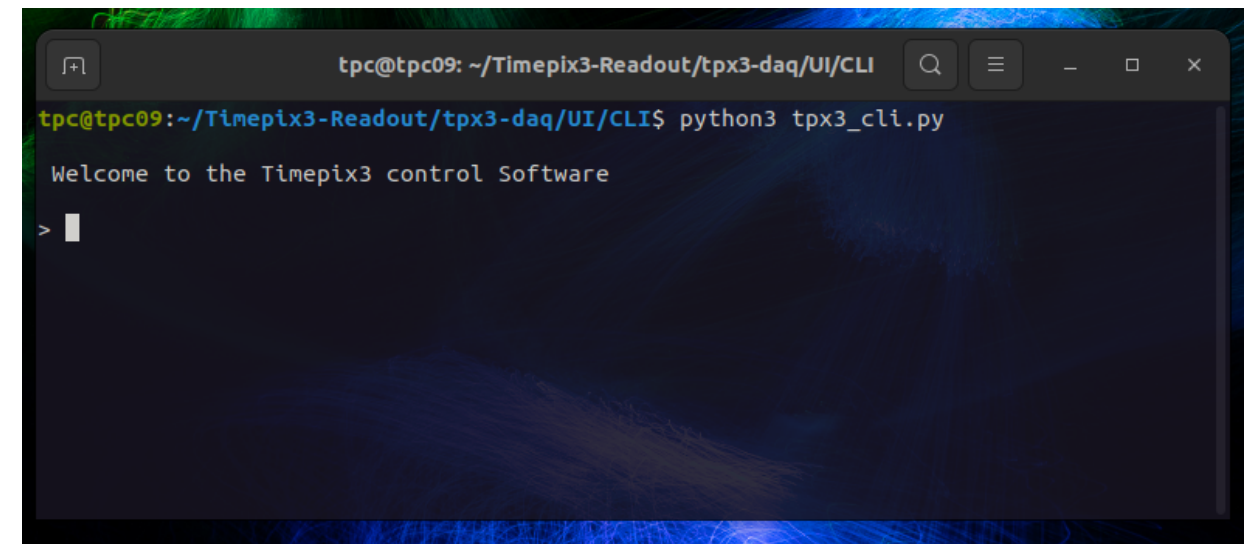
Timepix3 DAQ – User Interface

GUI



“easy to use”

CLI



No need for desktop environment

Scriptable tool chain

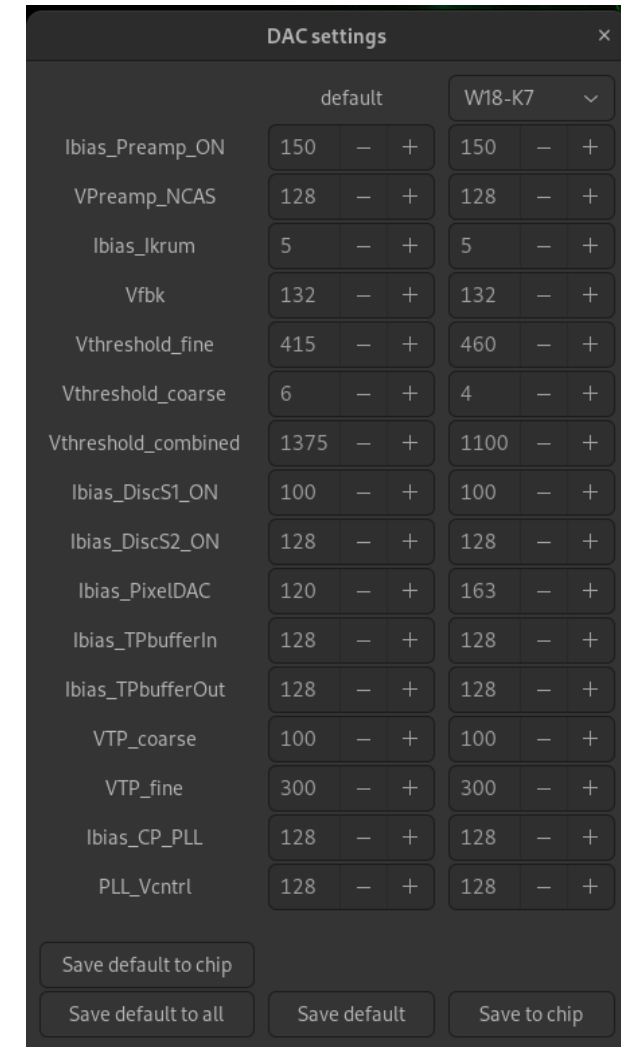
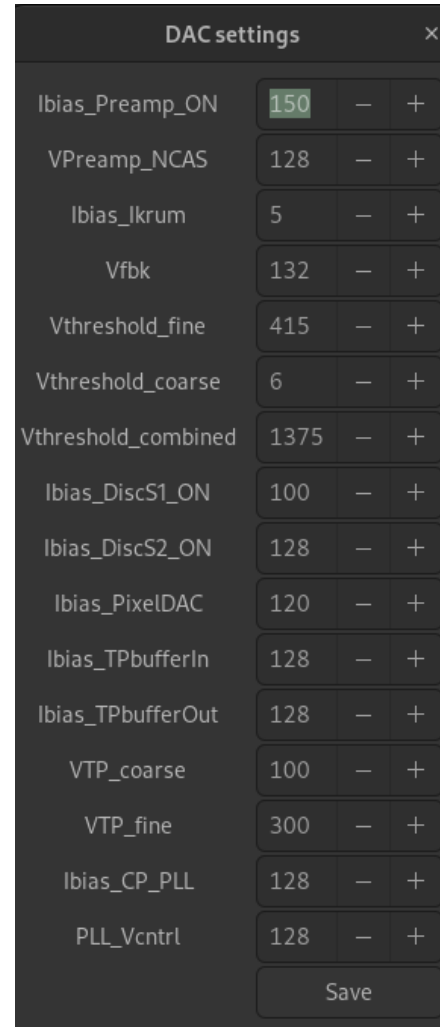
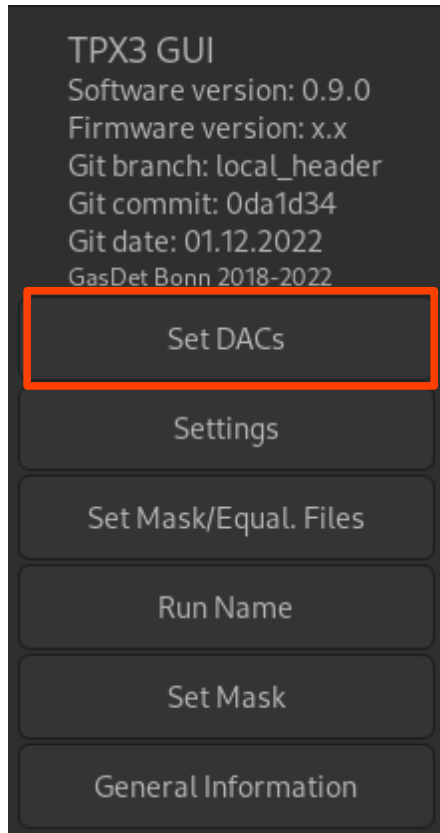
Timepix3 DAQ – GUI

TPX3

Carrier
Board

FPGA
Board

PC



Timepix3 DAQ – GUI

TPX3 GUI
 Software version: 0.9.0
 Firmware version: x.x
 Git branch: local_header
 Git commit: 0da1d34
 Git date: 01.12.2022
 GasDet Bonn 2018-2022

Set DACs

Settings

Set Mask/Equal. Files

Run Name

Set Mask

General Information

Settings

Polarity: NEG ☒ Expert

Fast IO: OFF

Operation mode: ☒ ToT and ToA ☐ Only ToA ☐ Event Count & Integral ToT

TP_Period: 3 - +

Readout Speed: 0.1

TP_Ext_Int: OFF

AckCommand enable: OFF

ClkOut_frequency_src: 160MHz

Sense DAC: BandGap_Temp

Chip links:

0	1	2	3	4	5	6	7
ON	OFF	ON	OFF	ON	ON	ON	ON

Save

Settings

Polarity: POS ☒ Expert

Fast IO: OFF W18-K7

Operation mode: ☐ ToT and ToA ☐ Only ToA ☒ Event Count & Integral ToT

TP_Period: 3 - +

Readout Speed: 0.1

TP_Ext_Int: OFF

AckCommand enable: OFF

ClkOut_frequency_src: 160MHz

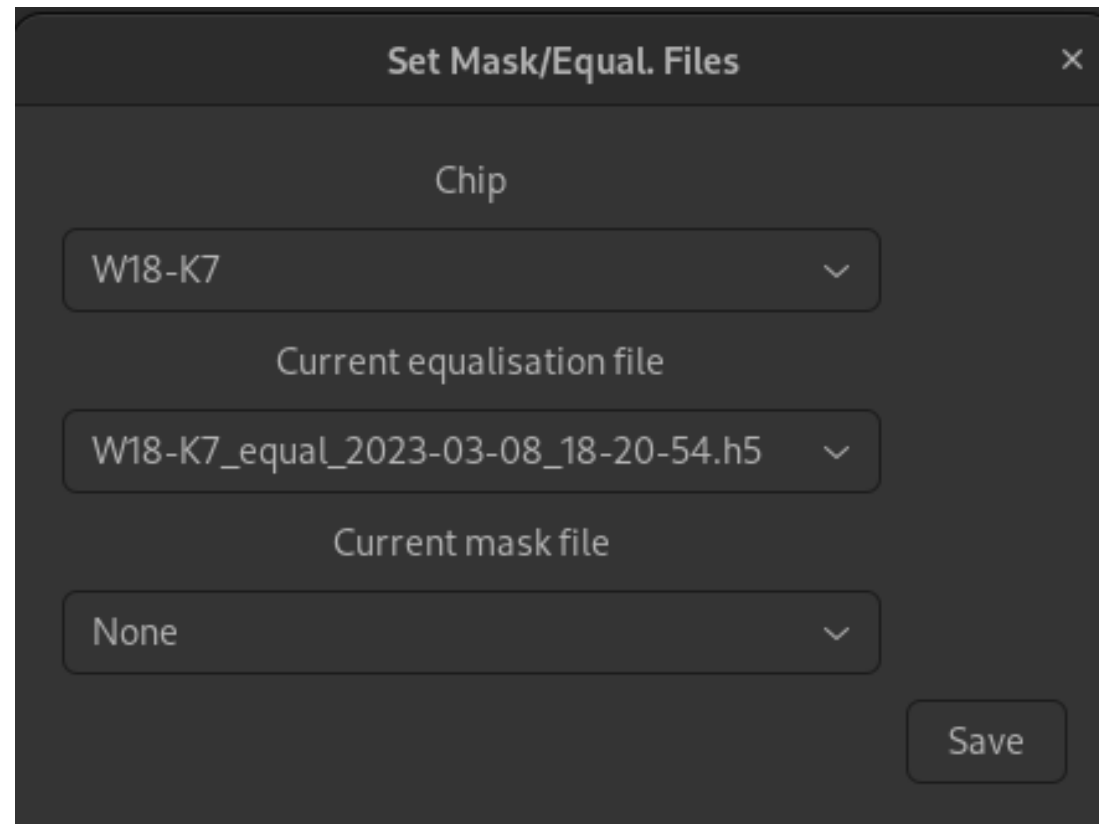
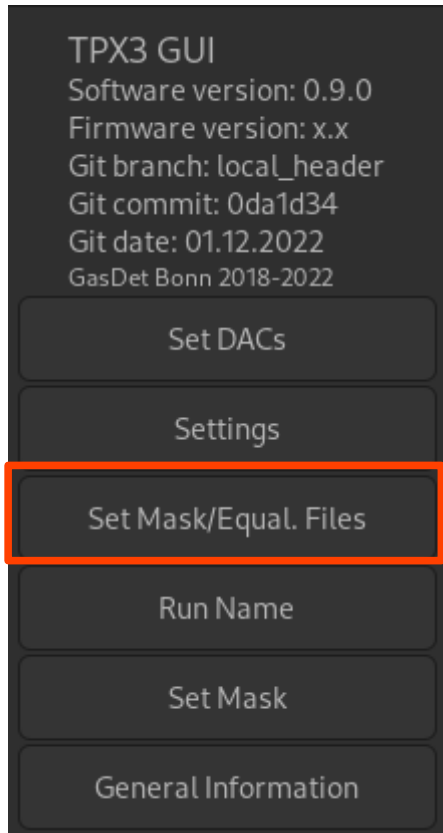
Sense DAC: BandGap_Temp

Chip links:

0	1	2	3	4	5	6	7
ON	OFF	ON	OFF	ON	ON	ON	ON
W18-K7	W18-K7	W18-K7	W18-K7	W18-K7	W18-K7	W18-K7	W18-K7

Save

Timepix3 DAQ – GUI



Timepix3 DAQ – GUI

TPX3 GUI

Software version: 0.9.0
Firmware version: x.x
Git branch: local_header
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Set DACs

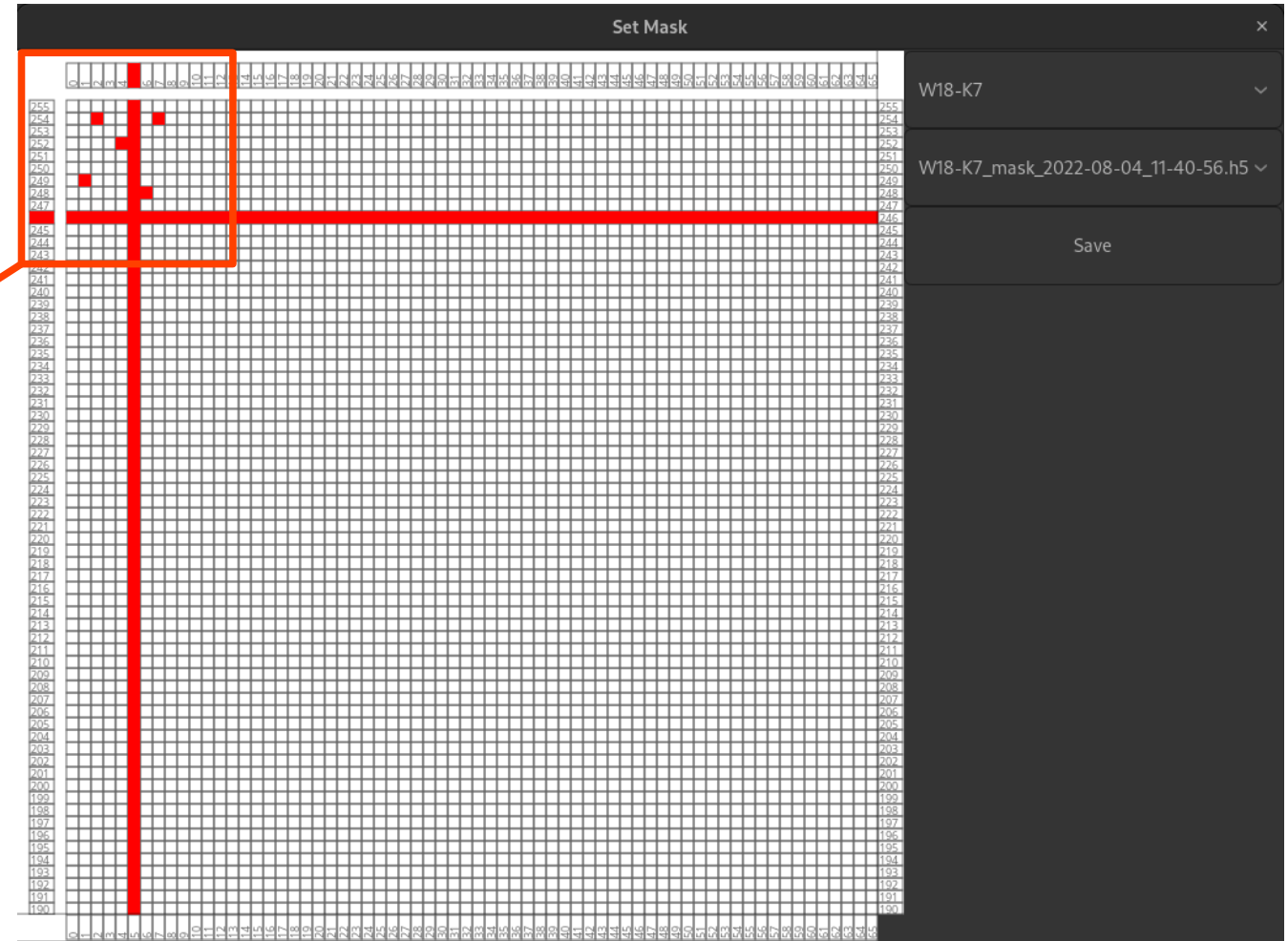
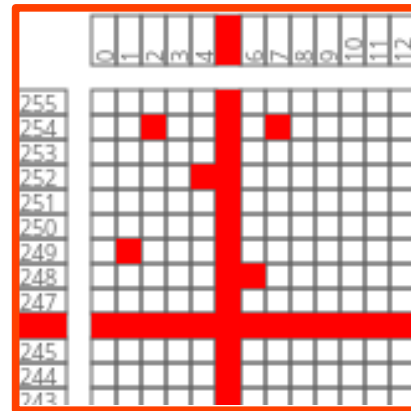
Settings

Set Mask/Equal. Files

Run Name

Set Mask

General Information

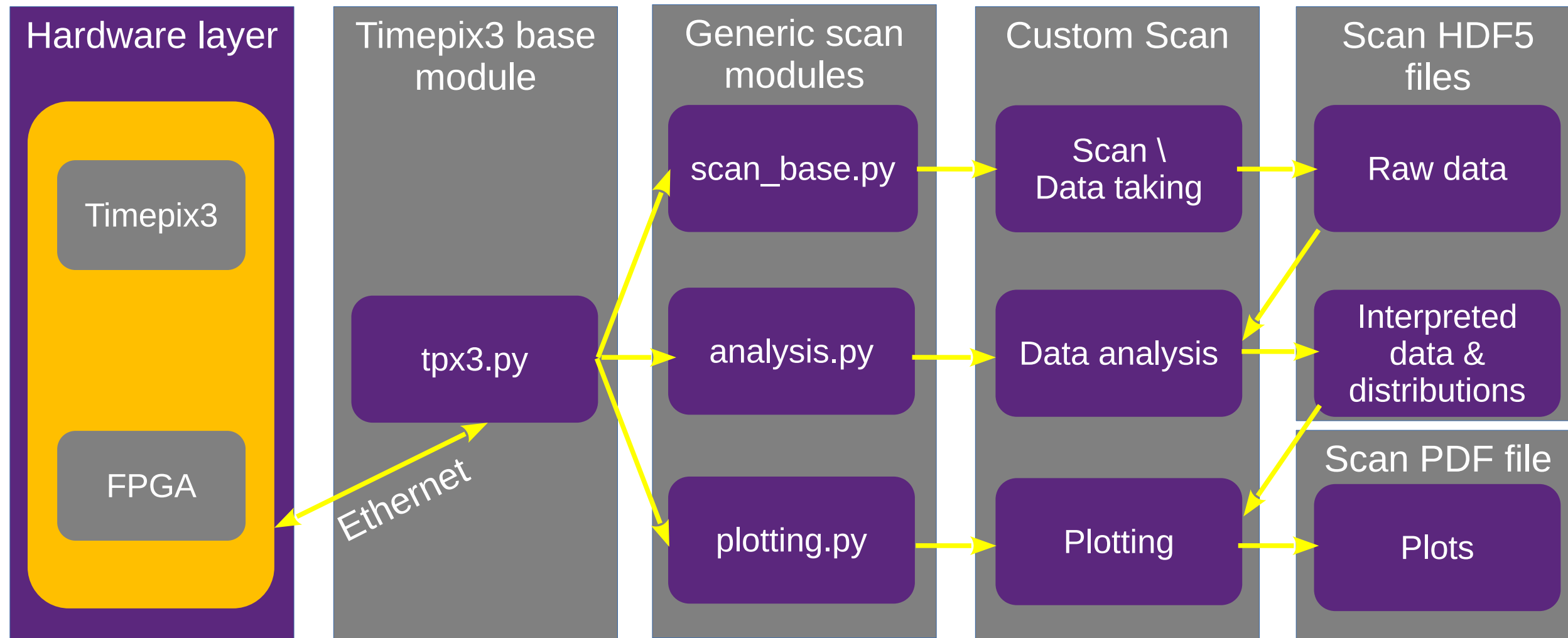


W18-K7

W18-K7_mask_2022-08-04_11-40-56.h5

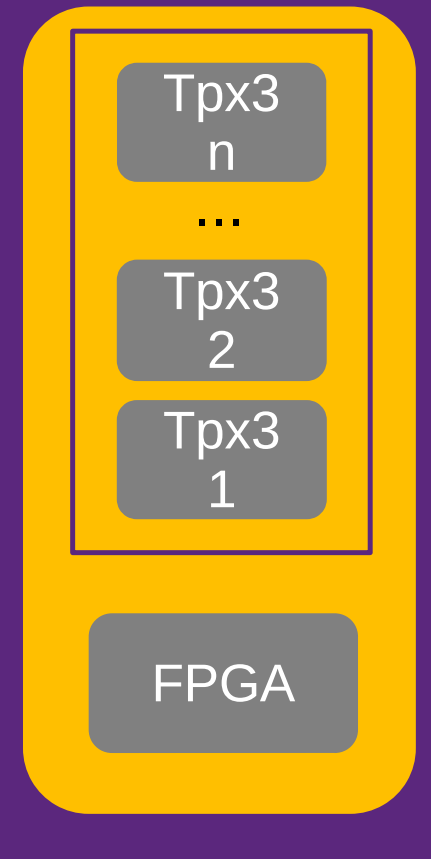
Save

Timepix3 DAQ – Software Modules

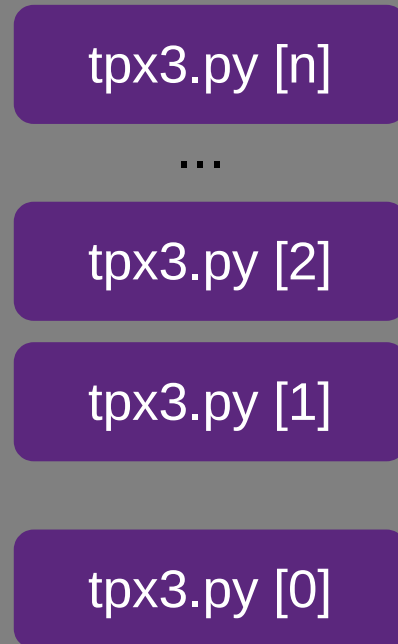


Timepix3 DAQ – Multichip Support

Hardware layer



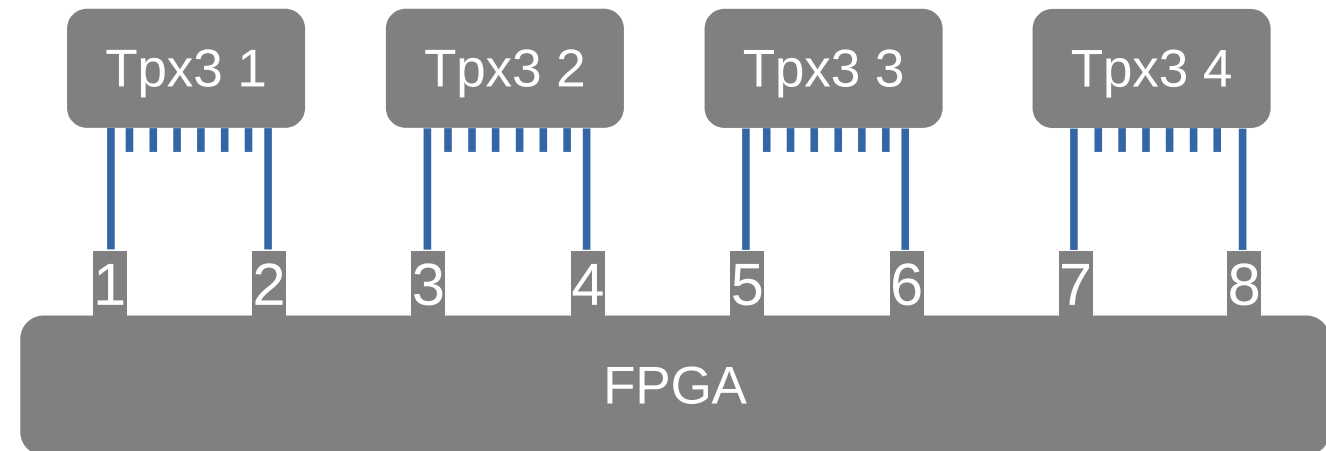
Timepix3 objects



tpx3 [0] object initialises board communication

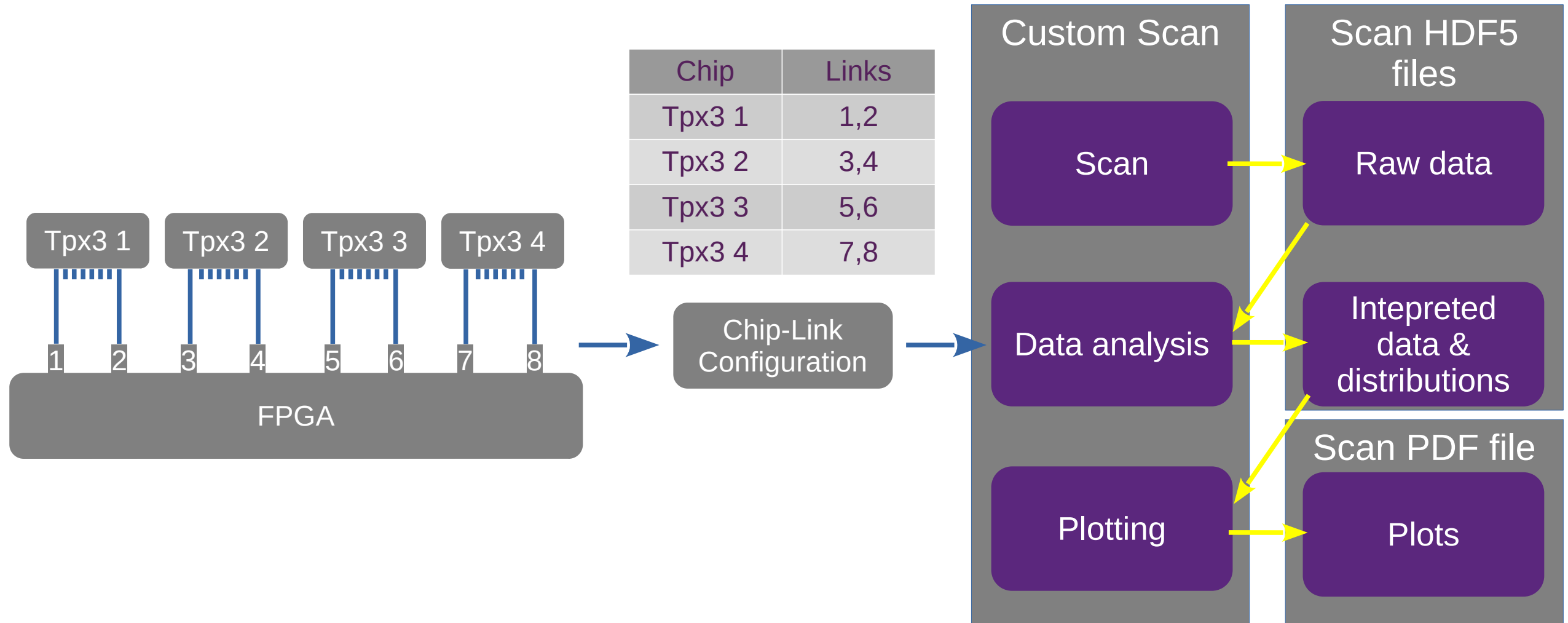
tpx3-object created for each connected chip

Initialisation creates chip link configuration

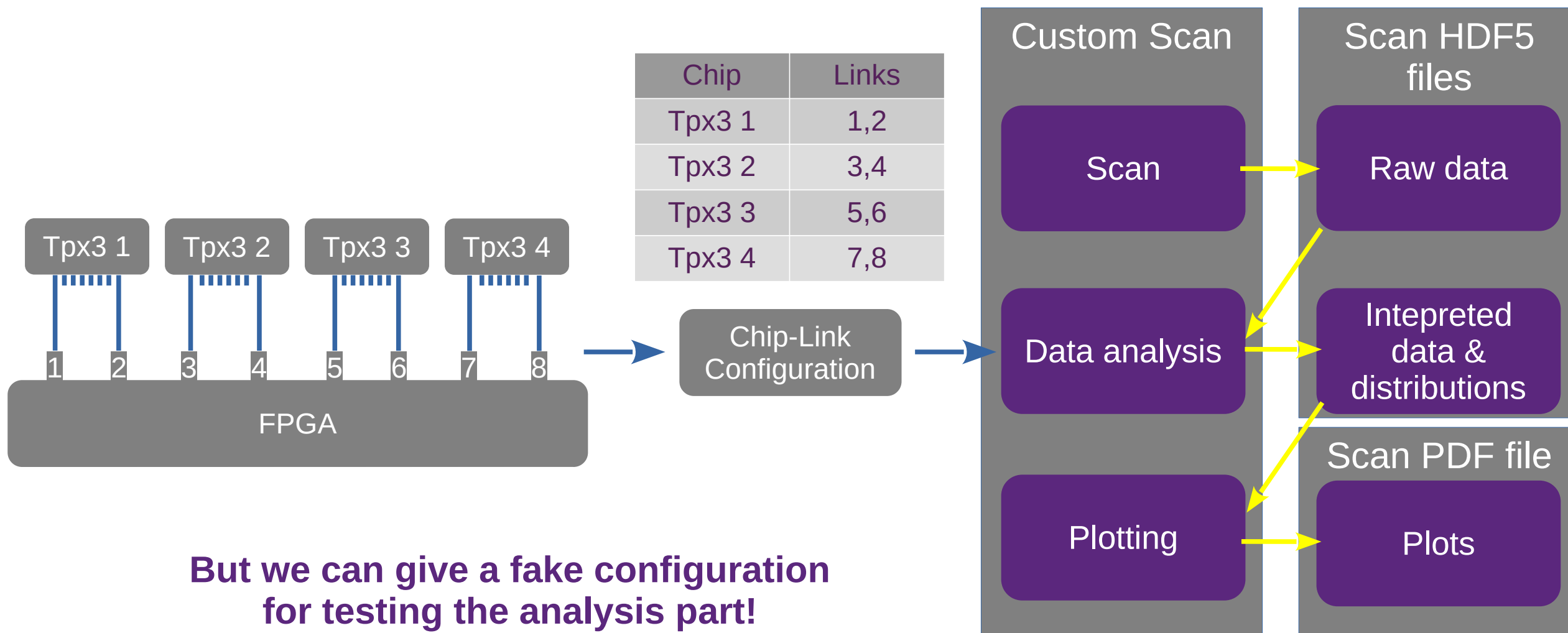


Will be tested with a multichip setup soon!

Timepix3 DAQ – Multichip Support



Timepix3 DAQ – Multichip Support



Timepix3 DAQ – What can we do with it?

Obvious: taking measurement data

But also testing and preparing chips

- Scanning of the pixel matrix
- Equalising threshold level of all pixels
- Calibration

Timepix3 DAQ - Scans

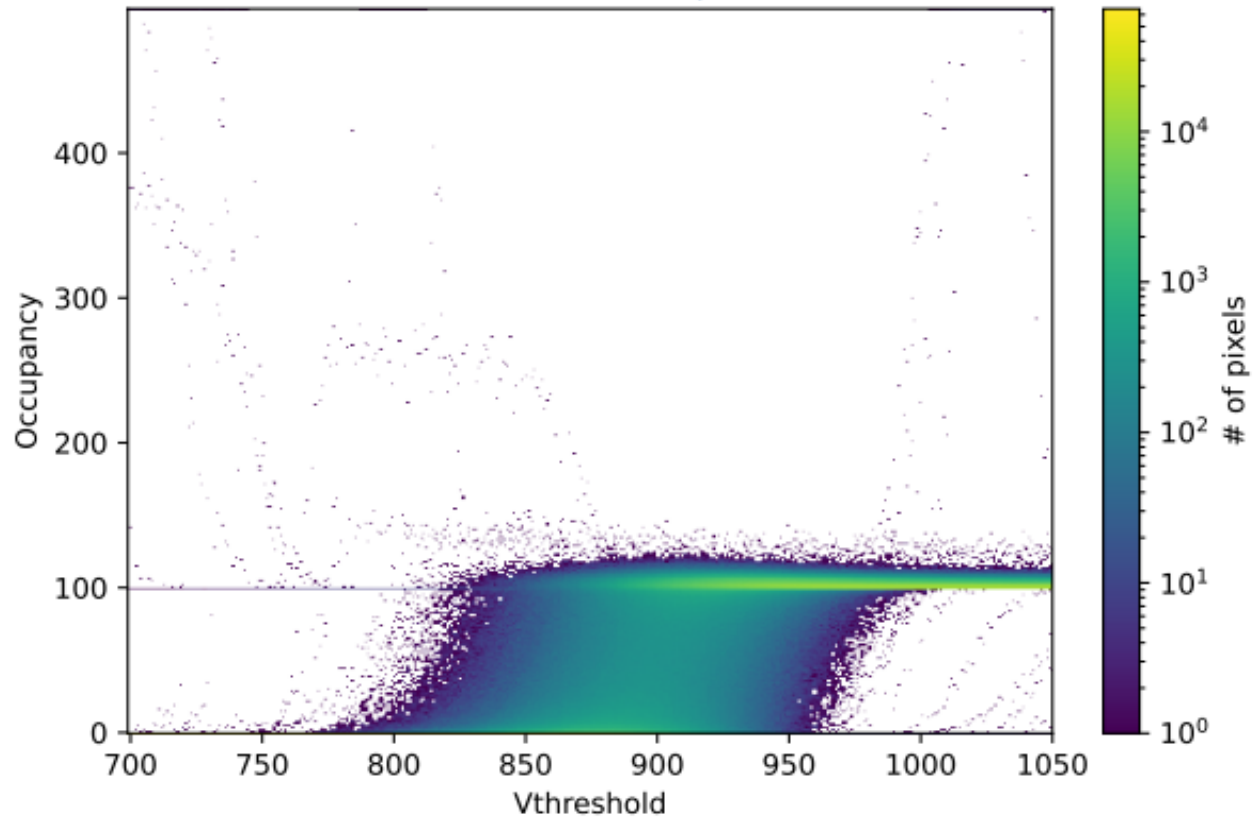
Scan	Scanned DAC	Constant DAC	Operation mode
Noise	Threshold	-	Hit count
Threshold	Threshold	Testpulse height	Hit count
Testpulse	Testpulse height	Threshold	Hit count

Timepix3 DAQ - Threshold Scan

Timepix3 draft

Chip: W18-K7

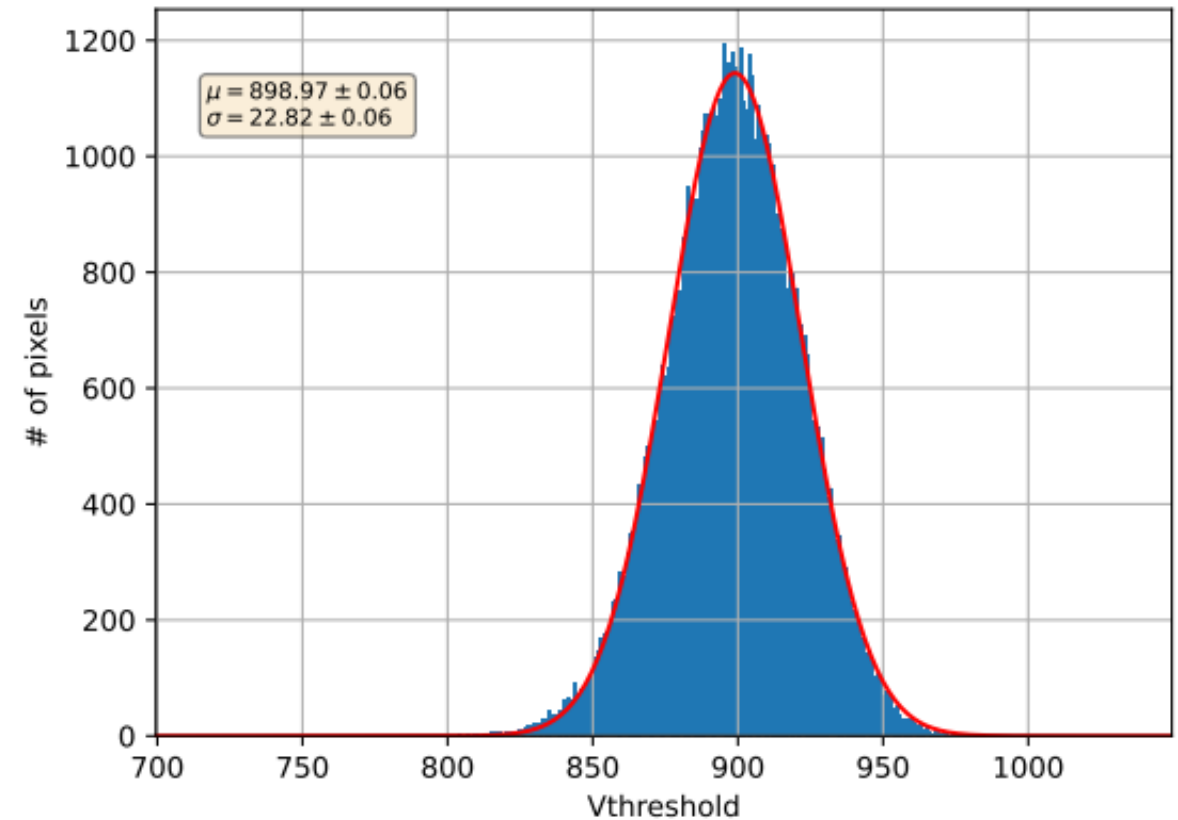
S-curves for 65536 pixel(s)



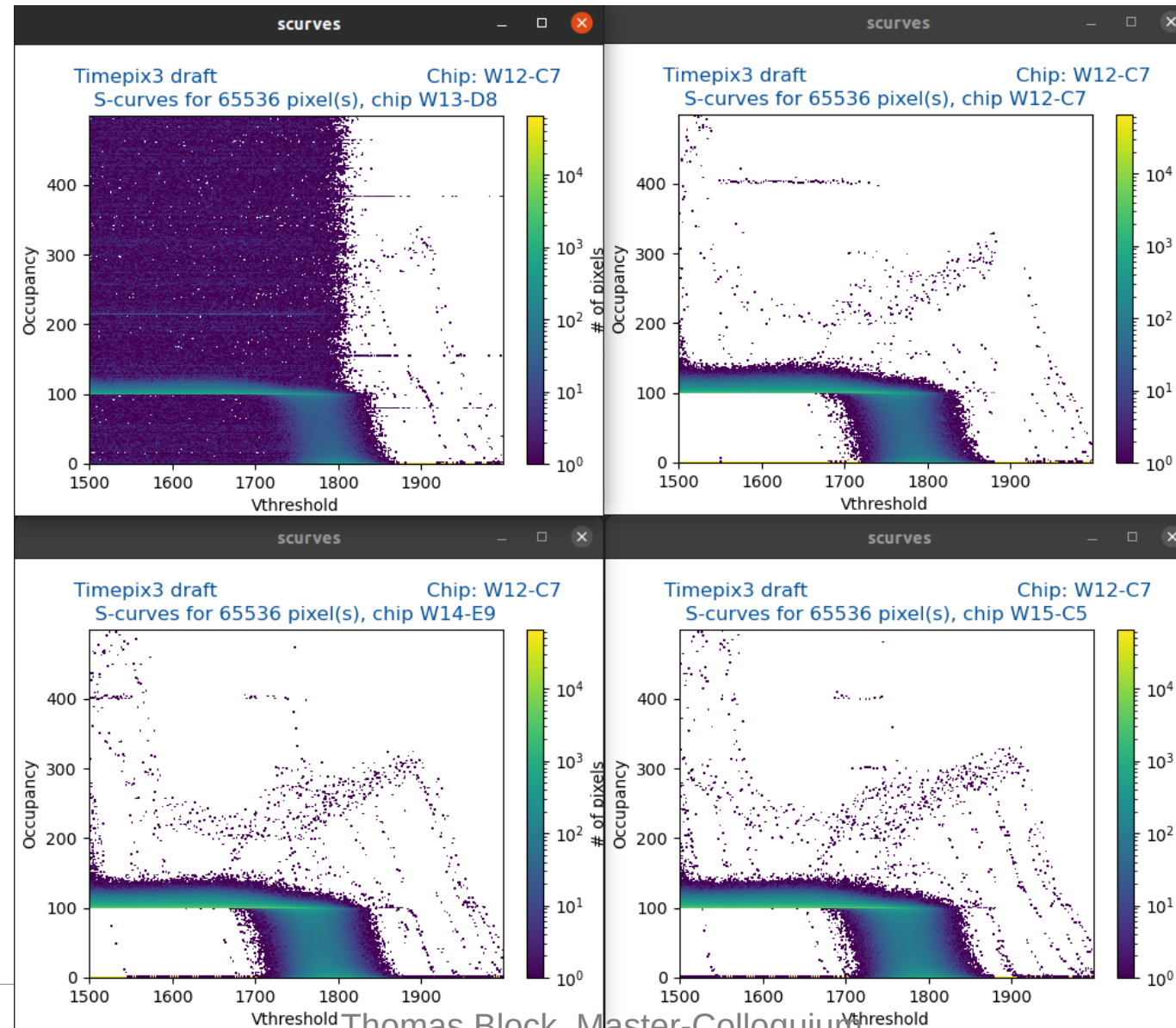
Timepix3 draft

Chip: W18-K7

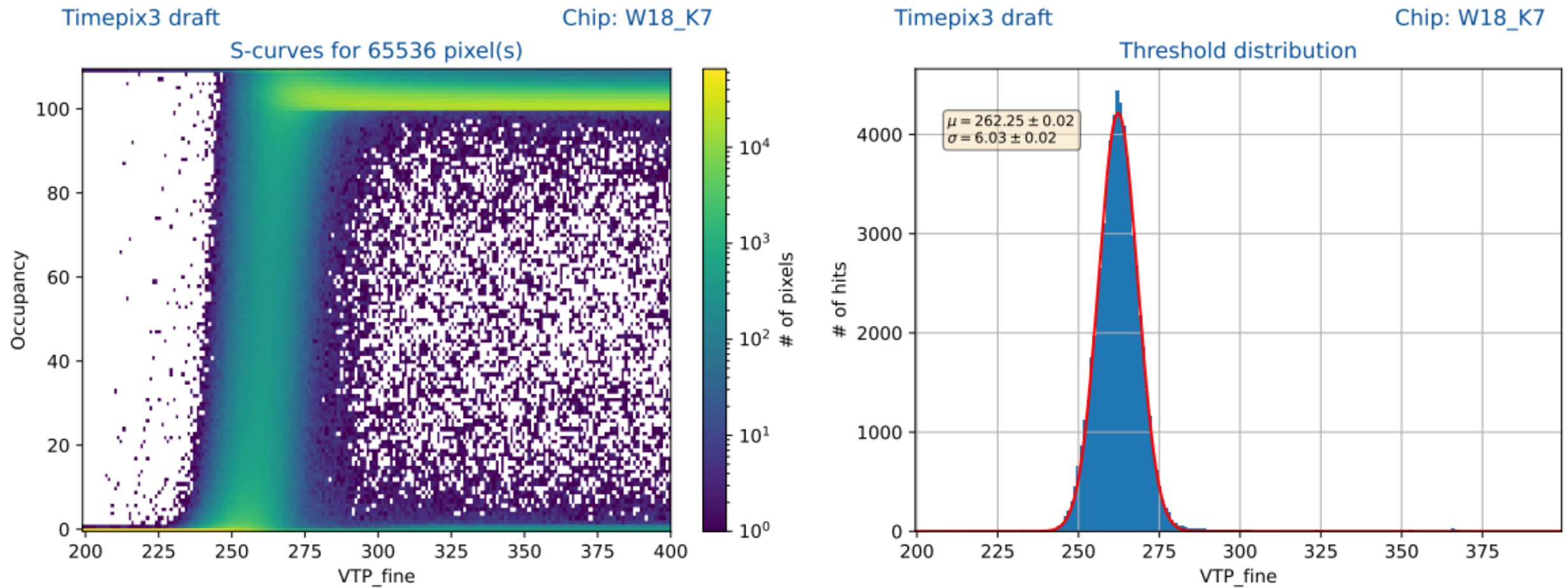
Threshold distribution



Timepix3 DAQ - Threshold Scan - Multichip Support



Timepix3 DAQ – Testpulse Scan

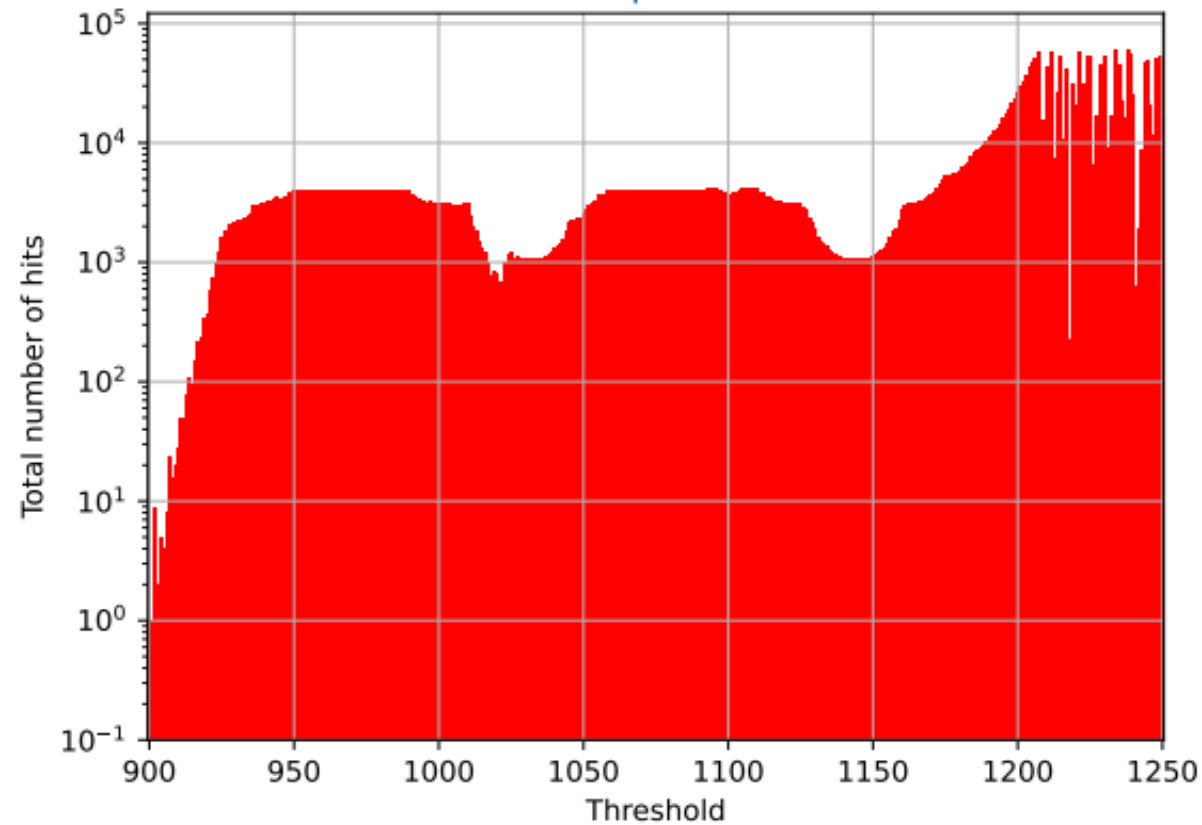


Timepix3 DAQ – Noise Scan

Timepix3 draft

Chip: W18-K7

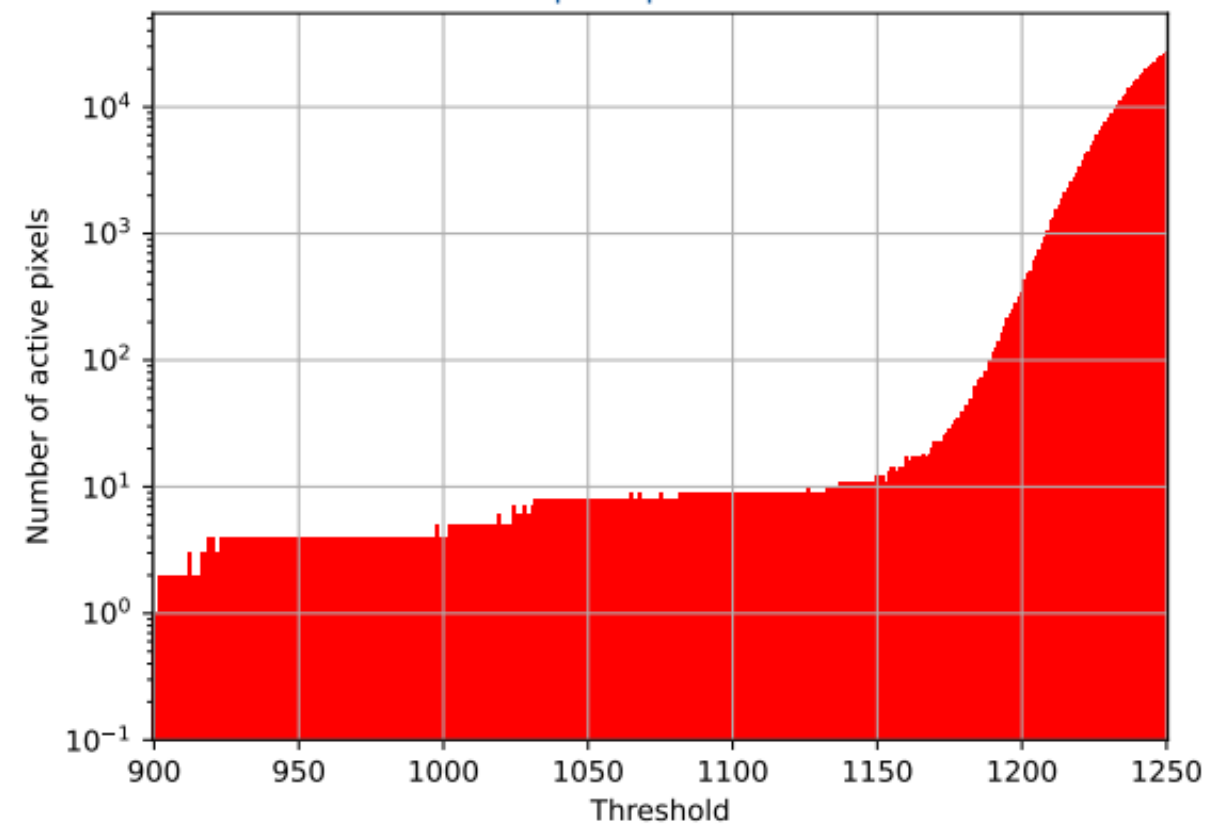
Noise hits per threshold



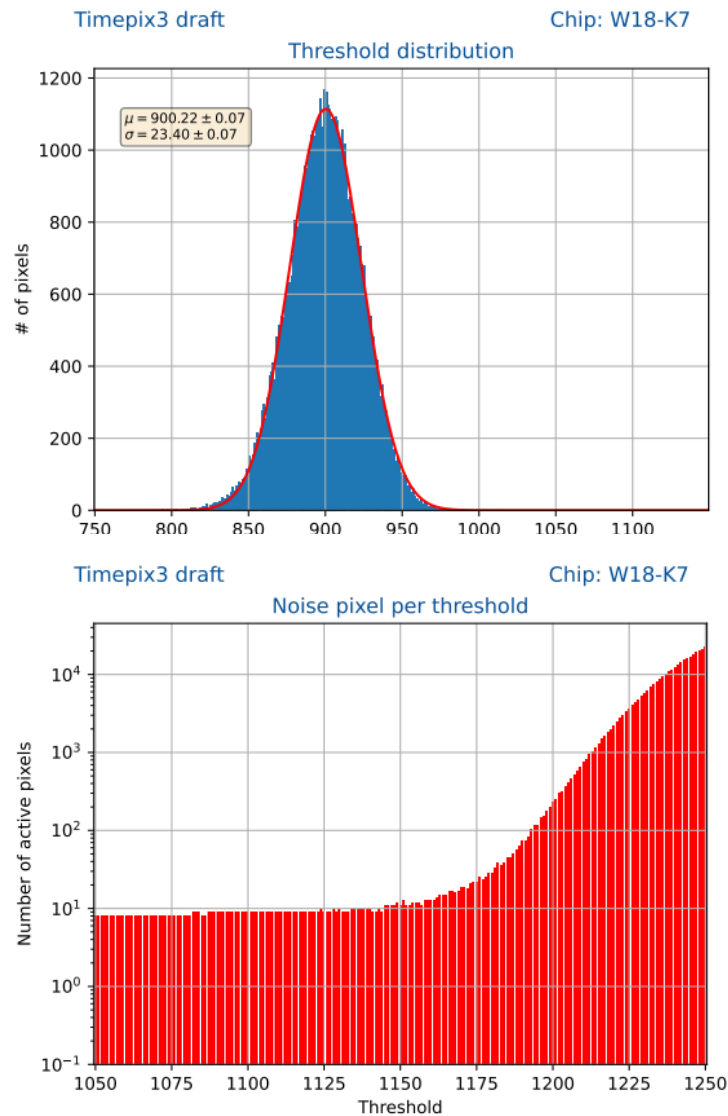
Timepix3 draft

Chip: W18-K7

Noise pixel per threshold

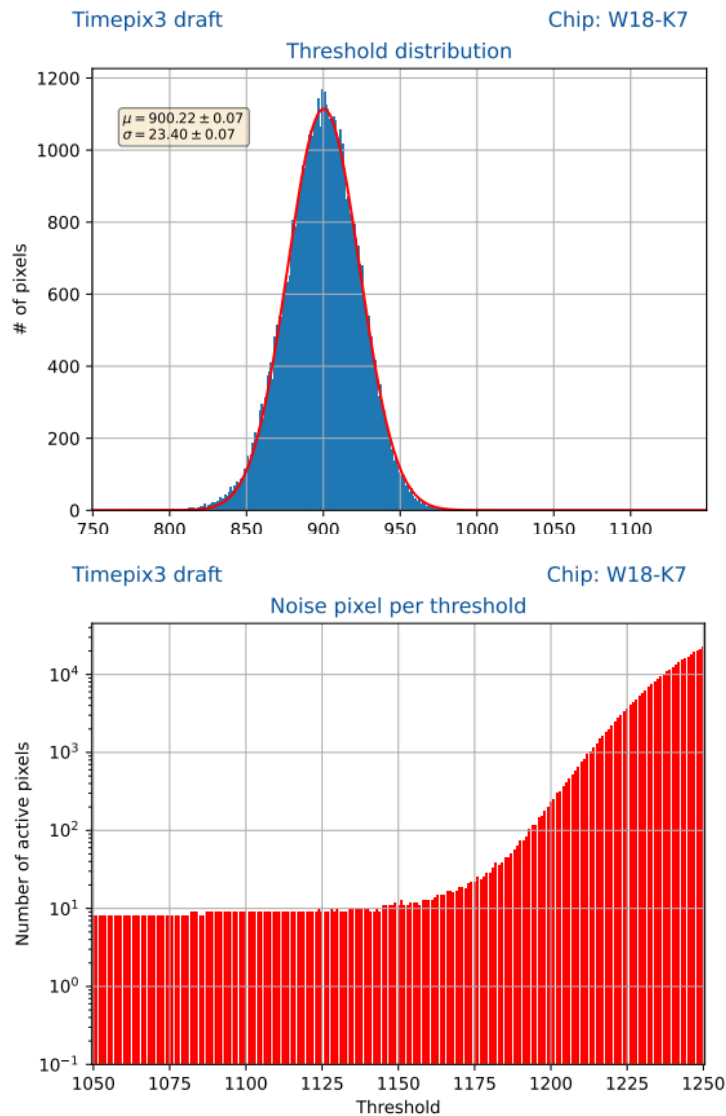


Timepix3 DAQ – Equalisation



Problem:
Pixel show different thresholds for same signal strengths

Timepix3 DAQ – Equalisation



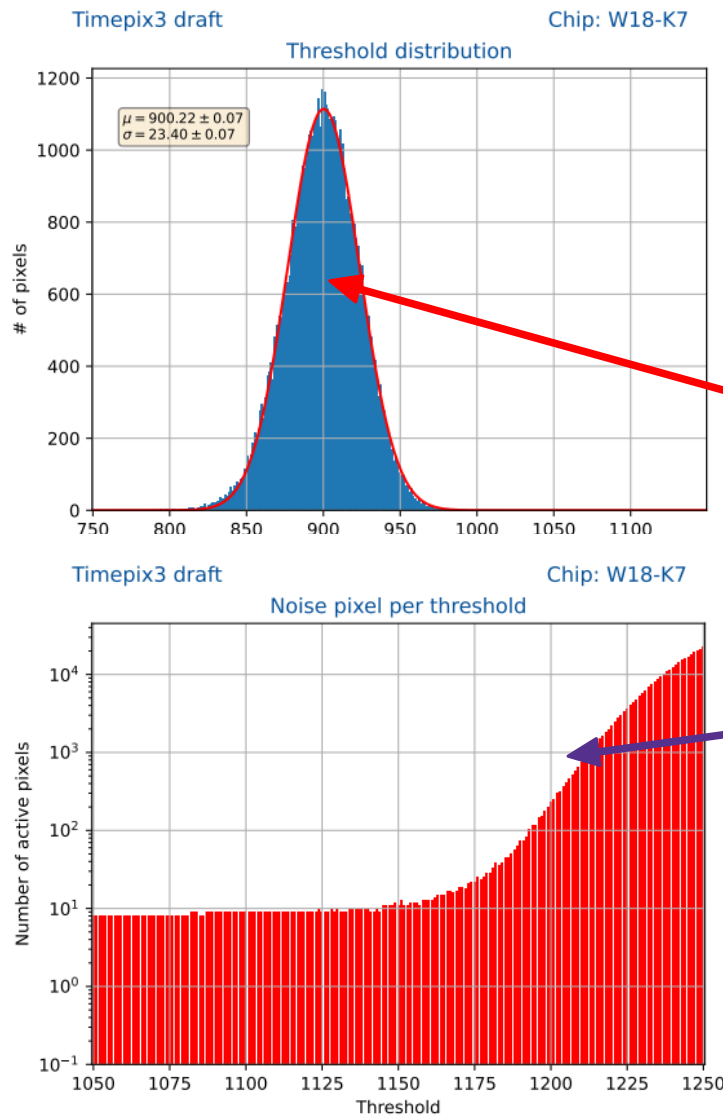
Problem:

Pixel show different thresholds for same signal strengths

Goal of the equalisation:

Equalizing the sensitivity/acceptance level of all pixels

Timepix3 DAQ – Equalisation



Problem:

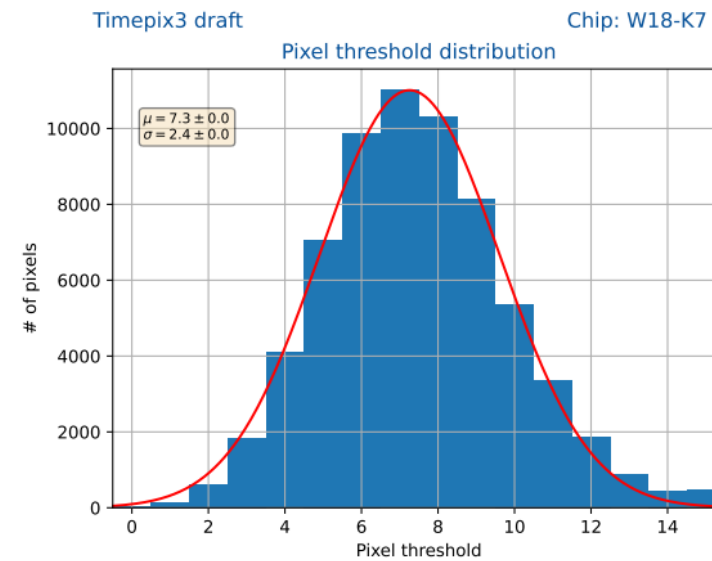
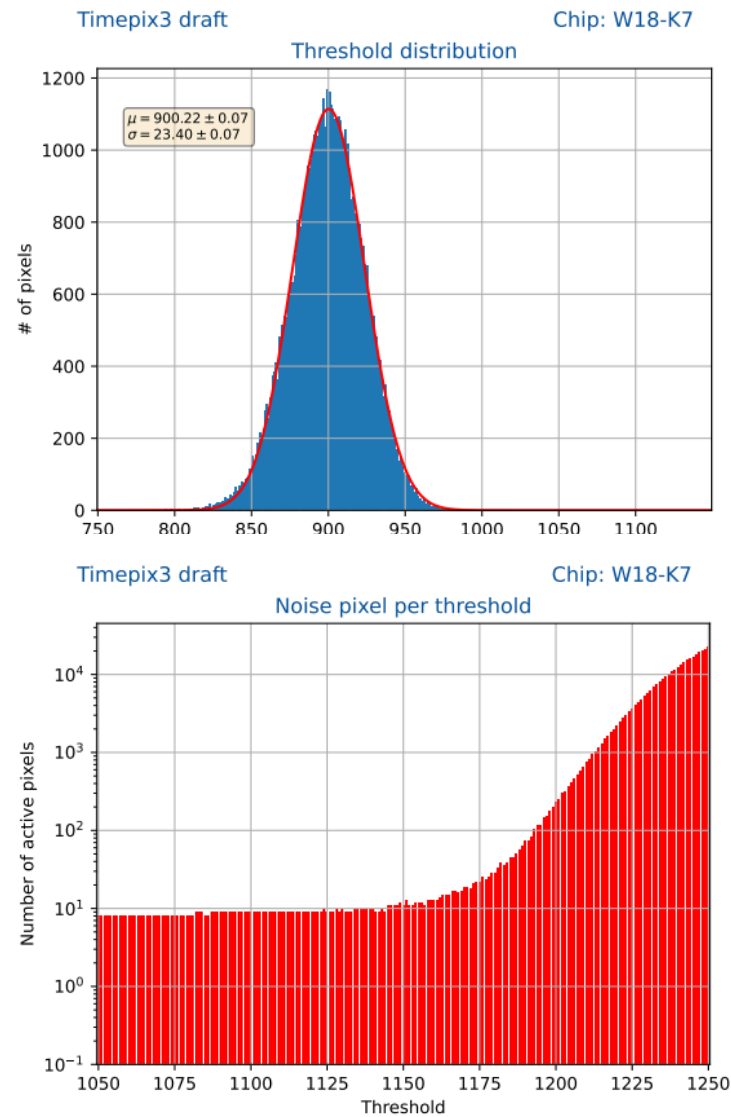
Pixel show different thresholds for same signal strengths

Goal of the equalisation:

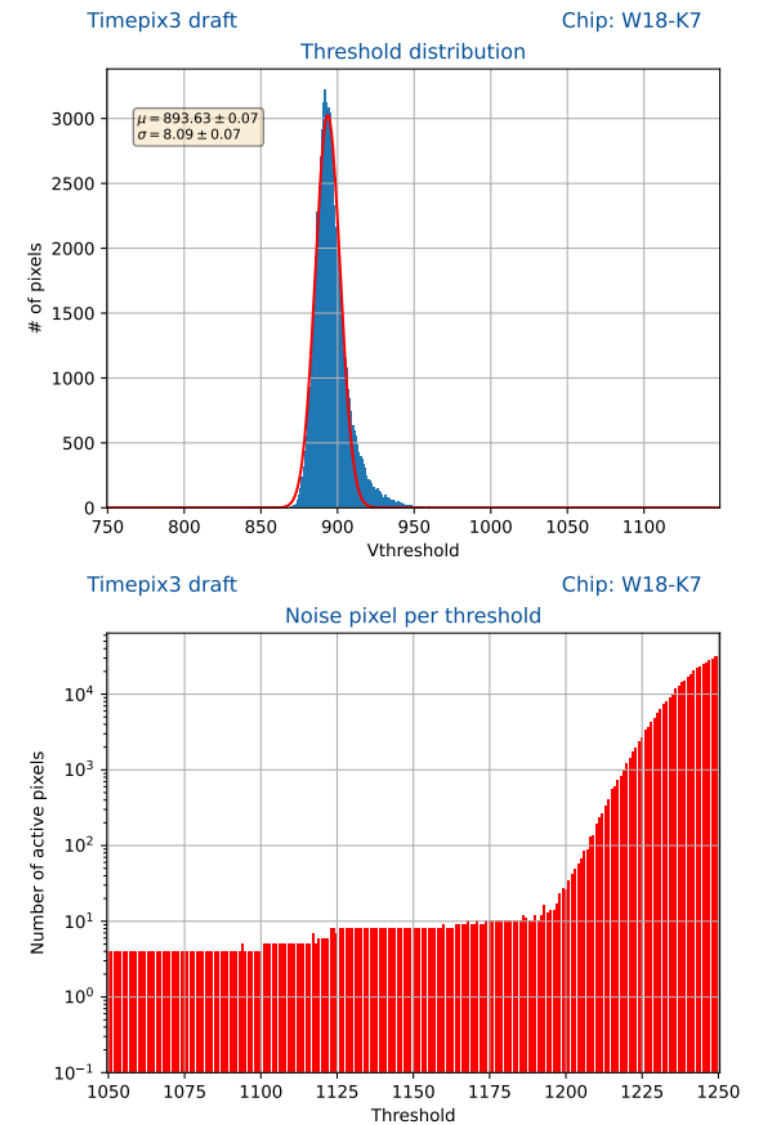
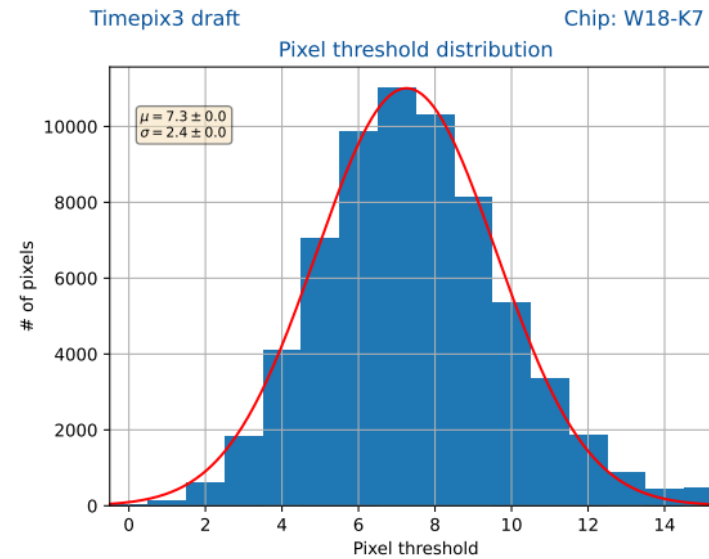
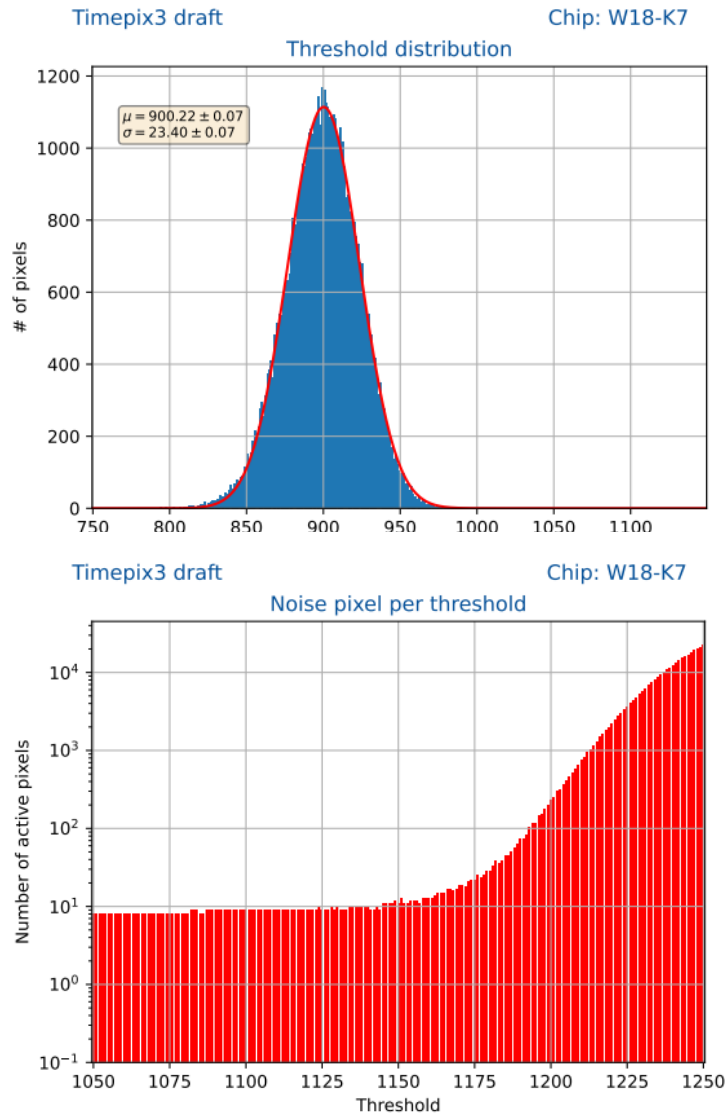
Equalizing the sensitivity/acceptance level of all pixels

Ideal result: Delta-function & Step-function

Timepix3 DAQ – Equalisation



Timepix3 DAQ – Equalisation



Timepix3 DAQ – Calibration

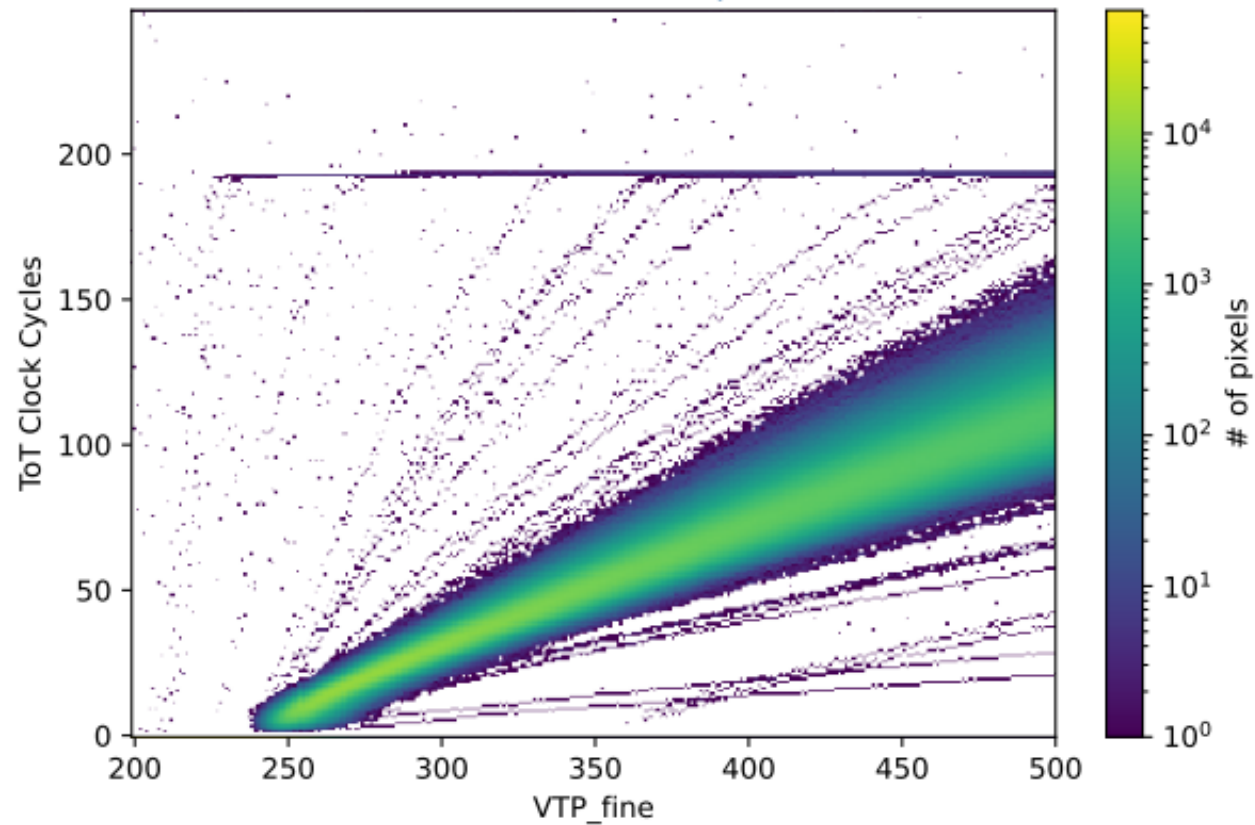
Calibration	Scanned DAC	Constant DAC	Operation mode
ToT	Testpulse height	Threshold	ToT+ToA
Threshold	Threshold (for n different pulse heights)	Testpulse height	Hit count

Timepix3 DAQ – ToT Calibration

Timepix3 draft

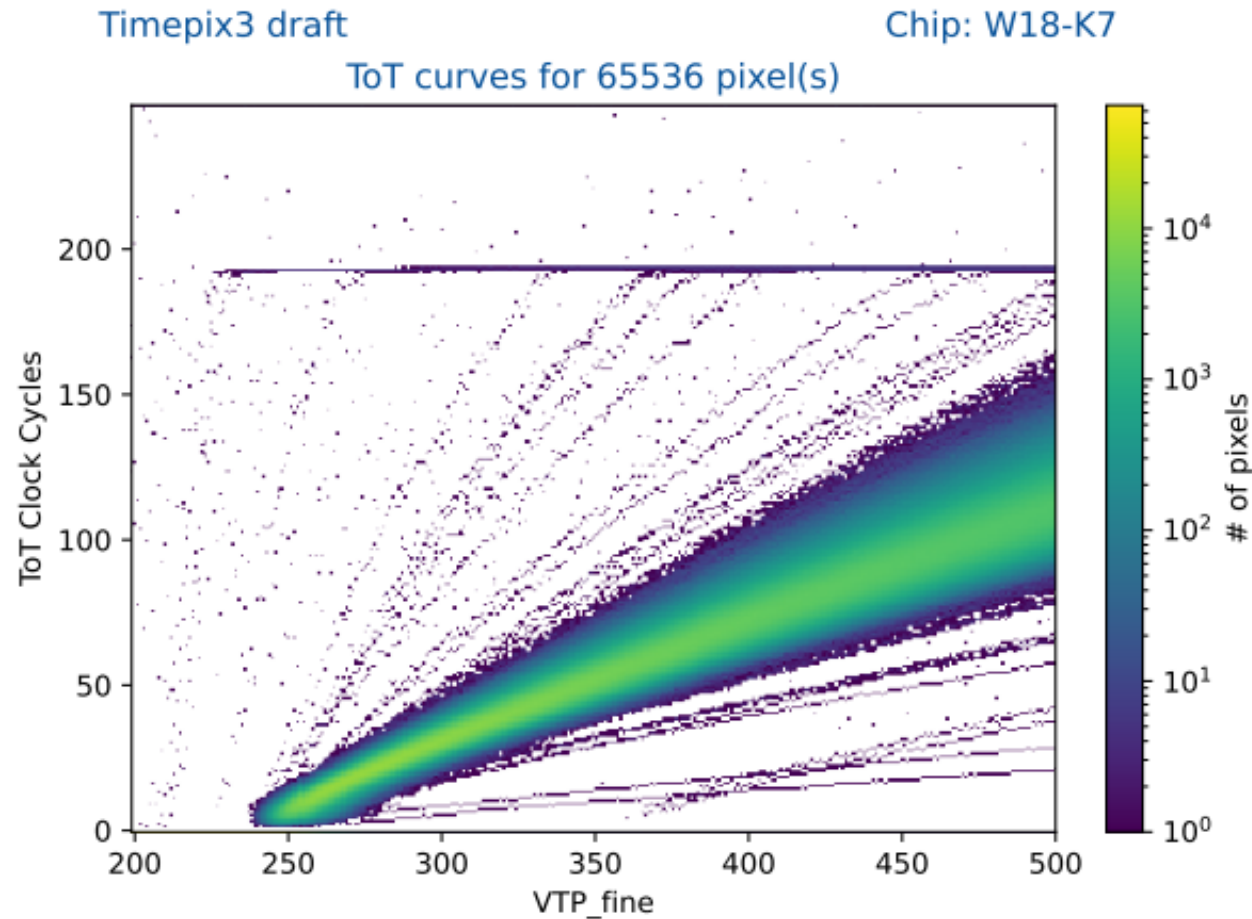
Chip: W18-K7

ToT curves for 65536 pixel(s)



For every testpulse height take the average and standard deviation of ToT clock cycles over all pixels

Timepix3 DAQ – ToT Calibration



For every VTP_fine take the average and standard deviation of ToT clock cycles over all pixels

Fit following function with fit parameters a, b, c, t

$$ToT \text{ clock cycles} = a * voltage + b - \frac{c}{voltage - t}$$

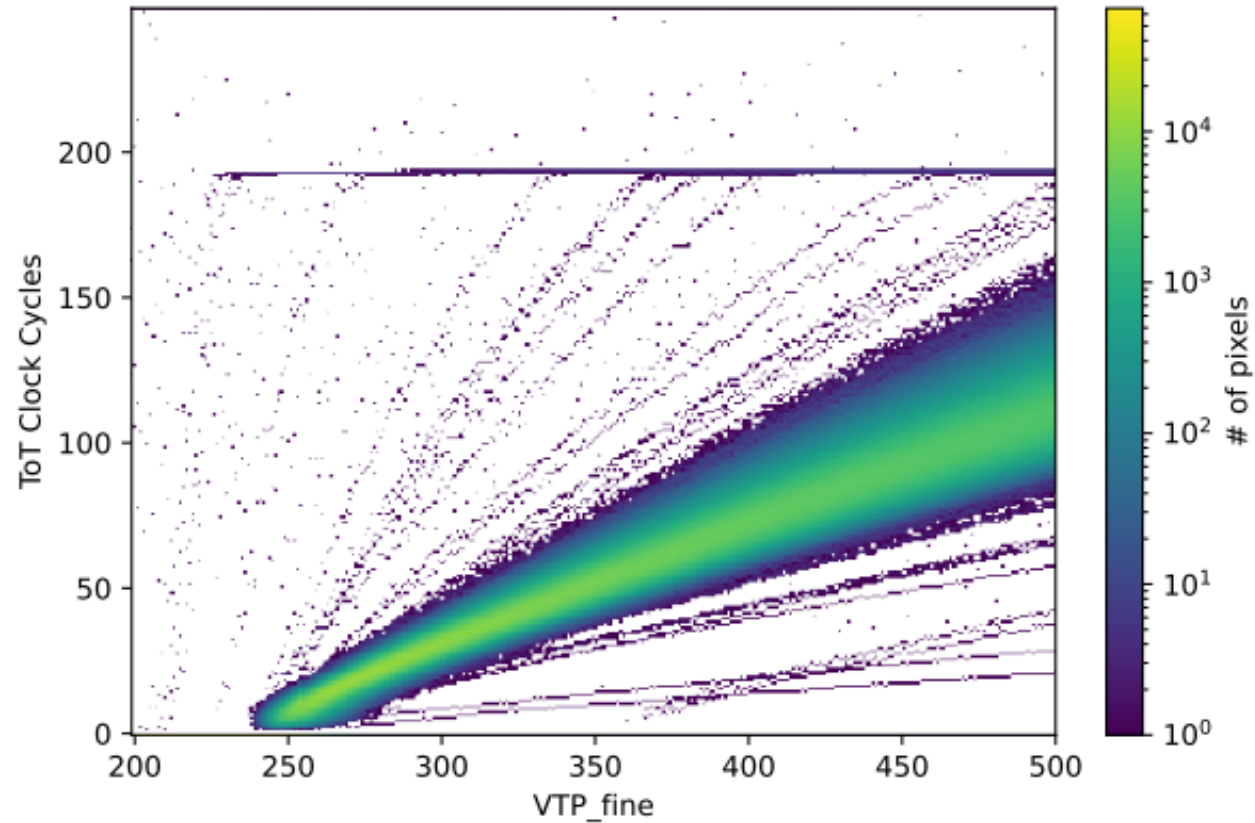
$$voltage = VTP_{fine} * 2.5 \text{ mV} - 500 \text{ mV}$$

Timepix3 DAQ – ToT Calibration

Timepix3 draft

Chip: W18-K7

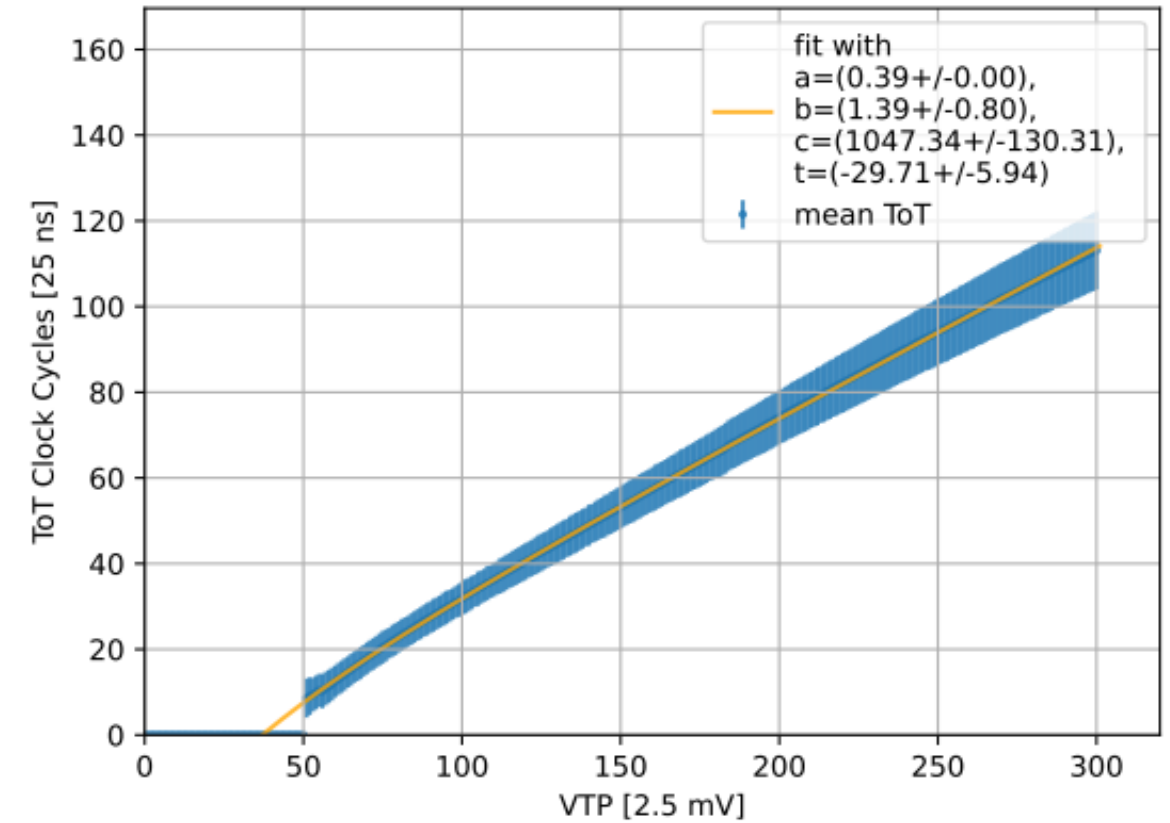
ToT curves for 65536 pixel(s)



Timepix3 draft

Chip: W18-K7

ToT fit



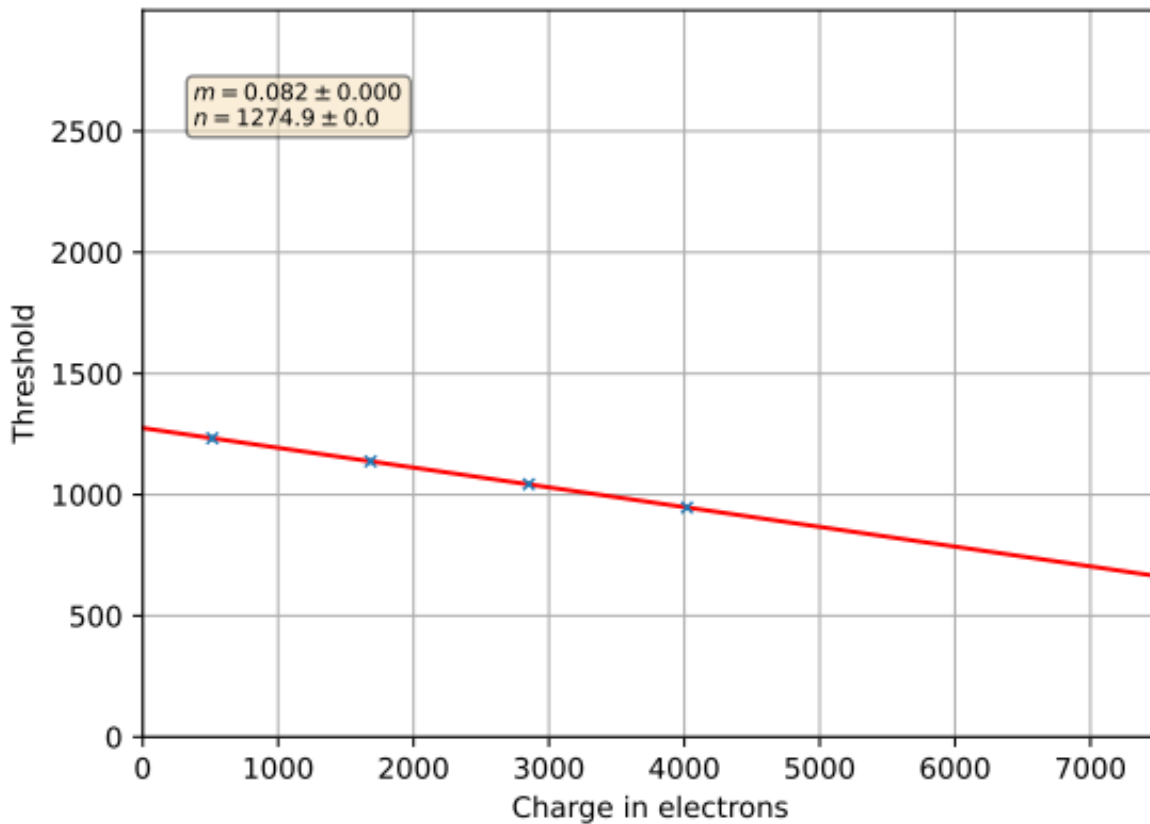
Timepix3 DAQ – Threshold Calibration

Timepix3 draft

Chip: W18-K7

Threshold calibration

For every test pulse height measure the threshold distribution and the average threshold

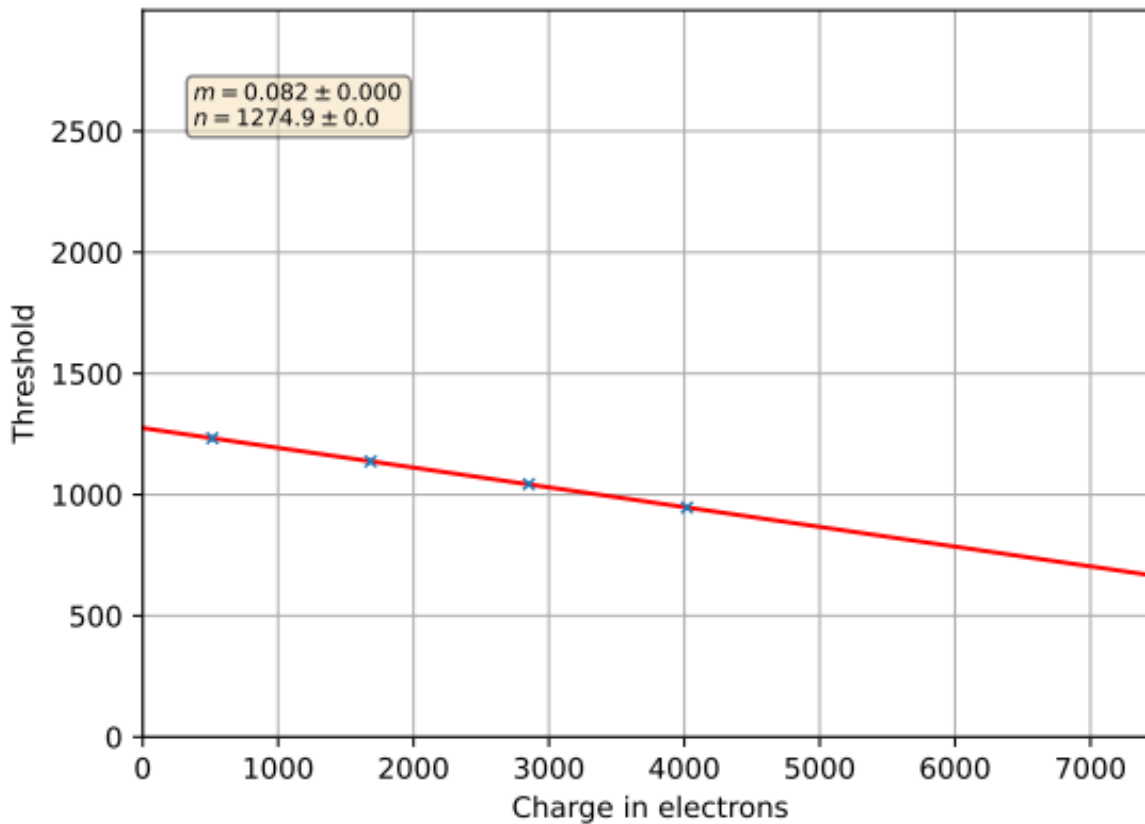


Timepix3 DAQ – Threshold Calibration

Timepix3 draft

Chip: W18-K7

Threshold calibration



For every test pulse height measure the threshold distribution and the average threshold

Assuming a 3fF input capacitance, calculate charge in electrons via

$$Q = C * U$$

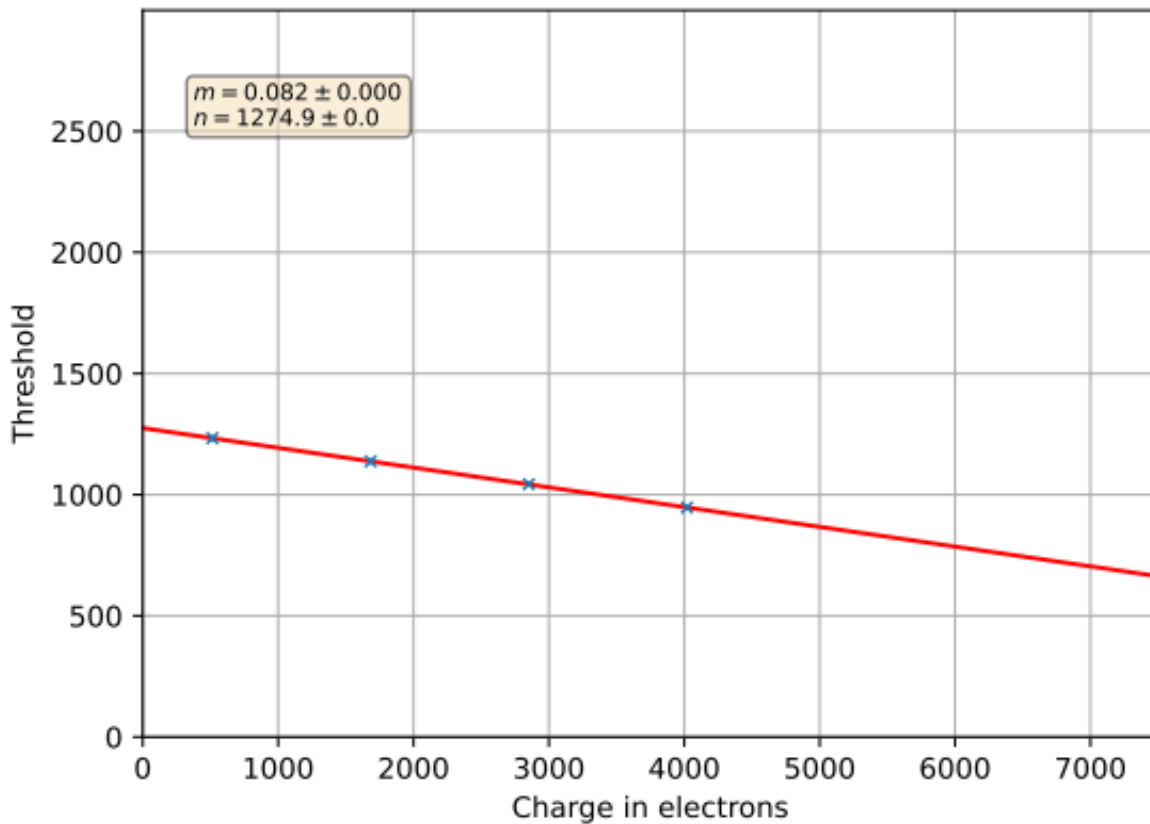
$$U = VTP_{fine} * 2.5 \text{ mV} - 500 \text{ mV}$$

Timepix3 DAQ – Threshold Calibration

Timepix3 draft

Chip: W18-K7

Threshold calibration



For every test pulse height measure the threshold distribution and the average threshold

Assuming a 3fF input capacitance, calculate charge in electrons via

$$Q = C * U$$

$$U = VTP_{fine} * 2.5 \text{ mV} - 500 \text{ mV}$$

Fit linear function

Conclusion & Outlook

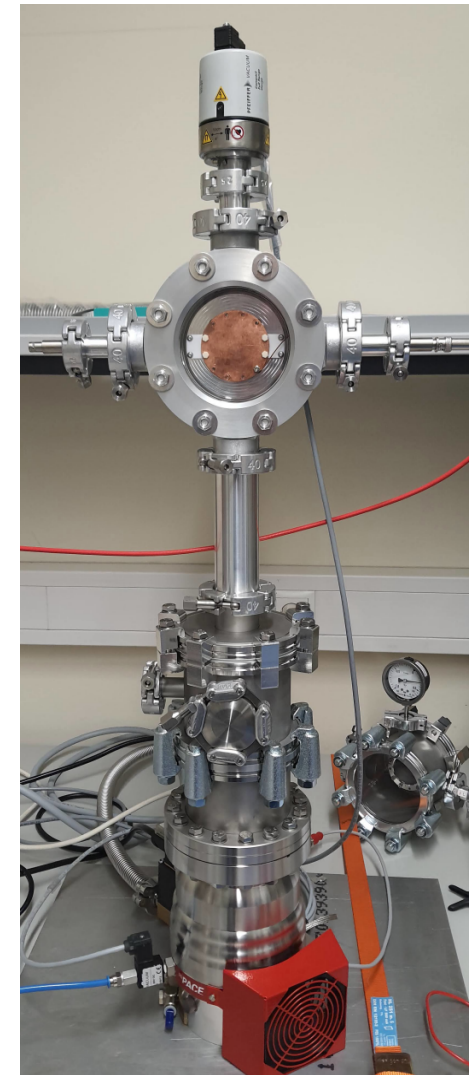
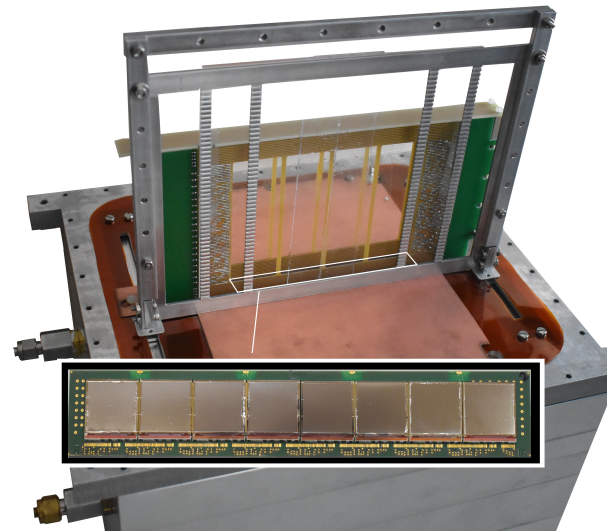
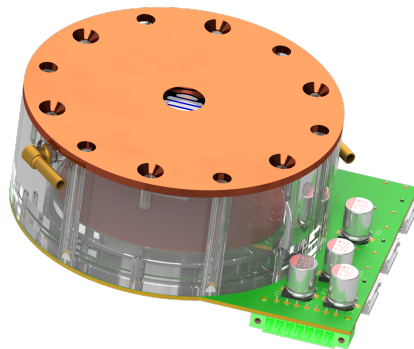
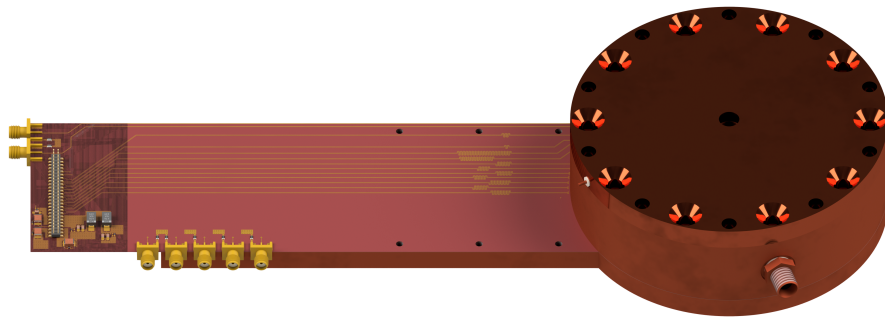
Timepix3 is a versatile pixel sensor ASIC

Timepix3 is/will be used in different detector projects in our group

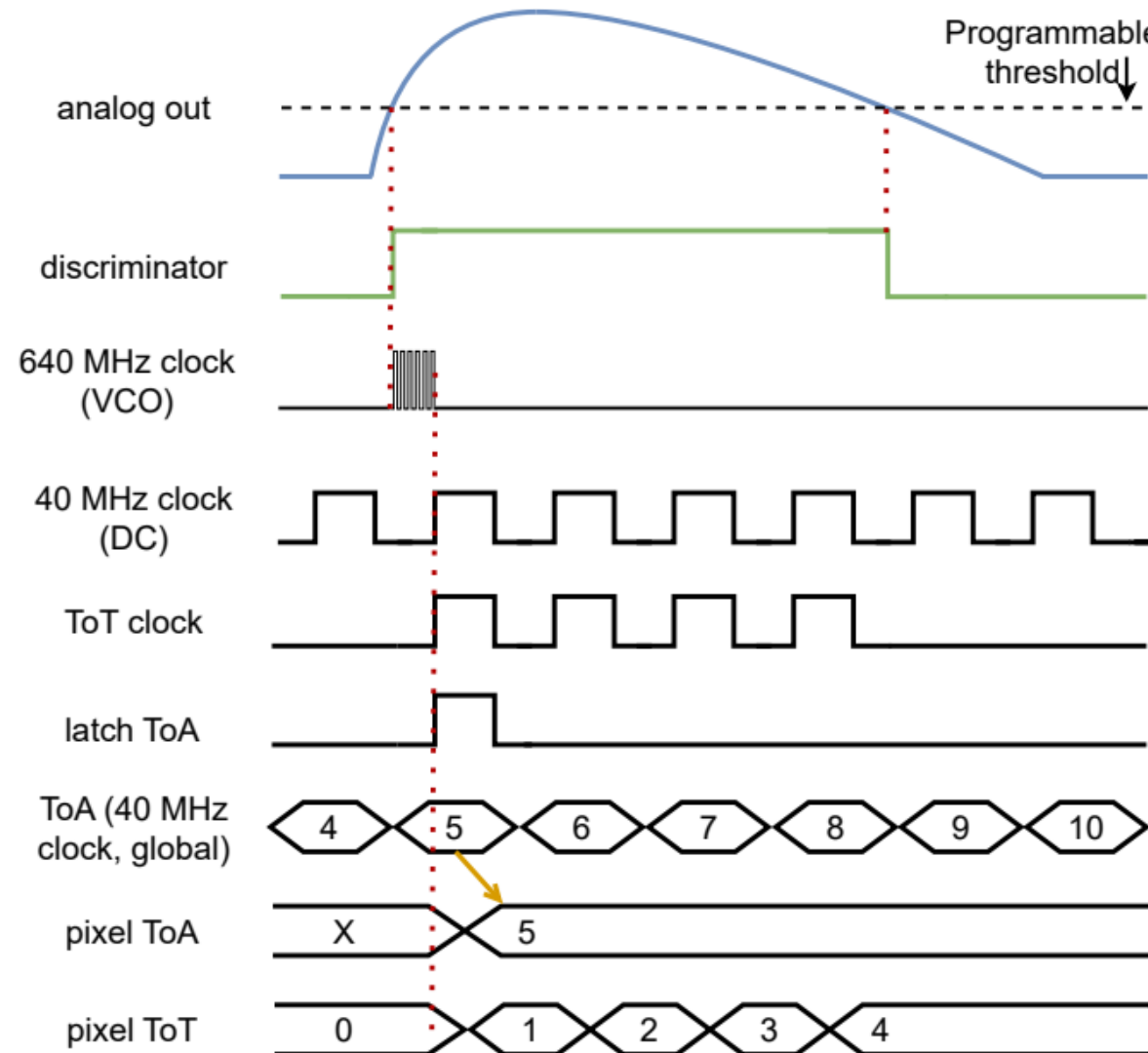
DAQ for testing and operating has been developed

Multichip support is in preparation, will be tested on real hardware soon

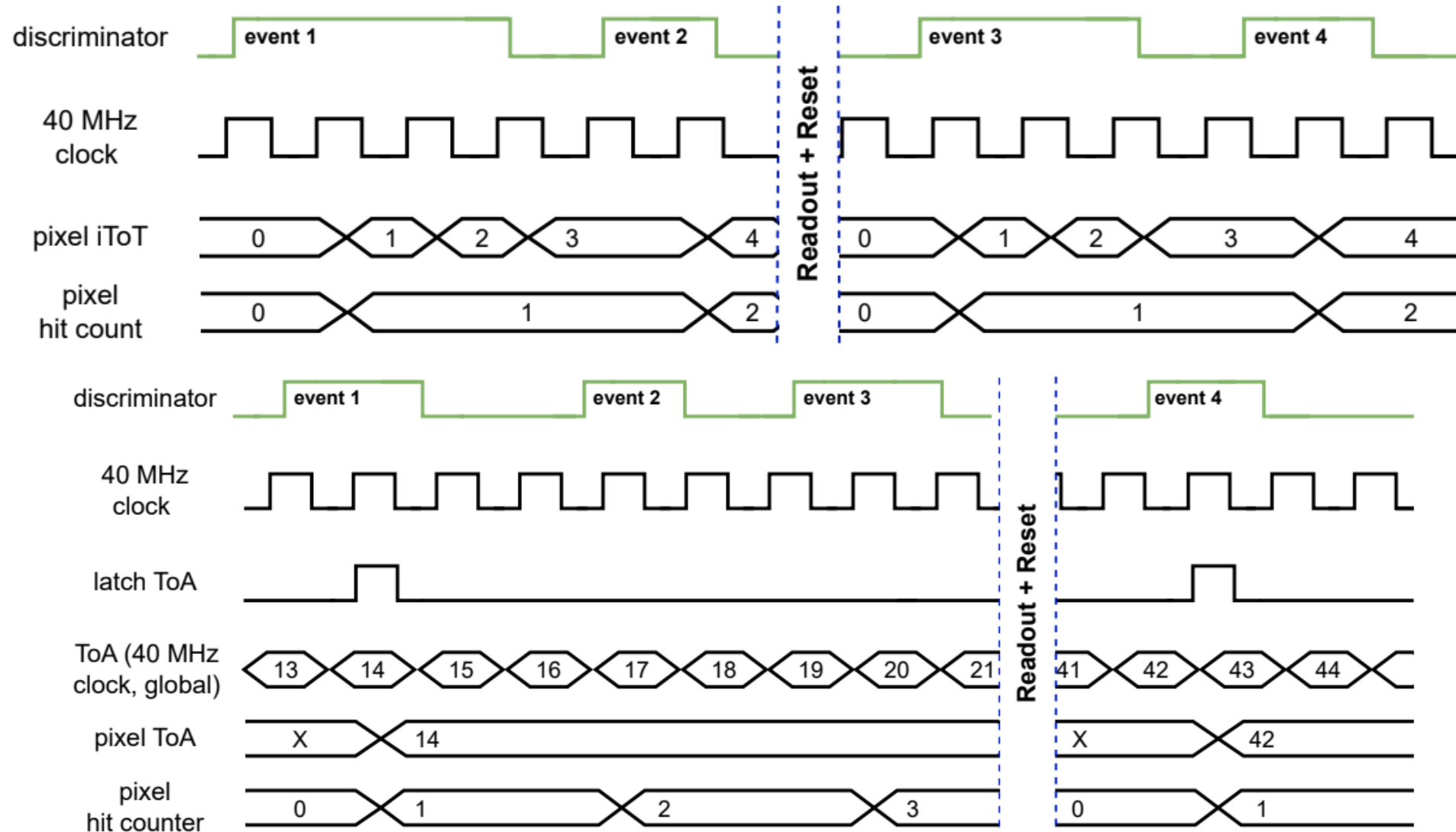
Detector Projects



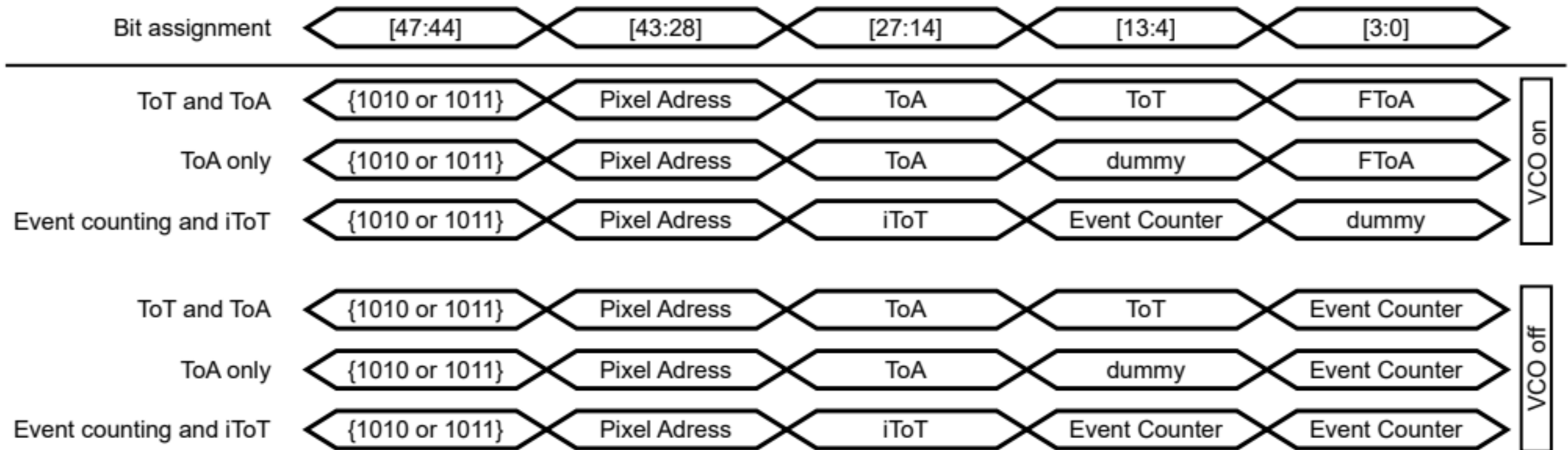
Backup – Signal Processing – ToA, ToT



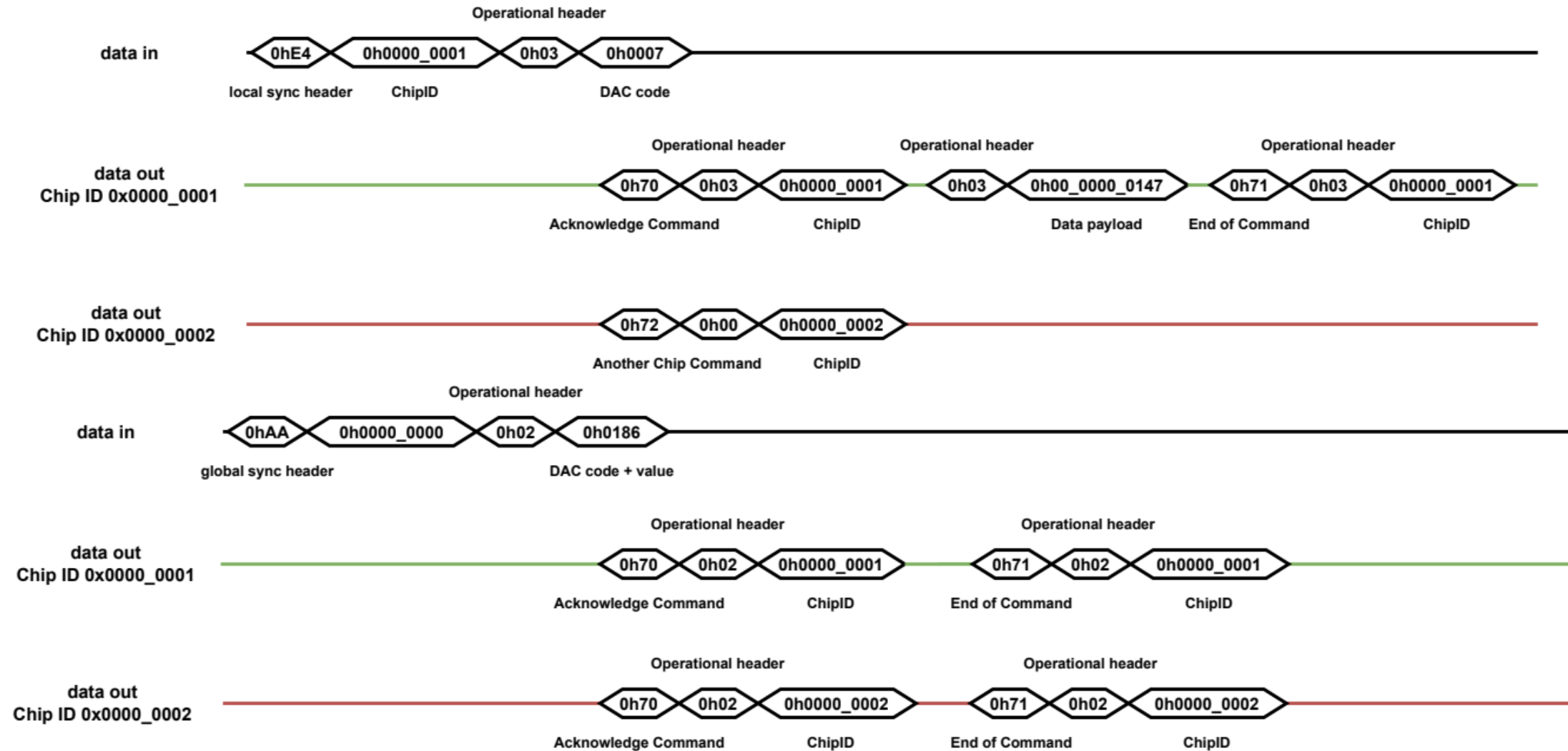
Backup – Signal Processing – iToT, Counts, ToA



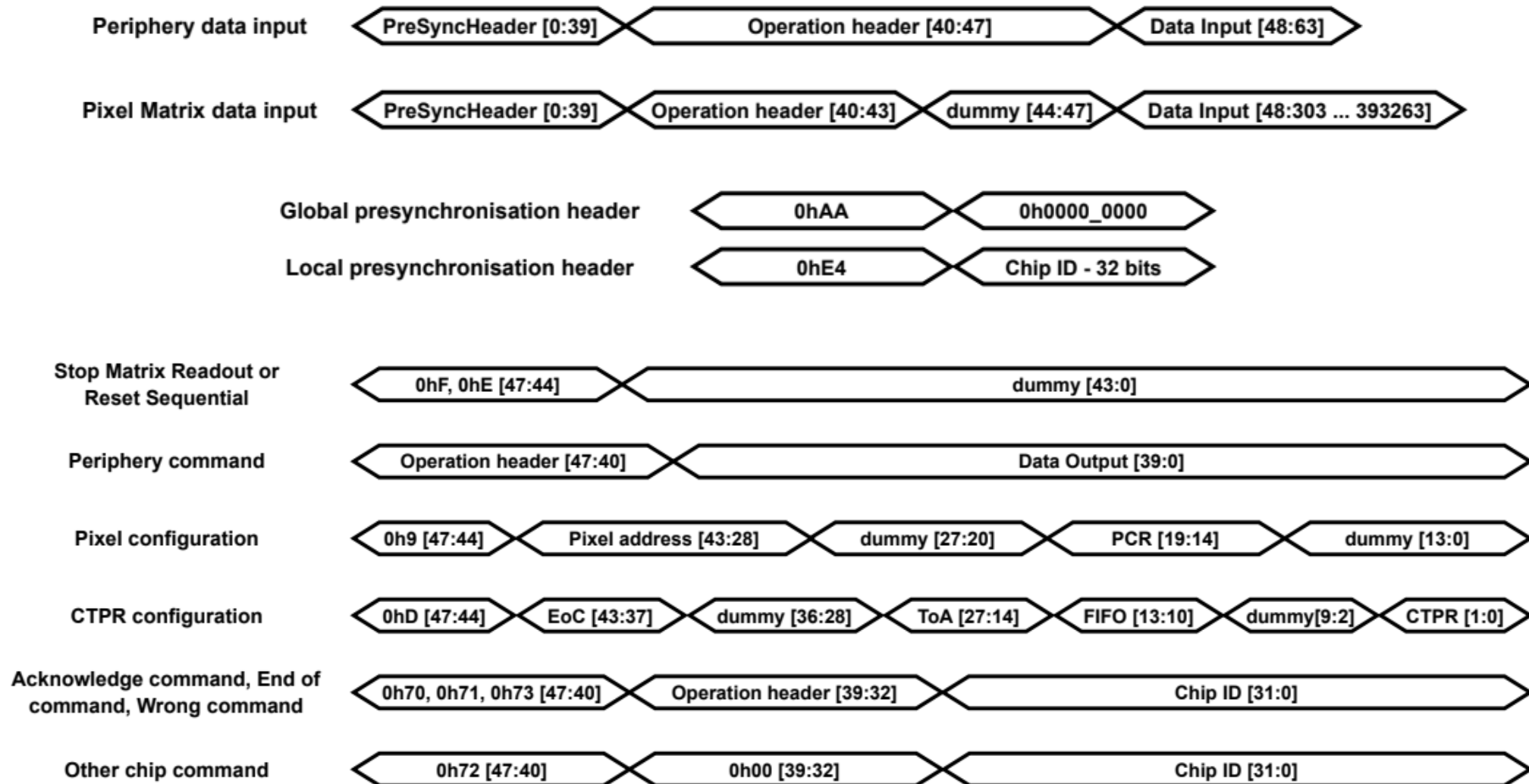
Backup – Data Packages



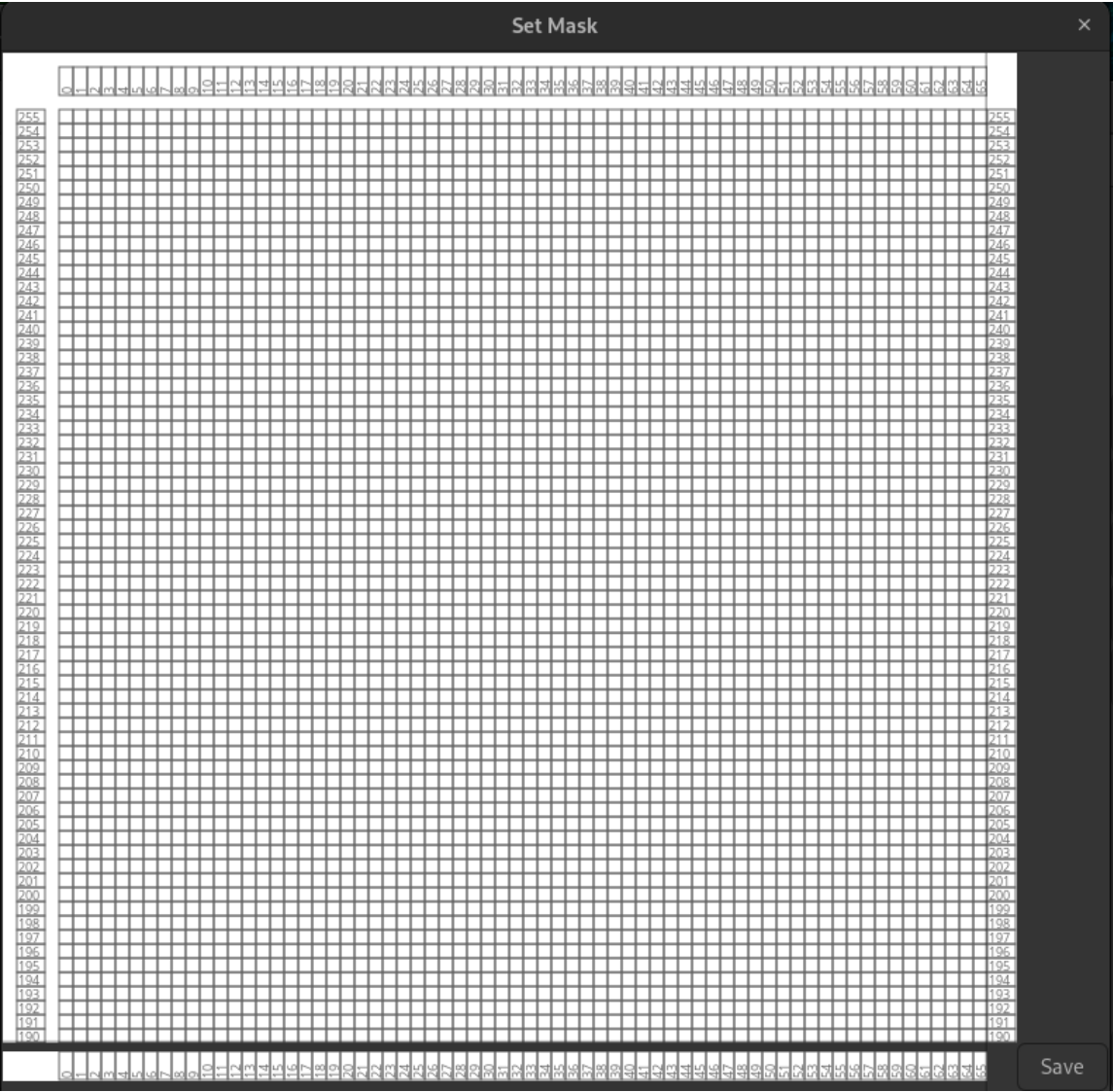
Backup – global vs. local header



Backup – Input and Output Packages



Backup – GUI, mask setting

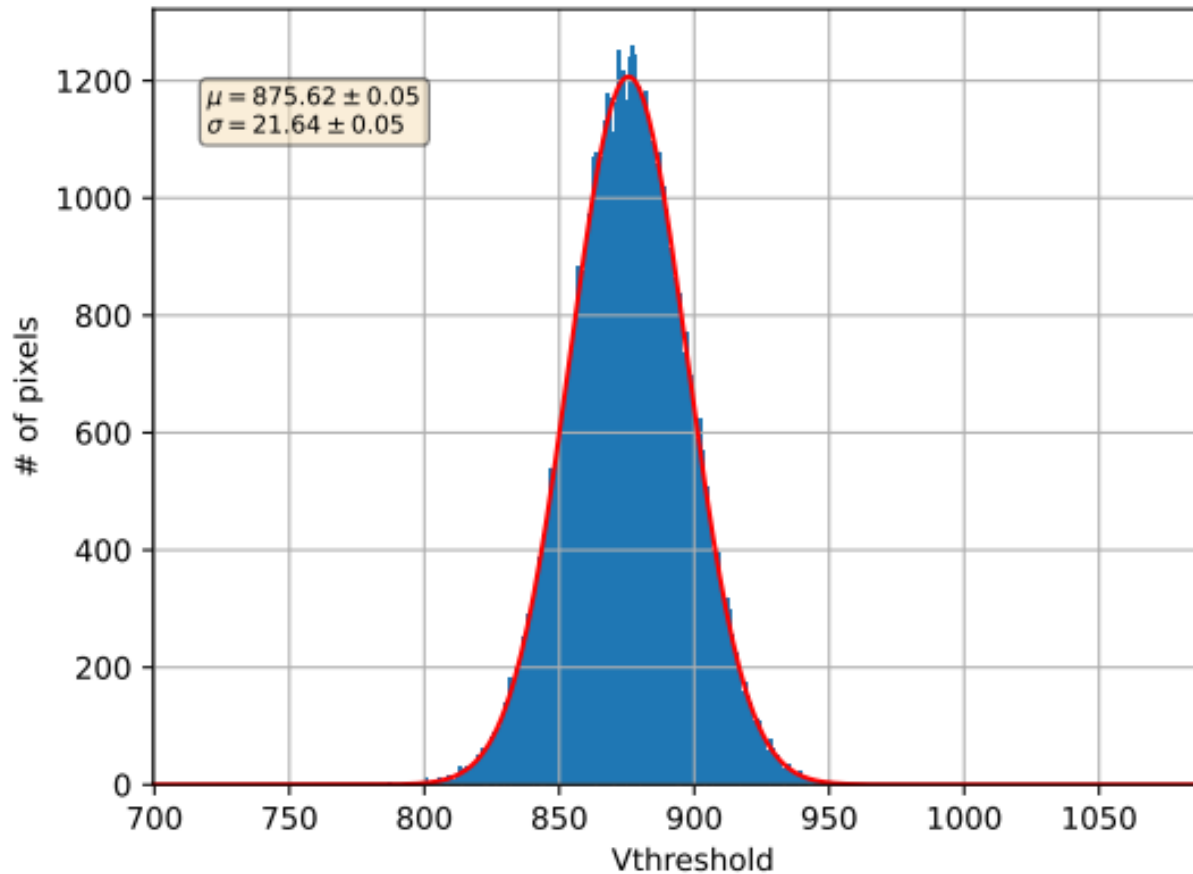


Backup – Threshold Scan, Bias 20, Threshold 0 and 15

Timepix3 draft

Chip: W18-K7

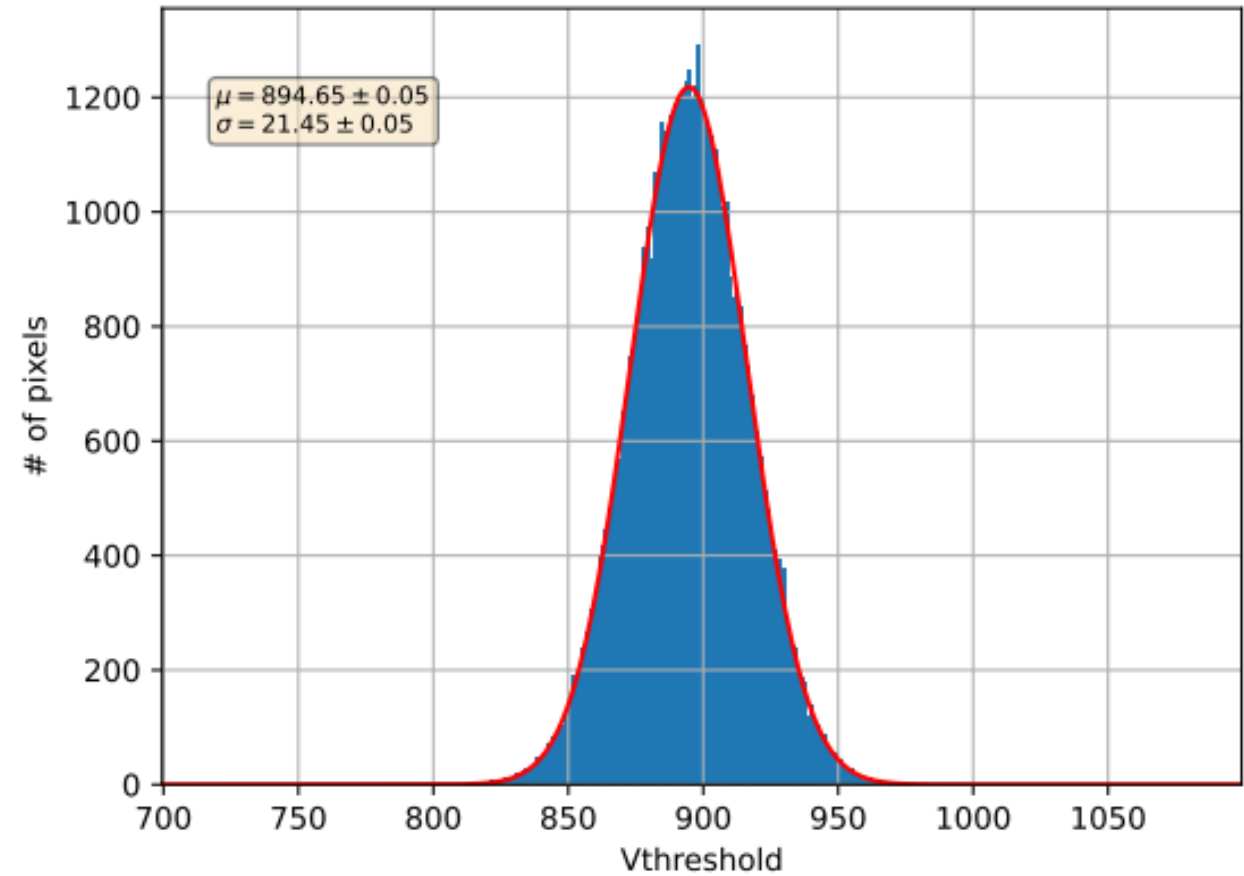
Threshold distribution



Timepix3 draft

Chip: W18-K7

Threshold distribution

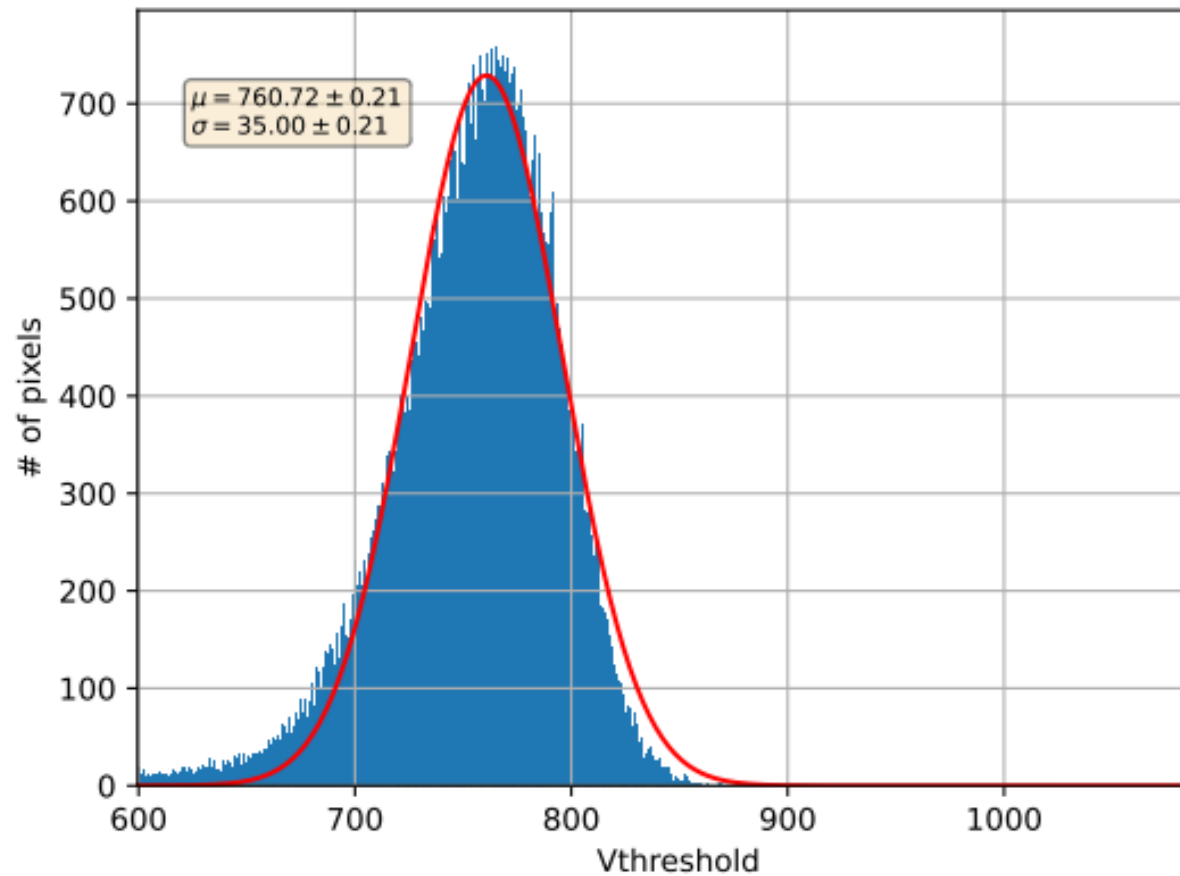


Threshold Scan, Bias 250, Threshold 0 and 15

Timepix3 draft

Chip: W18-K7

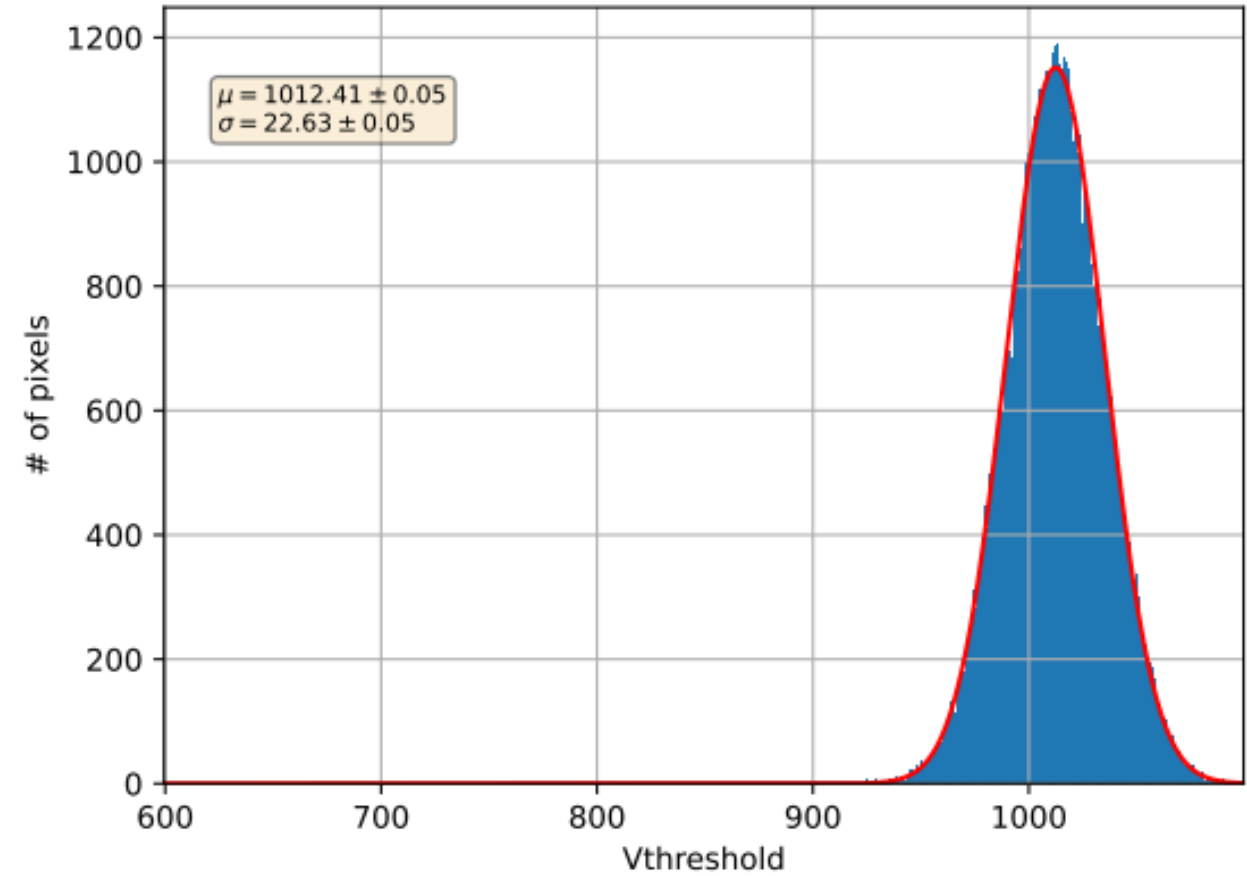
Threshold distribution



Timepix3 draft

Chip: W18-K7

Threshold distribution

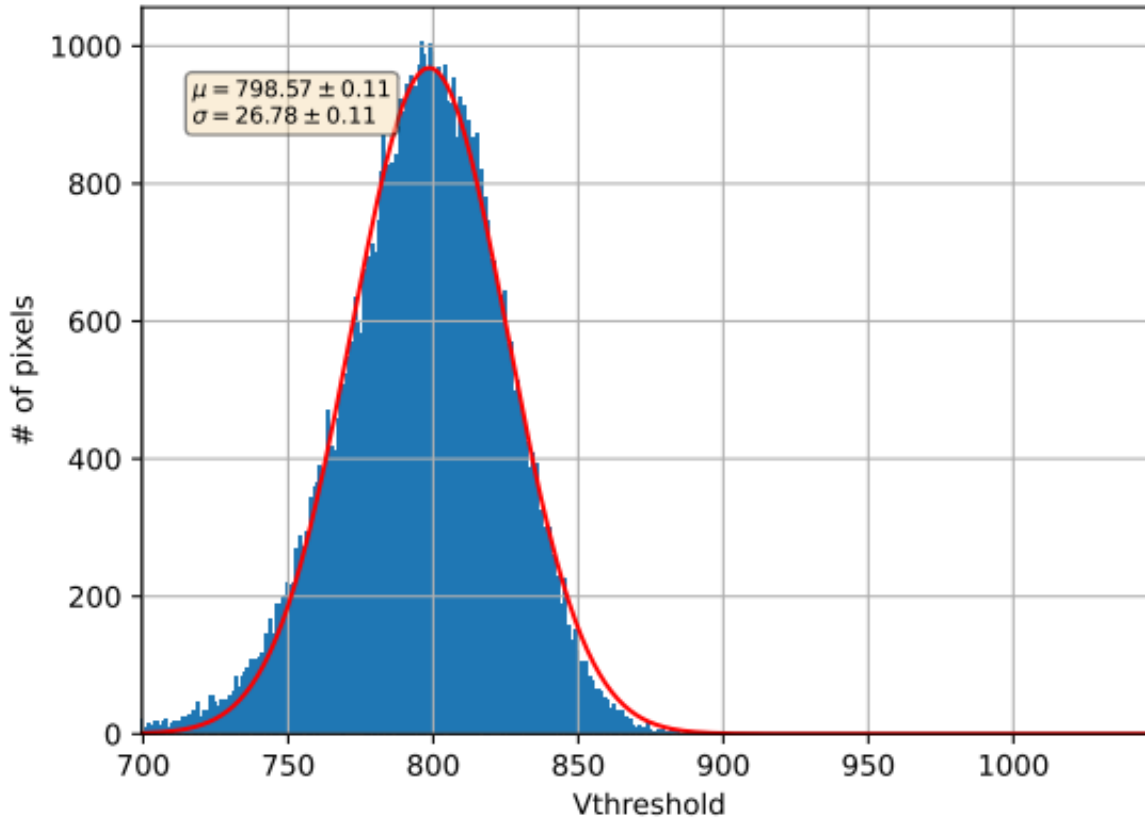


Threshold Scan, Bias 150, Threshold 0 and 15

Timepix3 draft

Chip: W18-K7

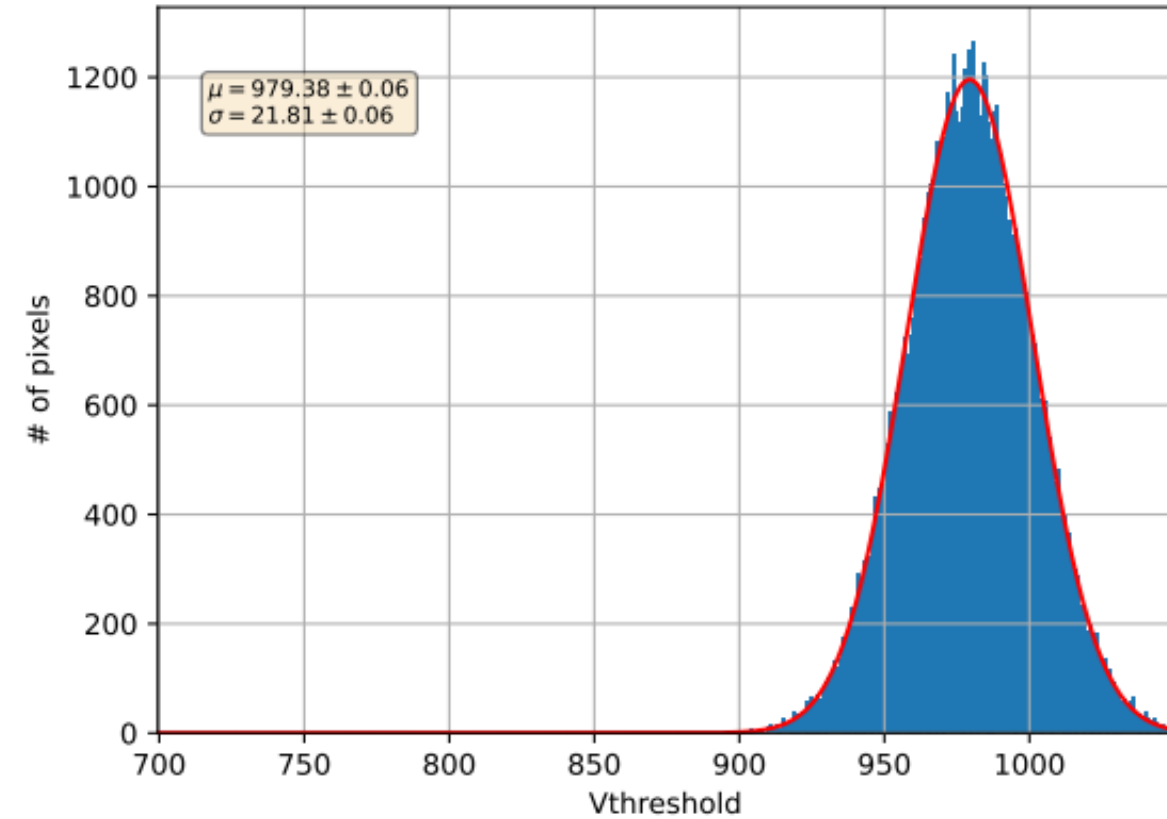
Threshold distribution



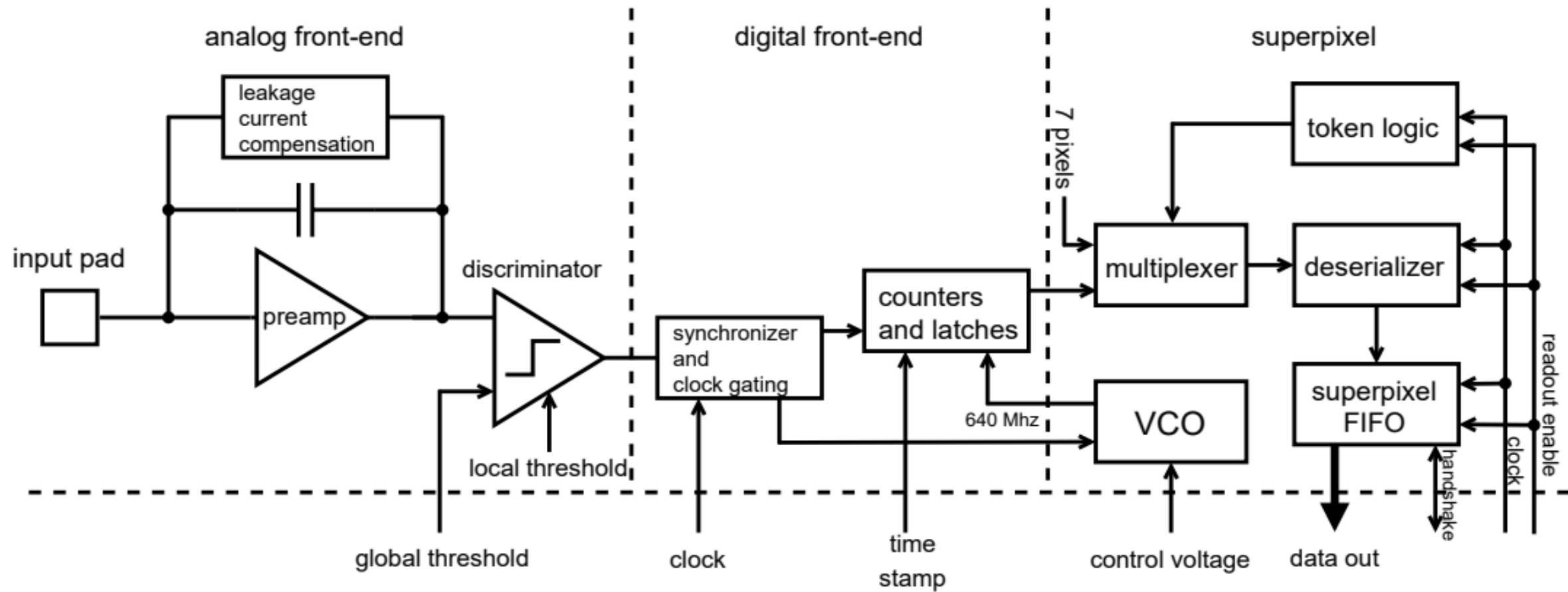
Timepix3 draft

Chip: W18-K7

Threshold distribution



Pixel Logic



Pixel Address

