

#### Low-Latency Track Triggering in High-Energy Physics

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## **HL-LHC CMS Tracker Upgrade**



High occupancy  $\rightarrow$  New silicon detector



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Only hit pairs with p<sub>T</sub> > 2 GeV ("stubs") are forwarded off-detector



Average 15 000 stubs every 25 ns stub bandwidth ~50 Tb/s



# **HL-LHC CMS Tracker Upgrade**



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- Average 15 000 stubs every 25 ns stub bandwidth ~50 Tb/s
- Increased data rate → New read-out electronics system
  - Capable of **reconstructing tracks** at the collision rate
  - With a total latency of **4 μs**



## **Track Finder Approach - Algorithms**





**DTC** reads the detector modules and performs time-division multiplexing

**TF** reconstructs the tracks for one event

## **Track Finding Algorithm**





## **Track Finding Algorithm**







## **Contributions to the Track Finder Algorithm**



#### **Geometrical Processor**



- Detector division in finer sub-sectors in  $\eta$  and  $\phi$
- Optimized for similar data rate per sector
- Latency reduced by a factor of 2 (58 ns) compared to other work
- **Resource saving** of 25 % less DSPs & 30 % less FPGA area

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#### **Duplicate Removal**



- It uses only 1 % of the resources used for the pair-wise comparison approach
- Contributes to the latency with only four clock cycles ~17 ns
- Remove duplicates without losing efficiency

#### **Track Finder Results**





Average track finding efficiency > 95 % (for tracks > 3 GeV)

## **Track Finder Demonstrator Latency**







< 4 µs requirement fulfilled!</p>

### **Tracker Finder Approach - Hardware**





**Detector**, Trigger & Control Boards **Track Finder** Boards

## 'Serenity' ATCA Board





- Board compatible with several high-end FPGAs (Xilinx VirtexUS+)
- Capable of handling up to 3.1 Tb/s of data bandwidth
- 124 high-speed optical channels
  @ up to 25 Gb/s
- Excellent optical performance 1E-12 Bit Error Rate (BER)
- Management mezzanine based on a heterogeneous computing device (Xilinx ZynqUS+)



#### Conclusions



- Demonstrated that reconstruction of tracks under the tight latency requirements of the CMS L1-trigger system is possible
- The reconstruction algorithm was fully implemented in hardware (FPGAs)
- Optimizations of such algorithms were fundamental for the overall scaling up of the system
- The 'Serenity' ATCA board has an enormous processing capability which greatly exceeds the requirements
- Serenity' is currently foreseen to be used at CMS in several sub-detector systems: Tracker, HGCal, L1-Trigger, MTD, & BRIL

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### **Track Finder Results**





- Robustness of the system over module failures
- Efficiency can be recovered by reducing the number of layers required to form tracks on the affected region



## **Back-End Electronics System**



#### L1 Trigger Accept



- Must handle the stub throughput ~50 Tb/s / a lot of information
- Must be capable of reconstructing tracks at the collision rate / possible?
- Total allowed latency for (DTC + Track Finder) is 4 μs / fast

### **Geometrical Processor (GP)**





- Detector division in finer subsectors in  $\eta$  and  $\phi$
- Shaded area duplicates data across neighboring sectors
- Optimized for similar data rate per sector
- "Bend filter" reduces output data rate of next stage (HT) by a factor of 4
- Latency reduced by a factor of 2 (58 ns) compared to other work
- Resource saving of 25 % less DSPs & 30 % less FPGA area (V7-690)

## **Duplicate Tracks Formation**



#### **Hough Transform**





- Every cell in the HT is independent from the others
- A "pair-wise" comparison of tracks in search for stubs in common was developed but not optimal



Kalman Filter

- Able to remove fake stubs and refine the projection
- Not able to remove duplicated tracks
- ~50 % output tracks are duplicates

## **Duplicate Removal**















- Looks only at a single track
- It uses only 1 % of the resources used for the pair-wise comparison approach (V7-690)
- Contributes to the latency with only four clock cycles ~17 ns
- Remove duplicates without losing efficiency

## **Reconstruction Algorithms**



