Overview of FPGA applications at XFEL

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PUNCH4NFDI TA5 - XFEL Joint Workshop on Machine Learning and Data Processing on FPGAs
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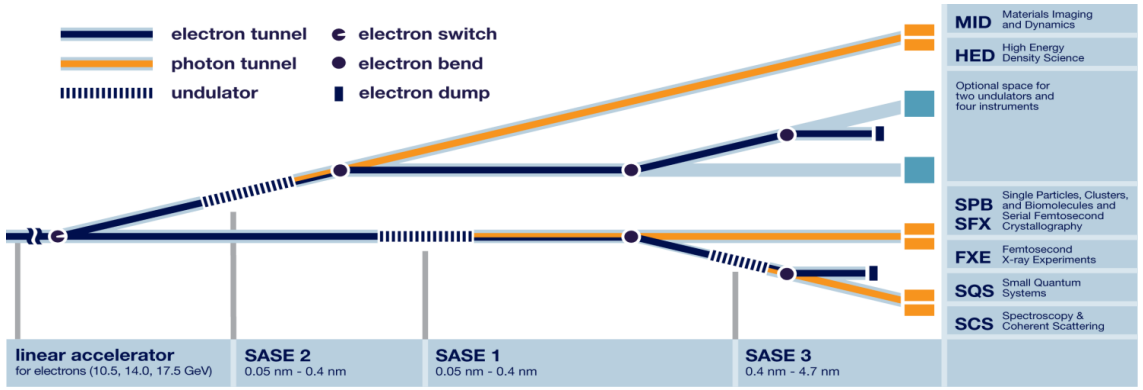
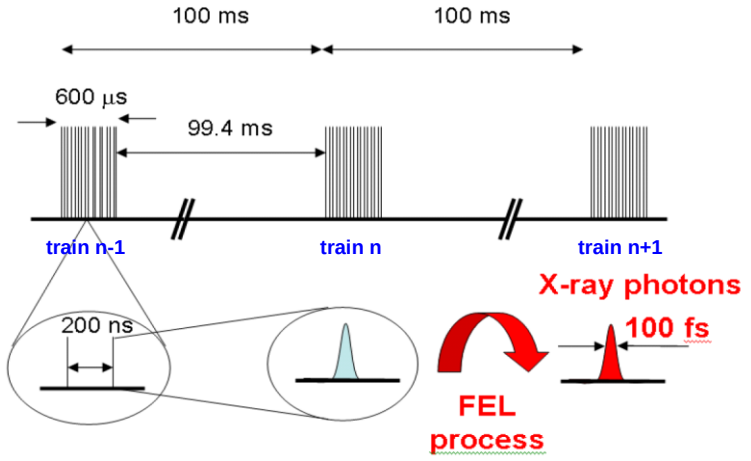
XFEL Overview



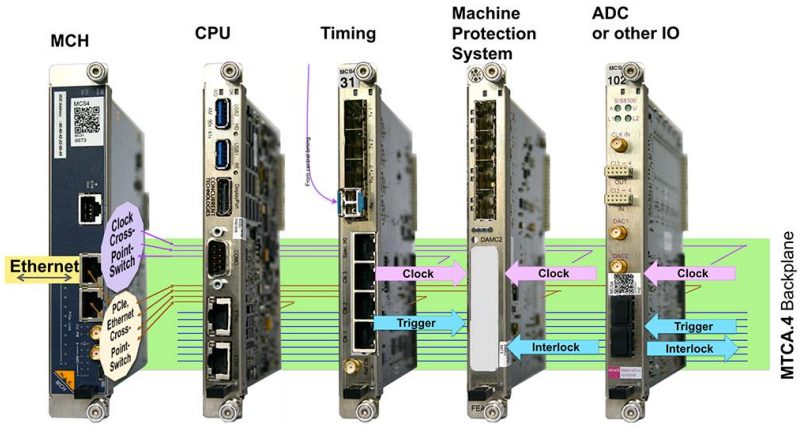
- The European XFEL generates up to 2700 X-Ray pulses
  - Inter pulse separation of 220 ns
  - Train repetition of 10 Hz
- First user operation started in September **2017**

Lasing in all three Undulators simultaneously



Overview of current FPGA platforms at XFEL

- MicroTCA standard was adopted as the platform for timing distribution
  - Communication channels available within the crate for distribution of **data and timing signals**
  - AMCs available with FPGA for digitization of signals, processing, external communication, etc.



Clock & Control RTM (University Collage London)

DAMC2 – Universal digital AMC (DESY)

Timing System (Stockholm University / DESY)

High-Speed Digitizer Family (Signal Processing Devices Sweden AB)

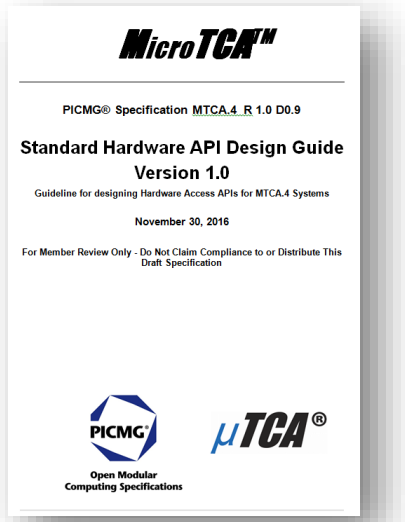
MicroTCA Carrier Hub (N.A.T.)

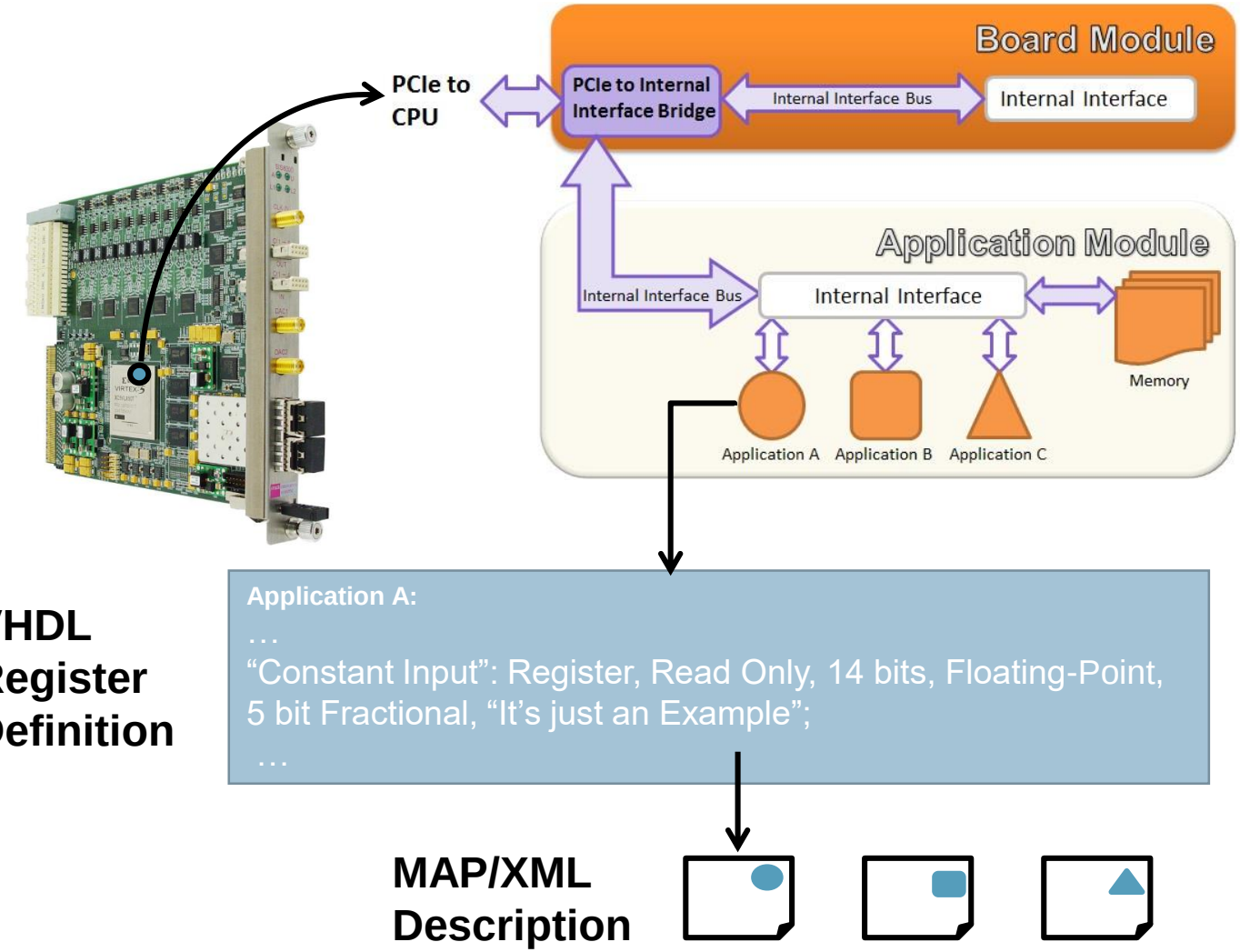
High-performance DSP and FPGA board (DMCS/DESY)

SIS8300 – ADC AMC (Struck Innovative Systems)

Standard interface in FPGA Development

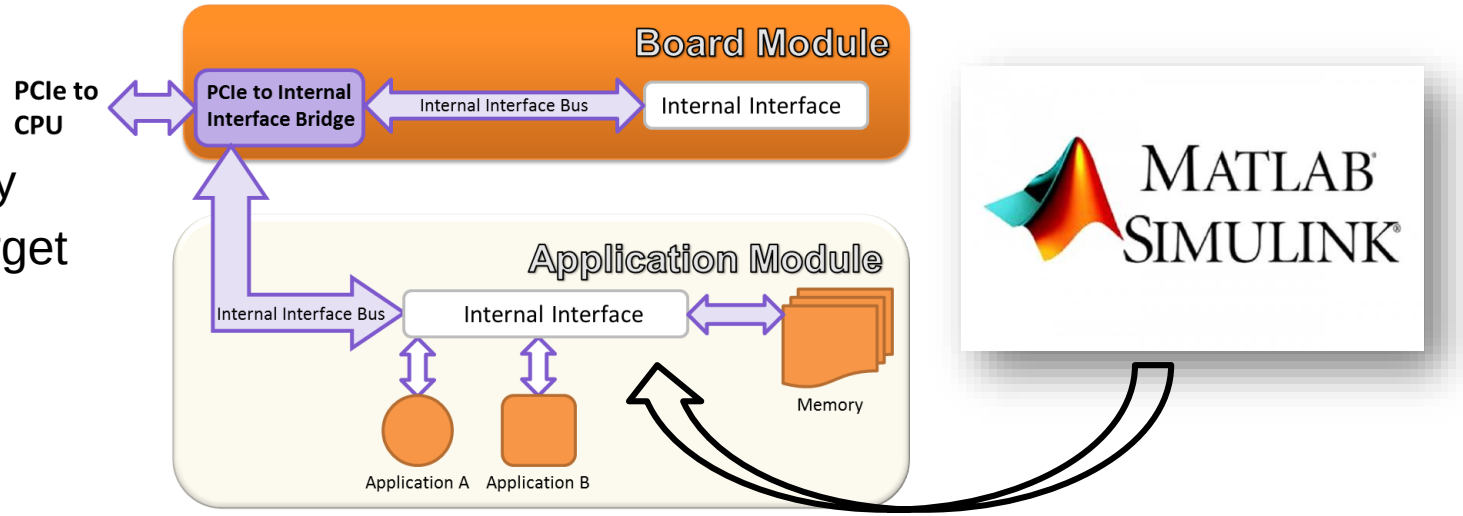
- Board and Application Module approach
- **Internal Interface (II)** module for Register Definition
  - Information regarding CPU interface is defined directly in VHDL

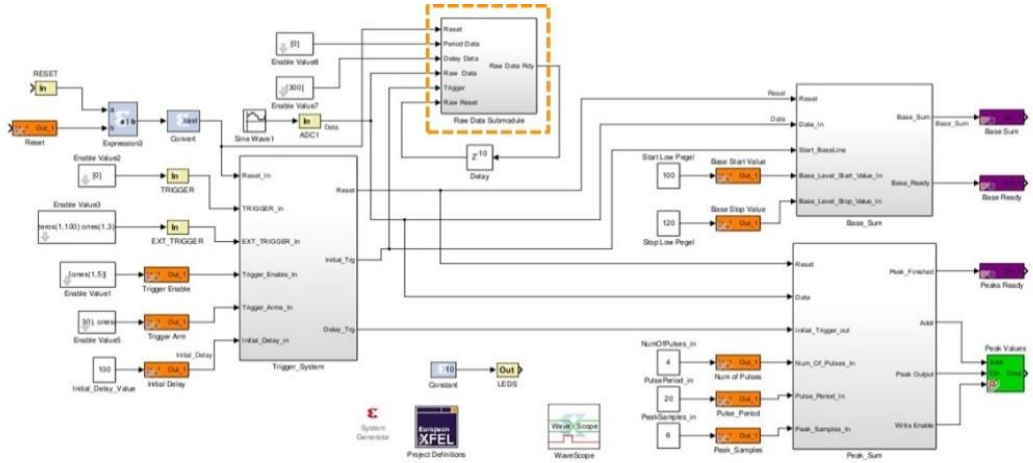




XFEL Simulink Environment

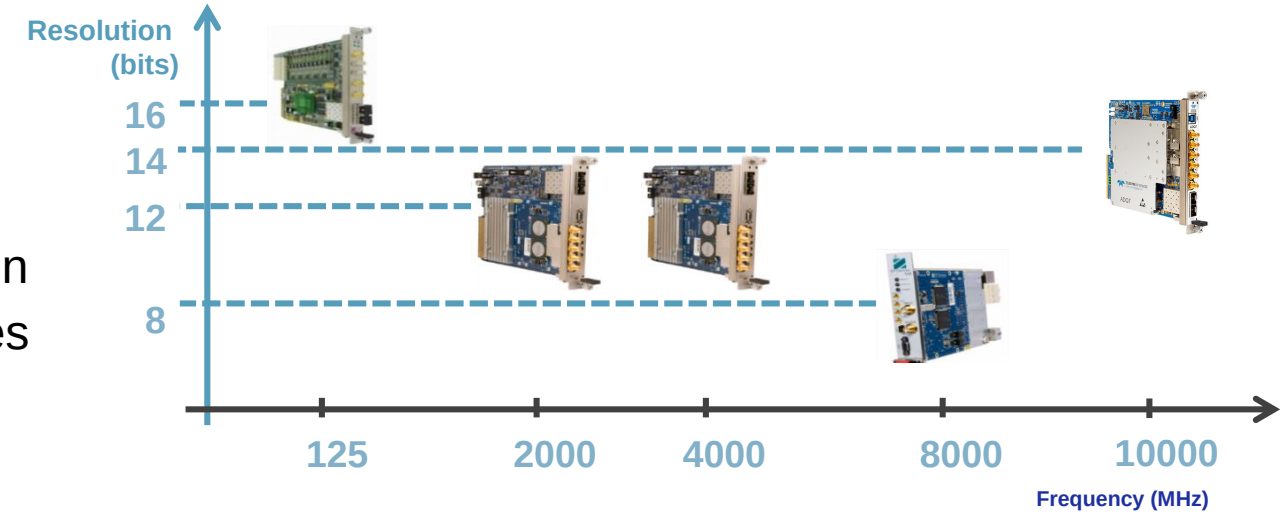
- Simulink environment which automatically setups the design environment for the target board and available features
- Library that allows definition of **registers and memories** to communicate via the chosen protocol
- Easy to **port and distribute applications** to other projects/boards
- Integration of **Matlab** allows for powerful test environments





Development in External FPGA environments

- VHDL custom development for commercially available MicroTCA Digitizers
  - Teledyne platforms
  - **TDC core** which improves trigger precision
  - XFEL does the initial tests of these devices for MicroTCA platforms

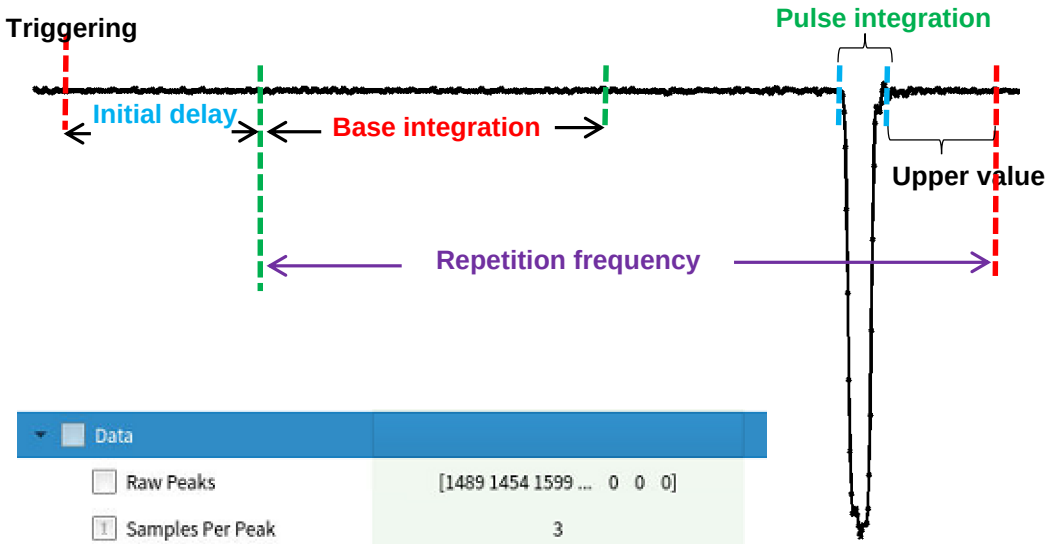


- ADQ14
  - 4 channel @ 1GSPS

- ADQ7
  - 1 channel @ 10GSPS or 2 channels @ 5 GPSP

XFEL FPGA processing algorithms

- Peak Integration
  - User definition of integration value
  - Based on user threshold value
  - Baseline per trace or pulse
- Zero suppression
- Virtual ADC channels (add/subtraction of raw data)
- Based on **Bunch Pattern decoding**
  - Automatic Peak Integration
  - Conditional and Dynamic Trigger
  - VETO decision



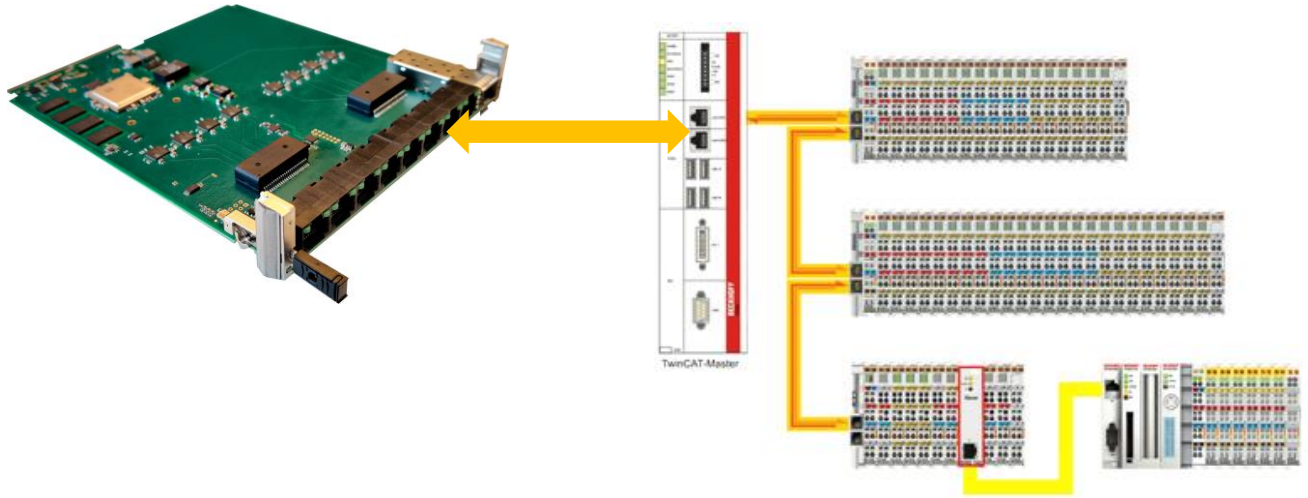
Data	
Raw Peaks	[1489 1454 1599 ... 0 0 0]
Samples Per Peak	3
Raw Baseline	5073
Raw MultiBaseline	[5073 0 0 ... 0 0 0]
Samples For Baseline	10
Baseline Value	0.009675979614257812
Peak Values	[-0.00020917 -0.0004317 0.00049019 ... ...
Mean Peak Value	0.00029987761129935585
Std. Dev. Peak Value	0.00042693489473406566
Raw Data	[512 520 462 ... 520 507 516]
Raw Data [V]	[0.00976562 0.00991821 0.00881195 ... 0....

On-going Integration Projects

- **SIS8300 KU Integration**
  - Update of current hardware platform
  - Uses Kintex UltraScale+ FPGA

- **Alveo Cards**
  - Evaluating the platform for Machine Learning applications

- **EtherCat AMC** solution for communication with the PLC hardware
  - Uses Zynq UltraScale+ FPGA
  - Collaboration between XFEL and N.A.T.
  - Direct communication of Information (TrainID, Beam Modes…)
  - Phase synchronization of PLCs with Machine



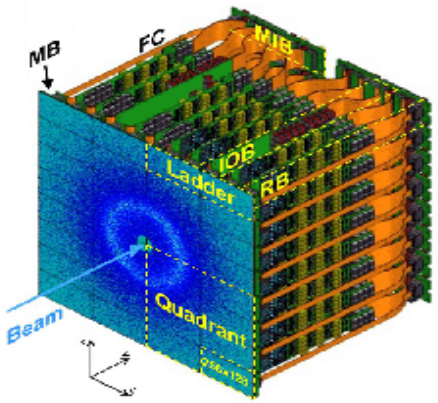
Detectors available

- AGIPD – Adaptive Gain Integrating Pixel detector

Images per train **352**

- LPD – Large Pixel Detector

Images per train **512**



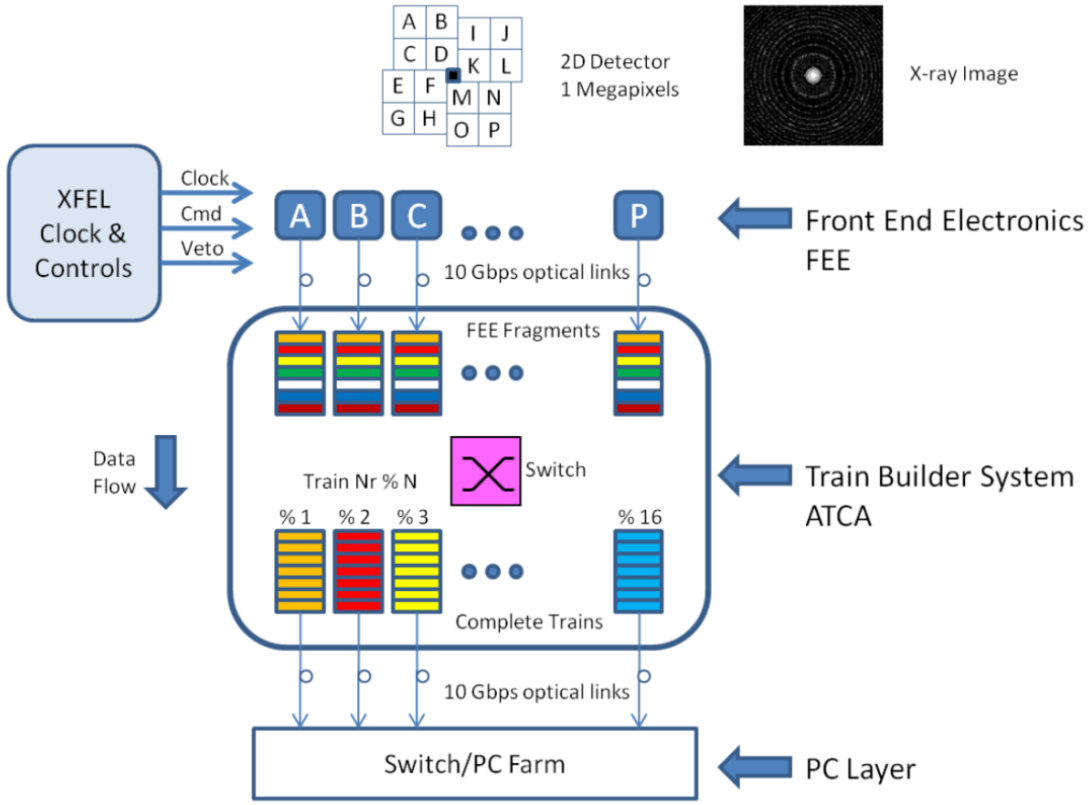
- DSSC – DEPFET Sensor with Signal Compression

Images per train **800**

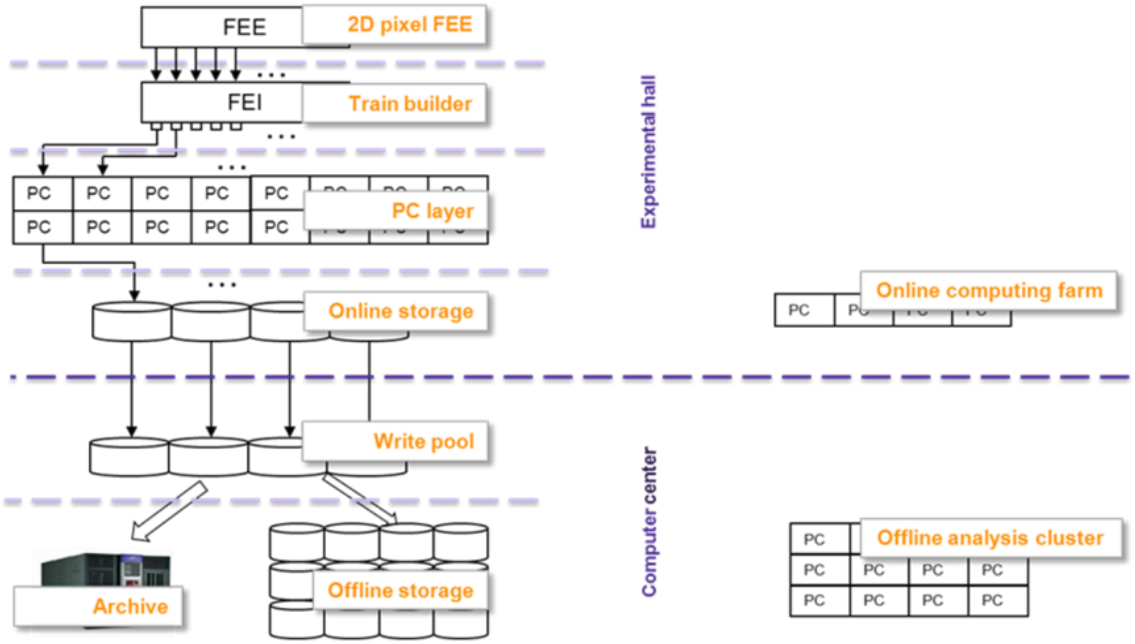
Amount of Data

Per train (10Hz) LPD produces 1024 MB of Data

Detector architecture and DAQ

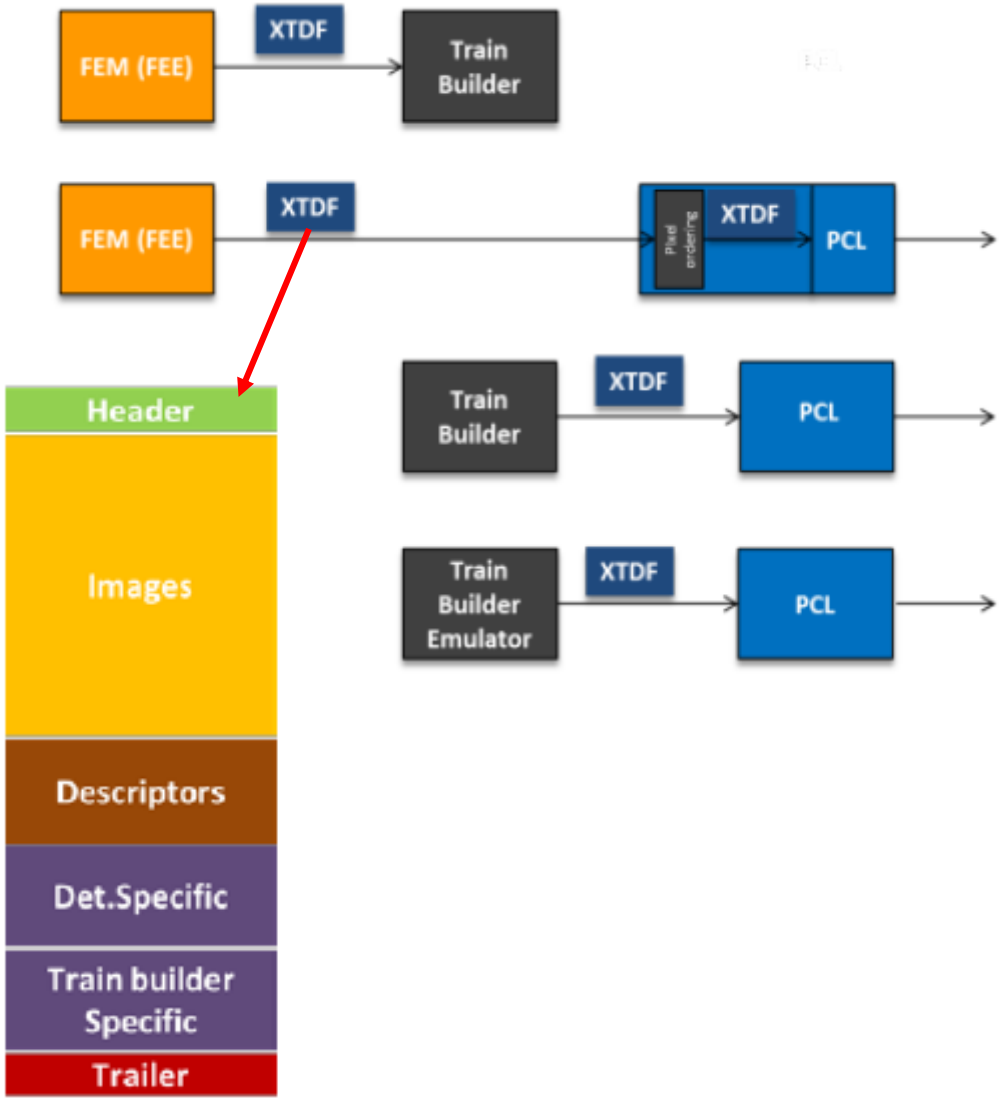


- General architecture of a 2D pixel detector in XFEL:
  - Top layer contains FEE of the detector
  - XFEL C&C distributes master clock, Command/VETO signals
  - Generated images are generated and sent via 10 Gbps SFP+ optical links via UDP/IP protocol
    - ► A total of **16 links** is require to readout 1 Megapixel
  - Data transmitted to PC layers via 10Gbps fiber links



Train data handling

- Train Transfer Protocol (TTP)
  - based on UDP and used for exchanging data between 2D detectors and the PC layer
  - TTP is agnostic to the carried data content
- XFEL Train Data Format (**XTDF**)
  - used to structure data generated by detectors
  - describes how the data is structured within a single train
- It allows PC layer to receive data from the **train builder**, **directly from the 2D detectors** or from **another platform emulating train builder hardware**



How are FPGAs platforms being used

- **Higher Abstraction**
  Institutes/Companies are focus on providing **tools, libraries and frameworks** that ease integration of FPGA platforms for data processing/acquisition:
  - Scheduling data transfer between CPU/FPGAs
  - Handling of custom **data formats** (integers with 5 bits, floating w/ 3 int and 5 frac, etc.)
  - Usage of High speed interfaces in FPGAs
  - CPU interface with FPGA modules for acceleration (kernels)
  - **Scaling** a solution to multiple platforms and/or higher data volumes

- **Machine Learning**
  prominent areas of interest are using FPGA-based accelerators for data pre-processing, image classification and FPGA inferencing of the GPU trained models

- **Dataflow-oriented architectures**
  optimized platforms that perform data transformations, with high throughput, allowing for direct connection to a network's processing layer

- **Real-time data processing**
  the parallelism and pipeline offered by the platform allows for fast feedback and/or feature extraction in real time

Where can FPGA applications benefit XFEL?

2D Detectors

Detector

Controls

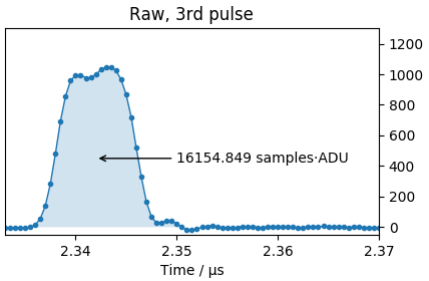
- Applications for fast feedback to determine the quality of the data and/or improve setup
- Feature extraction

- Data handling/formatting

User Devices

DAQ

ITDM



Data Analysis

Controls

1D Detectors

EEE

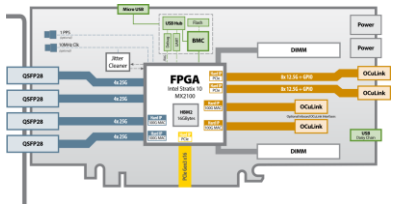
Controls

- Accelerate processing algorithms and/or Machine learning applications from XFEL and users

Investigation and evaluation of FPGA processing platforms and tool chains

- Multiple solutions are available which use **OpenCL, HLS compilers, graphical interfaces, open libraries…**
  - Quicker prototyping, focus on testing, easier code maintenance and easy of deployment in hardware
  - Keep in mind that **custom develop** for XFEL will always be necessary
- Companies provide solutions with standard interfaces that incorporated these tools/workflows
  - Not just from FPGA vendors (AMD/Intel)

AMD XILINX
Vitis™ HLS
Intel® High Level Synthesis Compiler
Intel® FPGA SDK for OpenCL™ Software Technology
Fletcher: A framework to integrate FPGA accelerators with Apache Arrow
SIEMENS
C++
SystemC
Catapult
LIBS
Fmax Target
ASIC
FPGA
eFPGA
hls4ml
SYCL™



BittWare
a molex company

Gidel

XILINX

intel

Machine Learning @ XFEL – Detector Protection

SPB/SFX side camera.

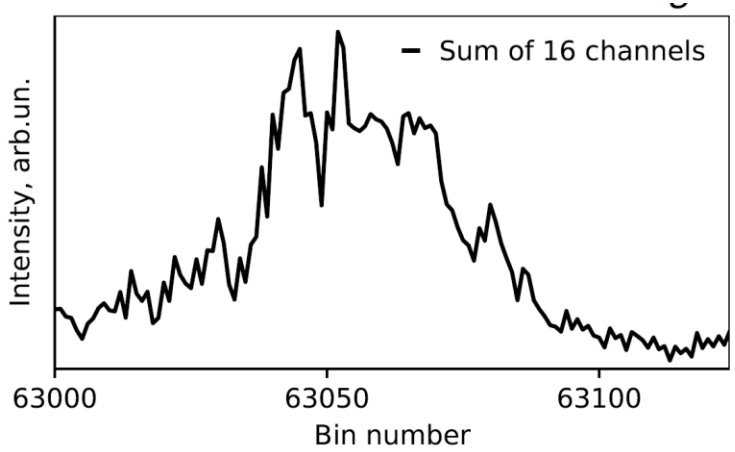
Two consecutive frames are separated by 0.1 s.

Prototype deployed at SPB/SFX. So far, all ice events detected.
Considering all alarms, about one third are false positives (WIP).

Machine Learning @ XFEL – Detector Calibration

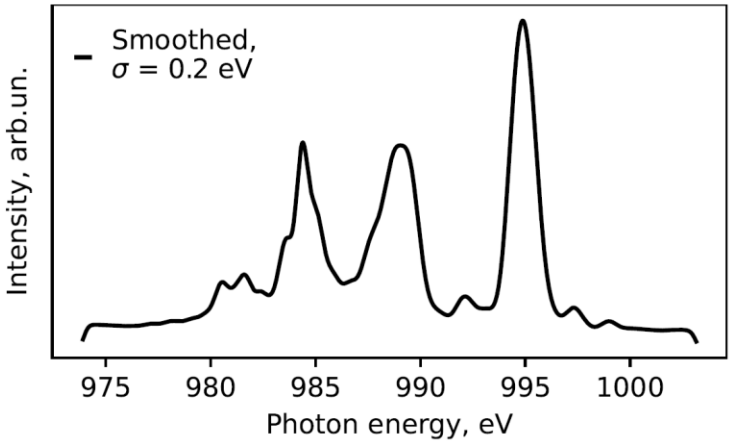
- Calibration of AGIPD Modules according to
  - Distance Detector to Sample
  - Sample
  - ROI

Machine Learning @ XFEL



Photoelectron spectrometer.

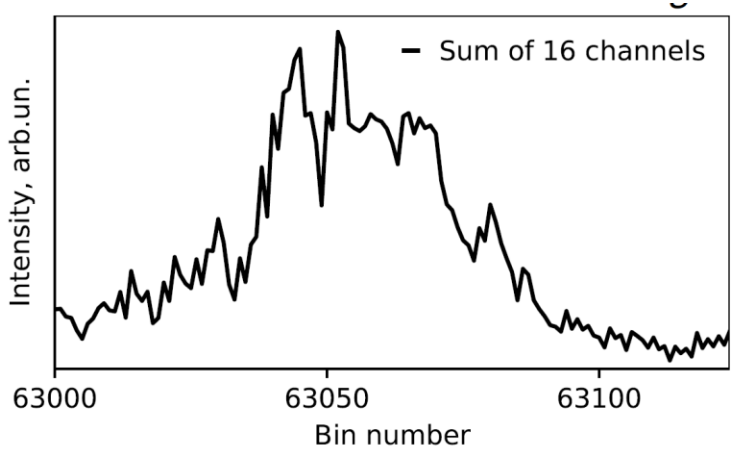
- Non-invasive.
- Pulse-resolved.
- Low-resolution.
- Complex calibration.



Grating-based spectrometer.

- Invasive.
- Train-resolved.
- High-resolution.
- Simple calibration.

Machine Learning @ XFEL



Photoelectron spectrometer.

- Non-invasive.
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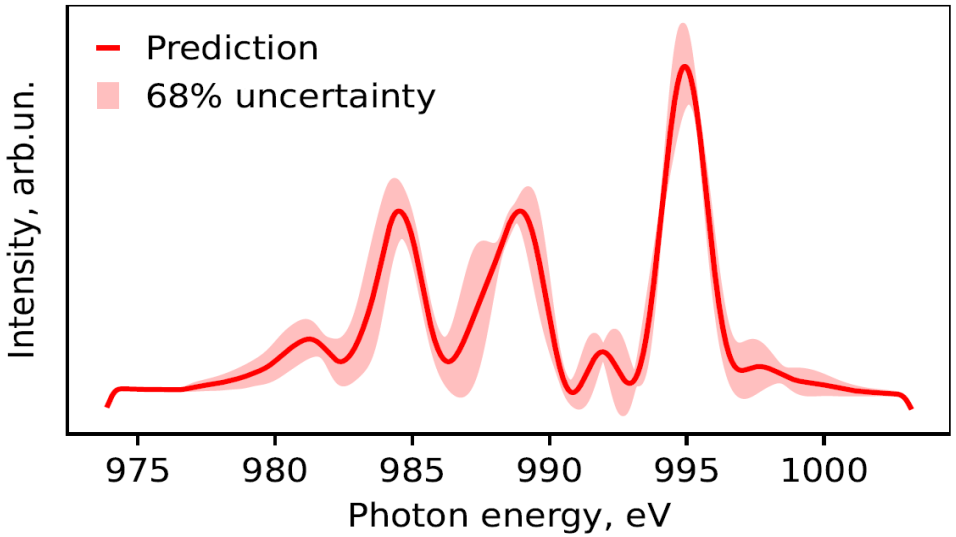
Derived from LR data.



Virtual spectrometer.

- Non-invasive:
- Pulse-resolved:
- Improved resolution:
- Simple calibration:

Outlook

- **Research on the topic and state of the art tools**
  Multiple platforms are available, each with their own tools and workflows. Taking XFEL infrastructure into account, we want to evaluate the effort/gain of integrating such platforms
  - For Machine Learning: familiarization with concepts is also desirable
- **Focus on standard interfaces/applications**
  Data input should be as generic as possible, so that ours/others developed solutions can be easily integrated and used in XFEL and other facilities
- **Take into account:**
  - Feedback from all other Data Department groups **is critical** for selecting a proper solution
  - High throughput, high data volume, low latency but **custom develop is always require**

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