CoRDIA:
An Imaging Detector for Next-Generation Synchrotron Rings and Free Electron Lasers

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Outline

- Motivation – not just “yet another Pixel Chip”
  - Existing Detectors
  - New Sources
  - New Challenges and Requirements
- “CoRDIA Cooking” - Ingredients
  - Signal path – Stage by Stage
    - Preamp with dynamic Gain Switching
    - CDS – Differential sampling Stage
    - SAR ADC
    - PCS & GWT
    - Sequencer

- ASIC Design
  - Superpixel
  - “Stonehenge” Layout
- Development Roadmap
- CoRDIA Systems – many TBDs
  - Chip Size
  - Readout Board Architecture
  - Outlook

Current Imagers

Imager example for Synchrotron Rings: **LAMBDA**

- Up to 10 megapixel (55 µm pixel size)
- 2 kHz frame rate (continuous)
- Photon counting up to 250k photons/pixel/s

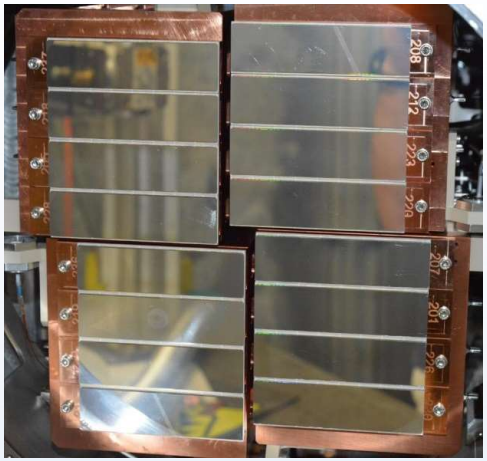
MM-PAD-1 → 2.1

- 1.1kHz →10 kHz (continuous)

CITIUS

- 17.4 kHz (continuous)

Imager example for European XFEL: **AGIPD**



- 1 megapixel (200 µm pixels), 4 megapixel in development
- 4.5 MHz burst imaging (internal storage: 352 images)
- Dynamic range – single photon to 10^4 photons /pixel/image

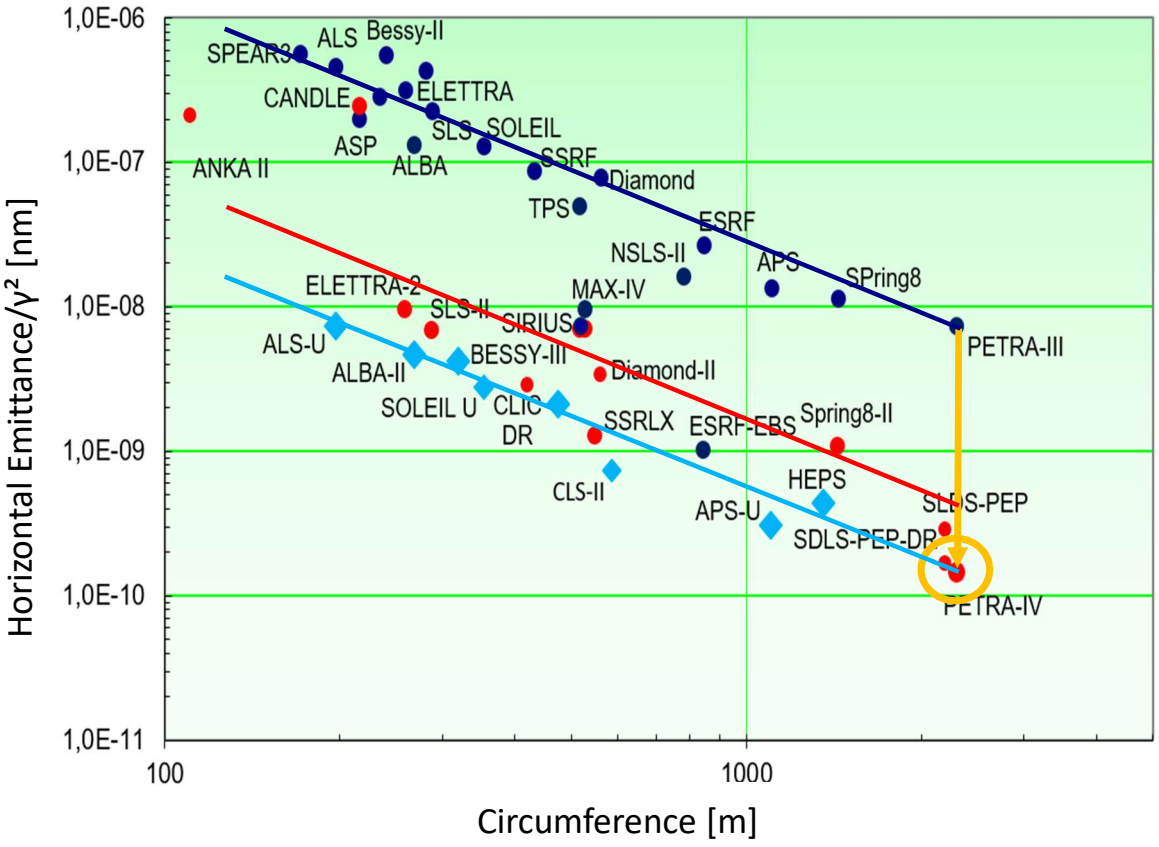
LPD (500µm, 500images)

- 4.5 MHz burst imaging (internal storage)

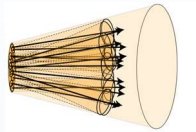
DSSC (hexagonal Ø≈230µm, 800images)

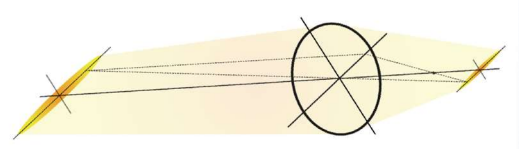
- 4.5 MHz burst imaging (internal storage)

3rd → 4th Generation Synchrotron Rings



3rd Generation Sources



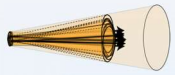


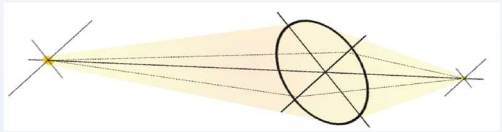
Extended Source – only fraction of light hits optics – extended focus

Multibend achromat technology

On-axis injection technology

4th Generation Sources (Diffraction limited)

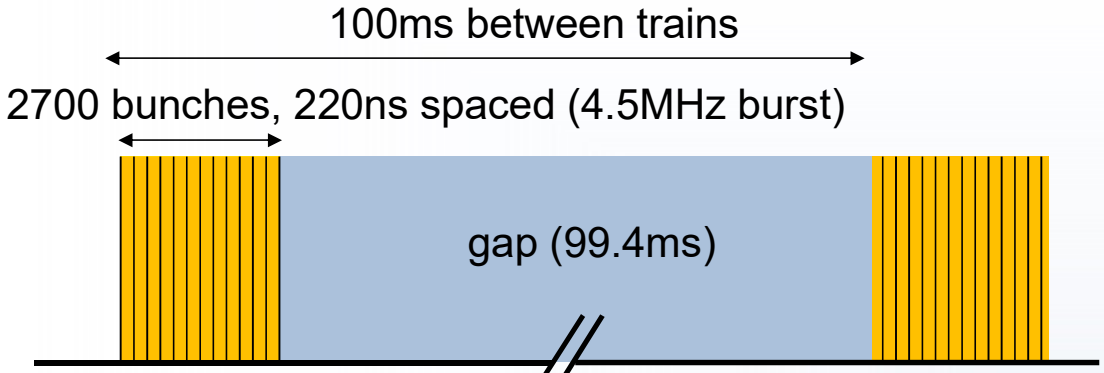




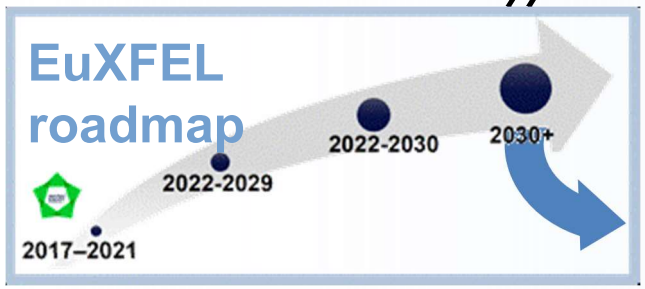
Collimated Beam – all light hits optics – point focus

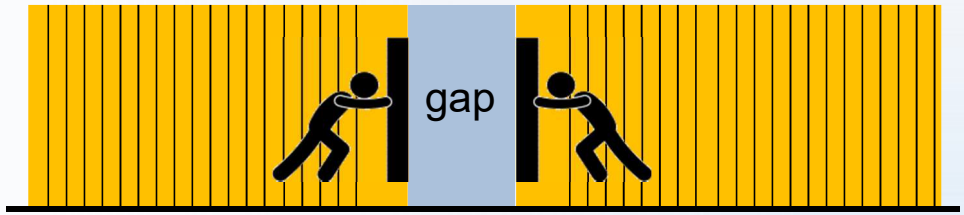
- high brightness and coherence up to high photon energies
- 100-1000 fold improvement in brilliance and coherent flux
- More photons/s on the detector
- Frame rate requirements in experiments increases from kHz to >100 kHz

FEL Upgrades: Reduced Gaps & Longer Trains CORDIA



fast acquisition (4.5 MHz) → in-pixel storage → relaxed readout





"many more" bunches
"slightly reduced" Rate

"much smaller" gaps
(ideally, full CW)

fast acq./relaxed readout no longer an option
(no space for large internal memory anyway)

What we can interpret as

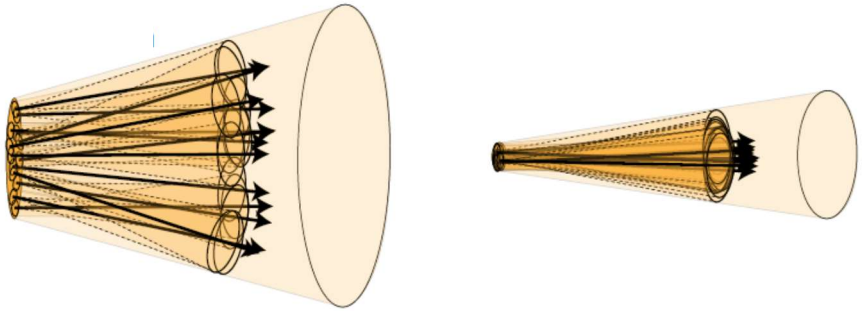
- bunches spaced 1µs
- to 100µs,

most of the time

Future Source Upgrades

PETRA-IV: Upgrade to diffraction limited ring (2028)

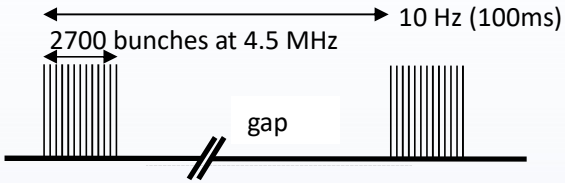
PETRA-III electron bunch PETRA-IV electron bunch



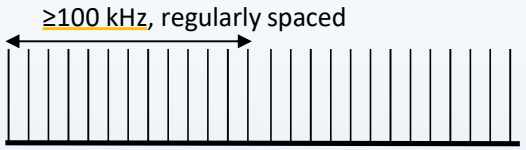
- 100-1000 fold improvement in brilliance and coherent flux
- Frame rate requirements in some experiments increase from kHz to >100 kHz (continuous) readout

European XFEL: CW mode operation (20??)

Current Eu.XFEL burst mode



Future CW operation



- many more [O(1)] bunches per second
- no gap for burst-readout of internal storage

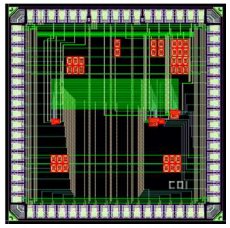
Common need for:
- continuous readout
- > 100kHz frame rate
- Small (~100µm) pixels

Continuous Readout Digitising Imager Array

CoRDIA

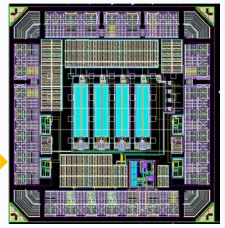
CoRDIA – Design Goals

- Pixel size 110µm × 110µm
- Continuous Frame Rate f_{FR} ≈ 150kHz (≥100kHz)
- Dead-time free pipelined operation
- Single-photon sensitive (@ ≤12keV)
- ≥ 10k photon Dynamic Range
- Little or no dead area

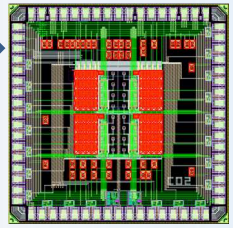


CoRDIA 0.1 (analogue)

HSI_ADC01 (SAR ADC) test chips



CoRDIA 0.2 (Superpixel)



CoRDIA – Implementation

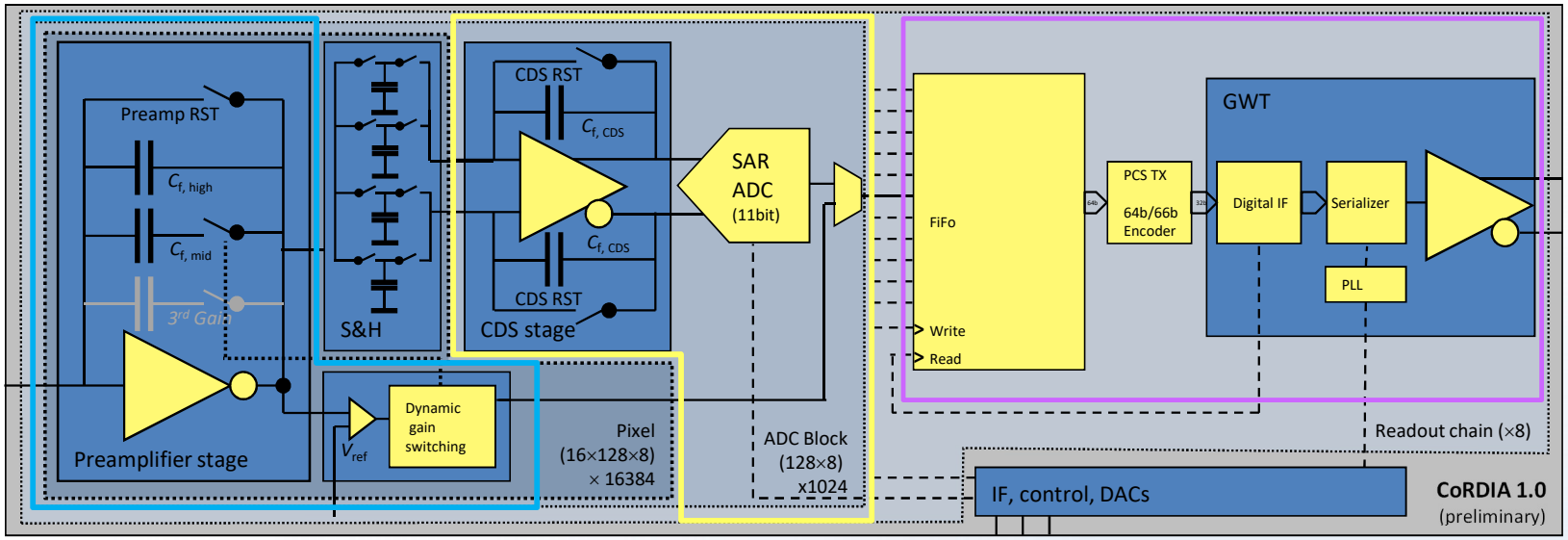
- Hybrid pixel detector
- Charge integrating
- Dynamic gain switching (à la AGIPD)
- Electron-collecting to be compatible with various sensors:
  - Si for hard (12keV X-Rays)
  - High-Z materials for E > 15keV
  - Active (LGAD) sensors for low E
- On-chip digitisation @ ≥ 10 bit
- Multi-Gbit data transmission (based on Timepix4 implementation)
- TSMC 65 nm technology

Collaboration of Bonn University & DESY

universitätbonn

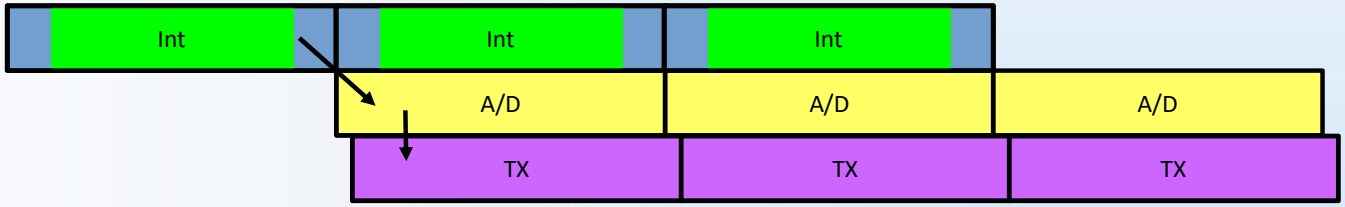
DESY.

CoRDIA – Architecture & Signal Path



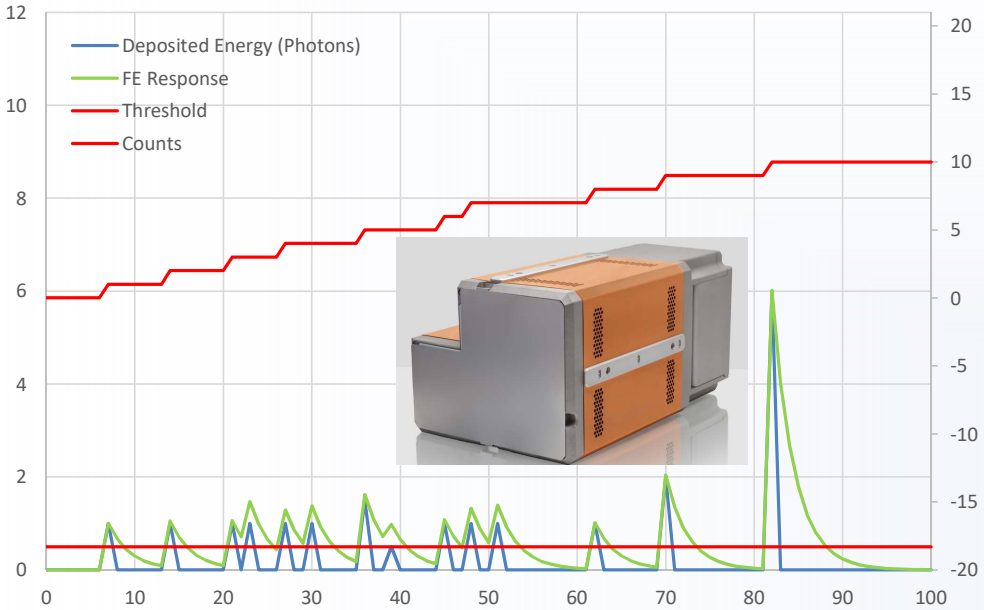
CoRDIA = **Co**ntinuous **R**eadout **D**igitizing **I**mager **A**rray

- CW (continuous wave) operation
- Pipelined
- Digitizing
- MGBT readout



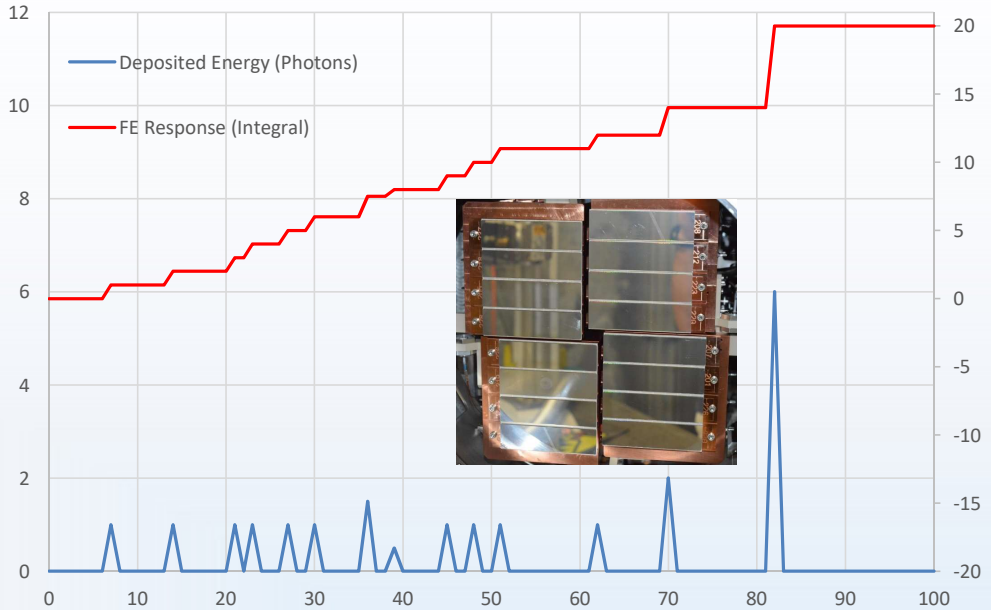
Integrating Preamp – An FEL Prerequisite

Photon Counting Detector



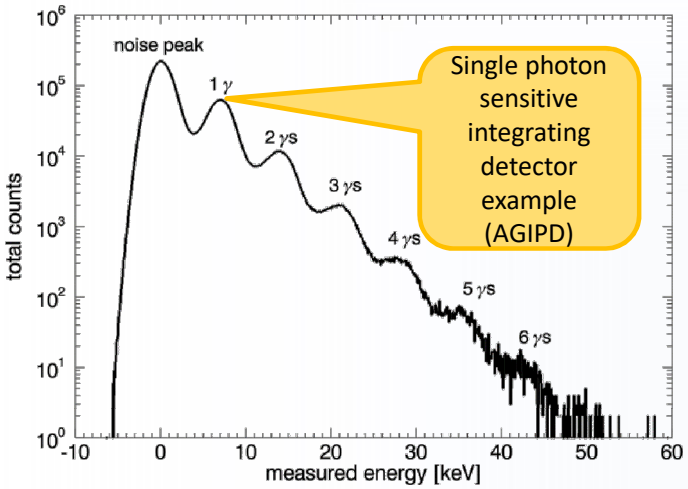
- Apparently noise-free
  - Response is a number
- Digital output
- Intrinsic dead time/pile-up
- Not sutable for FELs

Integrating Detector



- No intrinsic dead time
  - Integrates deposited charge
  - Limited spectroscopic capabilities
    - Not noise free
- Suitable for FELs

Single Photons and Dynamic Gain Switching

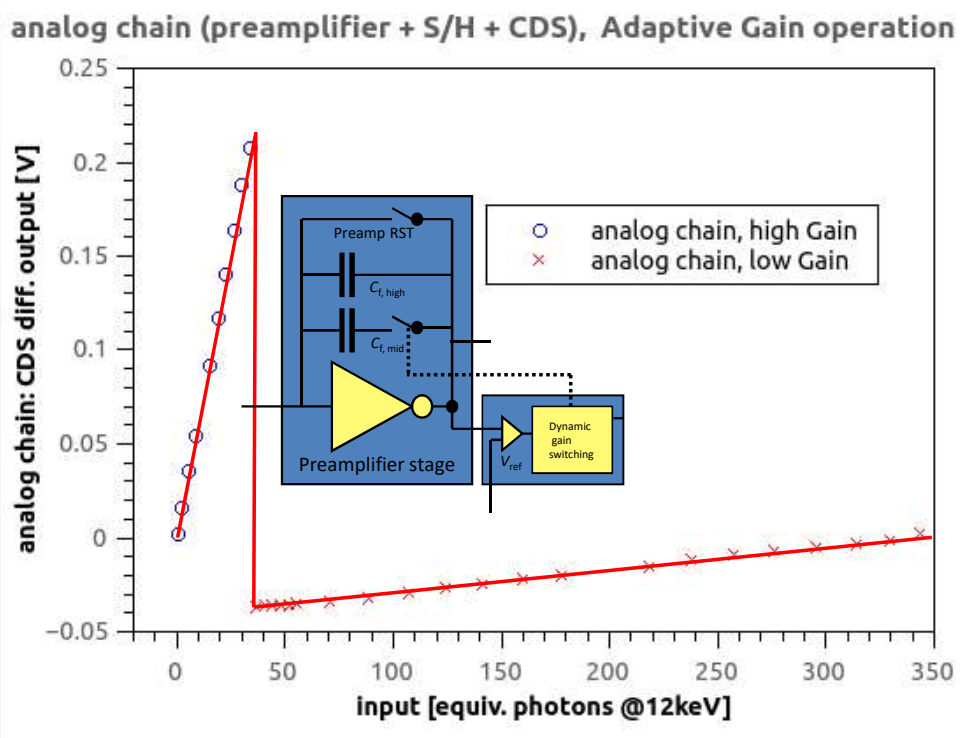


Charge integrating preamplifier conflict:

- High sensitivity
- Low noise
- Low dynamic range

or

- Low sensitivity
- High noise
- High dynamic range



Intrinsic accuracy limit of (counting) measurements:
Poisson Statistics ($\sigma \sim \sqrt{n}$)

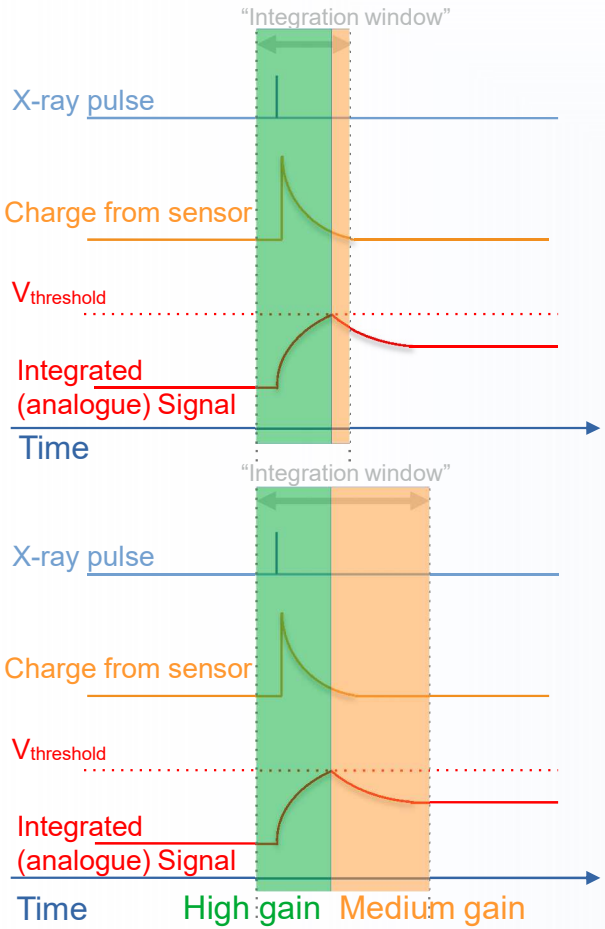
- Large signals don't need low noise

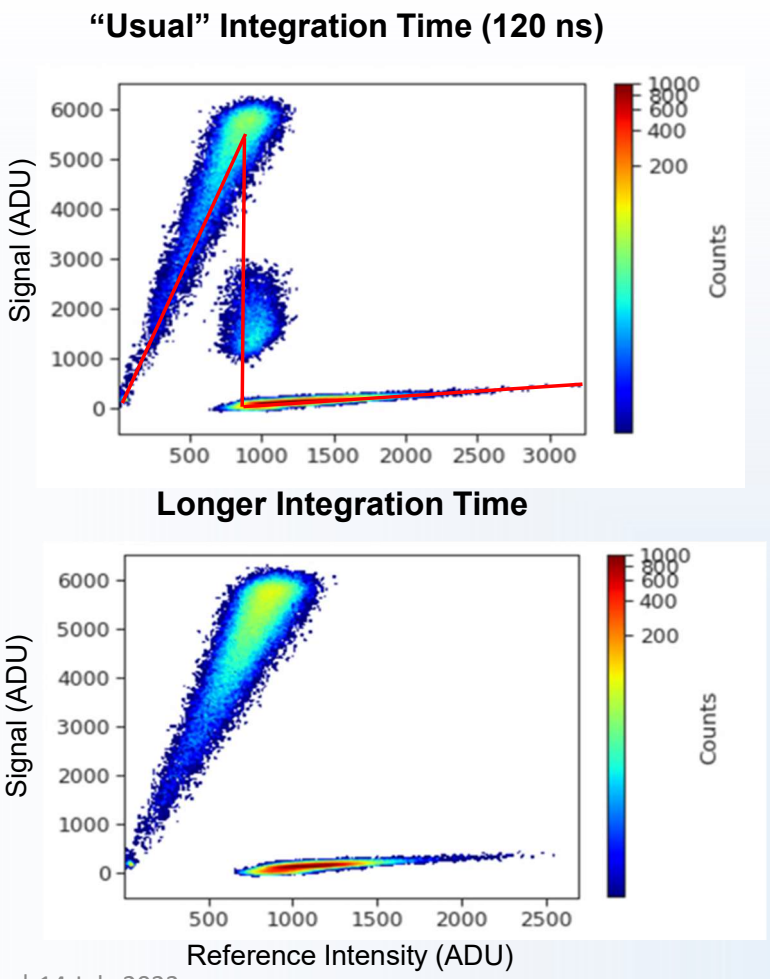
Solution:

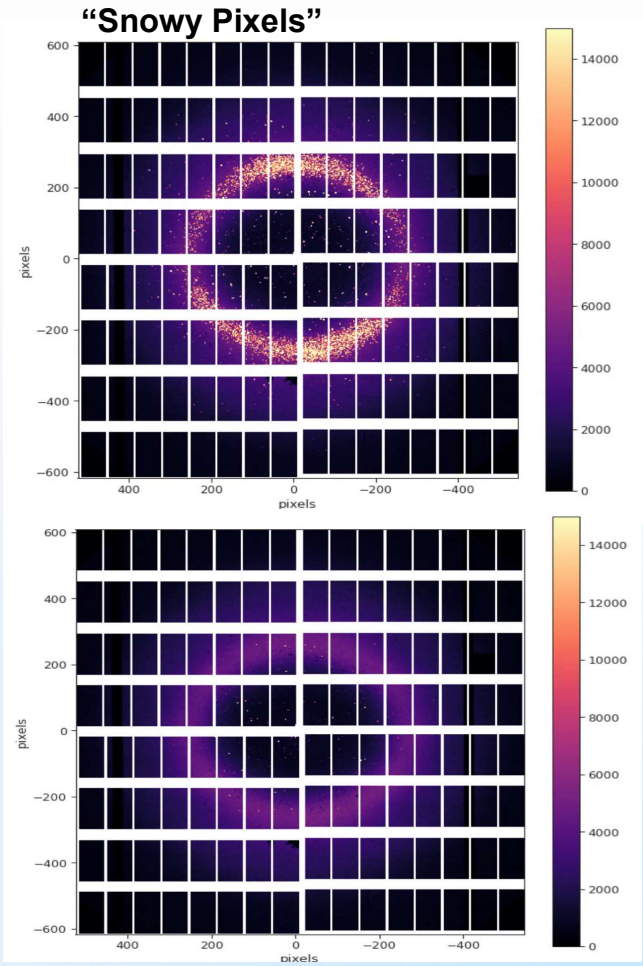
Dynamic Gain Switching – add a bigger feedback cap, if the small one is full

- **For risks and side effects, consult a detector expert or ASIC designer!**

Dynamic Gain Switching Side Effects: Late Gain Switching

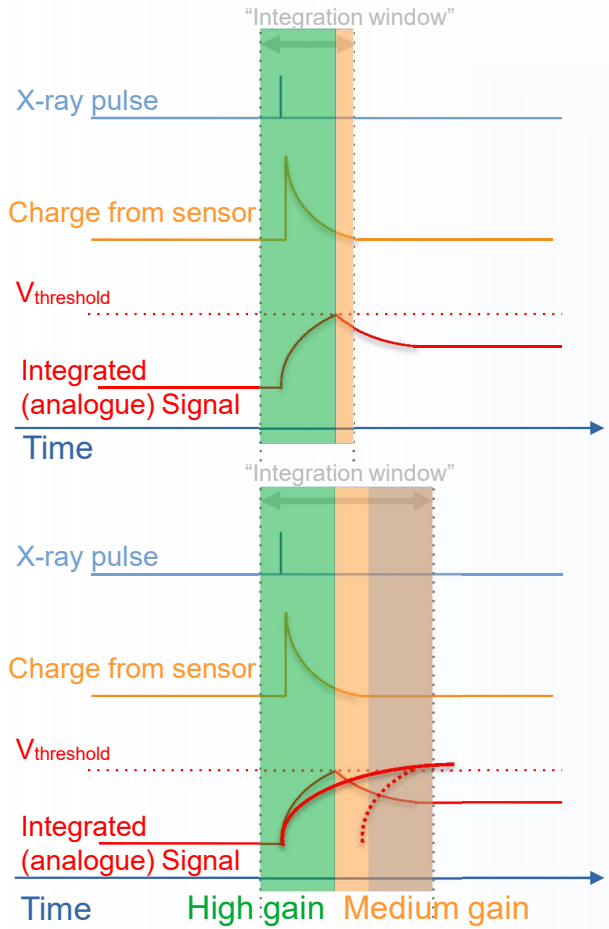


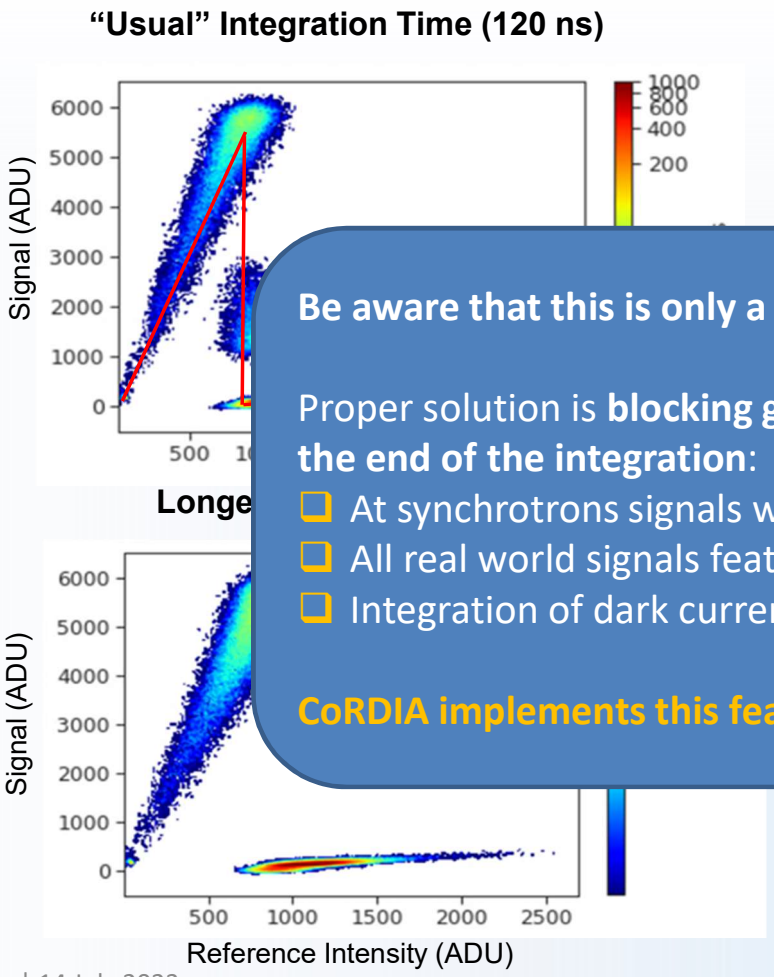


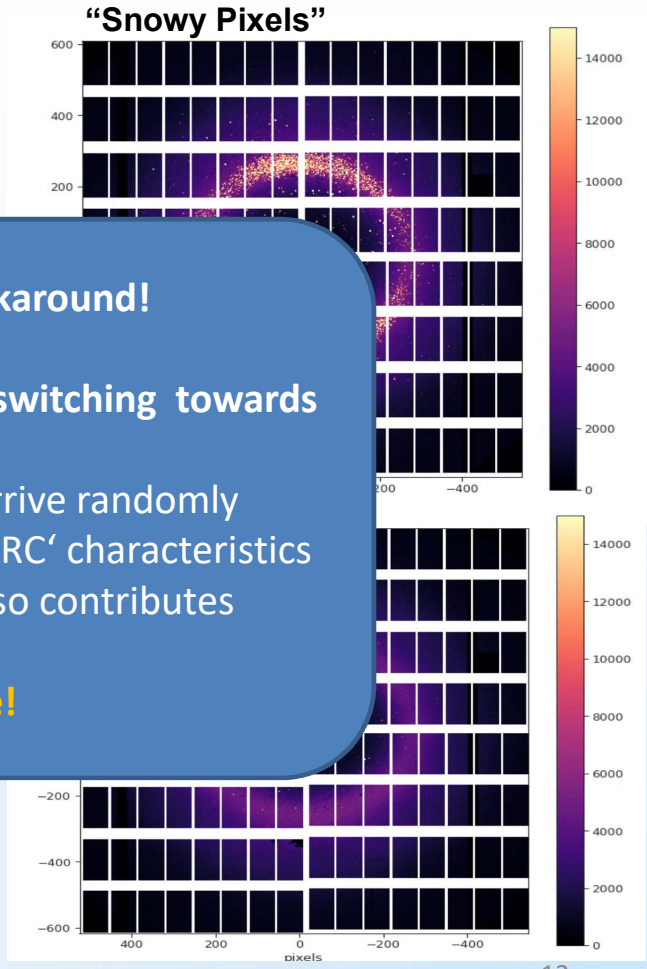


Figures courtesy of J. Sztuk-Dambietz (EuXFEL)

Dynamic Gain Switching Side Effects: Late Gain Switching







Be aware that this is only a workaround!

Proper solution is **blocking gain switching towards the end of the integration**:

- ❑ At synchrotrons signals will arrive randomly
- ❑ All real world signals feature ‚RC' characteristics
- ❑ Integration of dark current also contributes

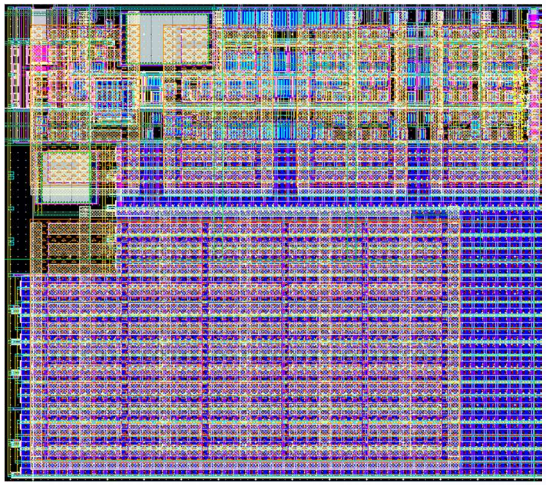
CoRDIA implements this feature!

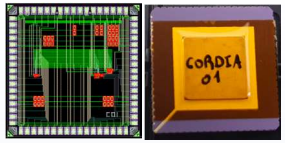
Figures courtesy of J. Sztuk-Dambietz (EuXFEL)

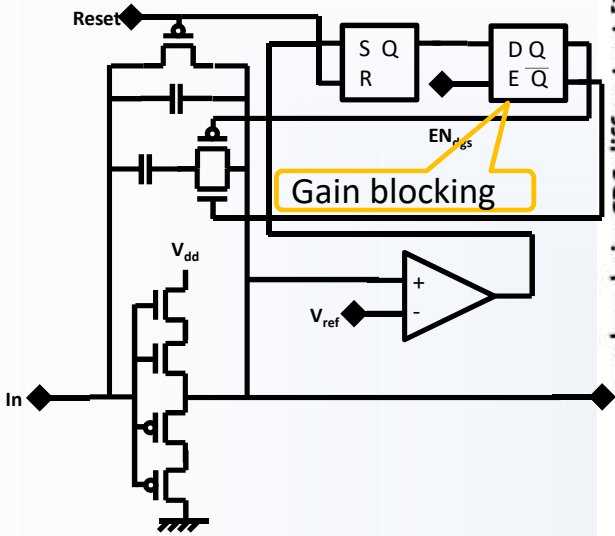
Preamp (CoRDIA 0.1)

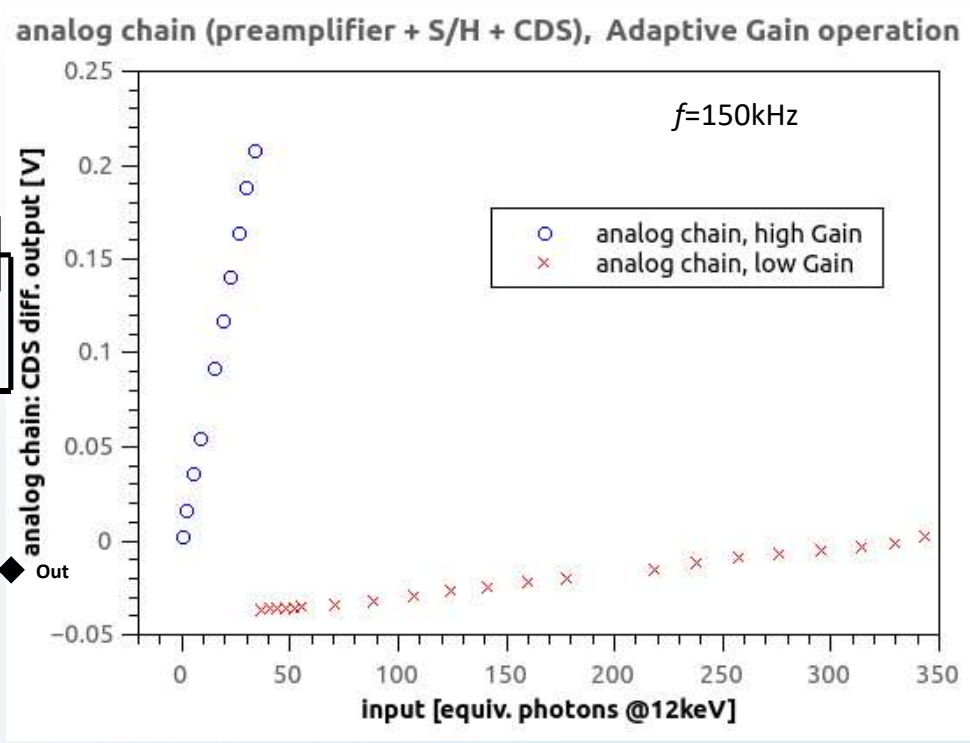
Adaptive gain architecture based on AGIPD

- 2 gains
- Core based on inverter stage
- ‘Std. cell grid’ layout









- Real estate not sufficient for a 10^4 photon FB cap
- Investigation of current dump and extrapolation (TuT) schemes ongoing

Preamp (CoRDIA 0.1)

Adaptive gain architecture based on AGIPD

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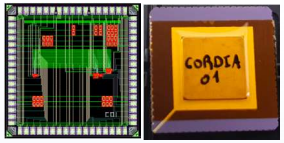
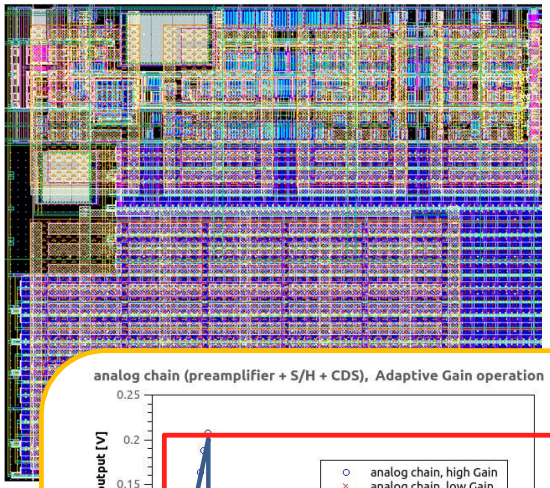
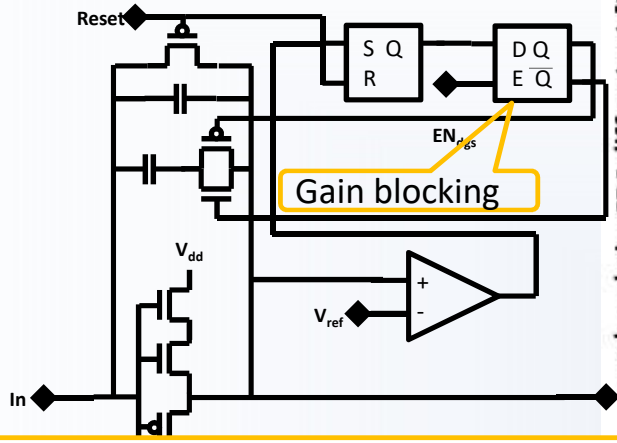
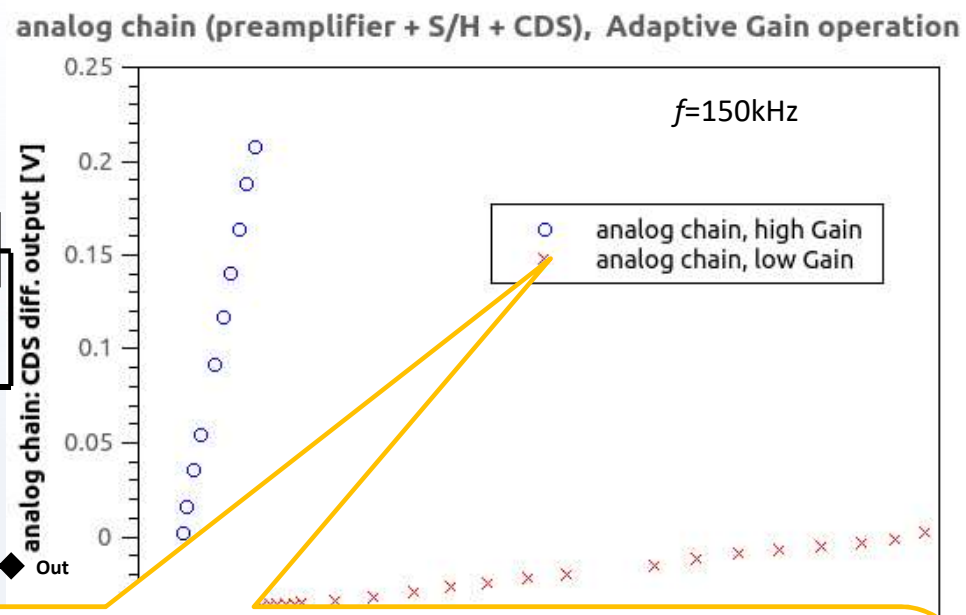
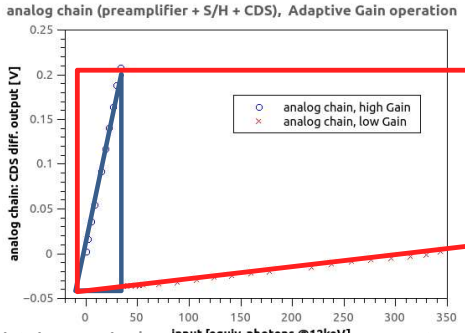




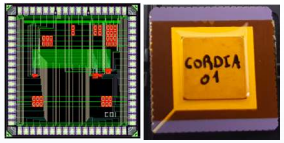






Extrapolation:
~2200 photons

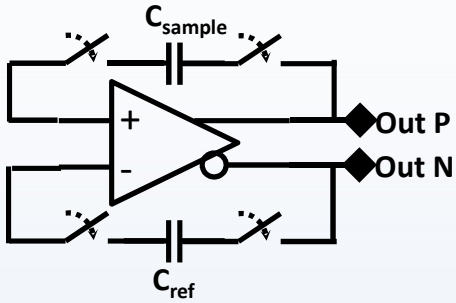
CDS – Correlated Double Sampling Stage



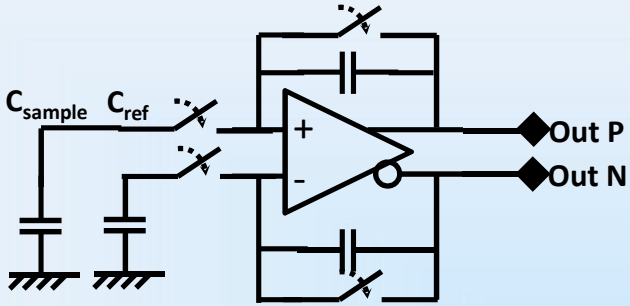
Based on a fully differential amplifier

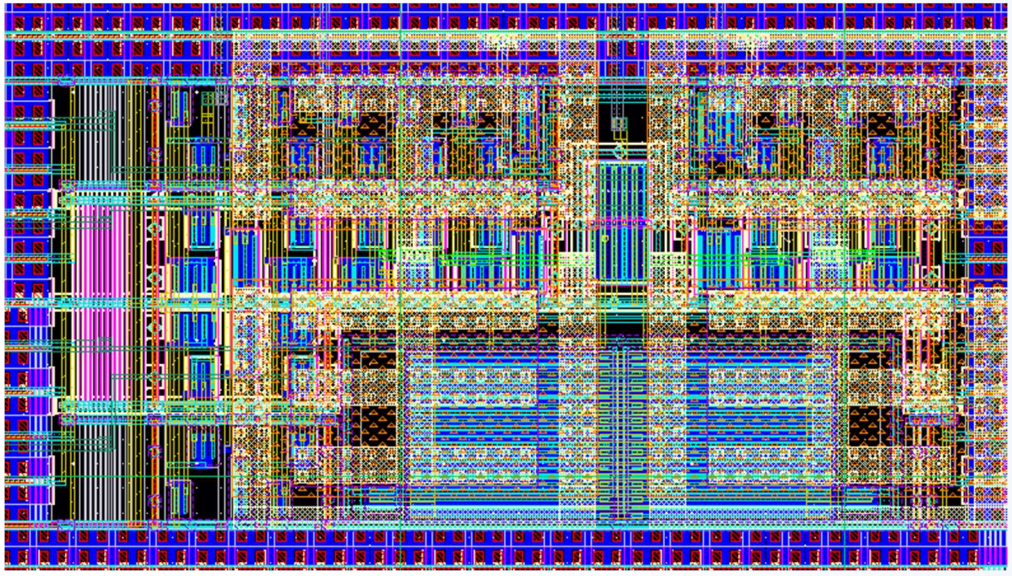
- Differential pair with simple CM feedback
- SC or continuous sampling (CS) mode
- 2 gains (in CS mode)

Switched Capacitor mode



Continuous Sampling mode

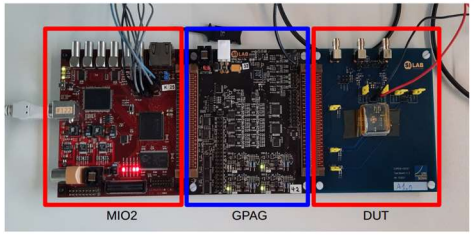


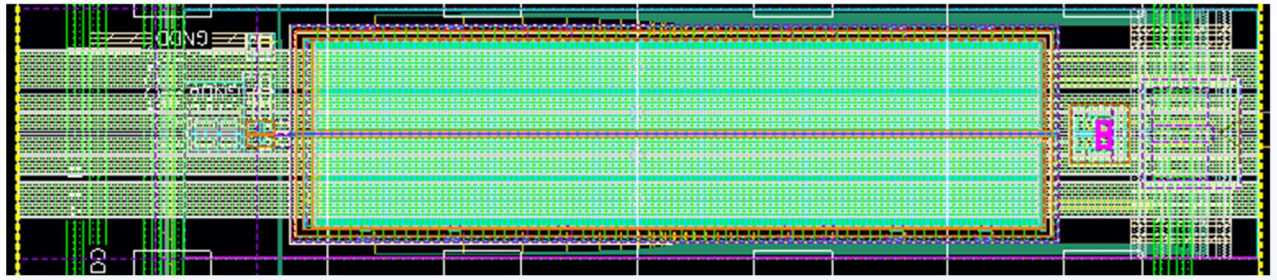


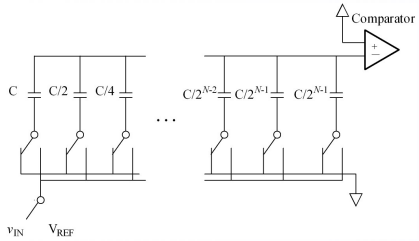
SAR ADC (HSI_ADC01)

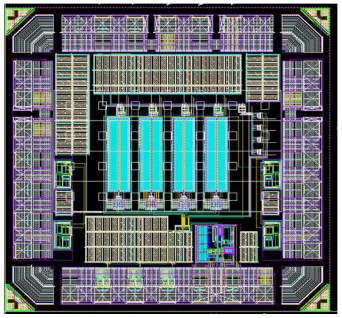
HSI_ADC01 contains 4 successive approximation register (SAR) ADCs

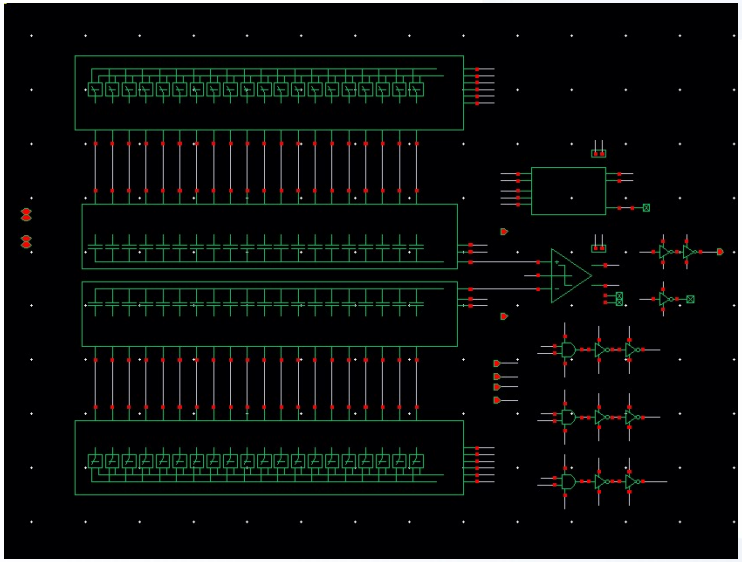
- Differential charge-redistribution type
- 11 bit
- ≥2.5 MSamples/s
- Serial data output
- ~10 ENOBs (best one)

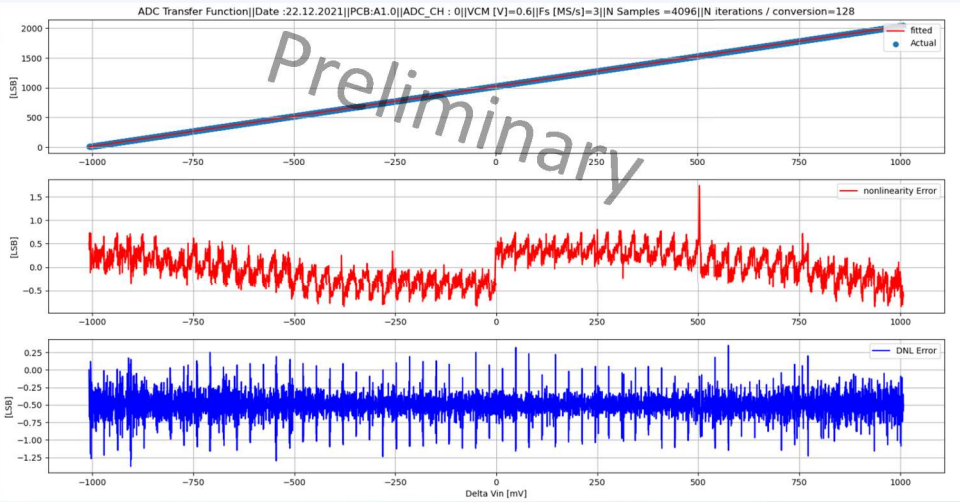






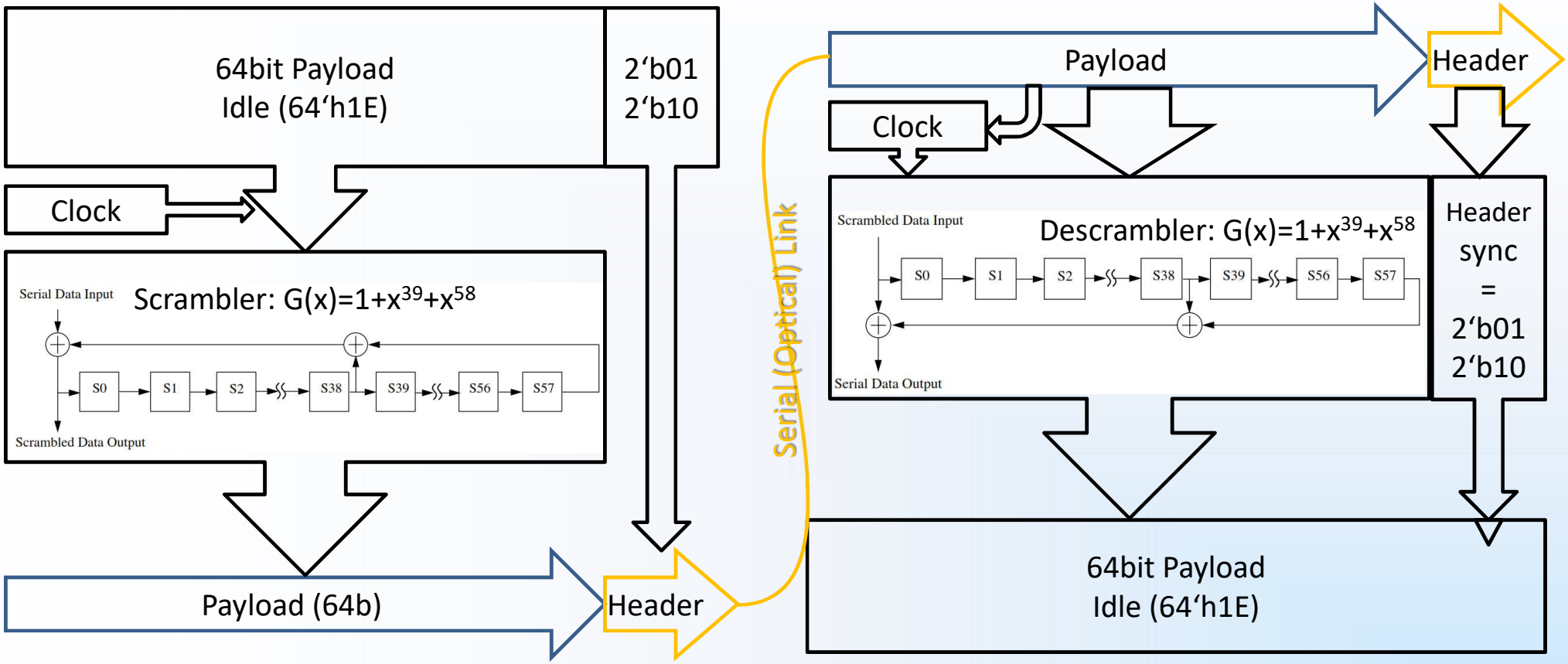






Nonlinearity (INL & DNL) ≤1 LSB => ~10 ENOBs

IEEE 802.3ae Gigabit Link in a Nutshell

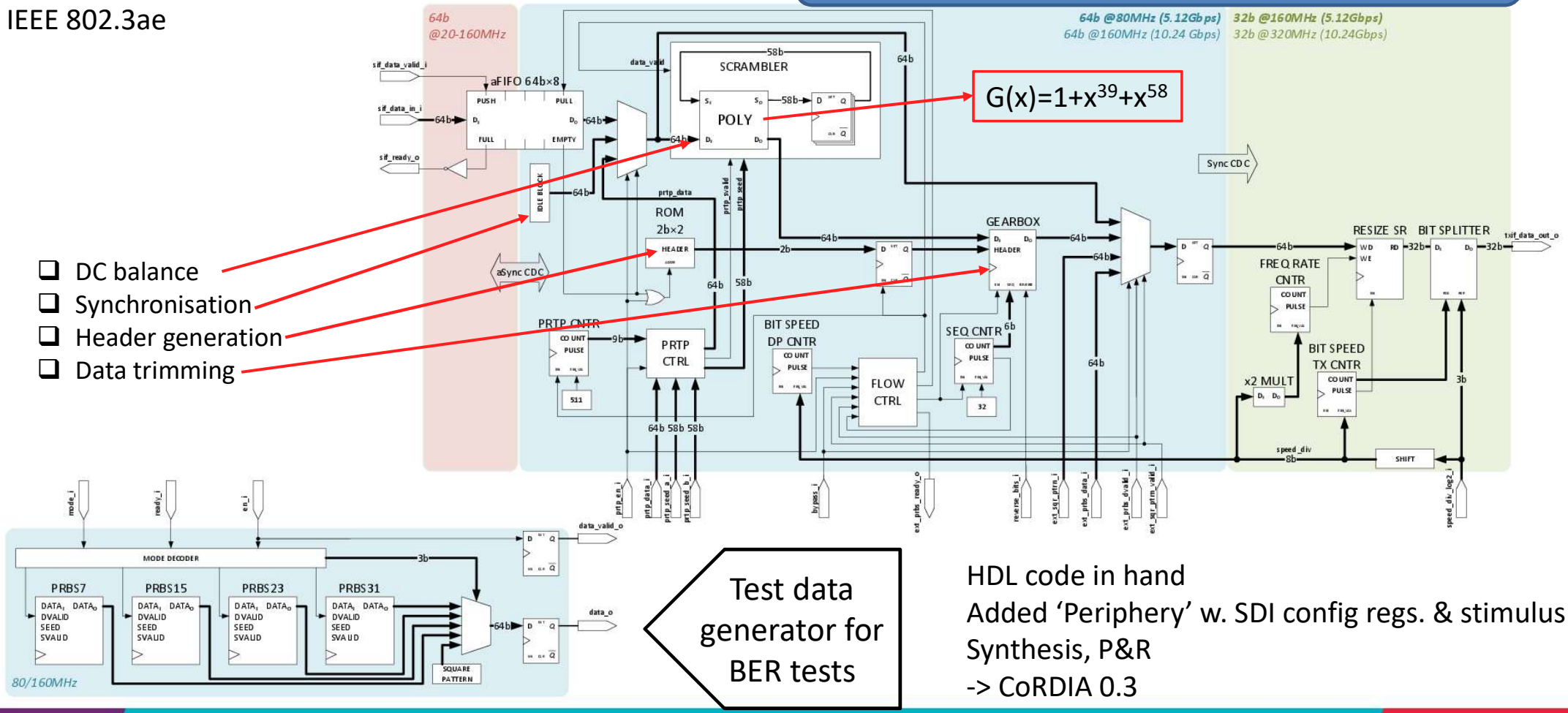


From Timepix4

PCS TX: BLOCK DIAGRAM

IEEE 802.3ae

Physical Coding Sublayer



- DC balance
- Synchronisation
- Header generation
- Data trimming

Test data generator for BER tests

HDL code in hand
Added ‘Periphery’ w. SDI config regs. & stimulus
Synthesis, P&R
-> CoRDIA 0.3

From Timepix4

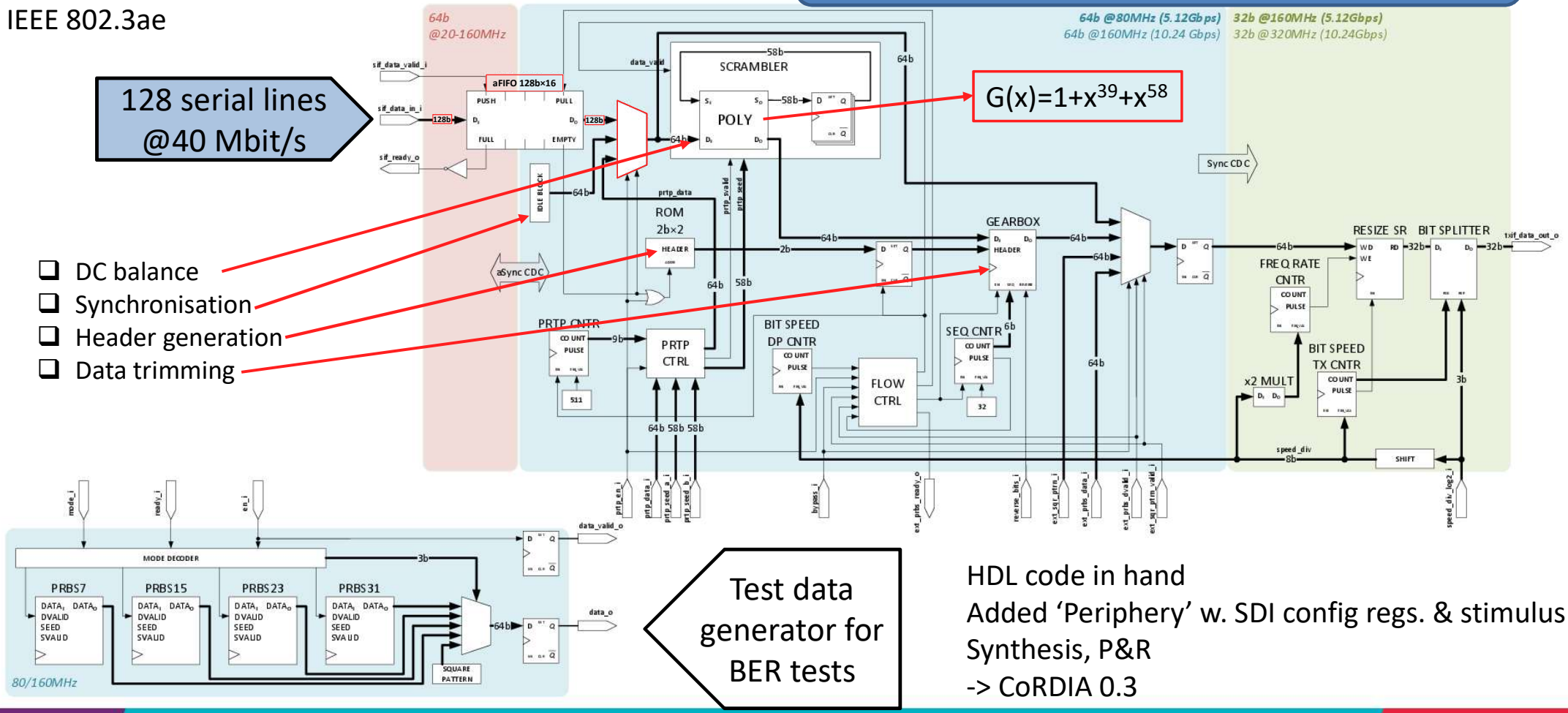
PCS TX: BLOCK DIAGRAM

IEEE 802.3ae

Physical Coding Sublayer

128 serial lines @40 Mbit/s

- DC balance
- Synchronisation
- Header generation
- Data trimming



Test data generator for BER tests

HDL code in hand
Added ‘Periphery’ w. SDI config regs. & stimulus
Synthesis, P&R
-> CoRDIA 0.3

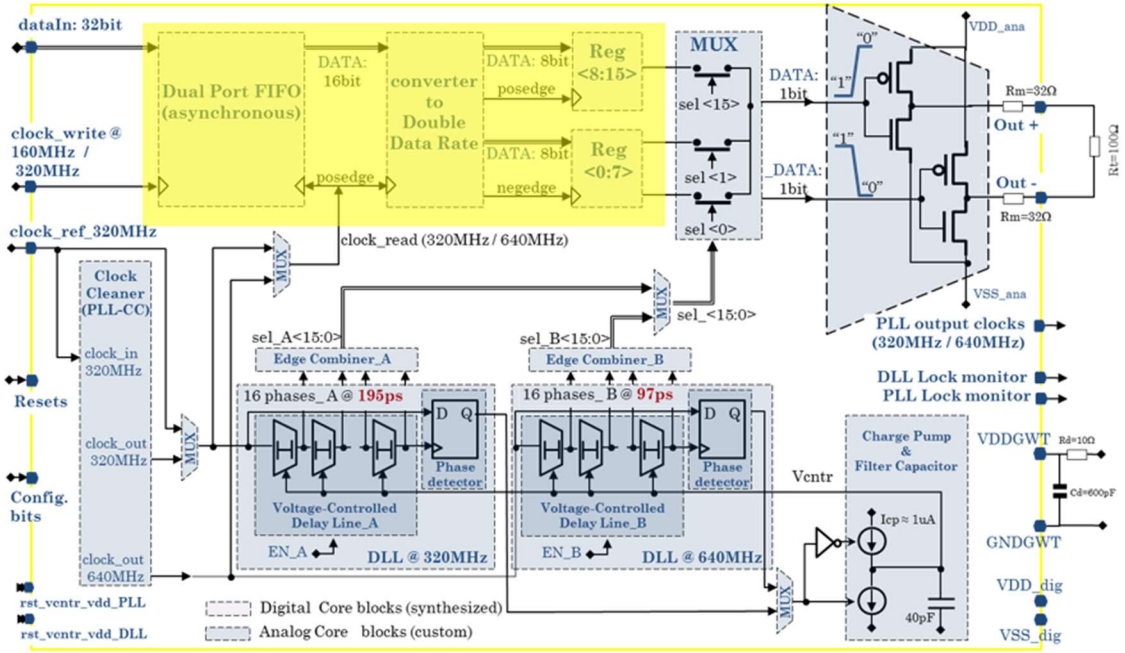
GWT – Gigabit Wire Transmitter

From Timepix4

Consists of a PLL & a 32 to 1 serializer/mux

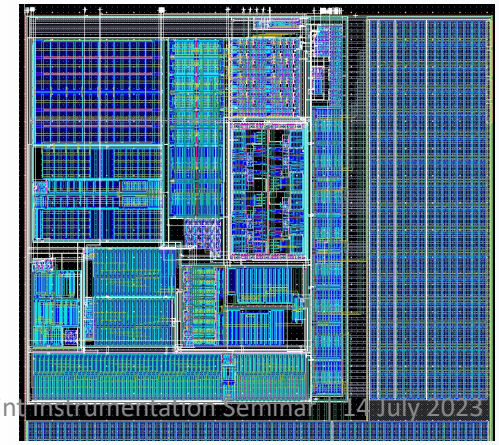
- PLL
- 320MHz or 640MHz
- 86 µm x 120 µm
- Serializer/mux
- 5.12 Gbit/s or 10.24 Gbit/s
- Individual DLLs for either speed
- Differential (100 Ω) off-chip driver
- 86 µm x 67 µm

Developed by
Vladimir Gromov (NIKHEF)

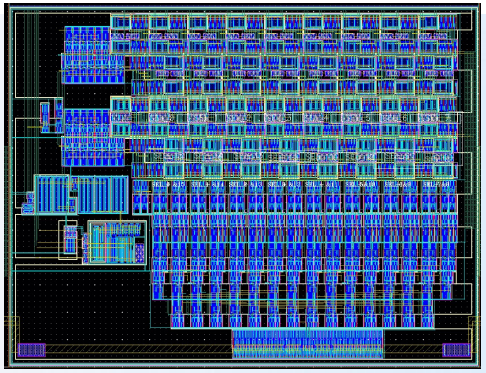


Schematics by Vladimir Gromov (NIKHEF)

PLL



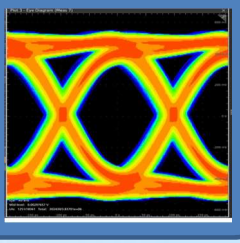
Serializer



-> CoRDIA 0.3

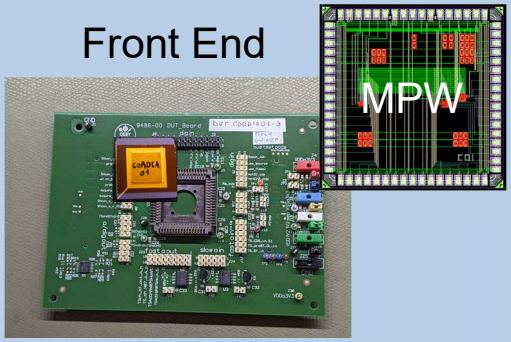
Timepix4 GWT @5 Gbit/s

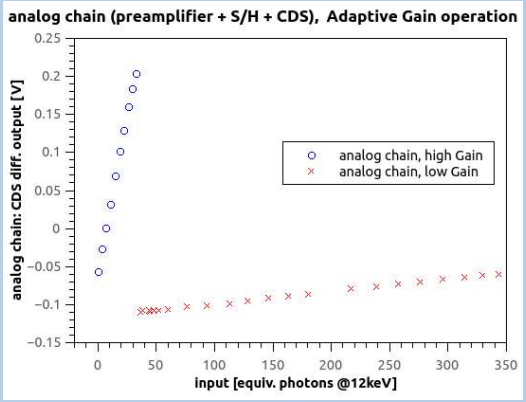
X. Llopart,
On behalf of the Medipix4 Collaboration
11 th February 2022
CERN seminar



Putting togeter the Ingredients…

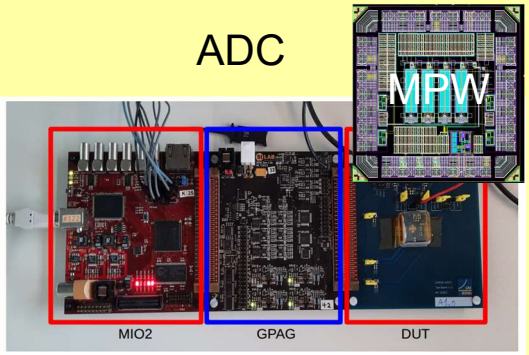
Front End

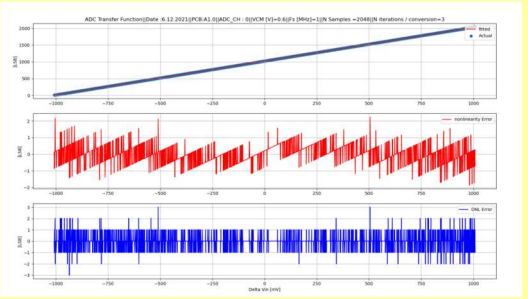




Adaptive Gain circuit tested by calibr. source (pulsed capacitor) @ expected frame rate

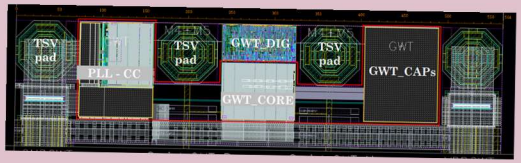
ADC



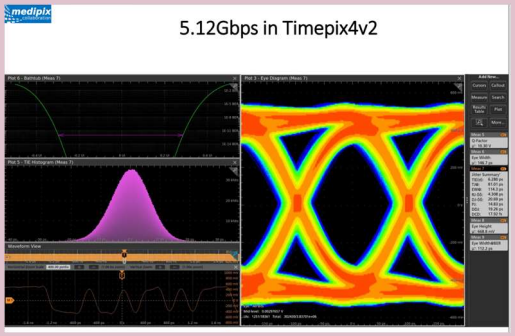


11-bit SAR developed, tested by UniBonn. DNL , INL test suggests >10ENOBs @ expected frame rate

PCS+GWT

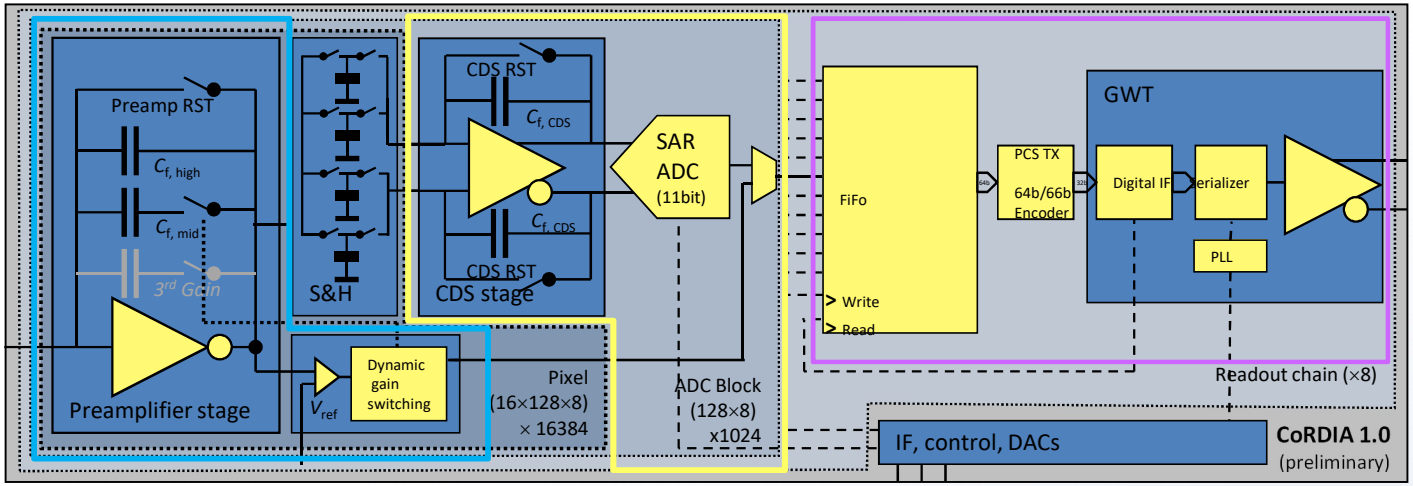


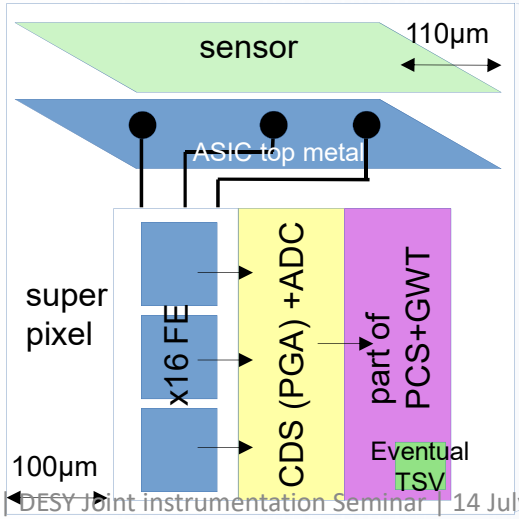
lazy-person approach: reuse Timepix4 solution

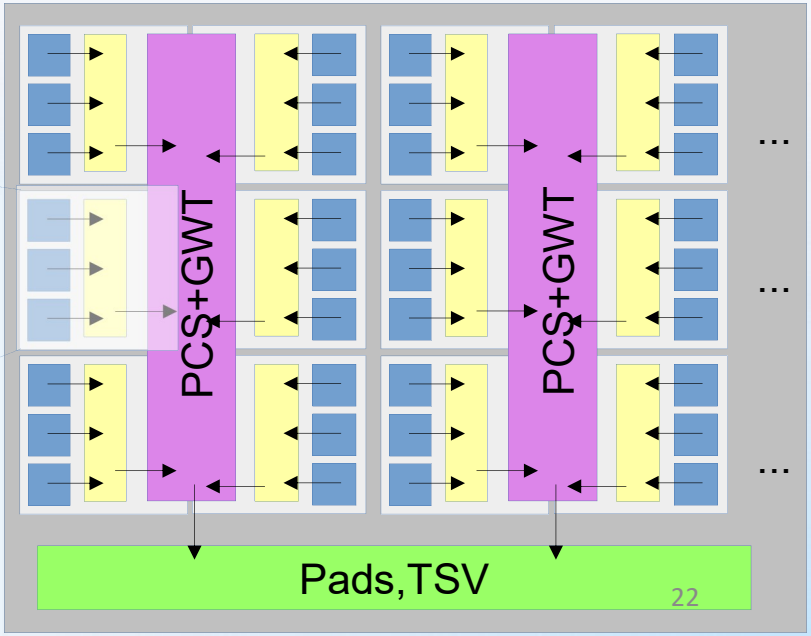


NIKHEF & Timepix collab.: good eye diagram @ 5.12 Gb/s. (possible to extend to 10.24 Gb/s, but wire/bump bonding limits)

…into Superpixels

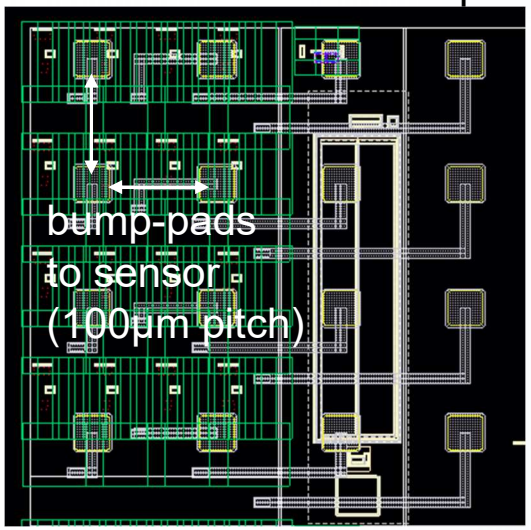


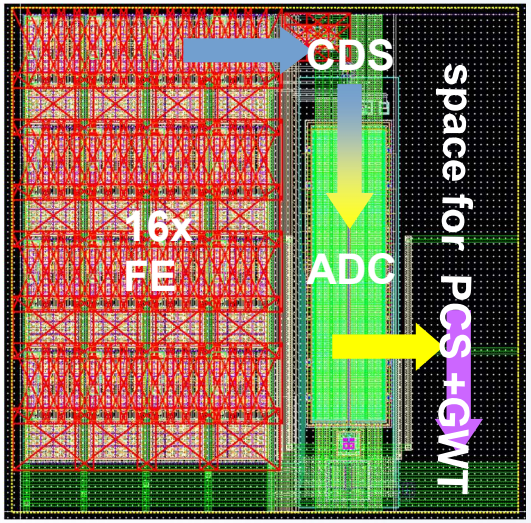


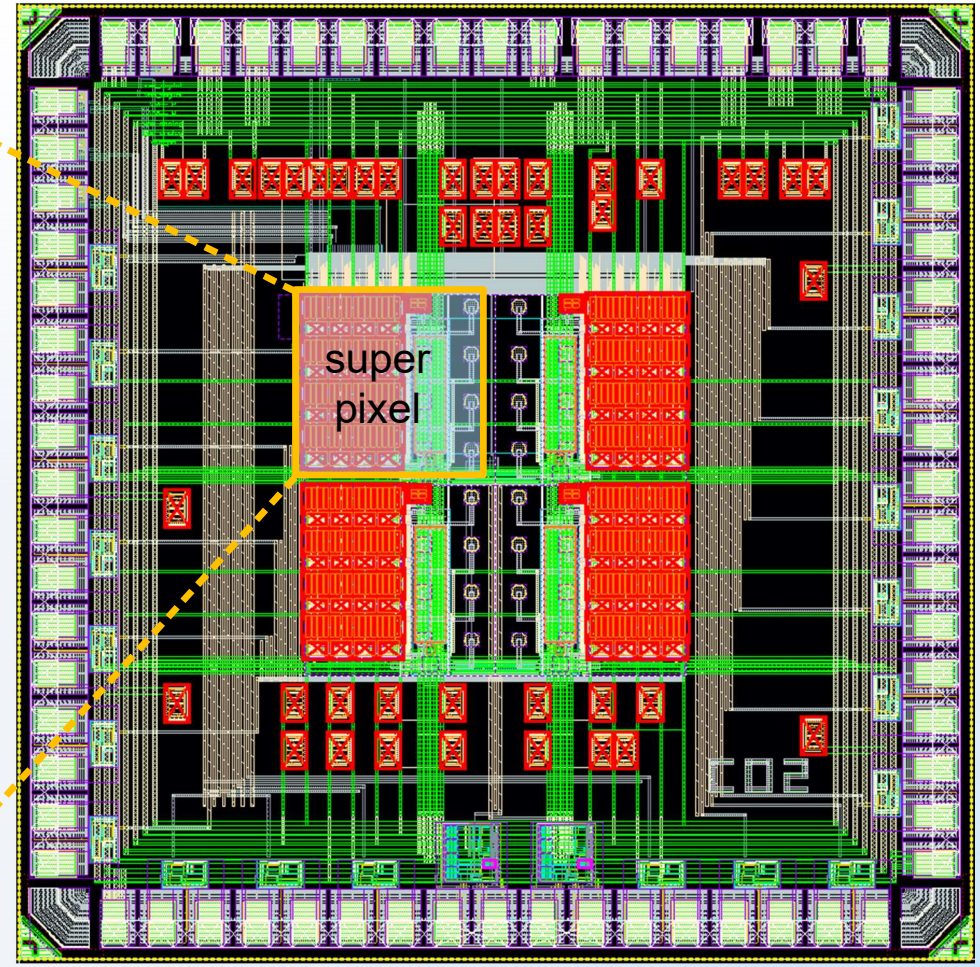


CoRDIA 0.2

Pad redistribution on top metal

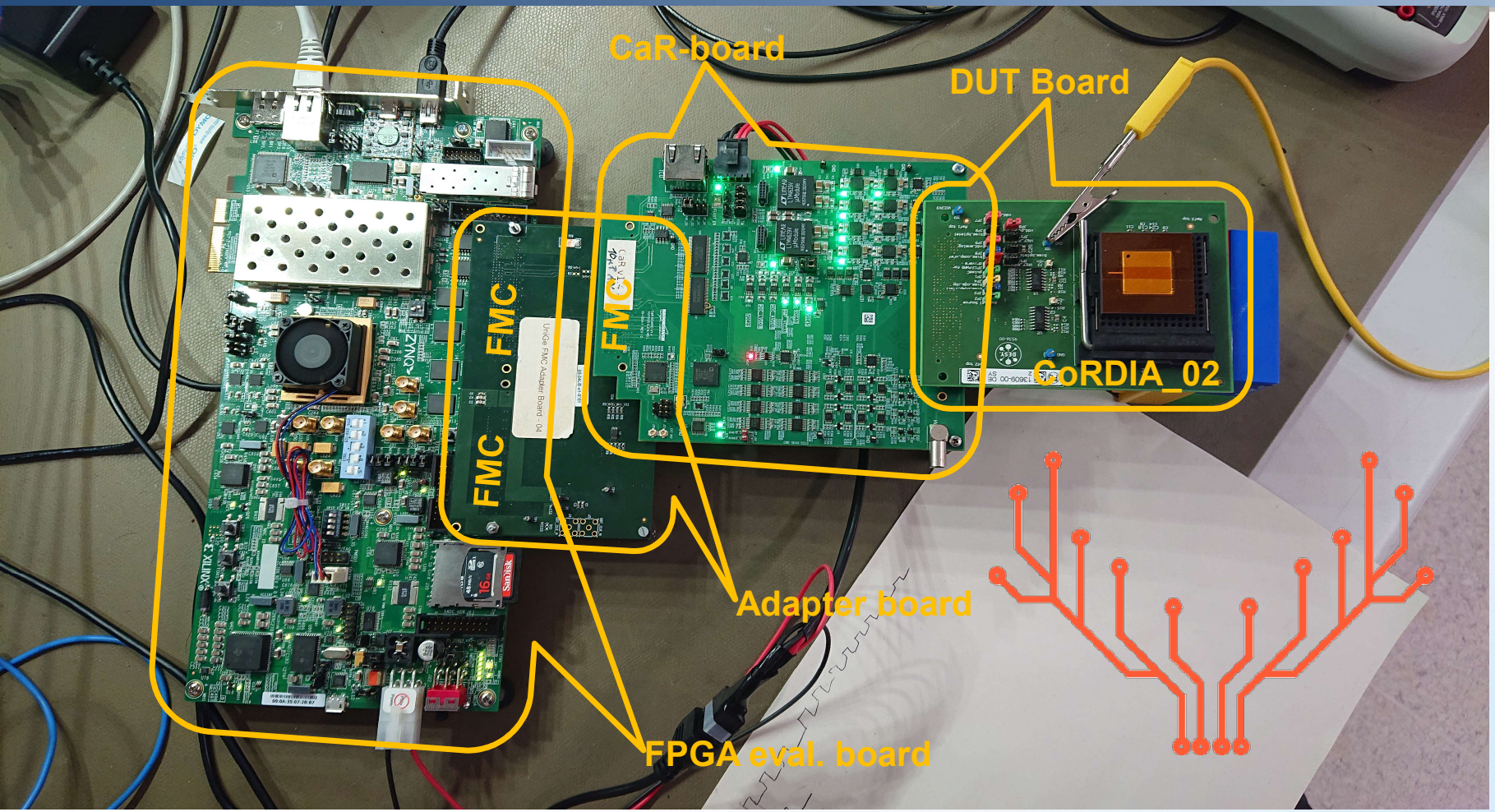






Silicon in hand since June 2023

Chip Test Environment



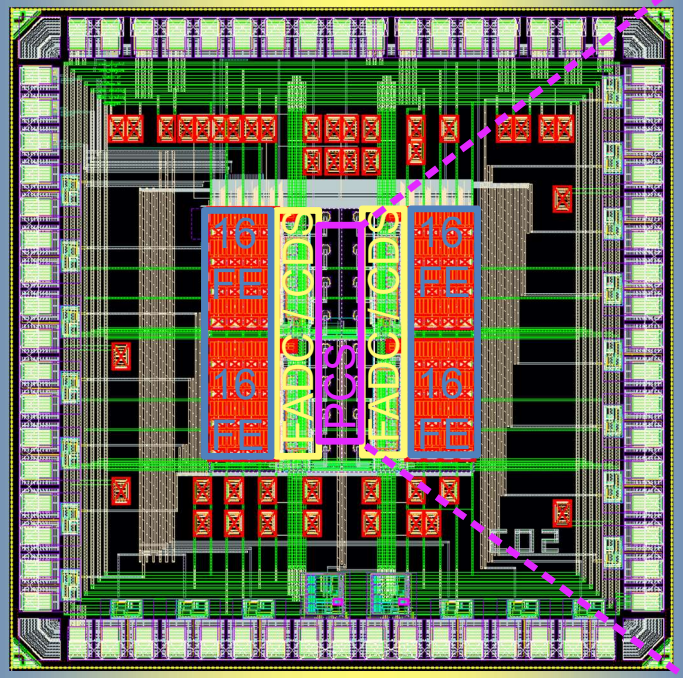
For chip testing we use a Caribou DAQ system developed by

- Brookhaven Nat. Lab
- Université de Genève
- CERN
- DESY

It uses an FPGA evaluation board with embedded Linux (Poky) and comes with DAQ software (Peary)

CoRDIA 0.3

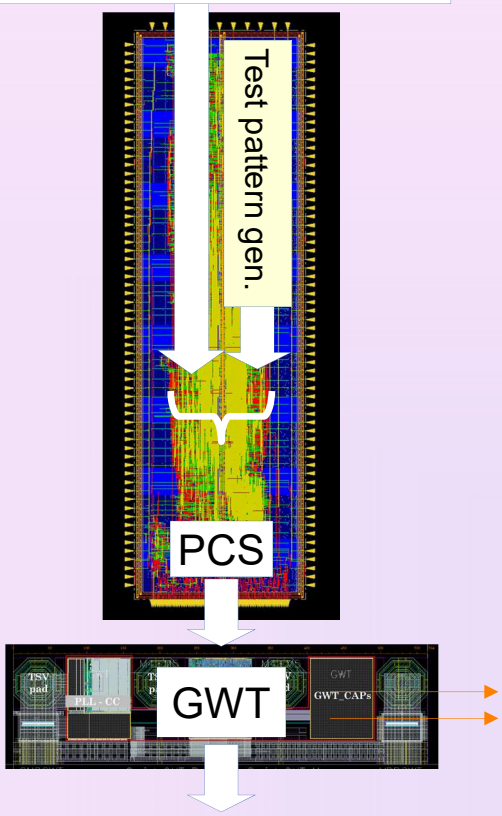
CoRDIA 0.2 (FE+FADC) Test Chip



Received 1st week of June
Just started testing

CoRDIA 0.3 (PCS+GWT) Test Chip

Data injection structure



- PCS (adapted to our design)
- GWT
- Peripherial structures
  - SDI configuration registers
  - Test pattern generator

expected submission on MPW
mid-September

debug
outputs

CoRDIA Development Roadmap

Test hardware

Cordia Chip Tester Board (CCTB) delayed due to excessive lead & mfg. times

Instead we adopted the Caribou DAQ system

Development based on a staged 'bottom up' approach

- FE &
- ADC components exist
- Gbit readout under development/implementation
- Individual chip size under discussion
- Target dynamic range needs a new approch
  - Not enough real estate for a big FB cap
  - Ideas exist
- First detectors ready for the start of PETRA IV

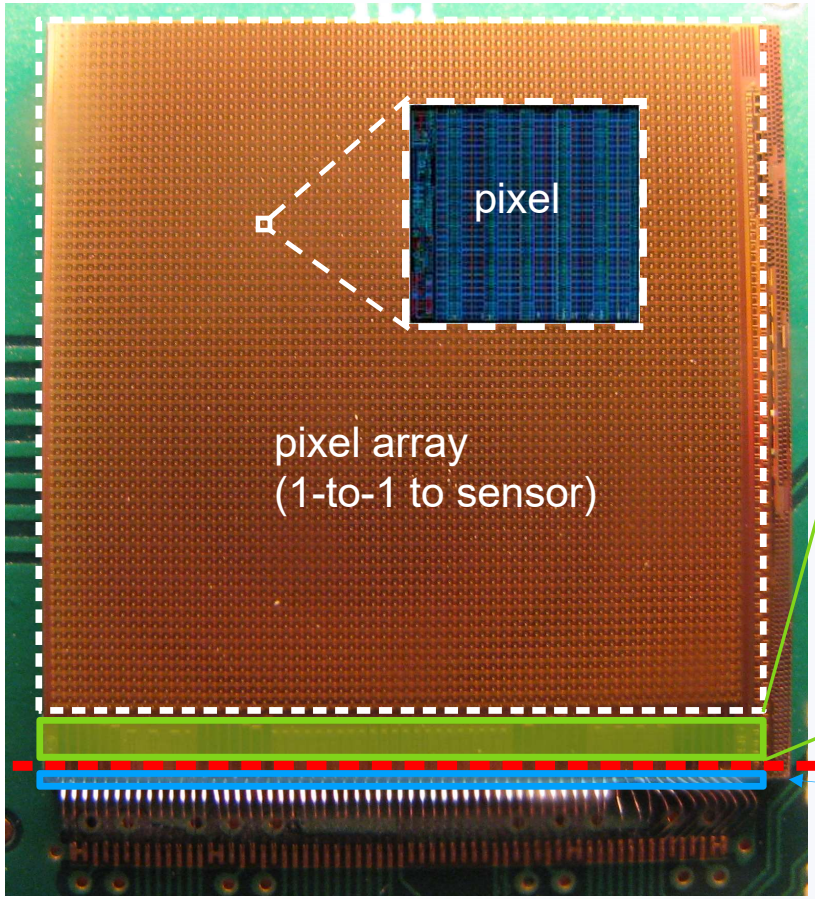
~2027
CW readout
≥150kHz

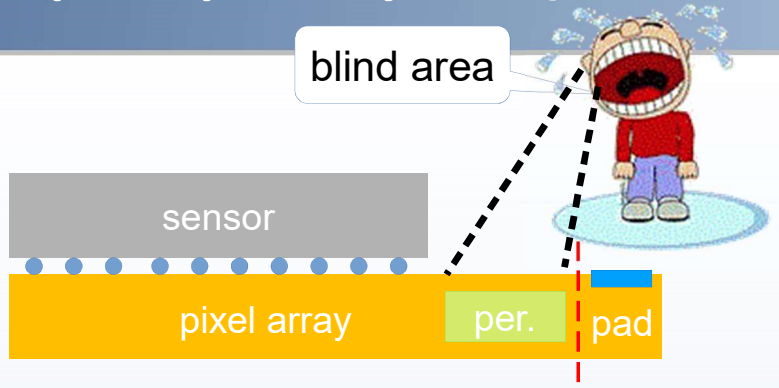
Detector systems for PETRA IV (in ambient)

>2027
Improved analogue performance (DR, noise)

Detector systems for CW XFEL (in vacuum), Systems with high-Z and LGAD sensors

4-Side Buttability - Hidden periphery request





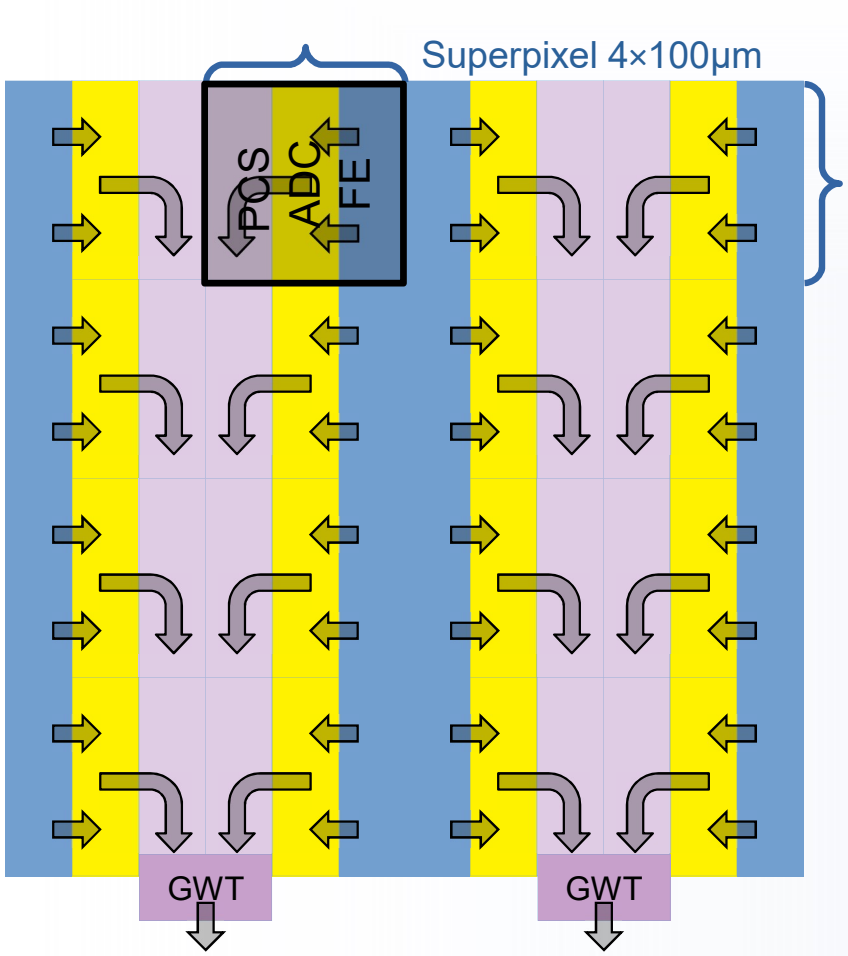
"Periphery"

C&C interface (= sequencer)
configuration registers (= SDI)

NOT covered by sensor → makes the system intrinsically non-4-sides-buttable

wirebond pads
(can be diced off if TSV)

Increasing the Pixel Size to 110µm

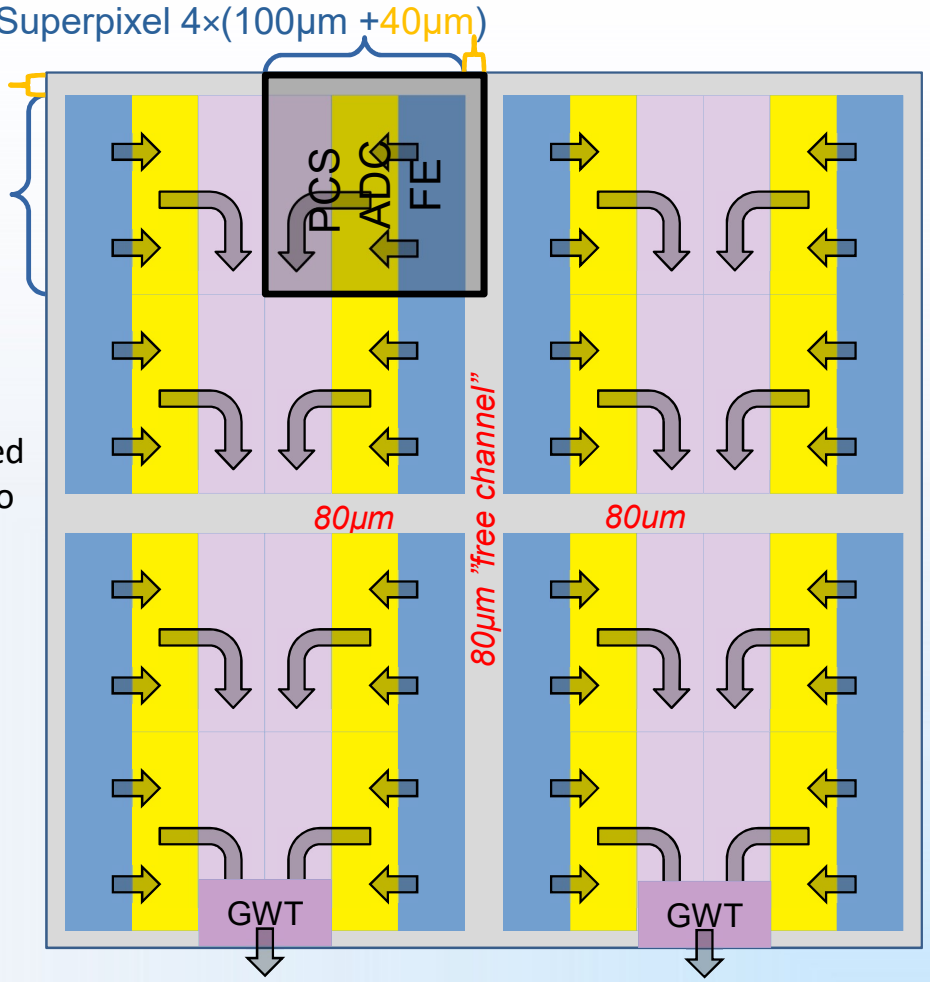


To profit from advanced sensor developments for Medipix/Timpix we decided to increase the pixel size to 100µm

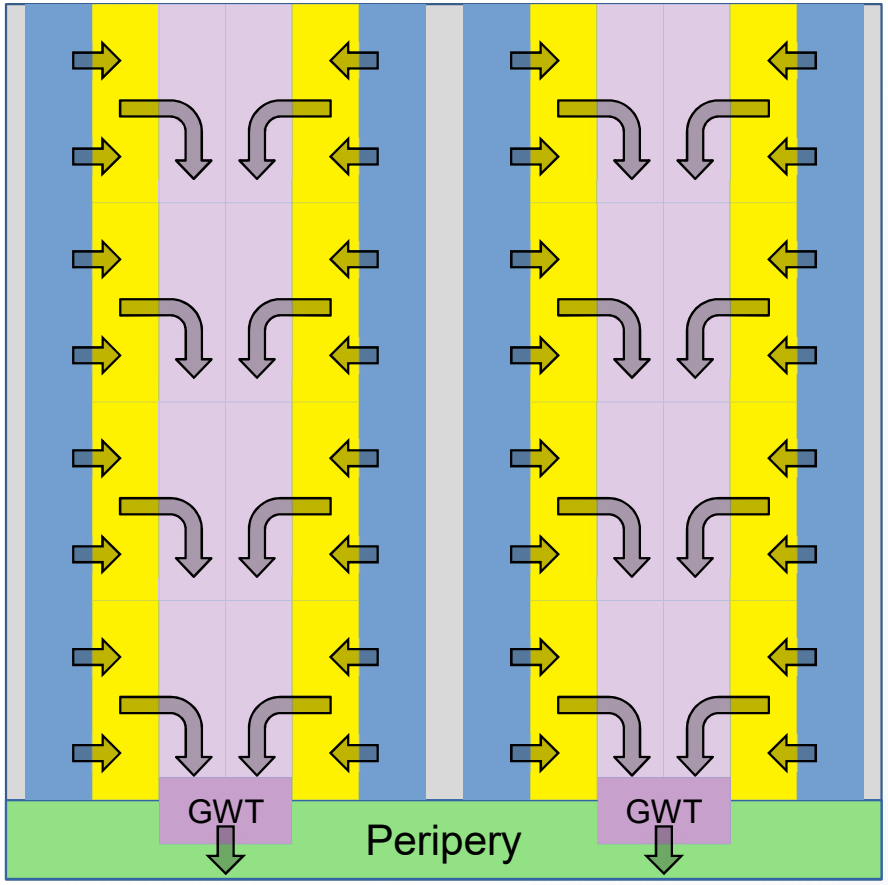
- +40µm per 'superpixel'

Space for

- Bias structures
- Hidden periphery
- Hidden GWTs



Two options for a Hidden Periphery

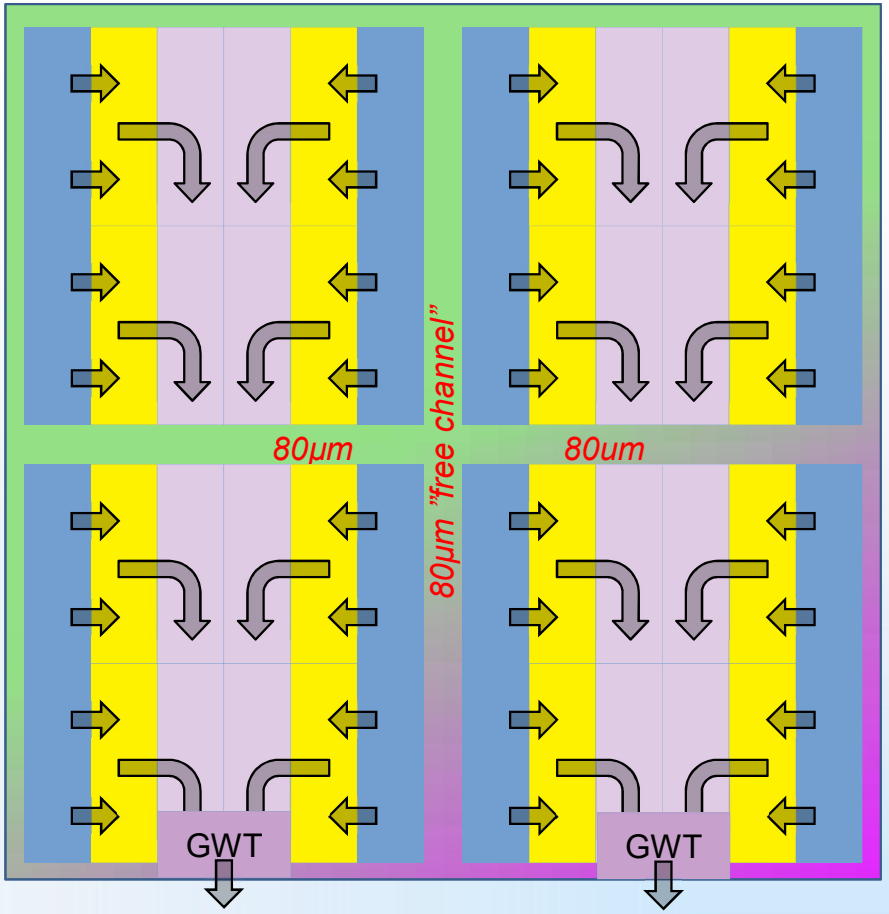


Timpix4 option

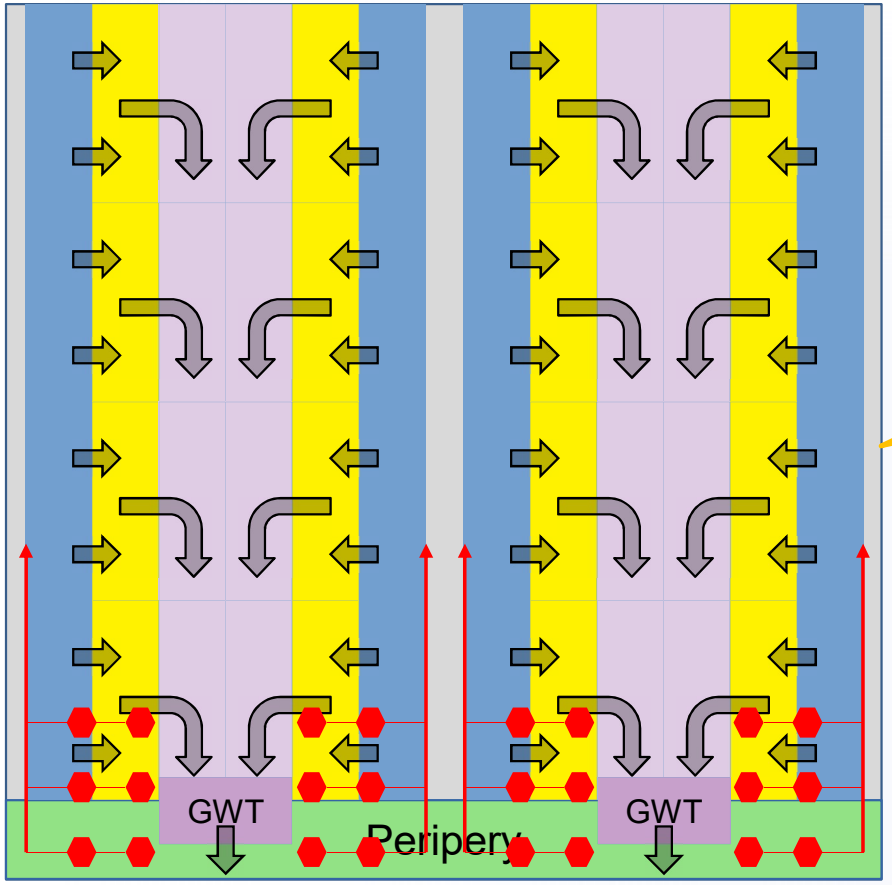
- Compact superpixel matrix
- Dedicated periphery
- Structure hidden under top layer

2nd Option

- Distributed periphery

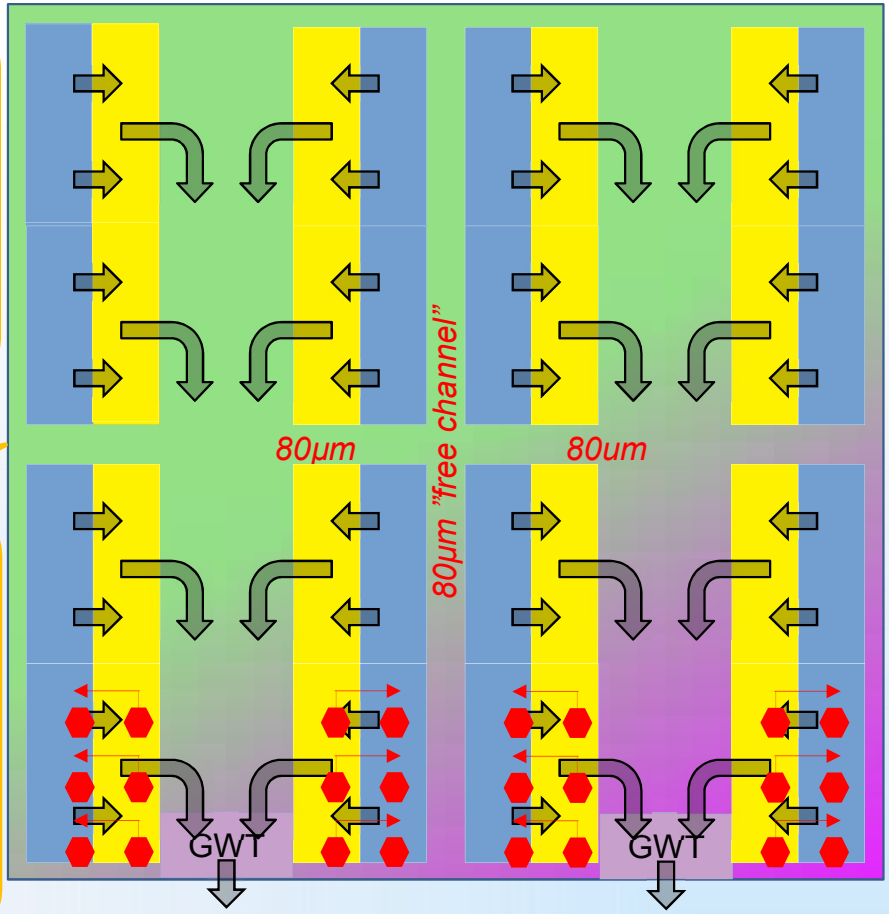


Two options for a Hidden Periphery

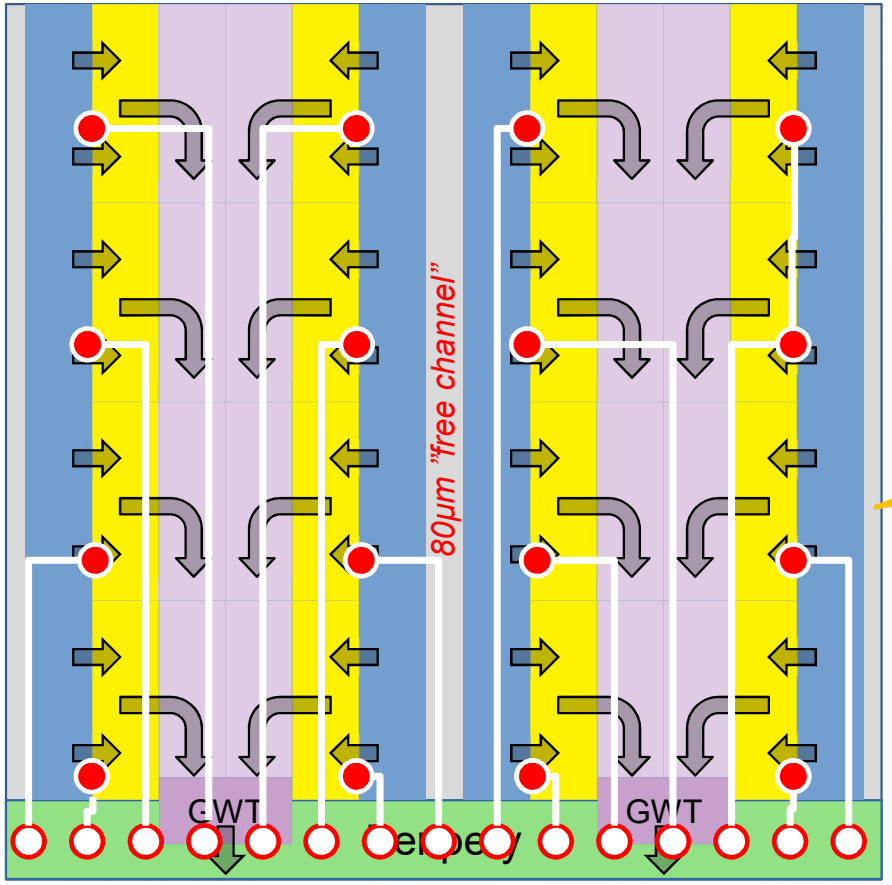


Hidden periphery
- Fanout to sensor bump-bonds
- Analog nightmare
- Many, thin, long, densely packed, analog lines (--)
- Works in TimePix4 (+)

Distributed periphery
- Mixed with the PCS design
- Pixels are analog islands in a digital sea
- Digital design neither modular nor repeatable (--)
- Only local analogue routing (++)



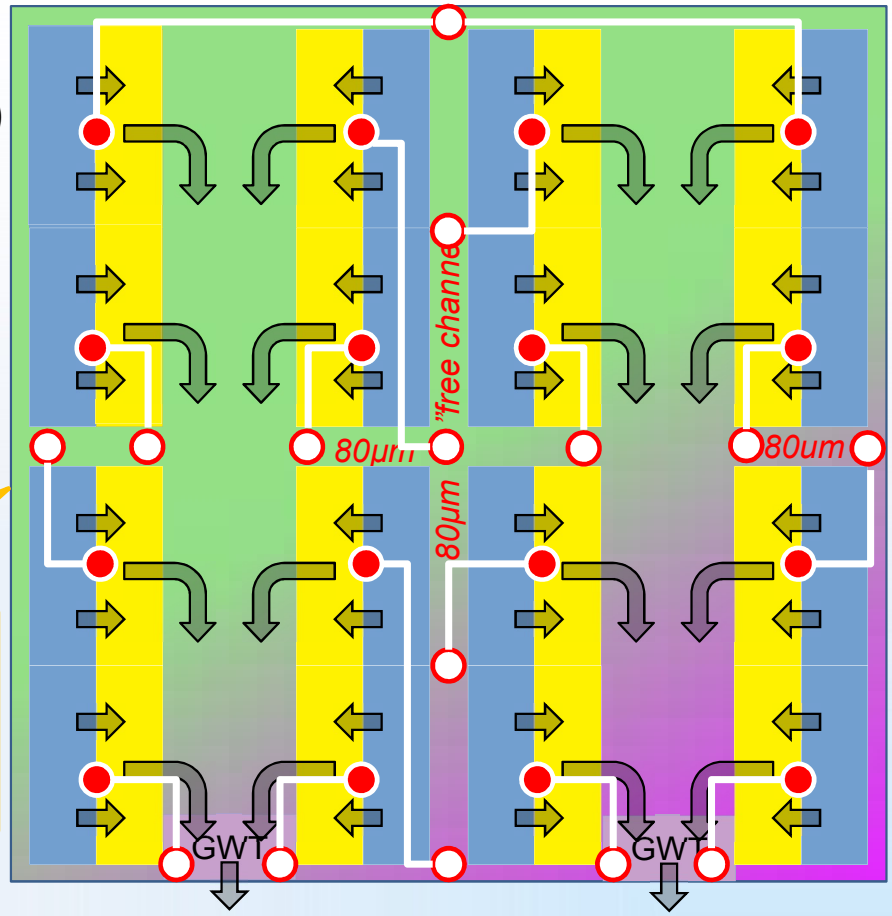
And how about TSVs…



- RDL bump pad
- Thru-Silicon-Via (TSV)

Hidden periphery
- ❑ TSVs in a row
- ❑ Complex RDL
- ❑ Power grid same as for WB chip
- ❑ Additional impedance of RDL

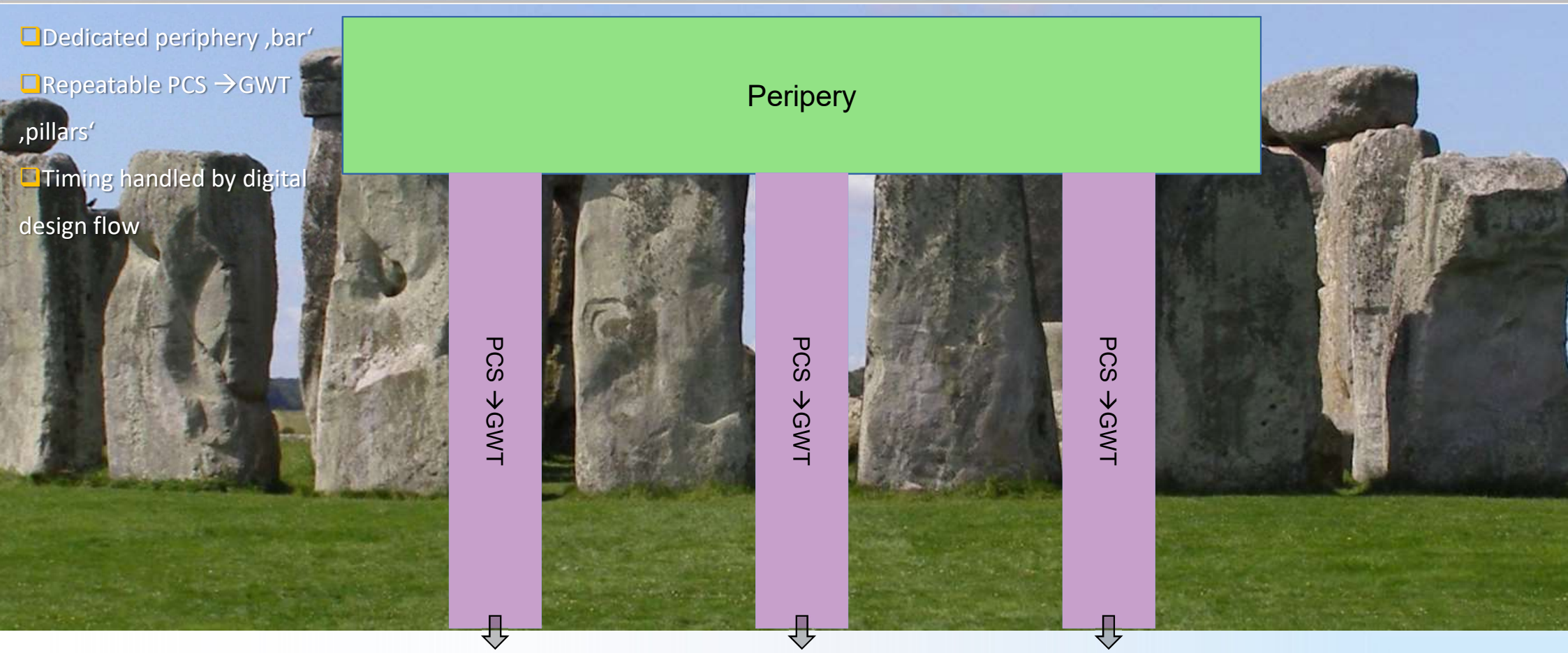
Distributed periphery
- ❑ Distributed TSVs
- ❑ Simple RDL (if at all)
- ❑ Power Grid ‘supported’ by TSV ‘local supplies’



An Old Approach to Using Silicon

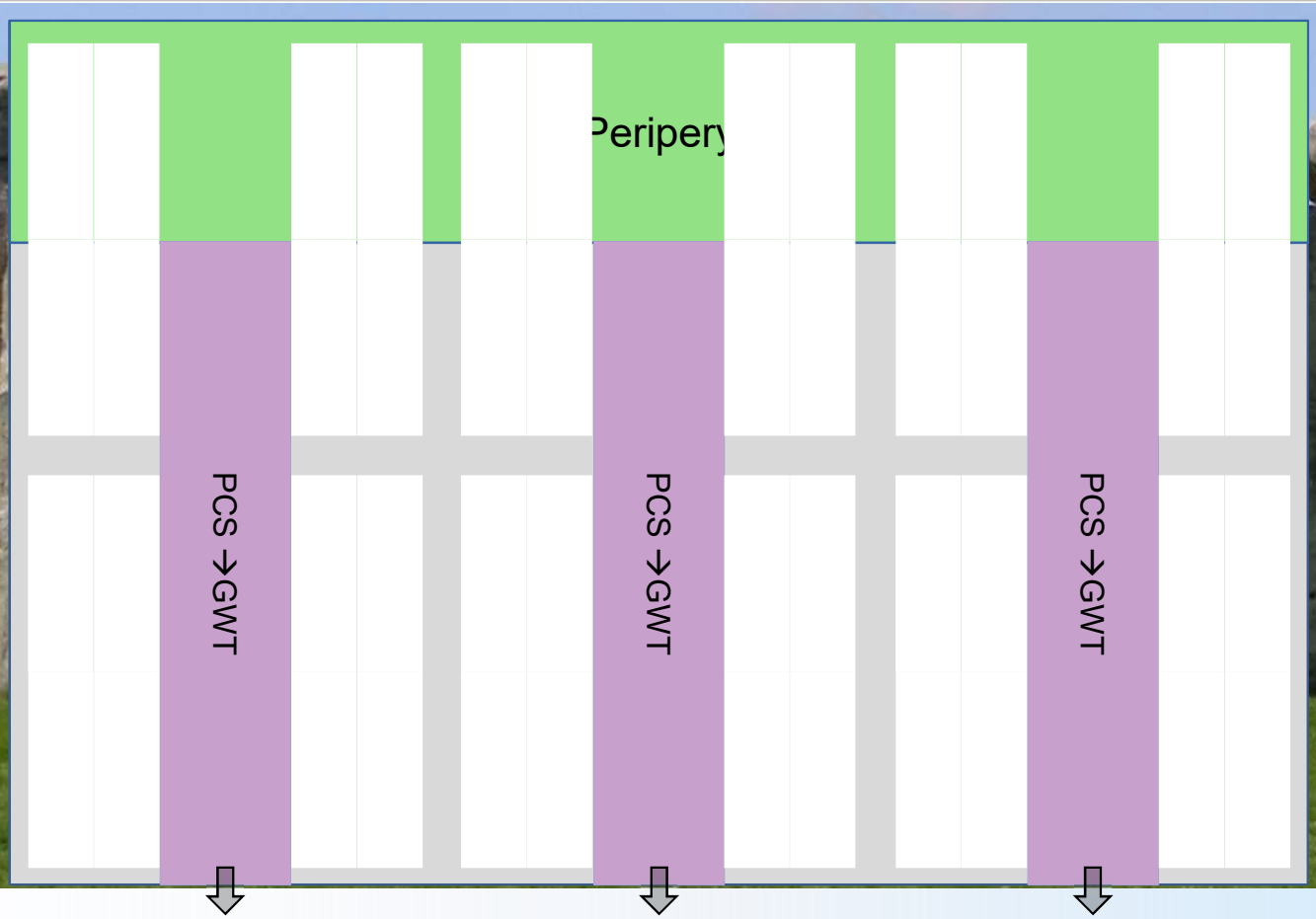
An Old Approach to Using Silicon

- Dedicated periphery ‚bar'
- Repeatable PCS →GWT ‚pillars'
- Timing handled by digital design flow



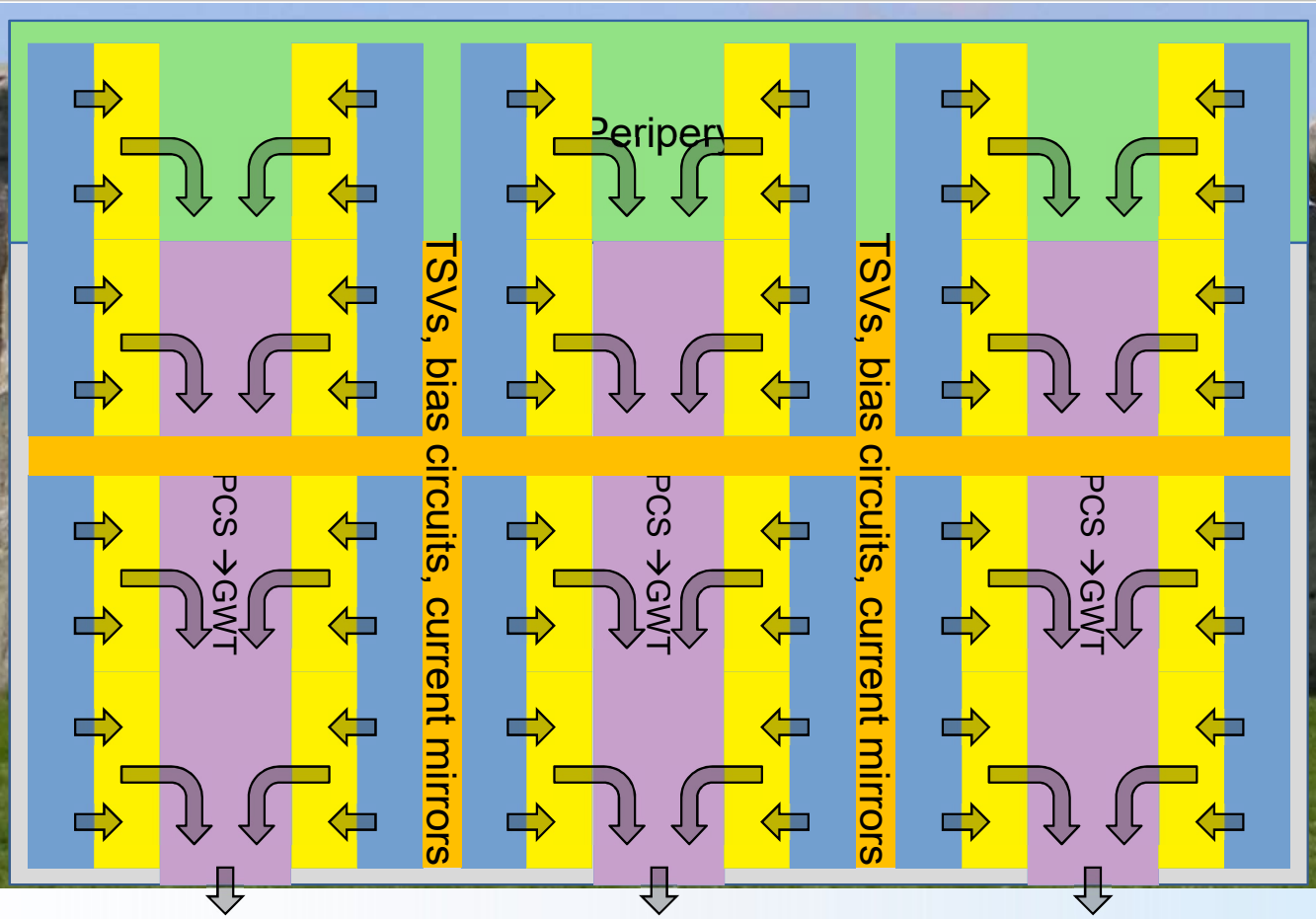
An Elaborate Approach to a Hidden Periphery

- Dedicated periphery ‚bar'
- Repeatable PCS →GWT ‚pillars'
- Timing handled by digital design flow
- Superpixels as analogue islands (i.e. abstracts in digital flow)

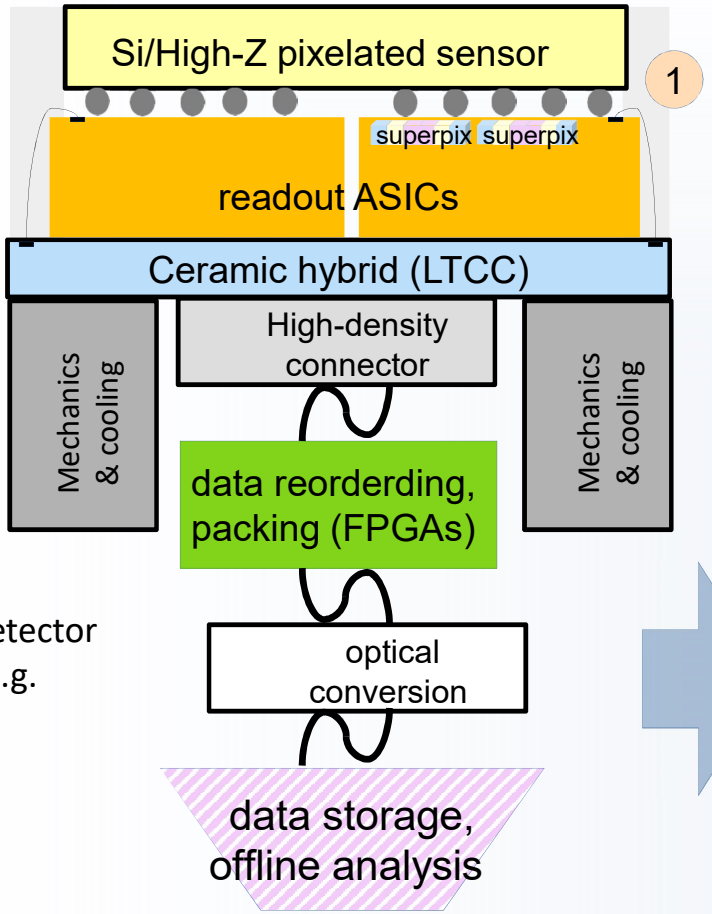


Top Level Design

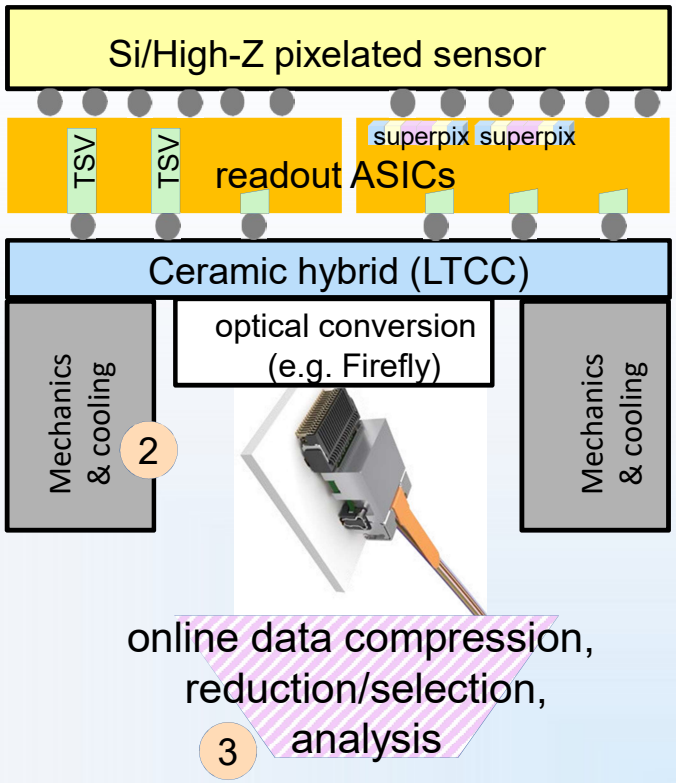
- Dedicated periphery ‚bar'
- Repeatable PCS →GWT ‚pillars'
- Timing handled by digital design flow
- Superpixels as analogue islands (i.e. abstracts in digital flow)
- Channels used for TSVs, bias circuits, and current mirrors



A Bigger Picture – Complete Systems



Current detector systems, e.g.
Lambda
AGIPD



CoRDIA

1. Get rid of dead areas
2. Keep the detector head simple
3. Reduction of data volume is mandatory

Après moi le deluge?

Per Pixel:
- 11 bit from ADC resolution
- 2 bit from gain encoding

- 13 bits/(image▪pixel)
- 150 kHz frame rate

- 1.95 Mbit/(s▪pixel)

Per ADC Block:
- 16 pixel/ADC

- 31.2 Mbit/ADC block

The 'Great Flood':
- **4 Gbit/(s▪2048pixel)**

1 Mpix:
- **256 GB/s**

Per MGBT Link:
- 128 ADC blocks
- 2048 pixel
- 64b/66b encoding

- 3.9935 Gbit/(s▪link) input

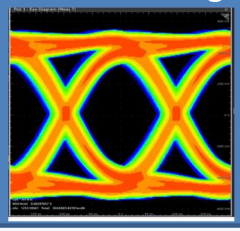
- 4.1184 Gbit/(s▪link) output ☺

ASIC :
- 100µm × 100µm pixel size
- 128 × 128 pixels

- 12.8mm × 12.8mm size
- 16384 pixels
- 8 MGBT links ☹

- Low enough to work with the Timepix4 GWT transceiver (IP block)
- Some margin to run faster than 150 kHz
- Lower requirements on PCB design

Timepix4
GWT @5 Gbit/s
X. Llopart,
On behalf of the Medipix4 Collaboration
11 th February 2022
CERN seminar



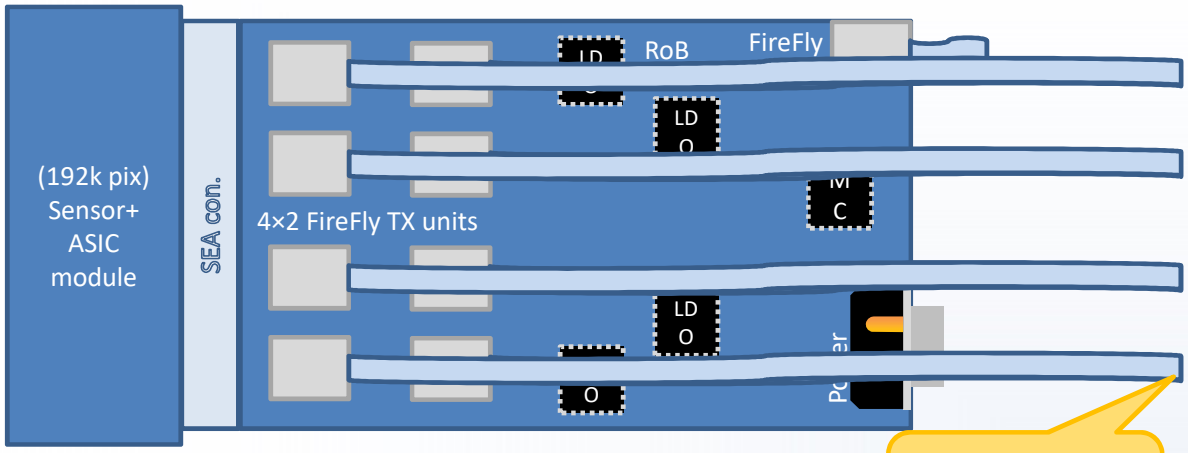
- Too many!
- 96 MGBT links for an Lambda-sized (6×2 chip) Module
- FPGAs with SoC are all ≤96 GTH/GTY TX
- Only Xilinx VU13P has 128 GTH/GTY TX, but no SoC

Sensor & 6×2 chip module

Readout board (w. SoC FPGA)

Partitioning, Chiplets & Readout Electronics

CORDIA



'Dumb' readout board option

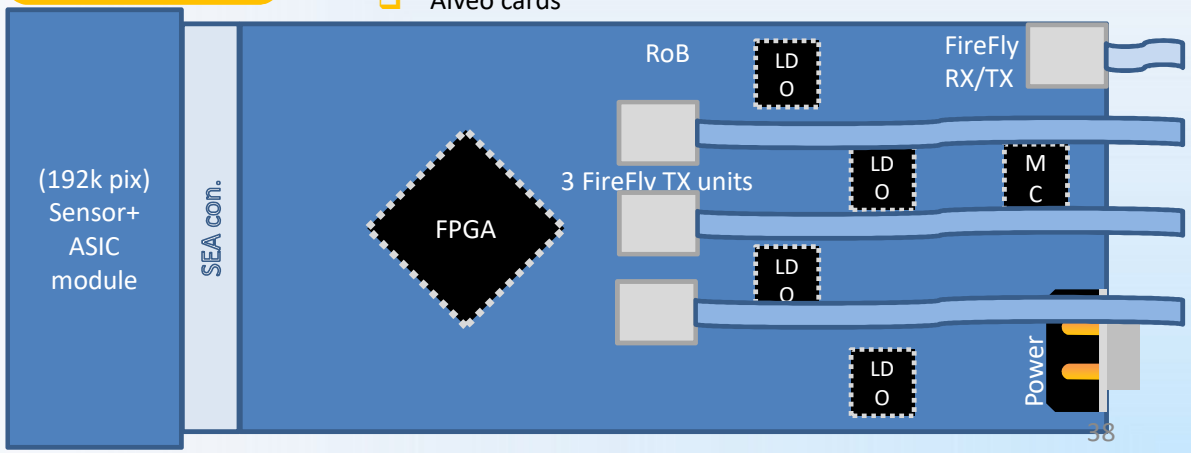
- Only cheap components
- Microcontroller
- Voltage regulators
- Samtc FireFly optical RX/TX in sockets
- Many optical fibres to
- DAQ system based on
  - FMC & FPGA evaluation boards or
  - µTCA boards
  - Alveo cards

Multiples of 12 channels

Multiples of 8 channels

FPGA based readout board option

- Expensive & heat producing components
- Low number of fibres
- Direct commercial network interface to DAQ servers
- Considerable development effort



Partitioning, Chiplets & Readout Electronics

Final chip size is still under discussion…

- Multiple of (16 × 128) pixel = 2048 pixels
- Choice of ROB architecture
- Yield
- Available sensor sizes

AGIPD sized chips

TimePix 4 sized chips

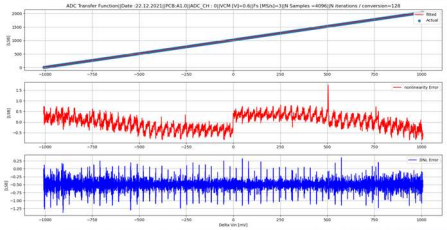
Chip size (pixl)	# of 5 Gbit links	Smallest reasonable FEM	FEM size (pixel)	# of FireFly TX (12 ch)	256 x 768 pix module size (chips)
128 × 128	8	2 × 3	256 × 384	6	2 × 6
128 × 192	12	2 × 1	256 × 192	2	2 × 4
256 × 192	24	1 × 1	256 × 192	2	1 × 4
256 × 224*	28	1 × 3	256 × 672	7	n/a

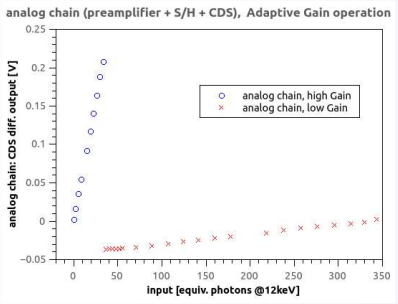
*limited by reticle size

Summary

CoRDIA – Continuous Readout Digitizing Imager Array - is…

- Targeted to DL Synchrotron sources (like PETRA IV)
- CW FELs (future CW Mode of European XFEL)
- Hybrid Pixel Detector
- Charge Integrating & dynamic gain switching
- Pixel size 110µm × 110µm
- Continuous Frame Rate f_{FR} ≈ 150kHz (≥100kHz)
- On-chip digitisation @ ≥ 10 bit
- MGbit data transmission





- All fundamental components exist
  - FE & ADC on test chips
  - MGBT readout on TimePix 4
- (Component) test chips show good performance
- Test of pixel blocks (with ADC) is ongoing
- Implementation of MGBT readout is in progress

- Full-size chips for detectors at PETRA IV ≈2027
- CW-FEL version with higher analogue performance ready later for future CW operation of Eu.XFEL

Thank you for your Attention!

And Thanks to my Fellow ‘CoRDIAns’:
Heinz Graafsma, Mohamed Lamine Hafiane, Alexander Klyuev, Hans Krüger, Sabine Lange, Torsten Laurus, Alesandro Marras, David Pennicard, Tianyang Wang, Cornelia ‘Trixi’ Wunderer