

DAMC-DS5014DR

The DAMC-DS5014DR, a high-speed Digitizer, leveraging the cutting-edge AMD ZYNQ Ultrascale+ RFSoc Technology in a MicroTCA.4 form factor.

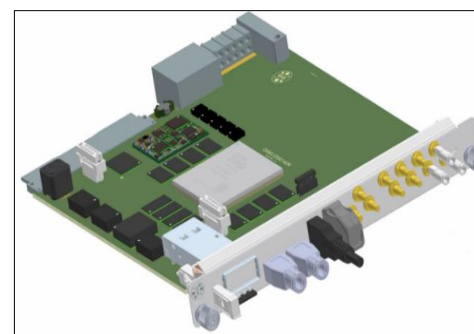
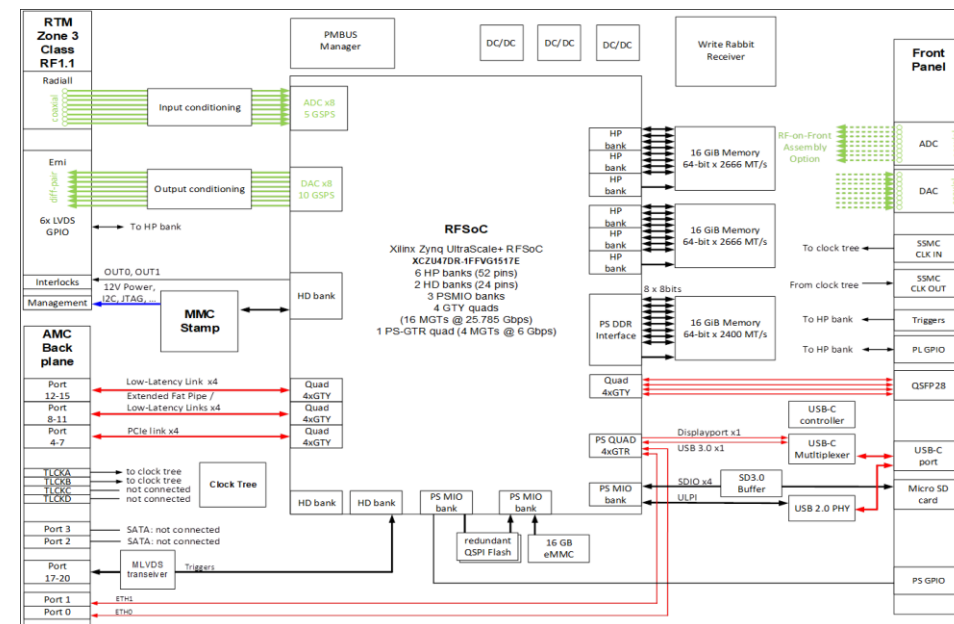
(13th MT ARD ST3 Meeting 2025 at DESY in Zeuthen, 25 to 27 June, Germany)

Behzad Boghrati, Michael Fenner, Cagil Gümüş, Szymon Jablonski,
Burak Dursun, Stanislav Chystiakov, Johannes Zink

The DAMC-DS5014DR, a high-speed Digitizer, leveraging the cutting-edge AMD ZYNQ Ultrascale+ RFSoc Technology in a MicroTCA.4 form factor.

Main Features

- **Form Factor:** Mid-size, double-width Advanced Mezzanine Card (AMC) board.
- **Processing Core:** 3rd-generation Zynq Ultrascale+ RFSoc ZU47DR with 930k logic cells and 4272 DSP slices.
- **Data Conversion:** 8-channel, 14-bit ADCs at 5 GSPS with 6 GHz analog bandwidth; 8-channel, 14-bit DACs at 10 GSPS.
- **Analog Input Features:**
 - Hybrid AC/DC coupling for input channels.
 - Signal pre-conditioning on the AMC board.
 - 8 single-ended inputs via Zone 3 Radiall COAXIPACK2 from RTM, supporting AC (0.03–6 GHz) or DC (DC–6 GHz) coupling.
 - User-customizable signal conditioning on the Rear Transition Module (RTM).
- **Analog Output Features:**
 - 4 differential outputs via ERNI to RTM, DC-coupled (DC–2.5 GHz).
 - 4 single-ended outputs via Radiall to RTM, AC-coupled (0.03–6 GHz).
- **RF Connectivity:** Zone 3 RF connector compliant with Class RF1.1.
- **High-Speed Interfaces:**
 - QSFP28+ supporting 100Gb Ethernet or optical PCIe Gen.4 x4 (16 Gbps/lane).
 - PCIe Gen.4.0 x8 for data transfer to the MicroTCA.4 backplane.
- **Timing and Triggers:** Eight independent timing/trigger inputs for event-coincident data capture.
- **CPU Functionality:**
 - Operates as a CPU module with a front-panel USB Type-C supporting DisplayPort and USB 3.
 - Up to 16 GB PS DDR4 and 32 GB PL DDR4 memory.
 - Runs Yocto Linux from eMMC, QSPI or SD card.
- **Clock Synchronization:** High-frequency clock synthesizer with inputs from RTM, front panel, or backplane.
- **White Rabbit Support:** CERN White Rabbit endpoint capability for precise timing.



3D Layout

	Digital Clock I/O	Digital I/O	Digital Clock Input	Digital User I/O			Differential DACs			NTC14.4 Management	
	10	9	8	7	6	5	4	3	2	1	
+	f	AMC-CLK	OUT1/DB-	RF-CLK3	DAC7-	D5-	DAC4-	D2-	TM5	TDO	
+	e	AMC-CLK+	OUT1/DB+	RF-CLK3+	DAC7+	D5+	DAC4+	D2+	TD1	TSD	
+	b	RF-CLK2	OUT0	RF-CLK1	D6-	D4-	DAC3-	D0-	SC1	ISA	
+	c	RF-CLK2+	OUT0+/D7+	RF-CLK1+	D6+	D4+	DAC3+	D0+	CCP+	MP	
+	b	RF-CLK0	AMC-CLK-	RTM-CLK-	DAC6-	D4-	DAC3-	D1-	DAC0-	PWRB2	PWRB1
+	c	RF-CLK0+	AMC-CLK+	RTM-CLK+	DAC6+	D4+	DAC3+	D1+	DAC0+	PWRB2	PWRB1
Simple Ended Analog Signals											
		2									
	A	ADC-IN7	DAC-OUT0	DAC-OUT3							
	A	ADC-IN6	DAC-OUT0	DAC-OUT2							
	B	2	2	1							
	A	ADC-IN1	ADC-IN3	ADC-IN5							
				ADC-IN4							

Zone 3 – Class RF1.1 pin assignment J30, J31, and J32 connector, AMC side view.

The DAMC-DS5014DR, a high-speed Digitizer, leveraging the cutting-edge AMD ZYNQ Ultrascale+ RFSoc Technology in a MicroTCA.4 form factor.

DS5014DR Analog Frontend Evaluation Board and High-Frequency Synthesizer Evaluation board

- **Primary Objective:** Assess the performance of the DS5014DR's hybrid coupling system, supporting both AC and DC coupling channels.
- **Hybrid Coupling Mechanism:** Utilizes an assembly option to toggle between AC and DC coupling modes.
- **AC Coupling Characteristics:** Employs a passive Balun design, supporting input frequencies from 30 MHz to 6 GHz.
- **DC Coupling Characteristics:** Features an RF fully differential amplifier (TRF1305B2) with a bandwidth from DC to 7 GHz, offering three power gain variants:
 - 5 dB (TRF1305A2)
 - 10 dB (TRF1305B2)
 - 15 dB (TRF1305C2)
- **DC Coupling Input Specifications:** In single-ended mode, supports a dynamic range of 1 Vpp (± 0.5 V) with a 0 V DC common mode input voltage.
- **Evaluation Using DS5014DR-AFE Board:** Measures analog converter dynamic performance, including:
 - Noise floor
 - Time latency
 - Static and Dynamic performance metrics
- **RF Switch and ADC Design:** Incorporates an RF switch and an RF-ADC with an interleaving architecture, potentially requiring calibration.

