LLRF System Overview
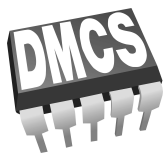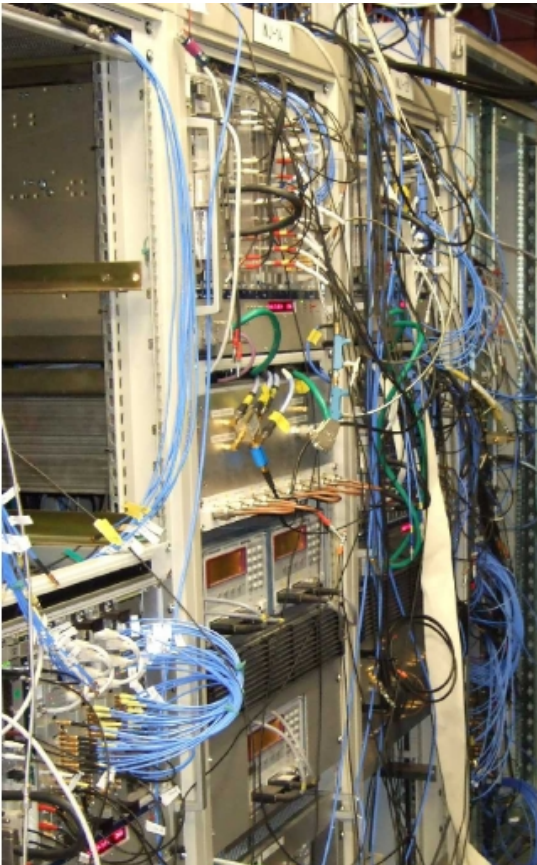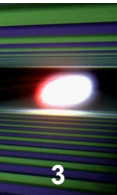# and
Roadmap

F. Ludwig / T. Jezynski
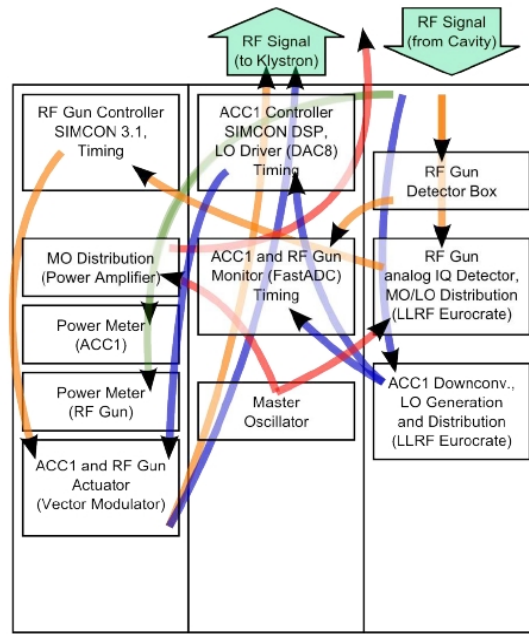for the LLRF - Team

Outline

- Experience from FLASH

- Rack distribution and occupation
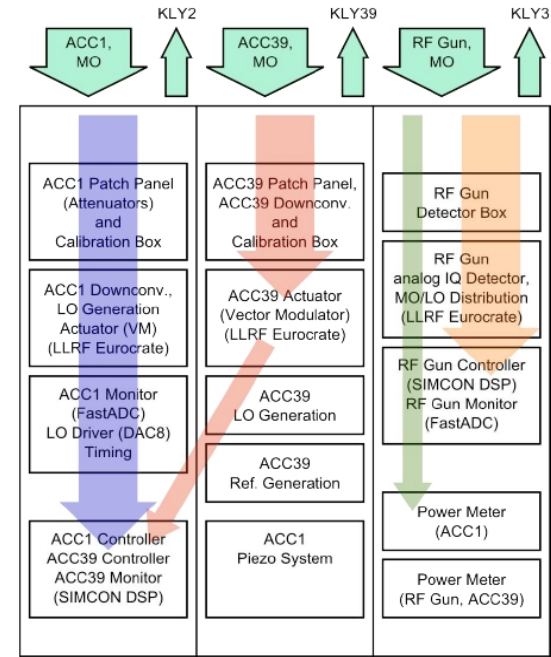
- UTCA Crate development

- Timeline

Upgrade of FLASHs LLRF System 2010

Previous LLRF rack layout

Current LLRF rack layout

Energy stability improved by
a factor of 3 to dE/E=0.5E-4.

Christopher Gerth, et. al.

We're done for the XFEL ? . . .

Consequences from FLASH operation

Actual FLASHs LLRF limitations

- Rack size is strongly limited (J0-16U, L1-26U) compared to (ACC1-42U)
- LLRF system is outside the tunnel
- Central FPGA concept (limited comp. power)
- Process only 8x3 cavity signals (P,F,R)
- SimconDSP 14-bit ADC limitation
- Baseband field detection
- No redundancy
- Pluggable connectors are not drift compensated
- No channel parallelization for performance

Roadmap for the XFEL LLRF

- VME -> uTCA (uAMC, uRTM) concept
- LLRF system is in the tunnel
- Distributed FPGA, DSP concept
- Process 2 times more signals
- Lowest spectral density (16-bit ADCs)
- Non IQ sampling scheme (no PM->AM)
- Redundant systems in the injector
- Rack will be fully drift compensated
- Scaleable system
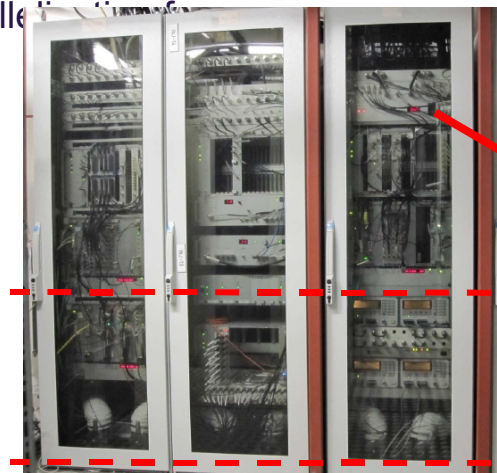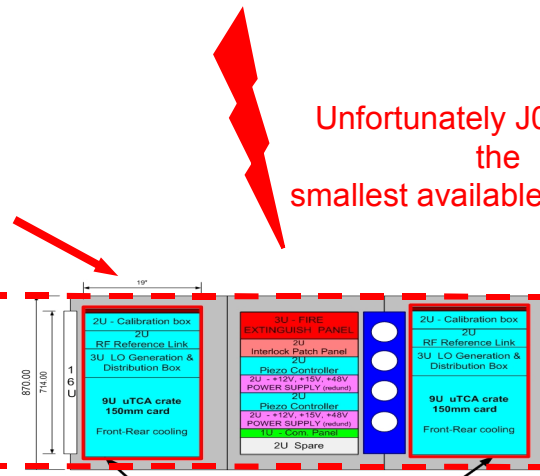
Unfortunately J0 has the smallest available area !

: 6

Consequences from FLASH operation
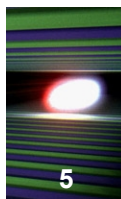
- **2 semi-distributed uTCA stations supply 4 cavity modules**
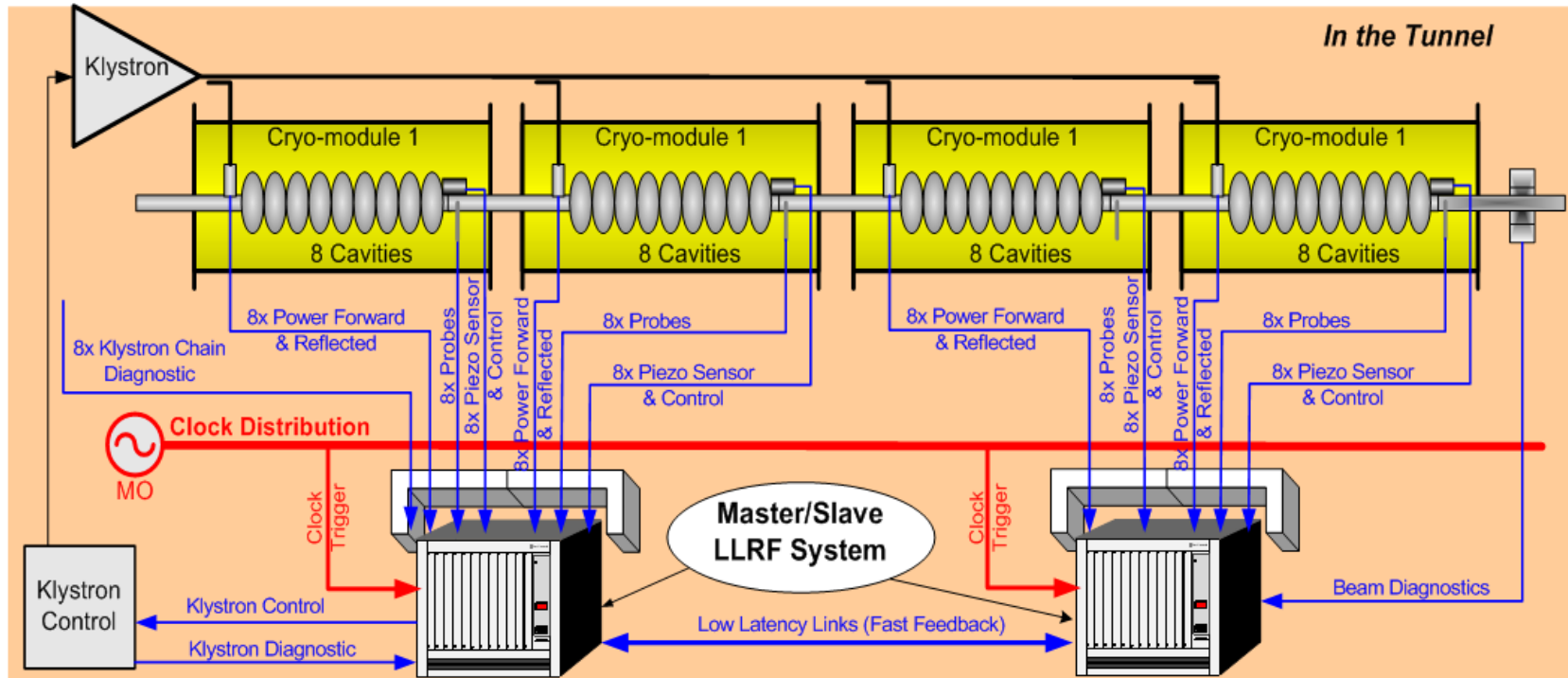
Driving Argument → Short pickup cables for low drifts (10fs/m/K) and prevent crosstalk from high power cables

European
XFEL | Semi-Distribution

6
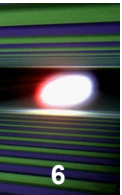
Schematic view of accelerataros and LLRF Stations positioning
18.10.2010
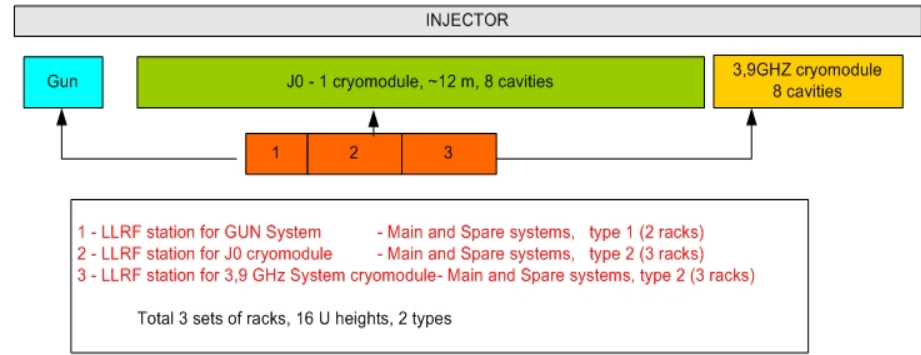
1 RF-station L1
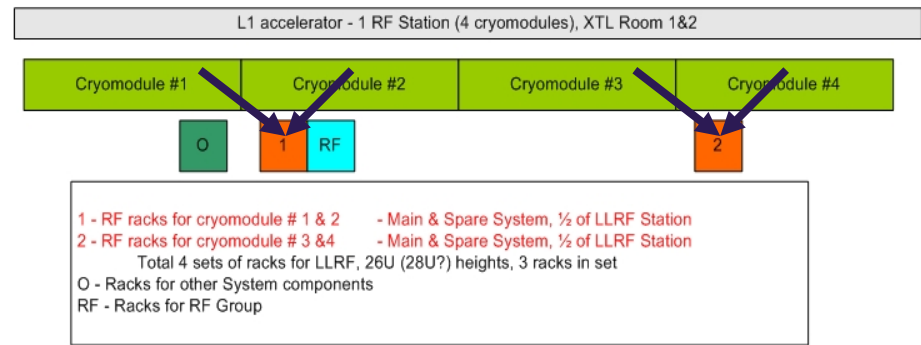
3 RF-stations L2
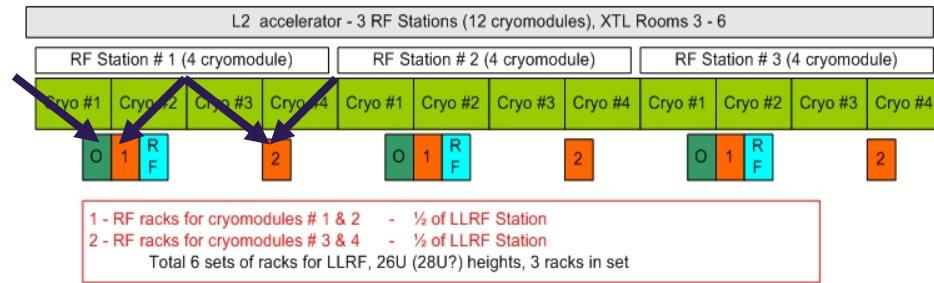
21 RF-stations L3

Courtesy:
W. Wierba / IFJ

HELMHOLTZ
| ASSOCIATION

LLRF rack occupation

European XFEL
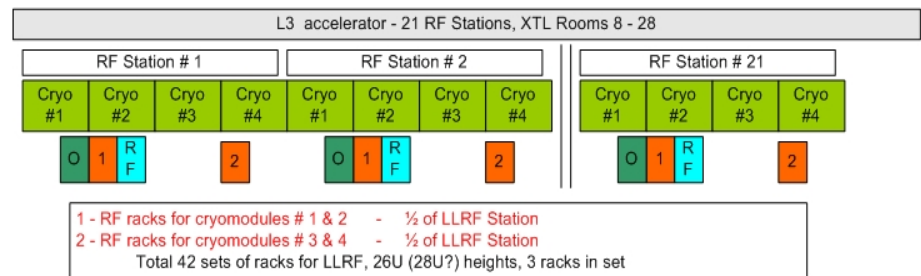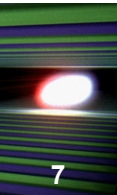
- **Injector (GUN, J0, 39) LLRF systems are completely doubled . . .**

SYSTEM IN INJECTOR FOR J0 -
uTCA DESIGN, 16_U RACKS
Two Redundant Systems

18/10/2010

19"

870.00
714.00

16 U

| 2U - Calibration box |
| 2U RF Reference Link |
| 3U LO Generation & Distribution Box |
| 9U uTCA crate 150mm card |
| Front-Rear cooling |

3U - FIRE EXTINGUISH PANEL
2U Interlock Patch Panel
2U Piezo Controller
2U - +12V, +15V, +48V POWER SUPPLY (redund)
2U Piezo Controller
2U - +12V, +15V, +48V POWER SUPPLY (redund)
1U - Com. Panel
2U Spare

| 2U - Calibration box |
| 2U RF Reference Link |
| 3U LO Generation & Distribution Box |
| 9U uTCA crate 150mm card |
| Front-Rear cooling |

One block - can not be splitted
and moved

- RF Cables Patch Panel
(on Top in calibration Box)

Crates in UG05/011
Electronic racks for
Main and Spare Systems

| 3U Clystron Driver Signal |
| 4U Freq. Tuning Motor Driver (Cold) |
| 4U Coupler Motor Driver (Warm) |

| 3U Clystron Driver Signal |
| 4U Freq. Tuning Motor Driver (Cold) |
| 4U Coupler Motor Driver (Warm) |
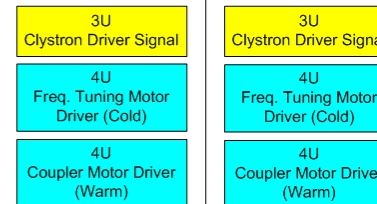
Courtesy:
W. Wierba / IFJ

Redundancy, LLRF performance measurement

FLASH 21/04/09, Beam Stability at
FLASH - Update', F.Ludwig et. al.

LLRF rack occupation

■ **. . . L1 is also redundant , . . .**

SET OF RACKS FOR RF STATION SYSTEM FOR **L1** IN XTL
u-TCA DESIGN HALF - DISTRIBUTED (four cryomodules)
Two Redundant Systems

18/10/2010

FIRST SET OF RACKS

SECOND SET OF RACKS

Courtesy:
W. Wierba / IFJ

LLRF rack occupation

- **. . . but L2, L3 are not redundant.**

SET OF RACKS FOR RF STATION SYSTEM FOR **L2** & **L3** IN XTL
u-TCA DESIGN HALF - DISTRIBUTED

18/10/2010

FIRST SET OF RACKS

SECOND SET OF RACKS

Must be on top of the rack

19"

1300.00

2U PIEZO Patch Panel
2U Interlock Patch Panel
4U Freq. Tuning Motor Driver (Cold)
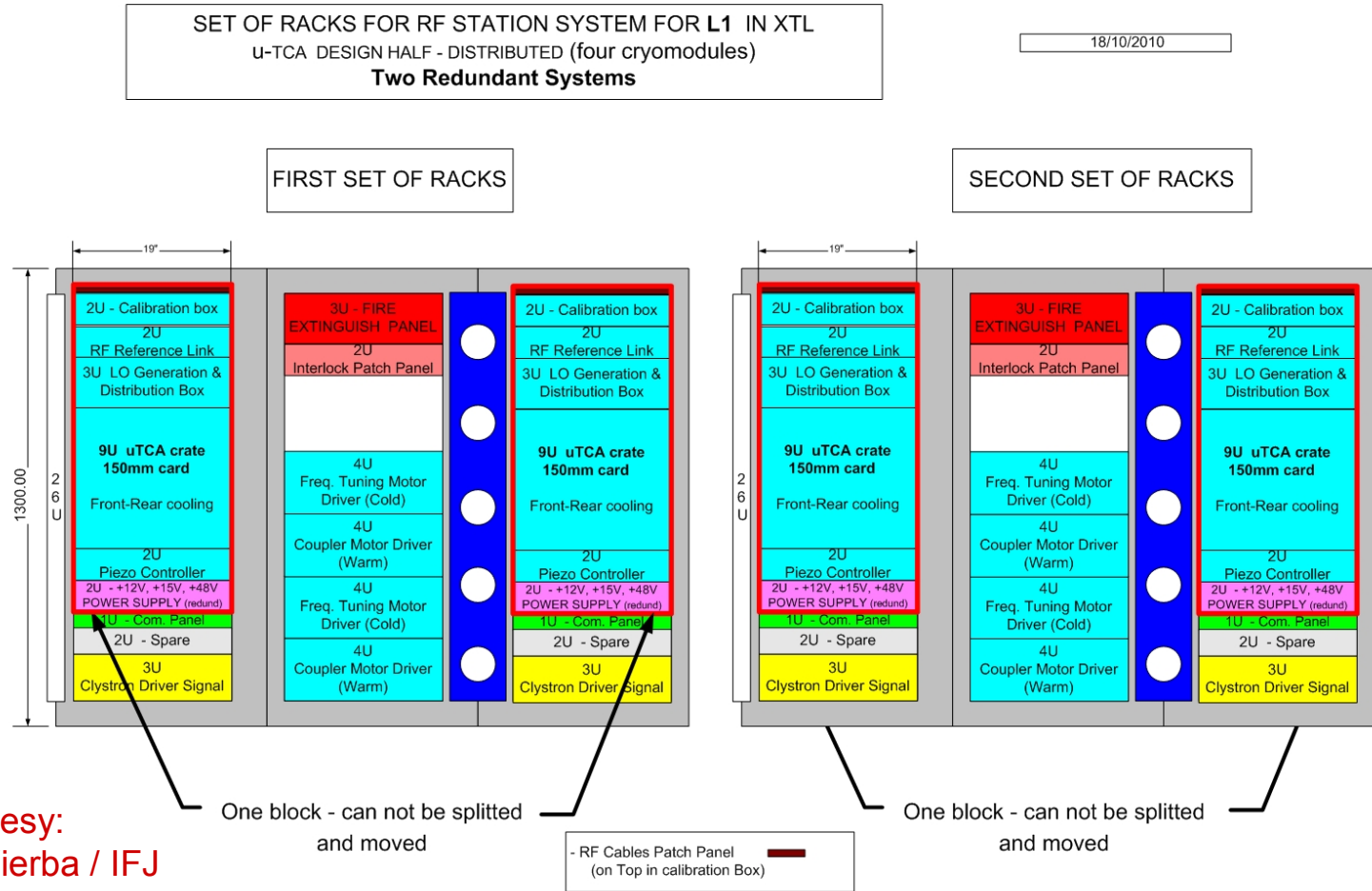4U Coupler Motor Driver (Warm)

3U - FIRE EXTINGUISH PANEL
4U Freq. Tuning Motor Driver (Cold)
4U Coupler Motor Driver (Warm)

2U - Calibration box
2U RF Reference Link
3U LO Generation & Distribution Box
9U uTCA crate 150mm card
Front-Rear cooling
2U Piezo Controller
2U - +12V, +15V, +48V POWER SUPPLY (redund)
1U - Com. Panel
2U - Spare
3U Clystron Driver Signal

26U

- RF Cables Patch Panel (on Top in calibration Box)

One block - can not be splitted and moved

Courtesy: W. Wierba / IFJ

LLRF rack occupation

- **How will a LLRF System look like inside . . . 19" modules . . .**

Inputs from cavitis

Calibration box — **ADCModule** (no drifts within the rack)
ISE, DMCS, MSK

LO Generation Box

— **LOGModule** (Local Oscillators)
ISE, MSK

LO Distribution Box

CU RTM

2U - Calibration box
2U RF Reference Link
3U LO Generation & Distribution Box

9U uTCA crate 150mm card

Front-Rear cooling

2U Piezo Controller
2U - +12V, +15V, +48V POWER SUPPLY (redund)
1U - Com. Panel
2U - Spare
3U Clystron Driver Signal

PU 230->12 Volt in CPU MCH ADC ADC ADC ADC DC TING ADC ADC PU 230->12 Volt in AMC

Interlock System
Timing System
BBF „Slave" Station

PIEZO Controller / Driver — **PIEZOModule** (Piezo driver)

Power supply (redundant) — **Power Supply** (redundant)
industry

uTCA Progress Status

- **Sharing resources within DESY and industry (status 10/2010)**

Application	AMC Type	RTM type
Timing	Timing receiver	---
Klystron	SIS8300	8 Rf receivers, 2 diff in
3.9GHz monitoring	SIS8300	9 RF receivers @ 3.9GHz
1.3GHz monitoring	SIS8300	9 RF receivers @ 1.3GHz
Coupler Interlocks	DAMC2	ADCs, tests, sources
BPM	DAMC2	---
Toroid	DAMC2	ADC
Beam Loss Monitor	DAMC2	ADCs
Wire Scanner	DAMC2	2 different signal conditioning
Beam Arrival Monitor	SIS8300	Optical in
EBPM	SIS8300	Optical in
Fs LASER sync	SIS8300	Optical in
Fs motors	DAMC2	Stepper card
Spectrometer	DAMC2	32 ch ADC
Machine Protection System	DAMC2	Signal conditioning
Kicker	DAMC1	---

DESY partners :

MCS,
MSK,
FEB,
FLC,
FLA,
MDI,
MIN,
MHF-SL,
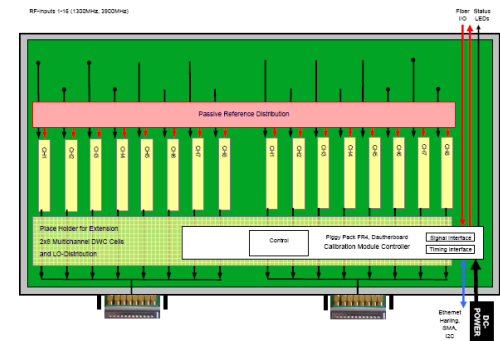**EXP-DAQ,**
SLAC,
TDS, RAEGAE, AMTF
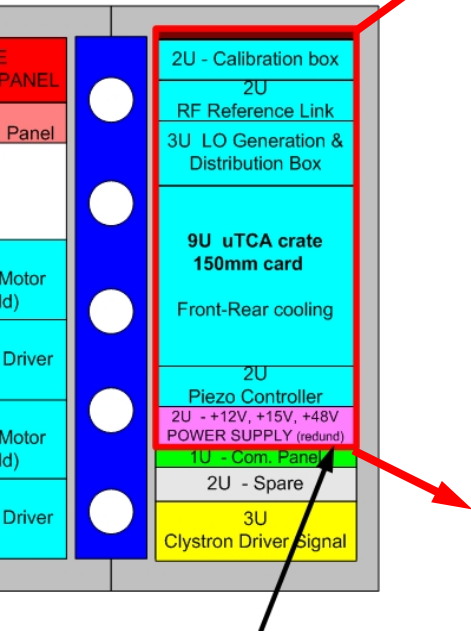
Industry partners:

struck innovative systeme
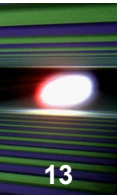
ELMA 50 years 1960-2010
Your Solution Partner

Courtesy: K.Rehlich / MCS

uTCA Progress Status

■ **Summary of LLRF module and uTCA progress status:**

▪ ADCM (Advanced Drift Calibration Module):	Design state
▪ REFM (Reference Module):	Design state
▪ LOGM (LO-Generartion Module):	Design state
▪ uTCA – Rack (LLRF boards):	Delivered, test state
→ DWC8300 (Down-Converter):	Delivered, test state
→ SIS8300 (ADC Digitizer):	Delivered, test state
→ uTLC (LLRF Controller):	Delivered, test state
→ uTLC VM (LLRf Controller):	Manufacturing
→ uRFB (RTM backplane):	Manufacturing
▪ PIEZOM (Piezo driver):	Delivered, during tests
▪ Power Supply	Specification / Ordering state

LLRF – rack layout

European XFEL

Inputs from cavitis

ADCModule Calibration box

Fref

Fref
LO
CLK

LOGModule LO Generation Box

LO Distribution Box

CU

AMC

RTM

Monitoring HP

CU

PIEZO Controller / Driver

PIEZO
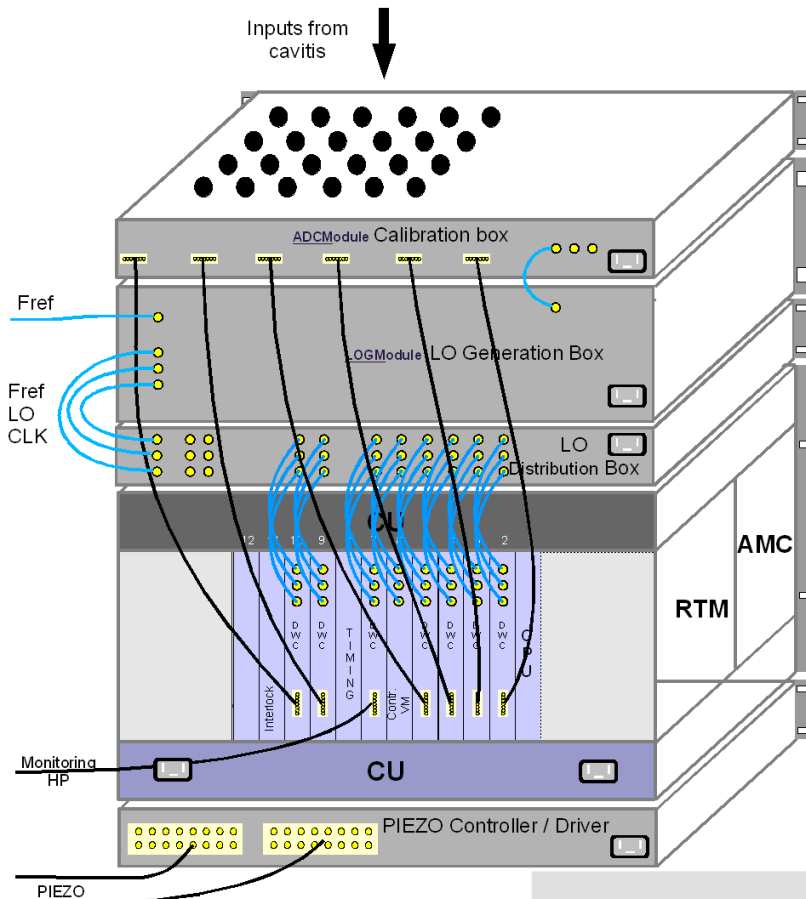
1. CPU
2. ADC – Pref
3. ADC – Pref.
4. ADC – Prob
5. ADC – Prob
6. Contrl.+VM
7. ADC – Monitoring
8. Timing
9. ADC – Pfor.
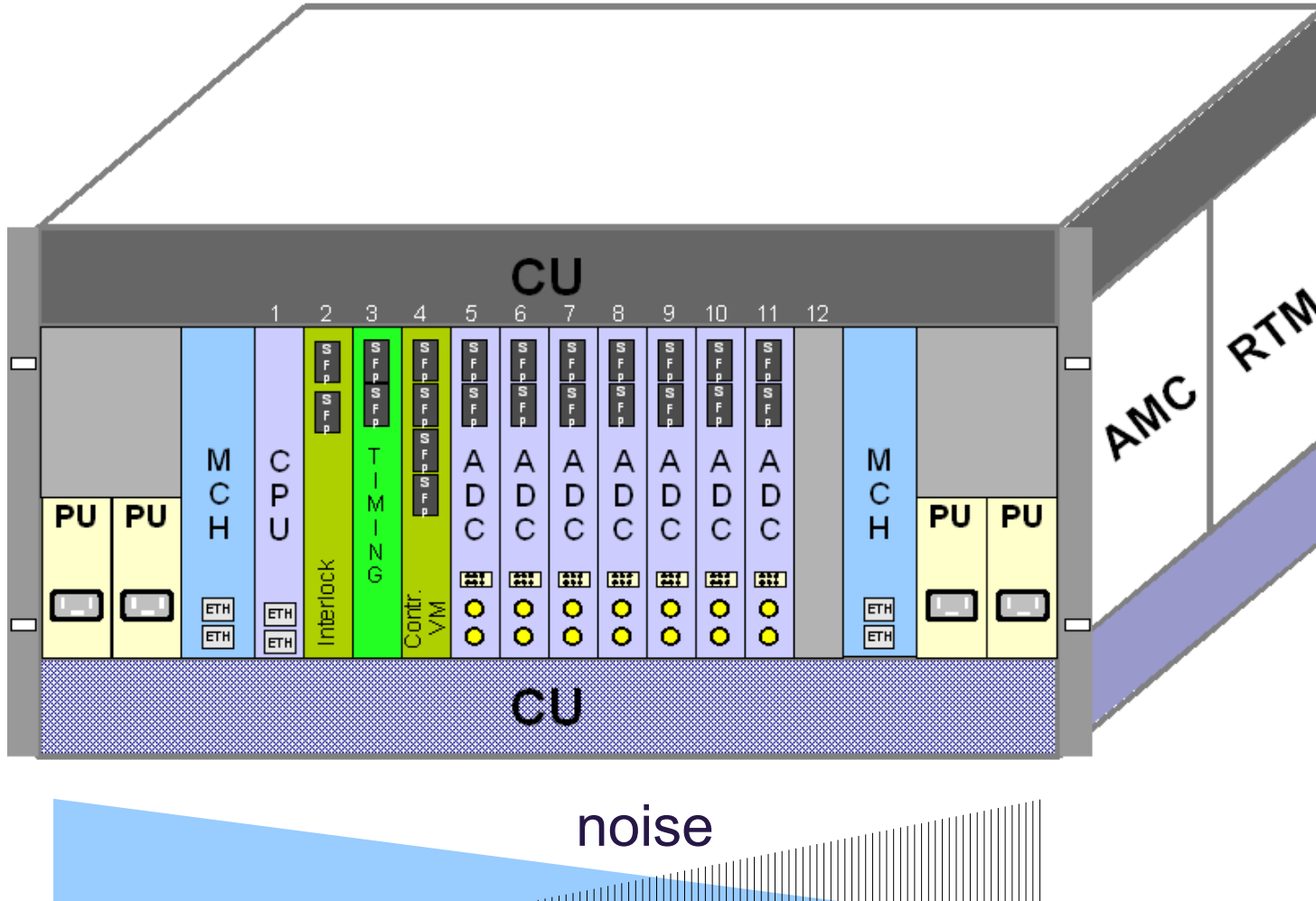10. ADC – Pfor.
11. Interlock

ADCModule Calibration box

LOGModule LO Generation Box

LO Distribution Box

CU

RTM

AMC

Interlock System

Timing System

BBF

„Slave" Station

CU

PIEZO Controller / Driver
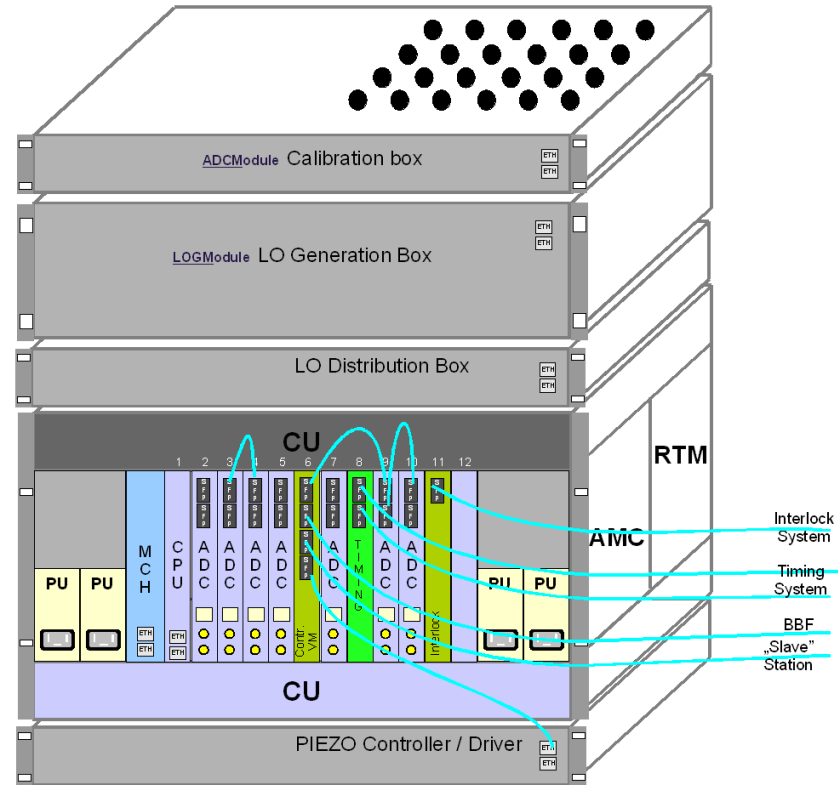
Order of boards for low distortions concept
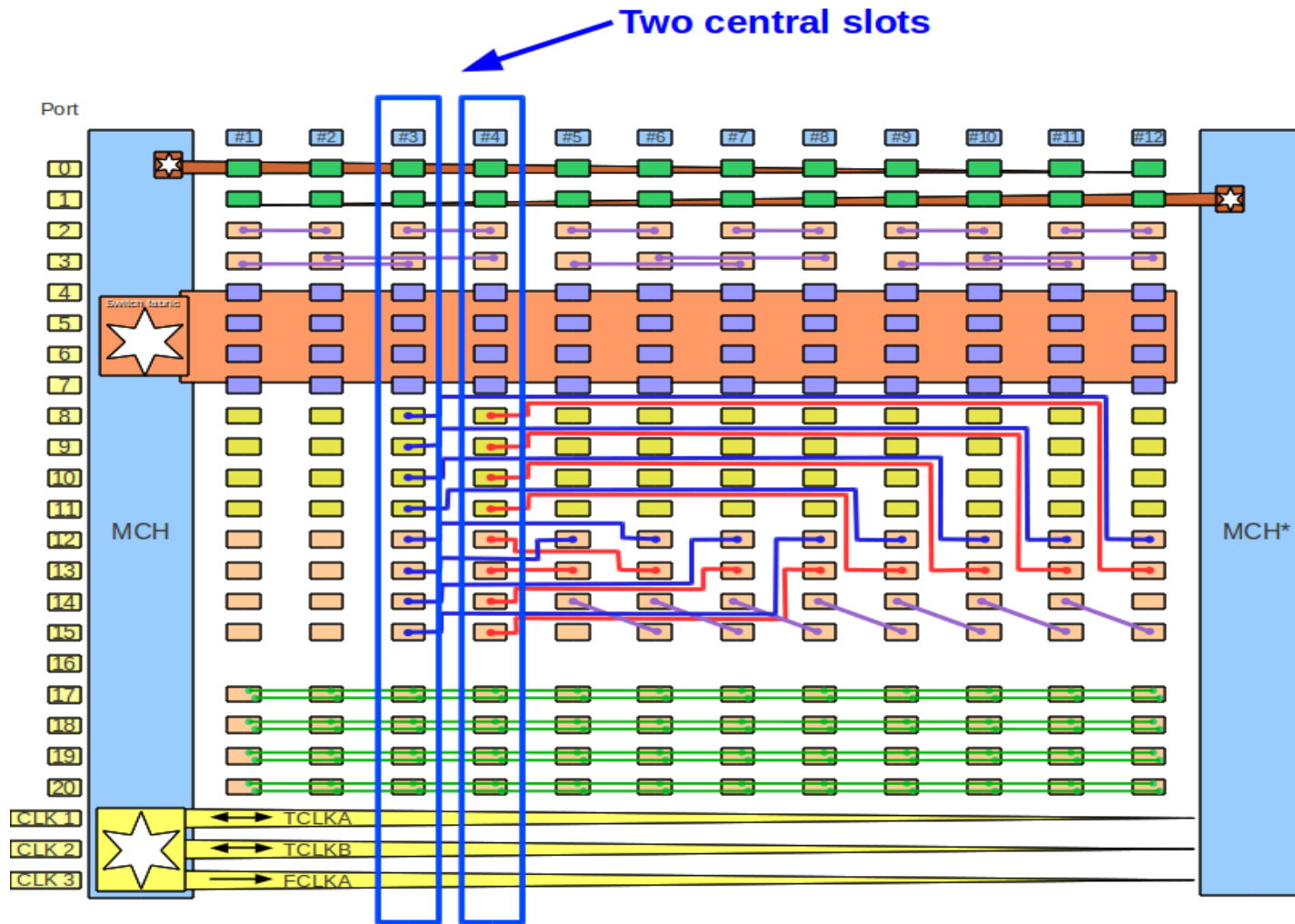
Complicated cable management

- LLRF AMC backplane

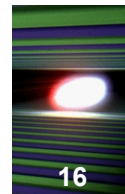- LLRF RTM backplane concept

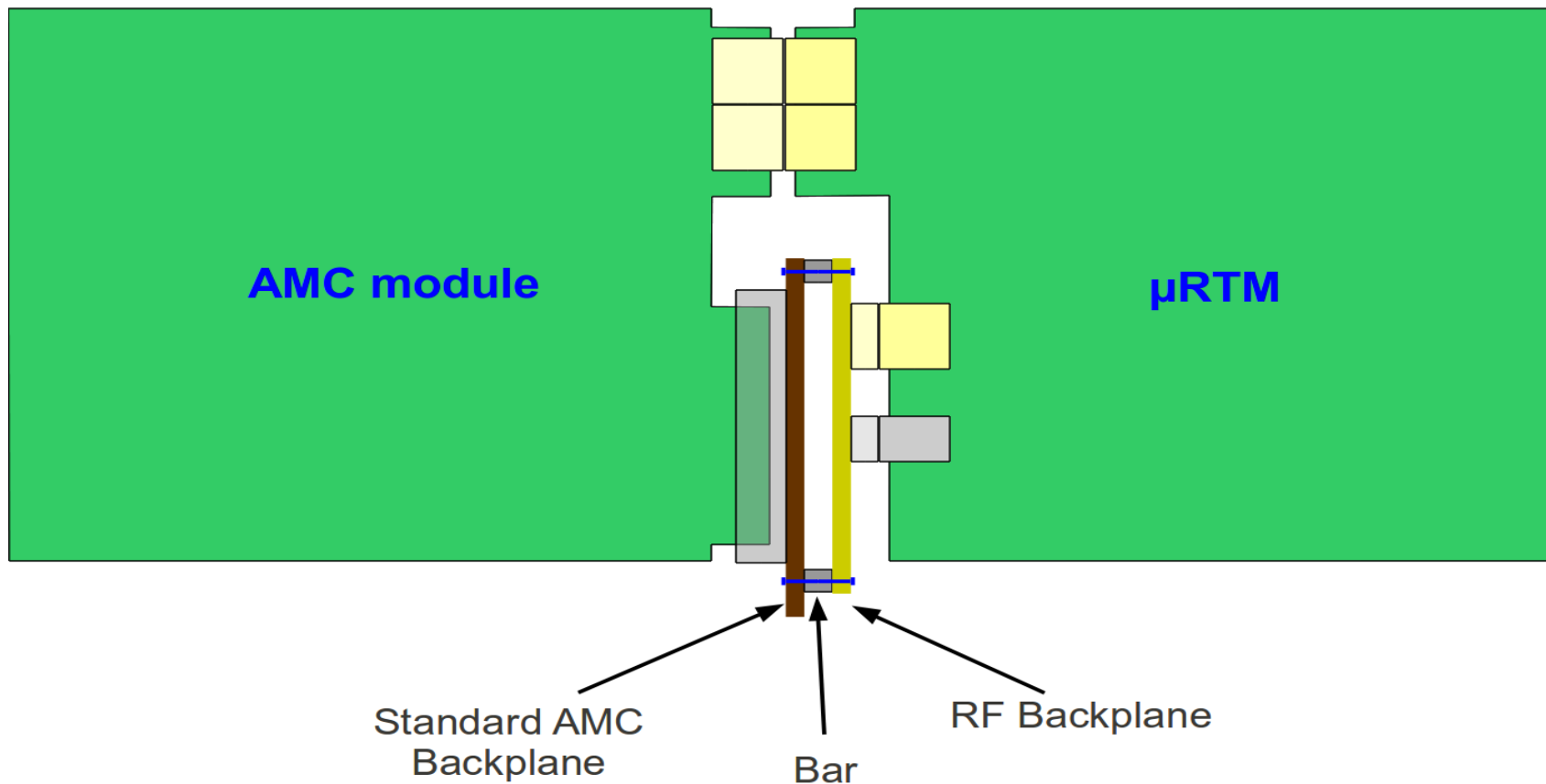# xTCA Crate for LLRF

xTCA LLRF Backplane

xTCA Crate – RF backplane

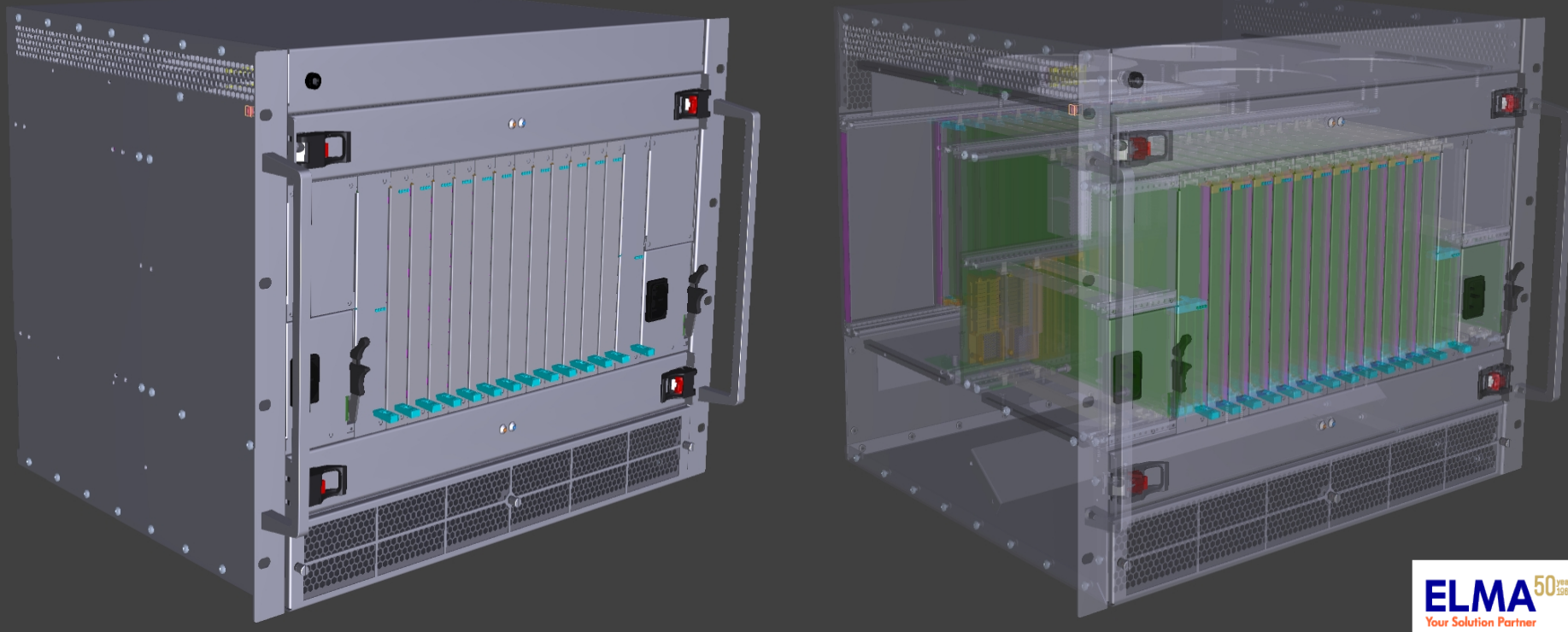FRONT   REAR

AMC module   **µRTM**

Standard AMC
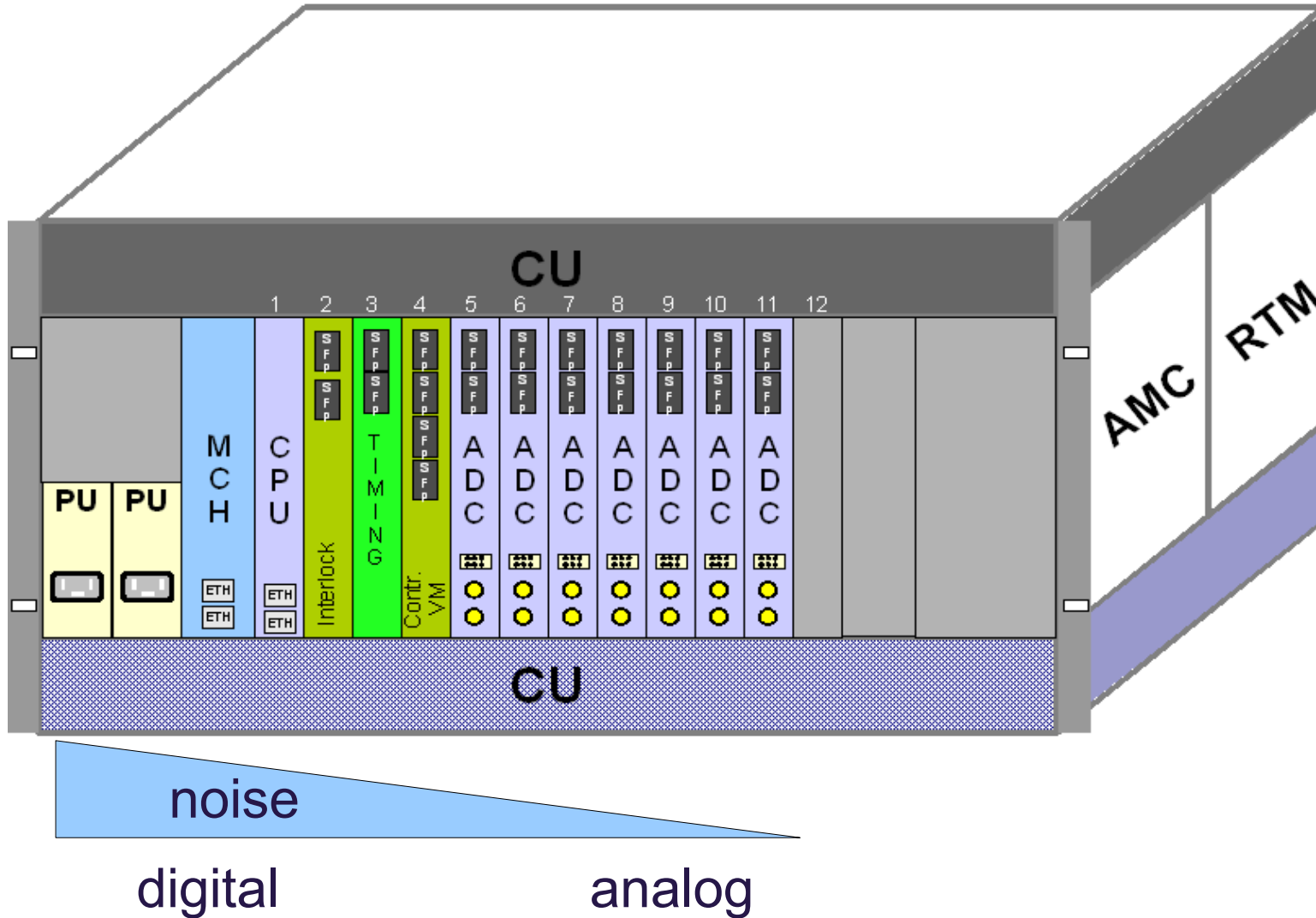Backplane   Bar   RF Backplane
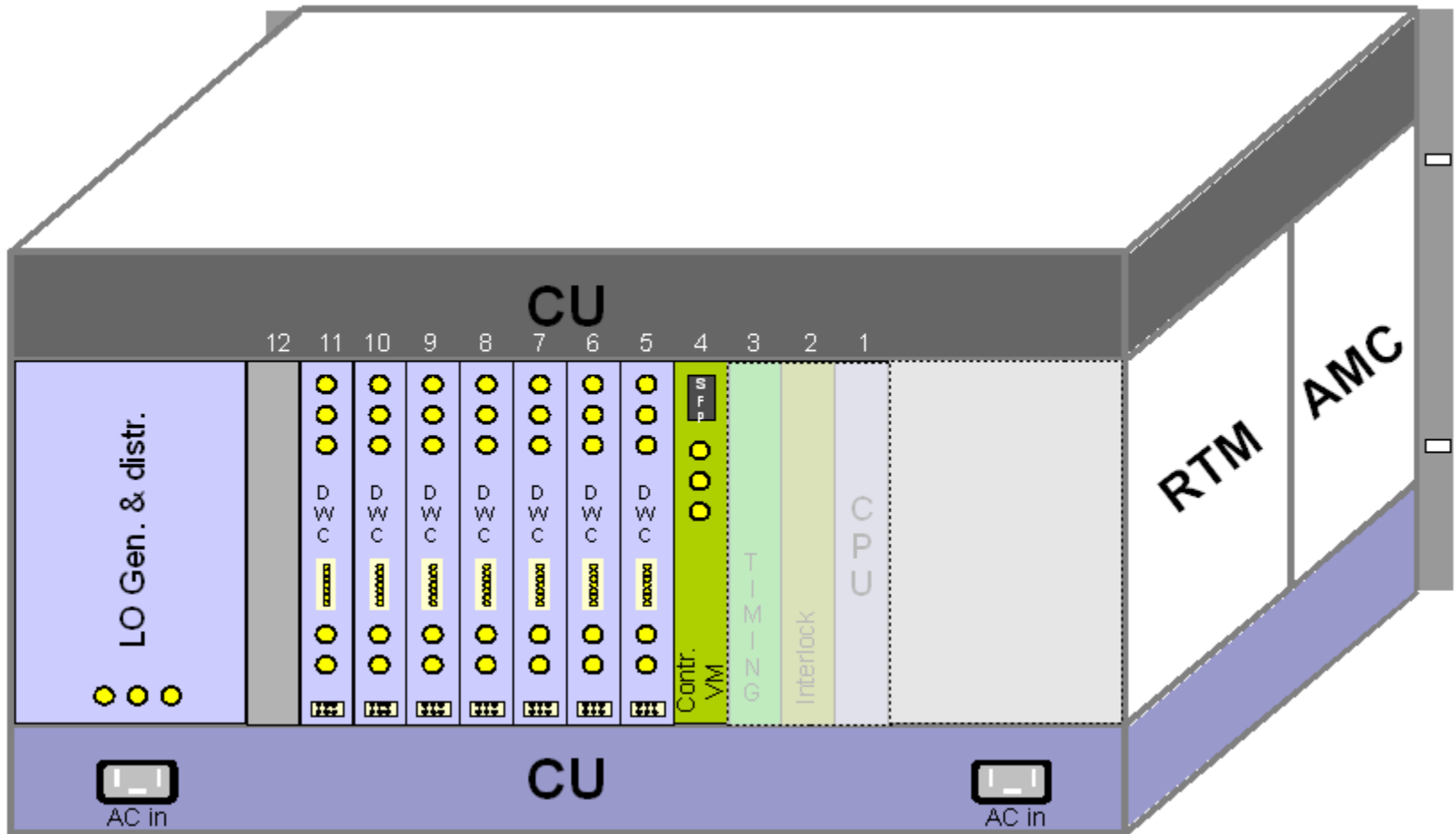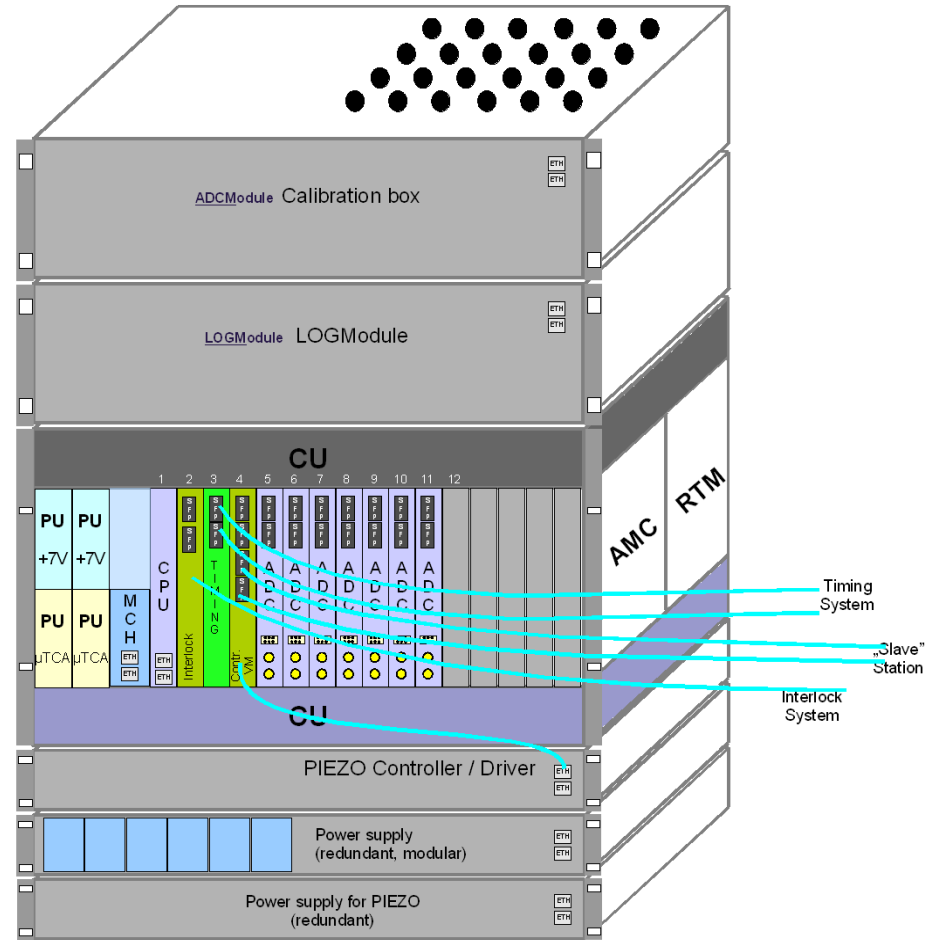
uTCA Progress Status
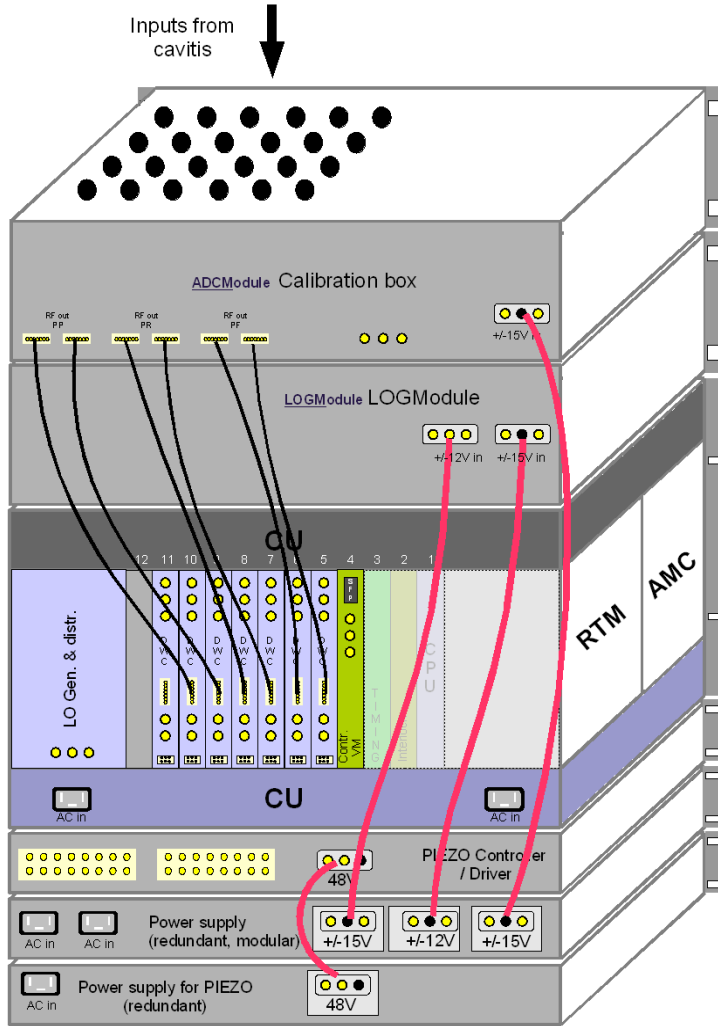
- **uTCA platform for cavity control**
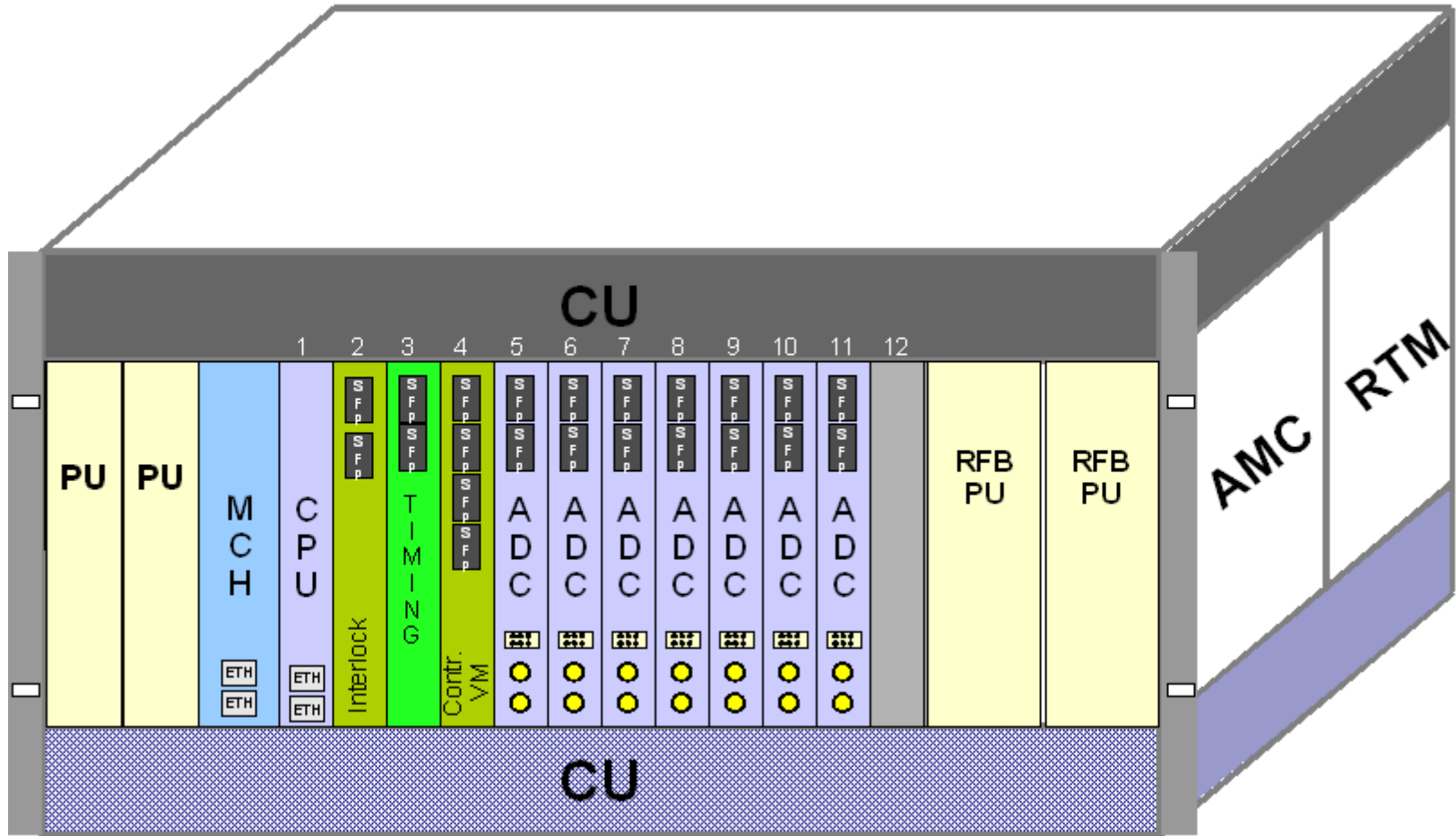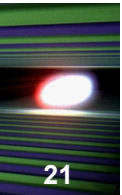

Courtesy: ELMA

xTCA Crate for LLRF – board distribution

xTCA Crate – rear view

European XFEL
LLRF – rack layout

xTCA LLRF Crate

European XFEL

Timeline

Time line

2010 **2011** **2012** **2013** **2014**

3 years left

Inst. INJ   Beam INJ

Inst. LINAC   Beam LINAC

Operation

Design frozen

Hardware design

12m   12m   5m   10m   4m

Reliability test   Production   Quality control   Installation   LLRF commissioning XTL
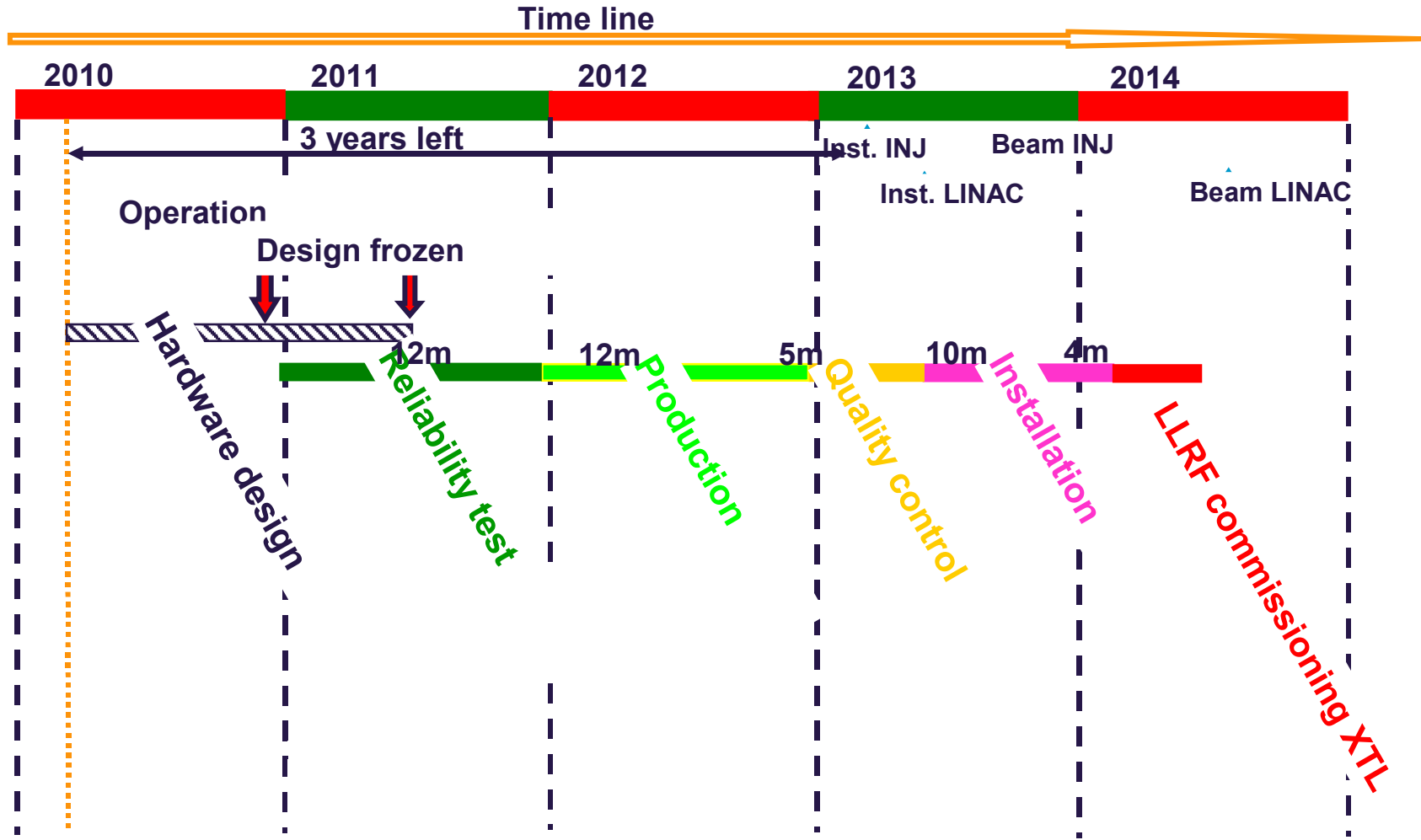
Courtesy: H. Schlarb / DESY

Summary of the XFEL LLRF Roadmap

- **Installation and infrastructure decisions**
  - 2 uTCA stations, 1 klystron supply 4 cavity modules for the whole XFEL
  - Injector systems are doubled for redundancy and crosschecks

- **LLRF rack decisions**
  - uTCA common shared crate standart
    - → Support 12 slot standart double sized uAMC and uRTM boards
    - → Low latency LLRF AMC backplane, distributed FPGA & DSP support
    - → 10 channel, 16-bit ADC 130Msps support (SIS8300)
    - → Customer backplane for 10fs RF-signals and 100fs low jitter clocks
    - → Separate redundant power supplies for analog & digital boards
    - → Ready for channel parallelization for future demands
    - → Separation of algorithmic and hardware firmware for easy software support
  - Multi-channel field detection
    - → Non IQ sampling method for easy servicing
    - → 1.3GHz, 3.0GHz and 3.9GHz operation for all customers
    - → 16x3 channels for Probe, Forward, Reflected signals
    - → Multi-pluggable coax cables for RF-signals or IFs for easy maintenance
  - Reference injection for a long-term stable machine operation
    - → Fixed N-type 1/2" Heliax cables for Probe signals
    - → Fixed N-type 3/8" Heliax cables for Forward, Refleced signals