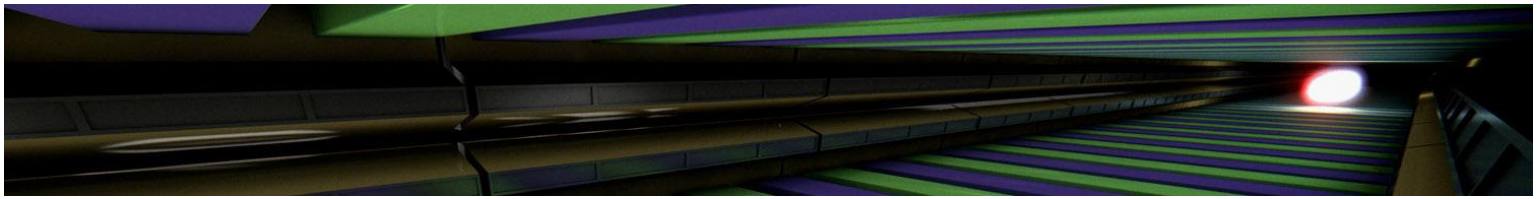


QC/QA for WP02

Maciek Kudla,

LLRF Collaboration Workshop,
Cracow
April 18, 2011

Contents

- Mission of QC/QA in WP02
- General remarks on QC/QA
- ISO 9000 basics
- QC/QA for WP02
- Closing remarks

Mission/Motivation

Mission of QC/QA in WP02 is help in:

- delivery to XFEL GmBH LLRF system fulfilling the project requirements
- effective usage of existing resources during WP02 lifetime

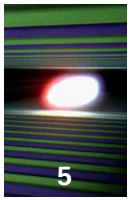
General remarks on QC/QA in WP02

- Proposed QC/QA methods are based on ISO 9000 family* standards and uses the vocabulary defined there, but are not fully implementing the standard requirements to minimalize the charges of QC/QA for WP02 team
- The proposed ideas are essential for hardware, but they can be implemented also in other domains (firmware/software, operation)
- WP02 is now in conceptual design phase (partially in design phase) – PDCA cycle is proposed for WP02 during this phase

** ISO 9000 Standards family:*

- ***ISO 9000:2005 -*** *Quality management system - Fundamentals and vocabulary*
- ***ISO 9001:2008 -*** *Quality management systems - Requirements*
- ***ISO 9004:2000 -*** *Quality management systems - Guidelines for performance improvements*
- ***ISO 9004:2000 -*** *Guidelines on Quality and/or Environmental Management Systems Auditing*

ISO 9000 standard family basics 1/4

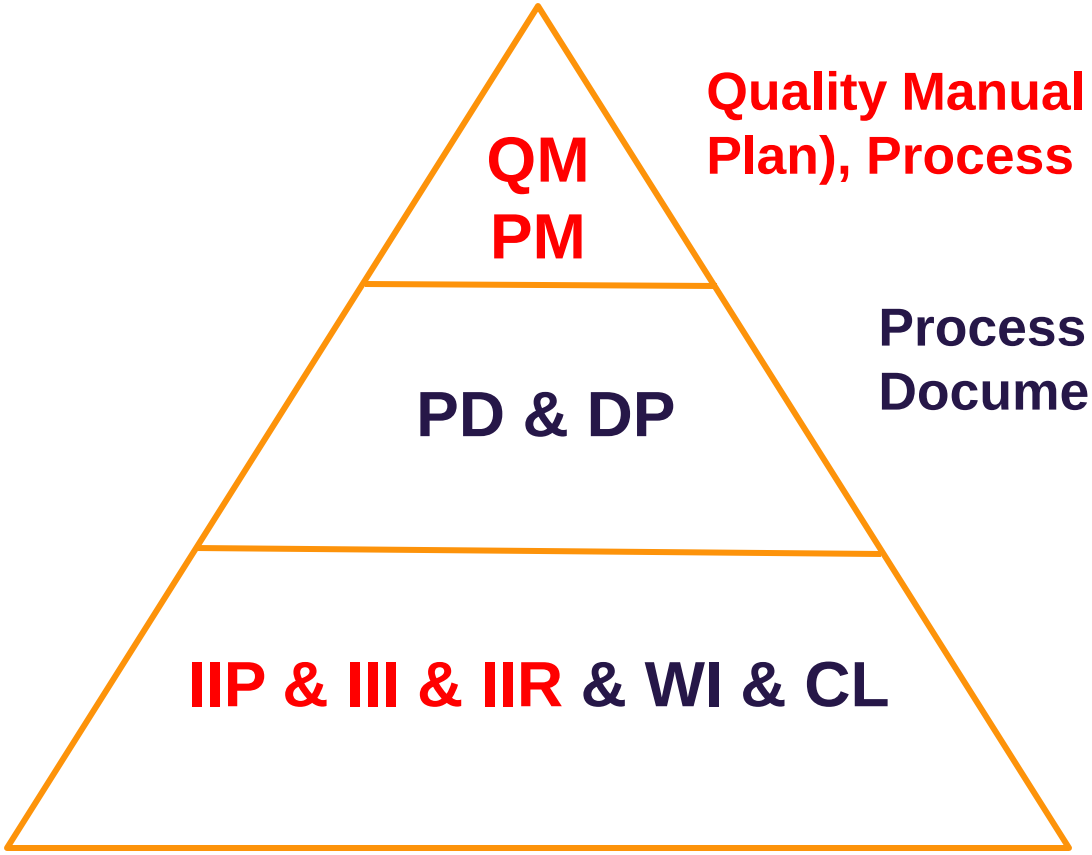


ISO 9001 requires for the project:

- quality manual describing the process-oriented structure of the WP02 (goals and the rules for QC/QA)
- definition of the processes, its sequences and interaction of processes
- definition of the documents (Process Descriptions, Documented Procedures, etc.) to control the processes
- control of documents and processes

ISO 9000 standard family basics 2/4

Documents



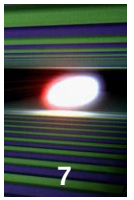
Quality Manual (Quality Management Plan), Process Map

Process Description & Documented Procedures

Incoming Inspection (Plans & Instructions & Records) & Work Instructions & Check Lists

Courtesy F.Eints

ISO 9000 standard family basics 3/4



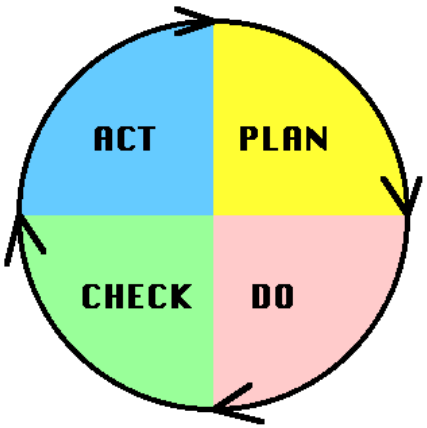
Six basic ideas for “Documented Procedures”

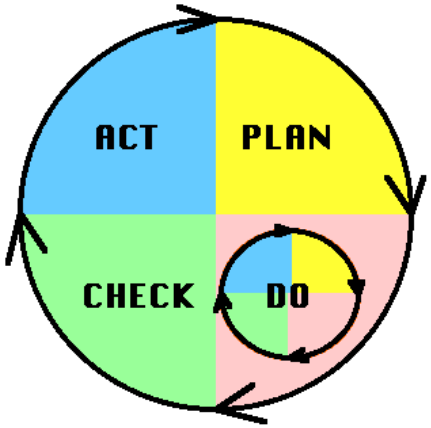
1. Control of documents
2. Control of records (i.e. : measurements, tests, etc.)
3. Internal audits (not foreseen by XFEL)
4. Control of “nonconformities” (i.e.: not conform products)
5. Preventive actions
6. Corrective actions

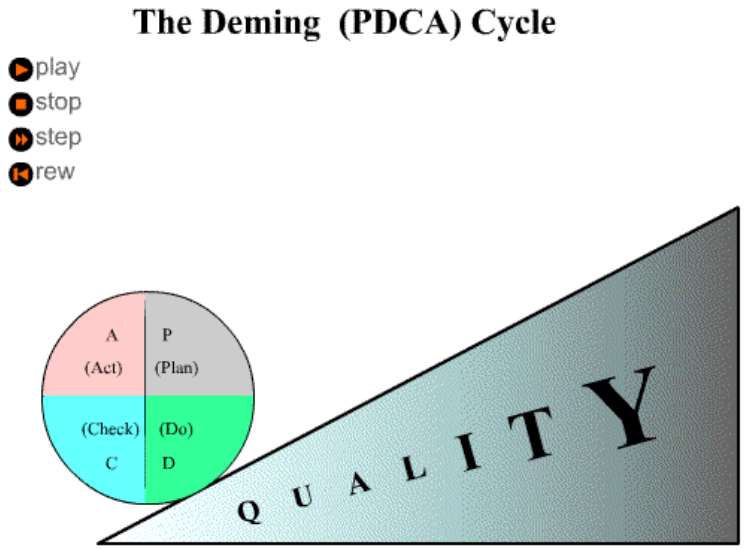
ISO 9000 standard family basics 4/4

PDCA, Deming Cycle

1. Plan. Recognize an opportunity and plan a change.
2. Do. Test the change. Carry out a small-scale study.
3. Check. Review the test, analyze the results and identify what you've learned.
4. Act. Take action based on what you learned in the study step: If the change did not work, go through the cycle again with a different plan. If you were successful, incorporate what you learned from the test into wider changes. Use what you learned to plan new improvements, beginning the cycle again.







QC/QA methods for WP02 1/9

WP02 – Hardware Breakdown

									Destinations ->	XFEL	Flash	AMTF	REGAE	PITZ	CMTB	Chechia	Vertical test Stand	Lab Test Stand	XFEL Test Stand	Production Test Stand	Spares	Total
										FL	?	?	MH	MH	?	?	?	?	?	?		
	#	Item	Type	Manufacturer	Responsible	Designer	Comment	Labels														
Modules	1	Container	Rack Container		WW	WW, MH		01		58	0?	4	0?	?	?	?	?	1	?	?	1	
	2	LOGM	19" module		MH	LZ, MZ		02		58												
	3	ADCM	19" module		MH	JP		03		58												
	4	REFM	19" module		HS	TL		04		58												
	5	PIEZOM	19" module		MG	KP		05		58												
	6	DWCADCM	19" module		TJ	JP, TJ		06		?												
	7	xTCA	xTCA crate		TJ	TJ		07		58		4	?	?	?	?	?	2	1?	1?		
	8	uRFB	xTCA backplane		KC	PP		08		58												
	9	xTCA PS	xTCA PS		TJ	TJ		09		58												
	10	uMCH	xTCA AMC		KR	KR	MCS	10		58												
	11	uCPU	xTCA AMC		KR	KR	MCS	11		58												
	12	uInterlock	xTCA AMC		KR	KR	MCS	12		58												
	13	uTiming	xTCA AMC		KR	KR	MCS	13		58												
	14	uADCHP	xTCA AMC		KR	KR	MCS	14		58												
	15	uADC	xTCA AMC	Struck	FL	Struck		15		326												
	16	uTLC	xTCA AMC		DM	DM		16		58												
	17	uAMCTEST	xTCA AMC		KC	DS.		17		?												
	18	uDWC	xTCA RTM		MH	JP, PB		18		326												
	19	uVM	xTCA RTM		KC	IR		19		58												
	20	uLOG	xTCA RTM	Itech	FL	Itech		20		58												
	21	TMCB	mezzanine	Itech	TJ	Itech		21		?												

Financial Codes

XFEL
Flash
AMTF
REGAE
PITZ

Preliminary!!!

QC/QA methods for WP02 2/9

WP02 – Software Breakdown

	#	Item	Firmware Responsible	Depends on	Server Responsible	Destinations ->	XFEL	Flash	AMTF	REGAE	PITZ	CMTB	Chechia	Vertical test Stand	Lab Test Stand	XFEL Test Stand	Production Test Stand	Total
							MG	VA	VA	MH	MH	WC	?	WC	?	?	?	
Tasks, Functions	1	RF controller (basic functionality)	Jalmuzna		Hensler		28	6	3	1	1	1	?	?	1	?	?	
	2	Board communication interface	Jalmuzna		Hensler		28	6	3	1	1	1						
	3	Piezo controller	Przygoda		Walla		26	3	3	0	0	1						
	4	Finite state machine		2	Hensler		28	6	0	0	0	0						
	5	Signal calibration (VS / GUN)	Jalmuzna	2	Ayvazyan		28	6	3	1	1							
	6	Quench detection/ handling	Jalmuzna	1,2	Ayvazyan		26	5	0	0	0							
	7	Detuning measurment /compensatior	Pzygoda	1,2	Pzygoda		27	5	3	0	0							
	8	Learning Feed Forward	Jalmuzna	1,2	Schmidt		28	6	0	1	1							
	9	Output Rotation correction	Jalmuzna	1,2	Schmidt		28	6	0	1	1							
	10	FF/SP trajectory optimization	Jalmzna	1,2	Schmidt		28	6	4	1	1							
	11	Beam loading compensation	Jalmuzna	1,2	Schmidt		27	5	0	0	0							
	12	Exception detection/ handling	Jalmuzna	1,2	Schmidt		28	6	0	1	1							
	13	Performance statistic measurments		1,2	Cichalewski		28	6	3	1	1							
	14	DAQ		1,2	Cichalewski		28	6	0	0	0							
	15	Calibration box software	Jalmuzna	1,2	Szewinski		54	6	0	0	0							
	16	Controller parameter design	Jalmuzna	1,2	Pfeiffer		28	6	0	0	0							
	17	Beam based control	Jalmuzna	1,2	Schmidt		5	6	0	0	0							
	18																	
	19	Breakdown																
	20	Front end server applications			Hensler		56	6	3	1	1							
	21	Middle layer server applications			Hensler		28	6	0	1	1							
	22	Interconnection RF station			Schmidt		20	6	0	0	0							
	23	Cavity tuning applications			Ayvazyan		28	5	3	0	0							
	24	Module test routines	Jalmuzna		Ayvazyan		1	1	3	1	1	1						
	25																	

Financial Codes

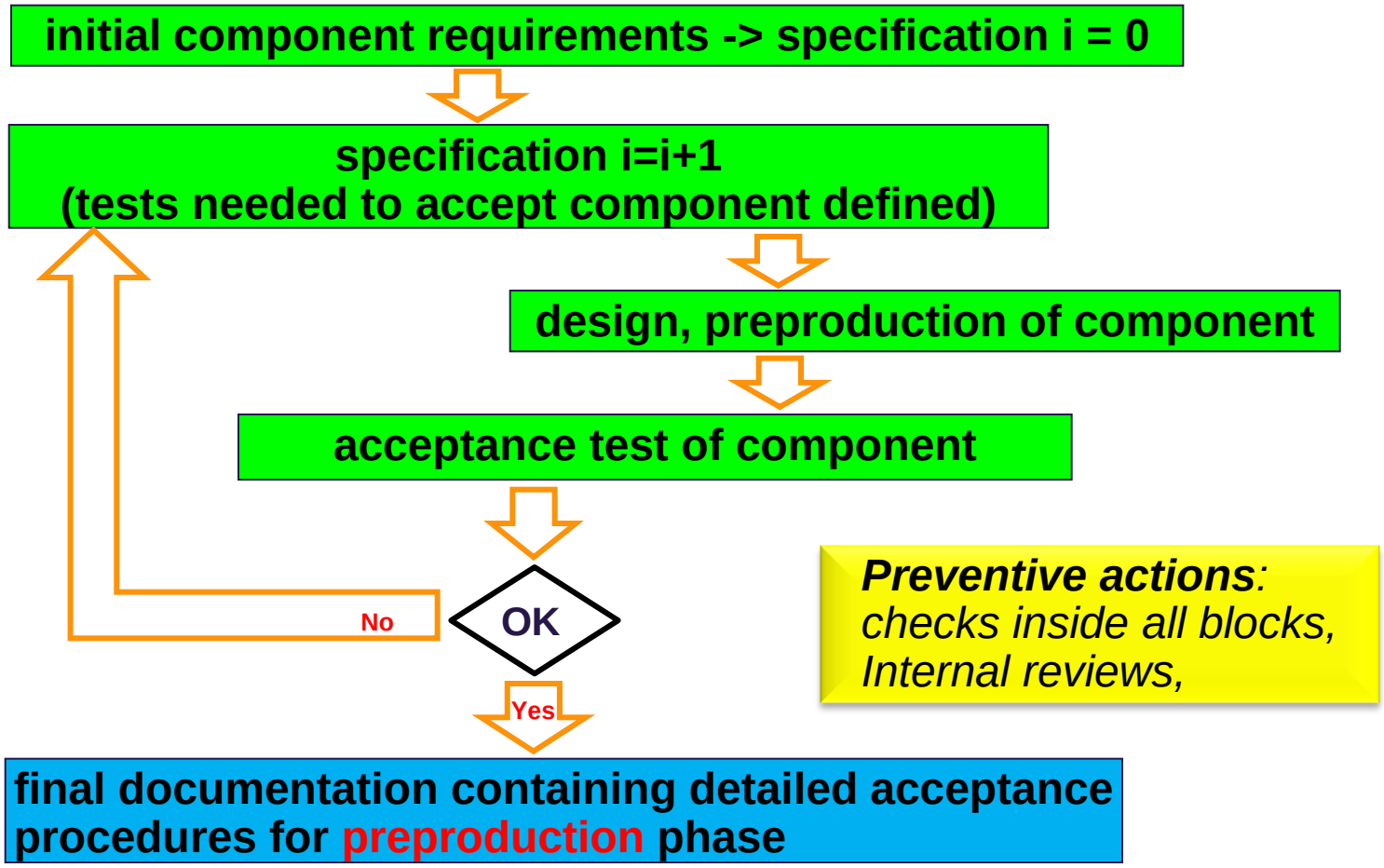
XFEL
Flash
AMTF
REGAE
PITZ

Preliminary!!!

QC/QA methods for WP02 3/9

For design (prototype) phase:

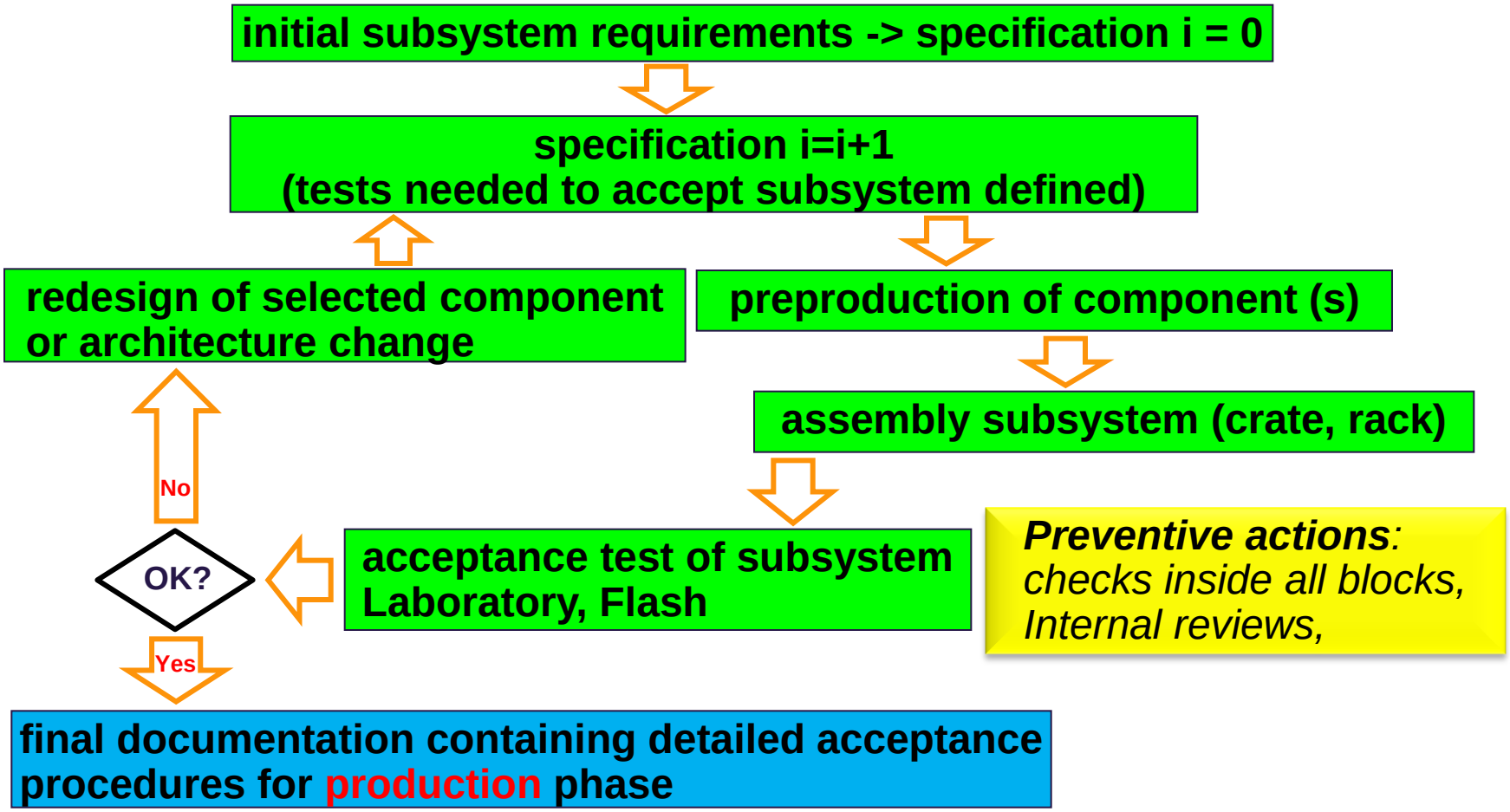
PDCA (Plan, Do, Check, Act) Cycle = (Deming Cycle)



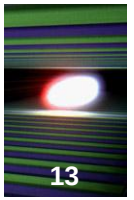
QC/QA methods for WP02 4/9

For design (preproduction) phase:

PDCA (Plan, Do, Check, Act) Cycle = (Deming Cycle)



QC/QA methods for WP02 5/9

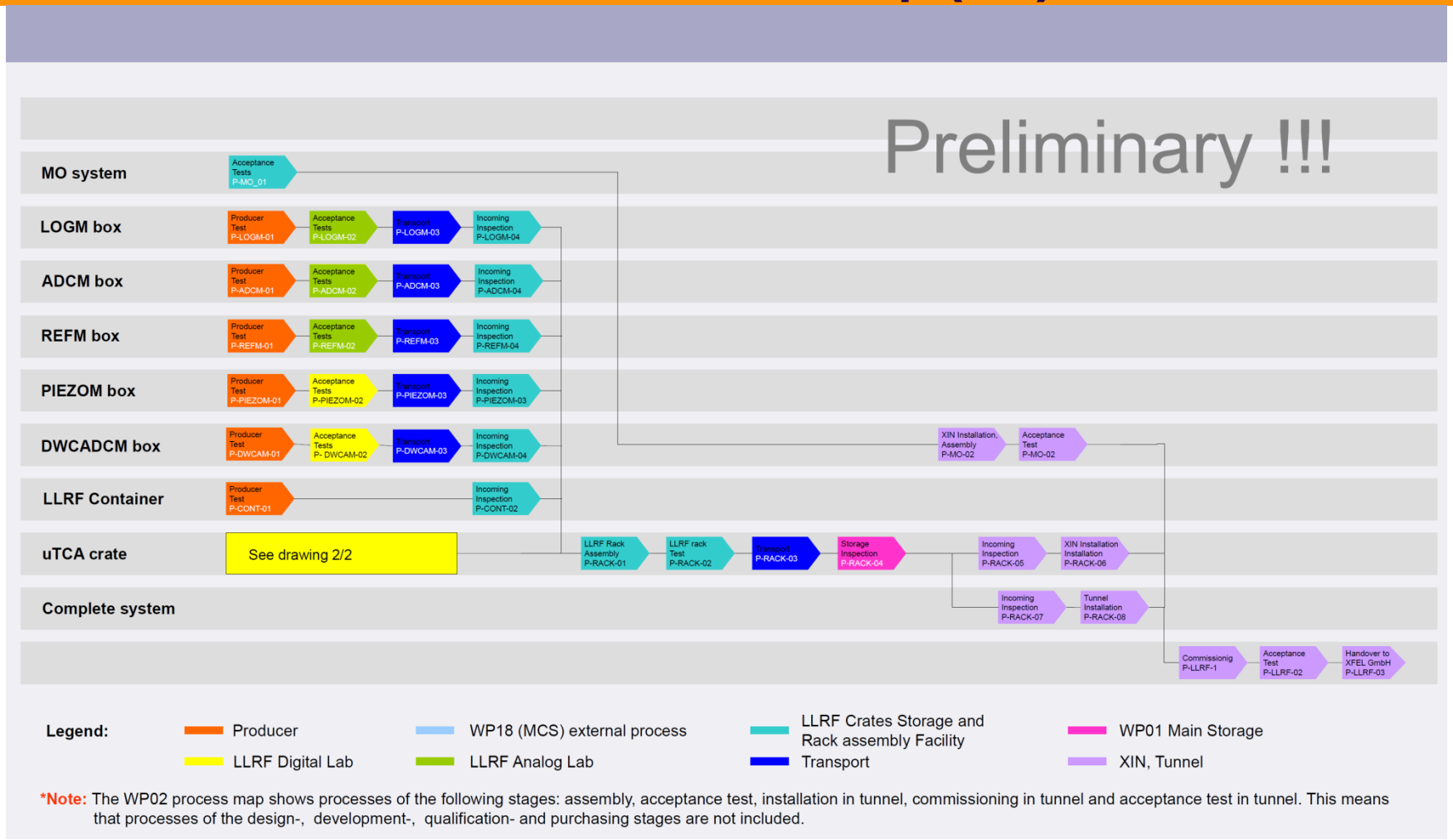


For the production phase following procedures (steps) are proposed:

1. producer tests (*established by producer and WP02*) -> Producer Test Report (PTR)
2. incoming test at DESY -> Incoming Inspection Report (IIR) (following Incoming Inspection Plan (IIP) and Incoming Inspection Instruction (III))
3. assembly to the crate, rack or other functional entity and functional tests -> Assembly Inspection Report (AIR)
4. transport to the storage

QC/QA methods for WP02 6/9

WP02 Process Map (1/2)

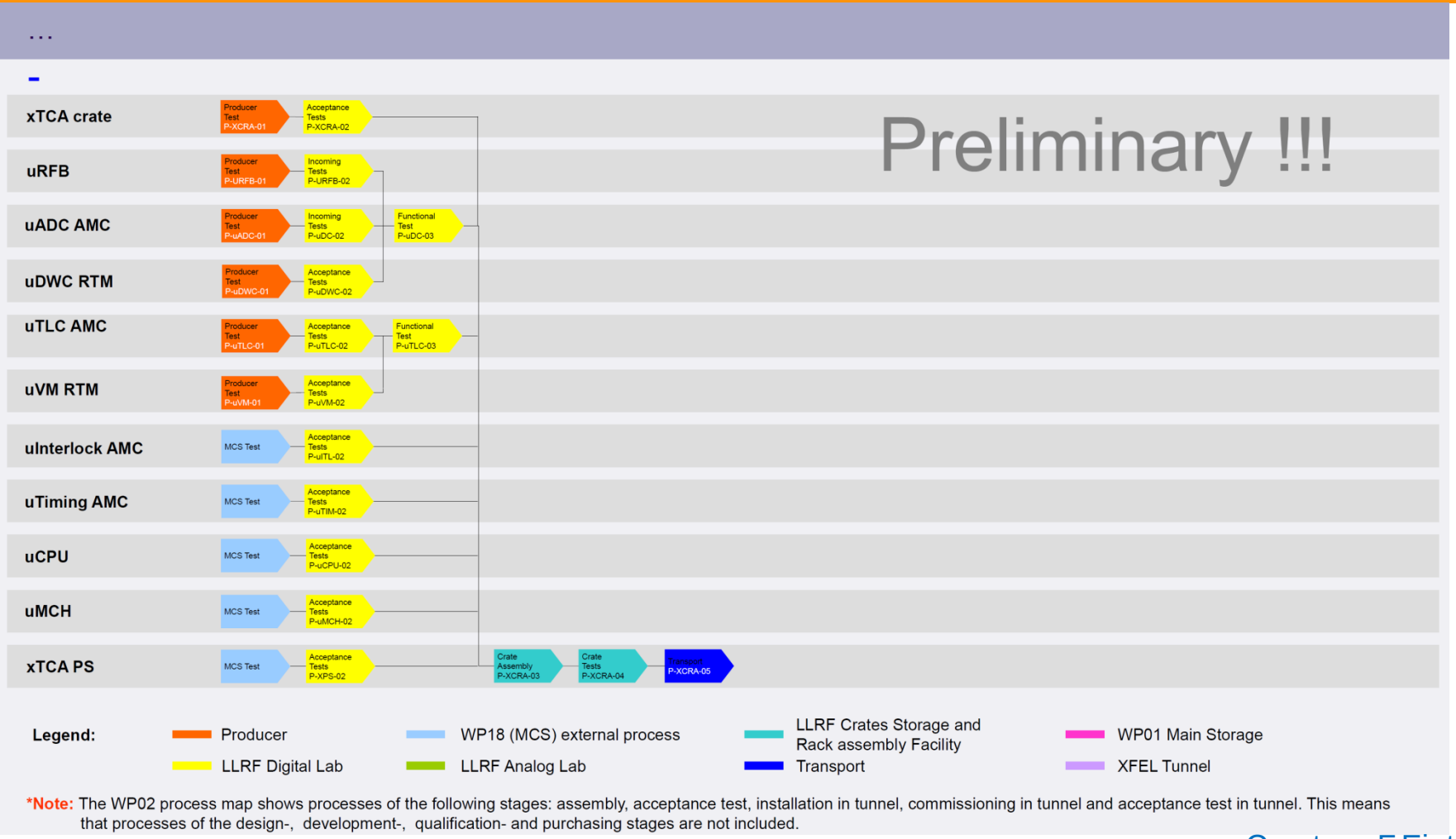


*Note: The WP02 process map shows processes of the following stages: assembly, acceptance test, installation in tunnel, commissioning in tunnel and acceptance test in tunnel. This means that processes of the design-, development-, qualification- and purchasing stages are not included.

Courtesy F.Eints

QC/QA methods for WP02 7/9

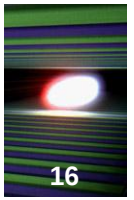
WP02 Process Map (2/2)



*Note: The WP02 process map shows processes of the following stages: assembly, acceptance test, installation in tunnel, commissioning in tunnel and acceptance test in tunnel. This means that processes of the design-, development-, qualification- and purchasing stages are not included.

Courtesy F.Eints

QC/QA methods for WP02 8/9



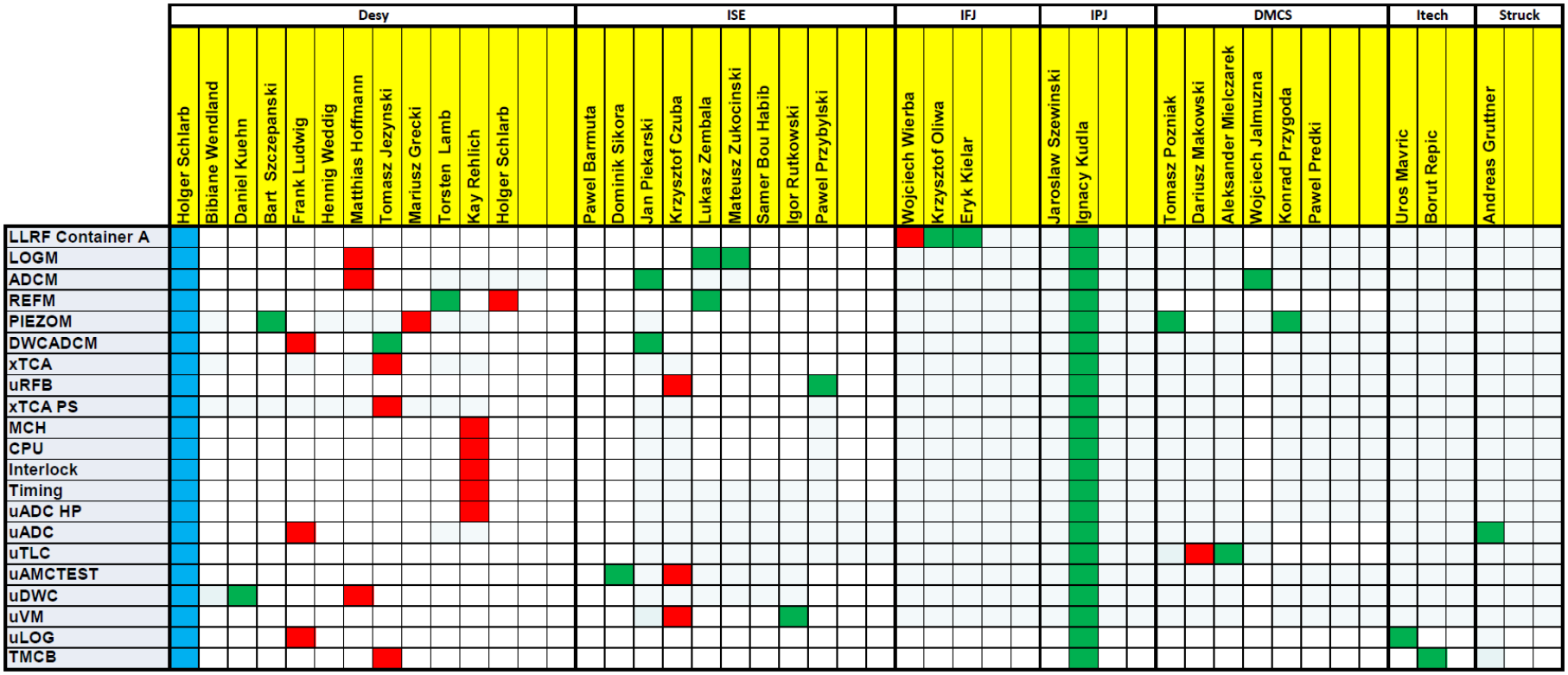
All design documents are stored on MSK disk (EDMS) in the common file structure (e.g.):

- 0Schedules&Plans
- 1Specification (FL template)
- 2Design
  - 21Version 1…
    - 211Schematics
    - 212PCB
    - 213Assembly
    - 214Tests
    - 215DesignFeedback
  - 2nFinal version
- 3Datasheets
- 4Final documentation
  - 41Manual
  - 42QA Docs

A sample of such structure is on MSK disk:
\mkudla\public\uTCA_DWC8300_RTM_PROPOSAL

QC/QA methods for WP02 9/9

WP02 Hardware Responsibility Chart (Version 1.0)

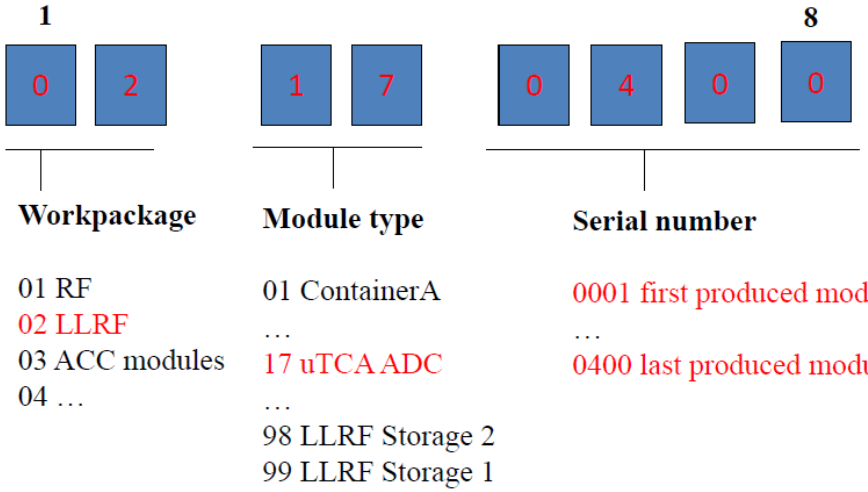


Process Owner
Process Responsible
Process Assistance

Preliminary!!!

QC/QA methods for WP02 10/9

WP02 labeling and Hardware DB Proposal



Preliminary!!!

The smallest label (for AMC modules)

„Double Click" procedure (installation, deinstallation) proposed to KDS support (under discussion)

Fields																					
Names				Version				Labels				Software (SVN, CVS)			Quality Docs (EDMS documents)				Others		
Item name	Item Abbreviation	Item Type	Item contact	Version	Revision	Ordering Option	Manufacturer	Desy Receiving Date	Producer Serial Number	Electronic Key	WP02 Label or MCS Label	Firmware Reference	MMC Software Reference	DSP Reference	Producer Test Report	Incoming Inspection Plan (IIP)	Incoming Inspection Instruction (III)	Incoming Inspection Record (IIR)	Link to History Events	Link to Graphical Interface (cables)	Location
xTCA_ADC_AMC	uADC	xTCA AMC	FL	1.0	2.0		Struck				02_15.0001_000						P_ADCA_2				02_07.0002_000
xTCA_ADC_AMC	uADC	xTCA AMC	FL	1.0	2.0		Struck				02_15.0002_000						P_ADCA_2				
xTCA_ADC_AMC	uADC	xTCA AMC	FL	1.0	2.0		Struck				02_15.0003_000						P_ADCA_2				02_98.0021_000
		xTCA_RTM																			
xTCA_uTL_AMC	uTLC	xTCA AMC																			
xTCA_LLRF_Crate	xTCA	xTCA_crate									02_07.0002_000										02_01.0021_000
Container	Container	Rack Container									02_01.0021_000										
LLRF_Storage1	Storage1	LLRF_Storage									02_98.0021_000										

QC/QA methods for WP02 11/9

WP02 Incoming Inspection Plan IIP (sample)

Some general remarks:

- All designed functionalities should be tested,
- All specified performances should be checked,
- Elaboration of final IIPs essential for preproduction/production stage is an iterative process made during the design stage
- All device designs should be preceded by device specifications

DESY	WP02	Low Level RF	Quality Assurance Management
uTLC_AMC module Incoming Inspection Plan			P-UTLC-2_IIP

Created M.Kudla	Initial date 07.03.2011	Revision no. 1.0 (30.03.2011)

1. Process overview			
Trigger of procedure P-UTLC-1	**Process owner** Holger Schlarb (WP02)	**Involved in procedure** D.Makowski, M. Kudla, P.Mielczarek	**Customer of procedure** P-UTLC-3
Purpose:	Acceptance tests of uTLC board. Board commissioning - functionality tests.		

~Etc.~

2. Process sequence I

Input	Process step	No	Involved	Output
Component types: uTLC v1.0				
	Preparation of WP02 labels	1	Kudla	Label
	Updating of WP02 Equipment list with received modules 1. WP02 label (on board and on front panel) 2. PCB serial label 3. Module Electronic Id. Number 4. Firmware Startup (Version & Revision) 5. Ordering options	2		
	Visual inspection (soldering of components, connectors, etc). Fitting to crate, to backplane, to RTM.	3		
	Supply voltage and currents checks	4		
	MMC, board configuration tests (IPMI)	5		
	Clock performance tests	6		
	FPGA downloading check (Jtag, IPMI, PCIe, PROM, SPI)	7		
	PCIe performance tests*	8		
	QDR/DDR2/Flash memory tests	9		
	DSP and its FPGA interface tests (max. transfer speed, interrupt handling time measurements)	10		
	SFP performance tests*	11		
	GbE performance tests*	12		
	RIOs performance tests*	13		
	RTM interface check	14		
	Front panel In, Out signals check	15		
	Backplane signals - interlock, clock A/B, trigger (MLVDS) tests	16		
	Front panel LEDs and on board switch check	17		
	Voltage, currents (voltage ripples, transients) at full board load measurements	18		
	WP02 Equipment list update with received module location and status	19		

~Etc.~

Courtesy F.Eints

QC/QA methods for WP02 12/9

WP02 Incoming Inspection Instruction III (sample)

DESY	WP02	Low Level RF	Quality Assurance Management
ADC_AMC module Incoming Inspection Instruction - Clock Quality			P-ADCA-2*6

Created M.Kudla	Initial date 07.03.2011	Revision no. 1.0

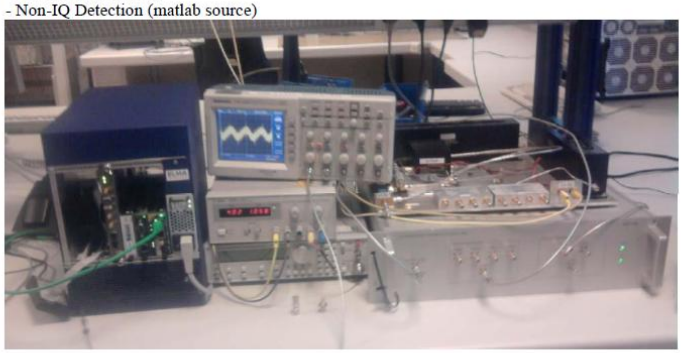
1. Process overview

Trigger of procedure	Process owner	Involved in procedure	Customer of procedure
P_ADCA_2	Holger Schlarb (WP02)	F. Ludwig, M. Kudla,	P_ADCA_3

Purpose:	Acceptance test of changes made in SIS 8300 v1.0 rev2.0 in clock signal routing.
Scope:	XFEL project
Phases:	Prototype v1.0 rev2.0 tests

~Etc.~

2. Process sequence I

Input	Process step	No	Involved	Output
Component types: SIS 8300 v1.0 r2.0				
	Setup test stand as described in: **DWC8300_SIS8300_Distortions\06_01_11_SIS8300_DWC8300\Summary** and The following components were used for the SIS8300, DWC8300 configuration: - DWC8300 Rev.1.0 (Supplied by external low noise power supply, uRTM meanwhile ready) - SIS8300 5/10, #004 - SSA E5052B, Agilent Phase Noise Analyzer - Differential to single Probe (self made using mini-circuit transformer) - 19" LO-Generation Module 1300MHz -> 1354MHz, 1309MHz, 3.3V output - ELMA uTCA crate - PSI 1.3GHz DRO - FPGA ADC readout - Non-IQ Detection (matlab source) 			
	Measure clock jitter at at the U230 phase shifter input	2		screenshot
	Measure clock jitter at the SIS8300, U230, AD9510 input at	3		screenshot

~Etc.~

	powered OFF			
	Measure RTM clock signal at U230 (pins:10,11)	10		Screenshot
	Measure ADC4 clock signal at U71 (pins:1,2)	11		Screenshot
	Prepare the report referring to the **DWC8300_SIS8300_Distortions\06_01_11_SIS8300_DWC8300\Summary**	12		Report

Courtesy F.Eints

Closing remarks

- For the success of QC/QA the collaboration of all members of WP02 team necessary. I am open to review presented ideas and I count on your help,
- Quality Management Plan (preliminary) for CDR prepared following XFEL template recommendations,
- Slide templates on process map and responsibility table comes from Frank Eints (WP01). I am also very grateful to him to practical introduction into the QC/QA issues