

AMC ADC Digitizer (SIS8300).

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LLRF – Collaboration Workshop

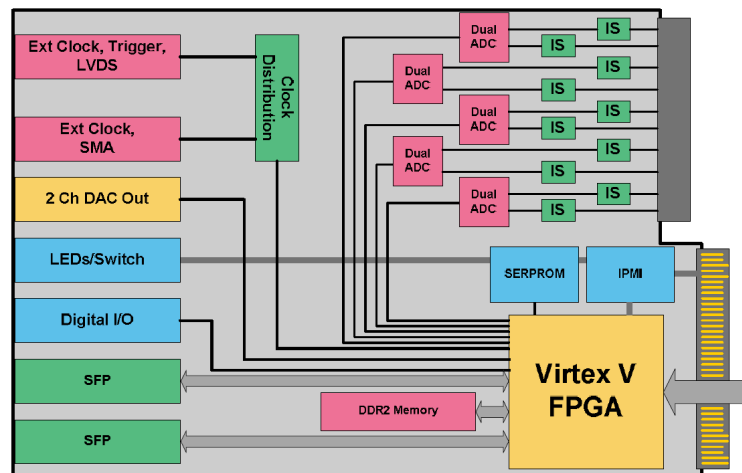
Cracow, 19.04.2011

SIS8300 – Overview.

Functionality:

- ◆ Double size μ TCA for Physics Board
- ◆ 4 Lane PCI Express Interface
- ◆ Dual SFP Card Cage for optional Multi Gigabit Link
- ◆ Xilinx Virtex 5 FPGA
- ◆ DDR2 Memory Interface
- ◆ 4 x 1 GBit default DDR2 memory
- ◆ Atmega128 IPMI
- ◆ External Clock and Trigger Inputs
- ◆ Frontpanel digital I/O (4in/4 out) on Harlink Connectors
- ◆ RTM ADC Analog Inputs, I2C-Bus
- ◆ 10 ADC Channels 125MS/s, 16-Bit
- ◆ 2 DAC Channels 125MS/s, 16-Bit
- ◆ Clock distribution with phase shifting
- ◆ 4 M-LVDS μ TCA Ports
- ◆ 2 μ TCA Clocks

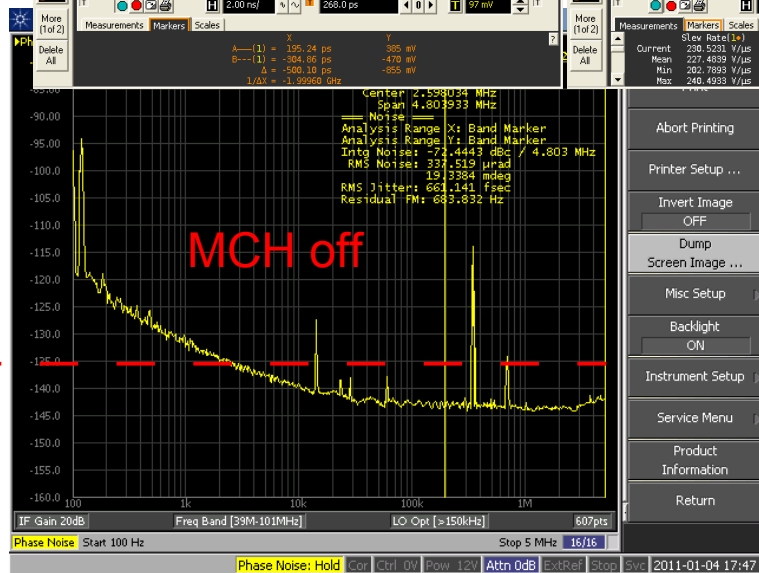
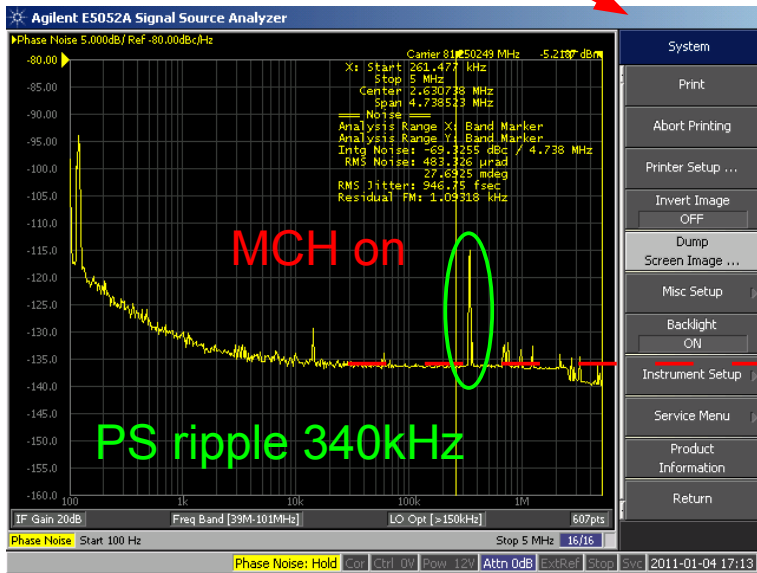
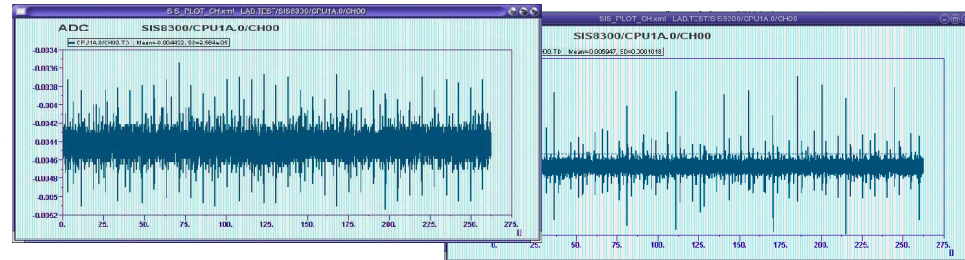
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Analog Input & Clock Tests.

> Layerstack/Routing violations

- Distortions on ADC inputs
- Spurious from PS (DC/DC 340kHz)
- Weak grounding of AGND
- Matching
- Crosstalk



81MHz CLK Phase Noise

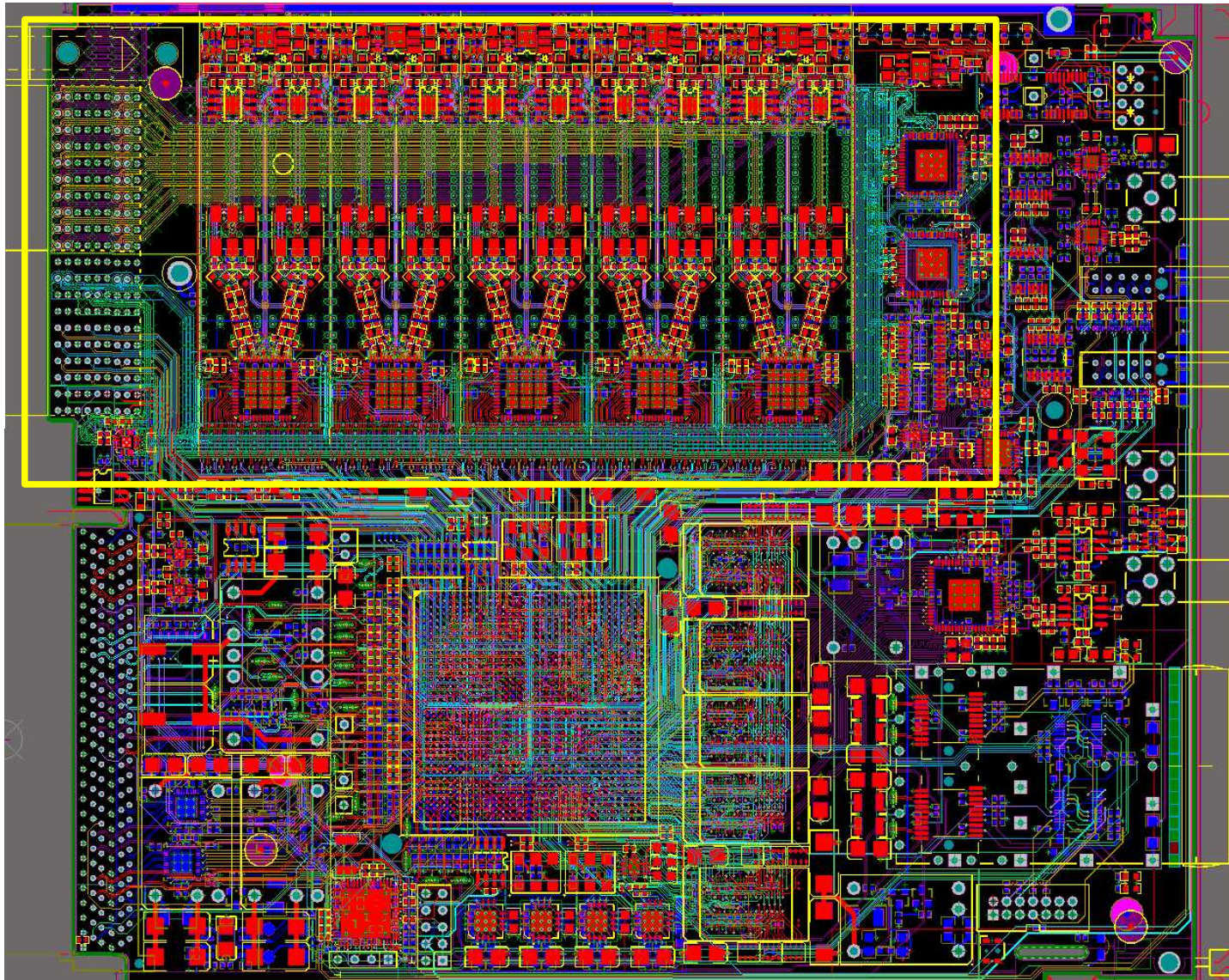


Version 1 to Version 2.

- Programmable MGT clock (10 or 25MHz Steps) (optional assembly)
- Components in ADC signal conditioning channel has been removed
- Change of ADC DC input connection on Zone3 connector (reversed numbering)
- RTM clock 2 configurable for PECL logic (optional assembly)
- New DAC chip (MAX5878)
- Onboard PCIe clock (optional assembly)
- Changes of power supply to get less ripple and noise
- Changes for better signal quality of ADC channels (rerouting signal lines)
- Improve layerstack and routing of CLK lines



Board Layout of SIS8300 V2.



Current Situation / Outlook.

Status:

- > Last week: Boards in assembly process
 - > This week: Debugging boards at Struck company
 - > (probably) Next week: boards will be send to DESY
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Outlook:

- > Tests of SIS8300 V2
 - Added jitter by clock distribution
 - Ripple on power supply
- > SIS8300 V2 and DWC8300 V1.0 or V1.1 (if available)
 - IF sampling tests at 54MHz and 9MHz
- > Complete test with uTLC, uVM, SIS8300 and DWC8300

