

Status of the CERN SPS MicroTCA Low Level RF

Arthur Spierer, 5th December 2023



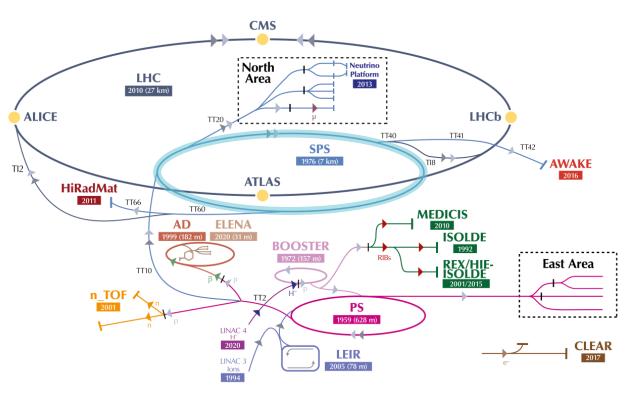
- Motivation for the SPS LLRF upgrade with MicroTCA
- Review of the system architecture and hardware
- Feedback after 3 years of operation



Motivation

High-Luminosity LHC (HL-LHC) -> injectors upgrade, including the SPS

- Doubling proton intensity -> 4 to 6 200 MHz cavities
- New LLRF HW required for the additional cavities
- System obsolescence
- Individual control the cavities (ion slip-stacking)
- MicroTCA
 - COTS
 - White rabbit integration
 - PCIe bandwidth
 - P2P & trigger lanes
 - Redundancy & remote diagnostics

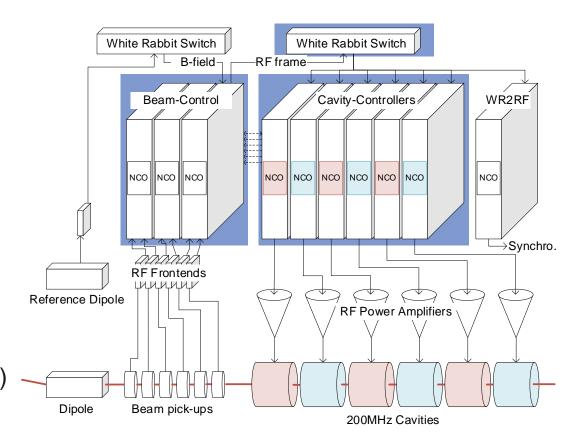




Architecture

• MicroTCA

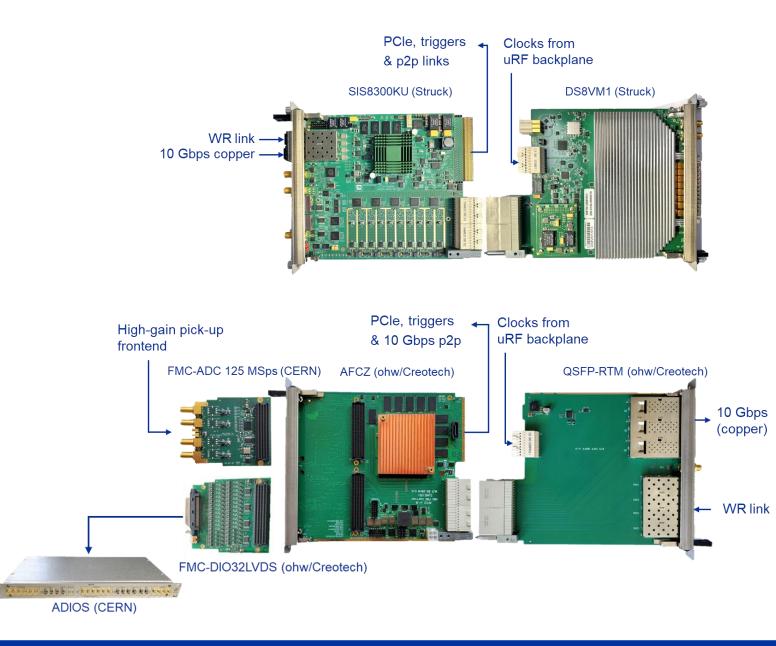
- Beam-Control: beam-base loops, frequency program
- 200 MHz Cavity-Controllers: fast feedbacks
- eRTM14-15: clock and LO generation
- Fits in two crates
- White-Rabbit based RF synchronization
- VME
 - 800 MHz Cavity-Controllers (operational in since 2016)
 - WR2RF: generation of beam-synchronous signals





Hardware

- 6x 200 MHz Cavity controllers
 - 125 Msps ADCs
- 2x Beam-based measurements
 - 5 Gsps &125 Msps ADCs
- 1x Beam control
 - 125 Msps ADCs





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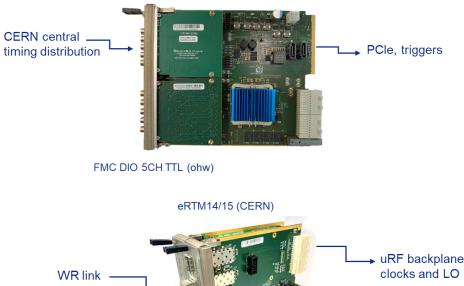
Hardware

• Crate 9U with RF backplane MTCA.4.1 (Schroff)

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- NAT-MCH
- NAT COMEx (RTM of MCH)
- 4x 600 W NAT Power modules
 - One for eRTM with FW upgrade (no need for analog supplies)
- Central Timing receiver
 - CTRA (Creotech AFC + FMCs)
- Clock distribution
 - eRTM14/15 (CERN ohwr)





USB controls



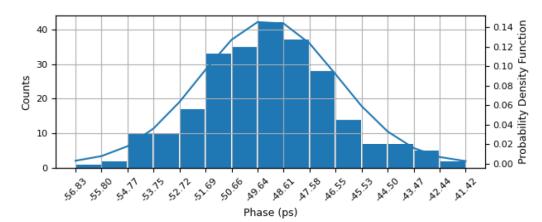
Clock & LO generation

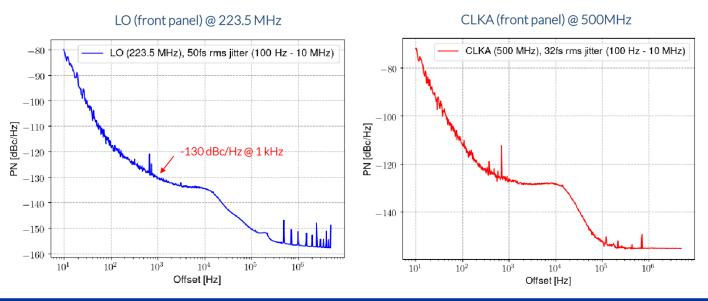
Temperature range (degC): • crate: 26.45 – 28.74 (Δ 2.29)

- crate: 26.45 28.74 (Δ 2.29
- lab: 24.89 26.68 (Δ 1.80)
- WRS rear: 26.14 27.84 (∆ 1.70)
- μ = -49.1927 ps; σ = 2.7105 ps; pk-pk = 15.413 ps



- Clock phase reproducibility = WR reproducibility
- Full characterisation ongoing with WR switches in cascade
- eRTM 14/15 phase noise performance

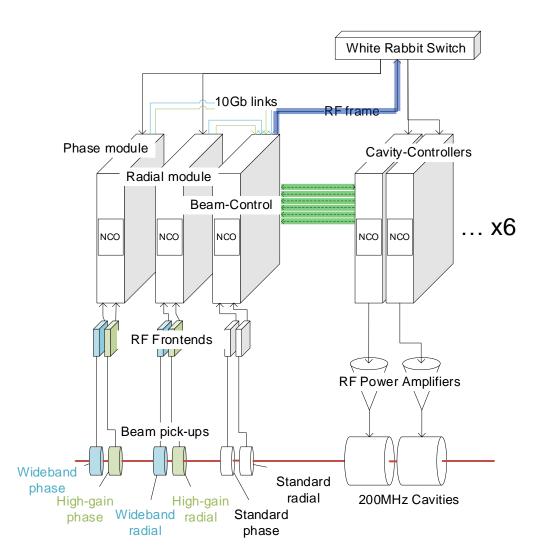






Beam-Control

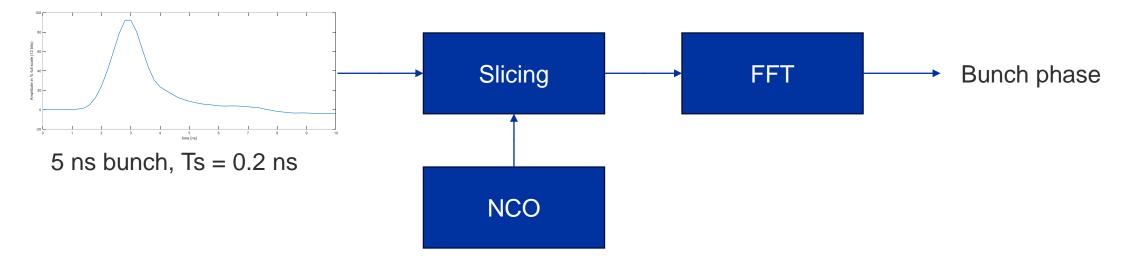
- Generates WR RF frame
 - Frequency Tuning Words + NCO resets
- Computes beam loops
 - From cavity voltages (10 Gbps copper attach)
 - From beam pick-ups (10 Gbps backplane/copper attach)
- Synchronizes with target machines
 - Samples pulses from Digital I/O FMC





Beam-based measurement

- Bunch-by-bunch measurement using a 5 Gsps fixed clock ADC
 - Beam phase loop, longitudinal damper, coupled-bunch instabilities analysis

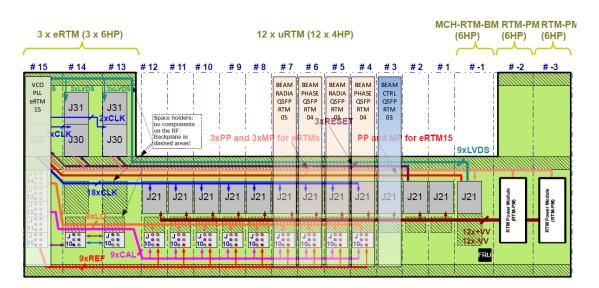


- Wish to go to 10 Gsps using FMC+
 - Necessity to have full control over the FW for real-time processing and CERN controls integration

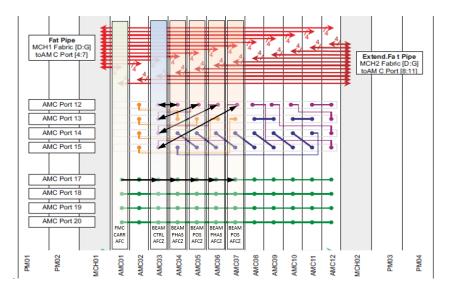


Beam-based measurement

- Clocks over RF backplane
- 10 Gbps p2p links over backplane
- Machine timing over backplane MLVDS
 - (No WR option)









Operational experience 1/2

- Excellent availability of the MTCA infrastructure (crate, PS, MCH & CPU)
 - Some crashes and power up failures due to MMC / i2c handling issues
- Grafana crate monitoring & logging
- Flashing over PCIe
 - Not obvious with MPSoC
- Direct sampling + WR synchronization
 - Limited need for calibration throughout the year

\$	88 BE-CEM-IN / M	icroTCA NAT Crate	Details				
а.	ОК			ОК		ок.	OK 172.18.194.219 rta 0.362
88	Upper Fan Tray	Lower Fan Tray	RTM	eRTM14	eRTM15		Historic Main Status
	ОК	OK	ок	OK	OK		
	MCH	MCH Clock	MCH PCle				
	OK	ОК	OK	eRTM14 Insert YES	eRTM15 Insert YES	-1 -05:00 06:00 07:00 08:00 - 0=0K 1=Warning 2=Error 3=Down	
	Power Supply 1	Power Supply 2	Power Supply 3	Power Supply 4	Power Supply 5	Historic Modul	les Status 0=OK 1=Warning 2=Error 3=Down
	No data	OK	ОК	OK	OK		
	PS1 Inserted	PS2 Inserted	PS3 Inserted	PS4 Inserted	PS5 Inserted		
	No				YES		
	Role M No data No data	Role M	Role M	Role M	Role M	05:00 06:00 07:00 06:00 — PS2Status — PS4Status — RTMStatus — MCHSta — eRTM14Status — eRTM15Status — PS5Status	09.00 10.00 11.00 12.00 13.00 atus — MCHClockStatus — MCHPoleStatus — FANTrayDownStatus — FANTrayUpStatus
	Yower Supplies						
	PS1 3.3V	PS2 3.3V	PS3 3.3V	PS4 3.3V		Power Supply 1 Temperatures	Power Supply 3 Temperatures
	PS1 12V	PS2 12V	PS3 12V	PS4 12V		No data	40 - mtcaPS3TempXFrm 44
							30 mitcaPS3TempPFC 36
	PS1 VIN AC	PS2 VIN AC	PS3 VIN AC	PS4 VIN AC			10 mtcaPS3TempREC 27
	POT VIN AC	222 V	222 V	224 V			0



Operational experience 2/2

• Rear power supplies

- Redundancy is expensive, could standardize power from front PS to eRTM
- No standard datalink for the eRTM from MCH CPU
- eRTM 15 cooling issue (too low airflow)
 - Customized fan tray for rear power module but not possible simultaneously for eRTM15 (Schroff), some other experiences?

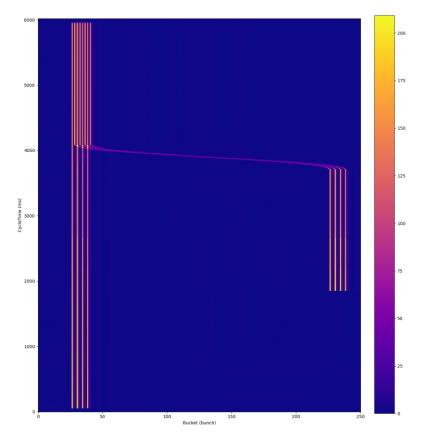
• Memory map generation tool Reksio/cheby now open source

• Support for PCIe address space, axi & whishbone buses



Results & outlook

- Reached target intensities
- First slip-stacked beams extracted to LHC
- MicroTCA & RF over WR will be used for future designs
 - HL-LHC upgrades and crab cavities
 - PS 200 MHz
- AFCZ possible upgrade to support FMC+





Acknowledgement

CERN LLRF

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CERN BE-CEM (WR & Controls)

M. Lipinski, J. Palluel, M. Rizzi, J. Serrano, T. Wlostowski,



Questions?

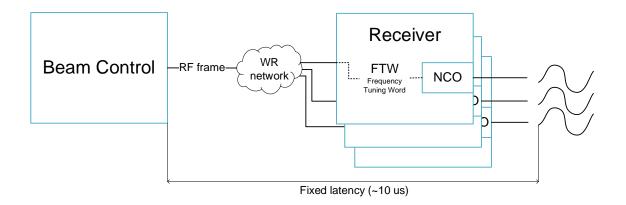


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RF over WR

- Numerically Controlled Oscillator
- Synchronized over White Rabbit (WR) network (Ethernet + precision timing)





References

• eRTM14/15, WR precision & thermal issues

• https://indico.desy.de/event/31387/contributions/113538/attachments/70479/89731/desy_mtca_workshop_2021_final.pdf

• 200 MHz Cavity controllers

- https://indico.desy.de/event/31387/contributions/113585/attachments/70462/89707/MTCA_2021_CERN_SPS_CavityController_hagmann.pdf
- HL-LHC and Crab cavities MTCA LLRF
- SPS beam control
 - https://cds.cern.ch/record/2845762?In=en
- Beam-based measurements
 - https://inspirehep.net/files/691b7c597f838f13a4dd8f9fdc9dabf5
- Memory map management
 - https://gitlab.cern.ch/Cheburashka/gui

