Summary of ongoing MTCA projects at SOLEIL

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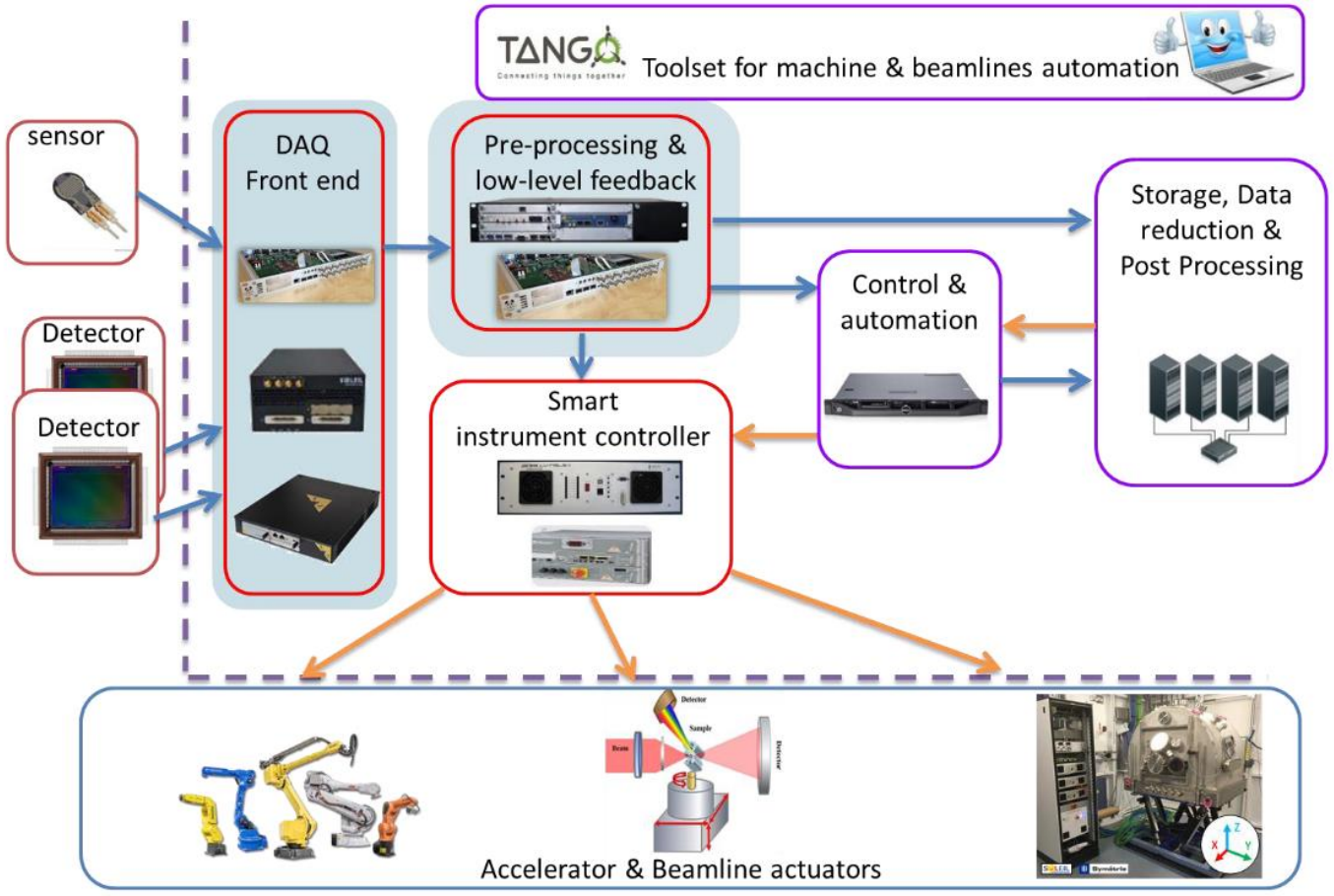
Presentation outline

- **MTCA integration strategy**
- LLRF application at SOLEIL
- Fast Orbit Feedback application at SOLEIL

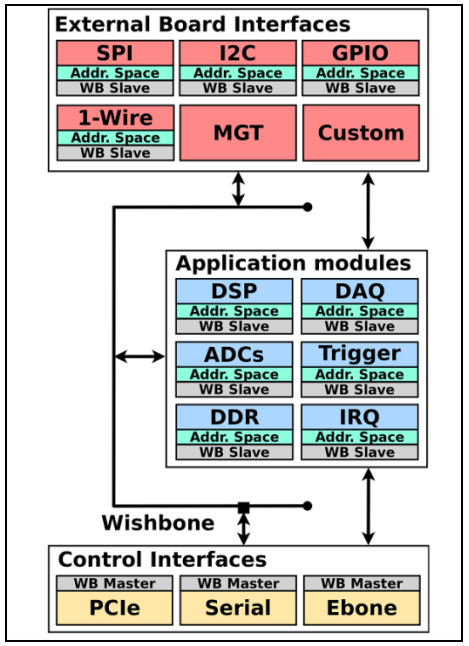
MTCA at SOLEIL

- 3rd generation synchrotron light source
- **SOLEIL II**: Upgrade scheduled in oct. 2028
- MTCA selected as one of the platform for acquisition

  Applications: sensor / detector acquisition, FOFB, LLRF, more to be defined

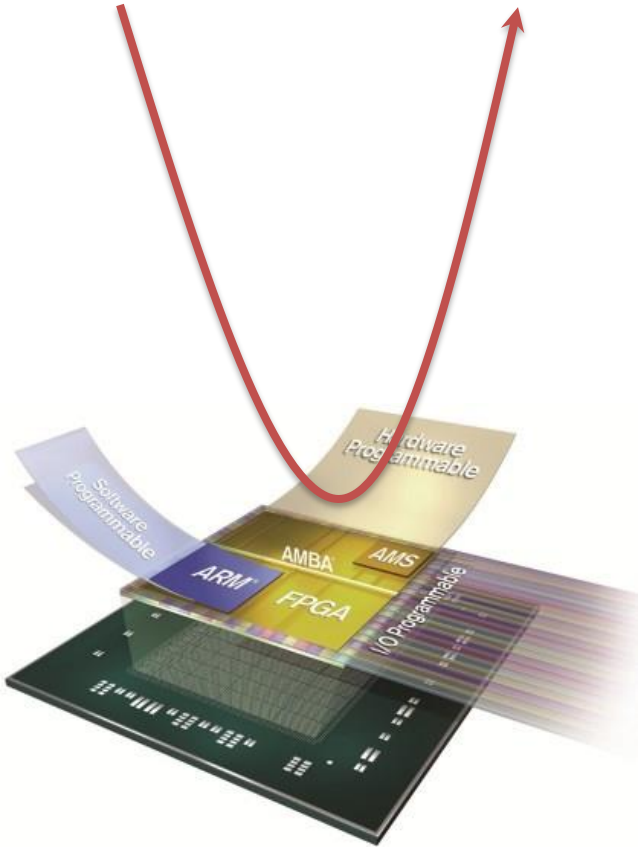


Modular Interfacing & Processing

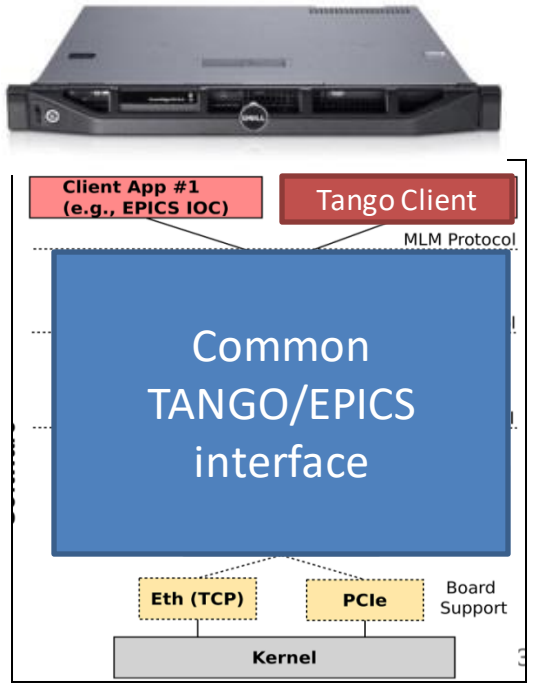


Gateware

Data flow



Control Framework Ready

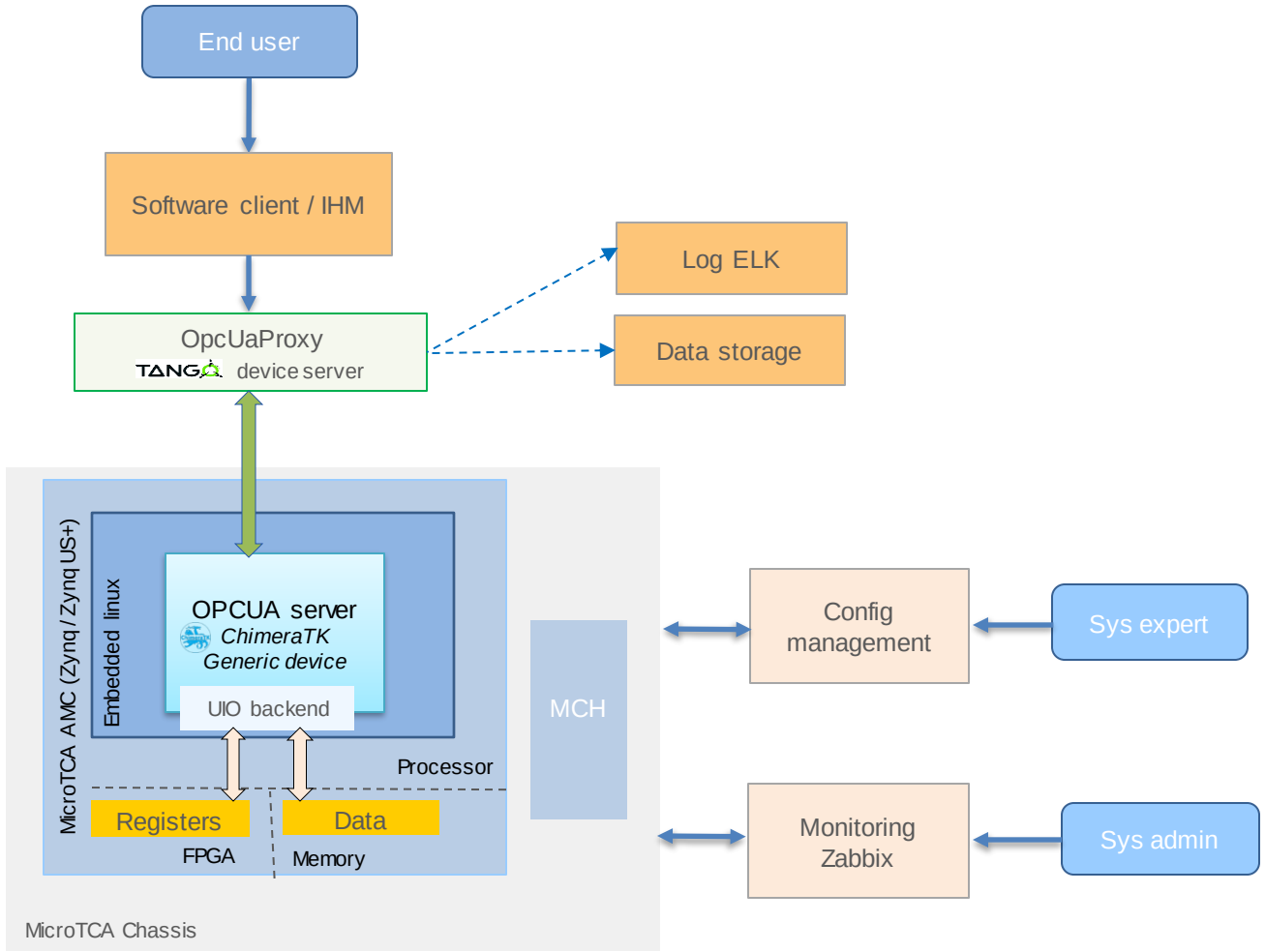


Software

Modular Powerful Connectable

Flexible Framework architecture

MTCA integration strategy : architecture

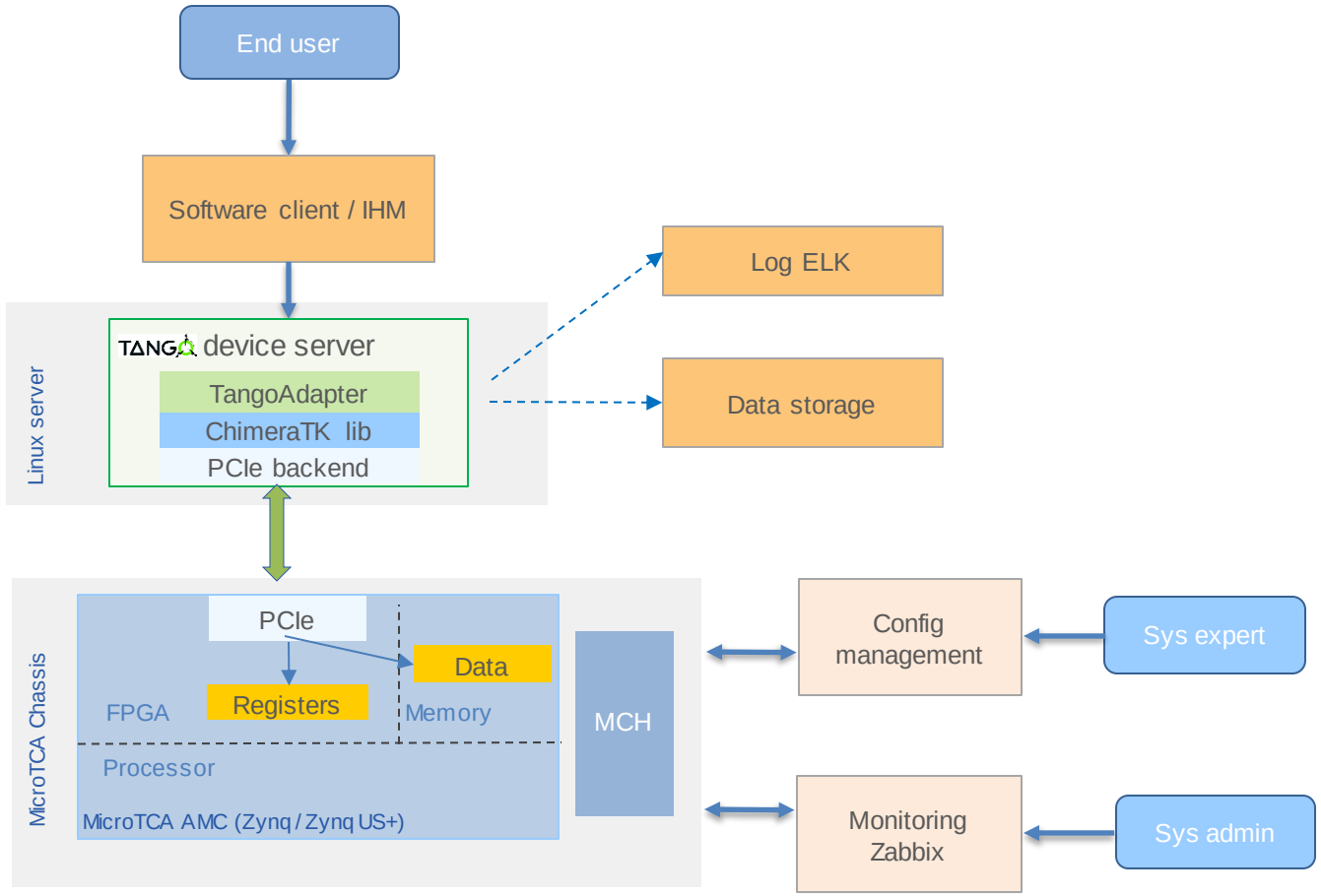


First architecture

- Embeded linux
  - ChimeraTK generic device takes FPGA data from AXI bus and expose them in OPCUA server
- OpcUaProxy
  - Tango device server as OPCUA client
  - Communicate with OPCUA server through ethernet
- Ongoing deployment on the FOFB upgrade project by Diagnostic group

* OpcUaProxy: developed at Synchrotron SOLEIL, using Eclipse Milo library
Available at git@gitlab.synchrotron-soleil.fr:software-control-system/tango-devices/communication/opcuaproxy.git

MTCA integration strategy: architecture

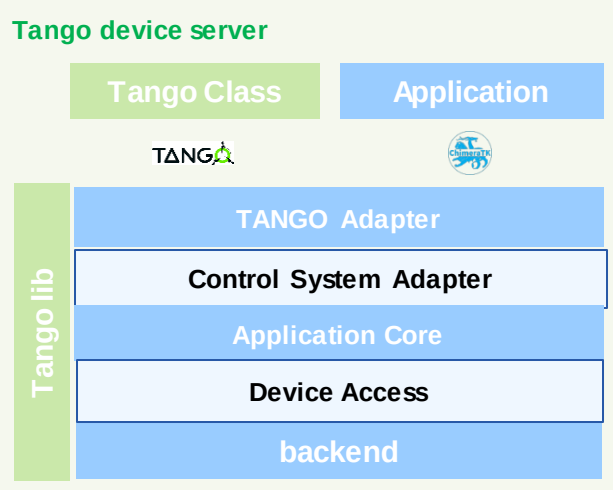


Second architecture

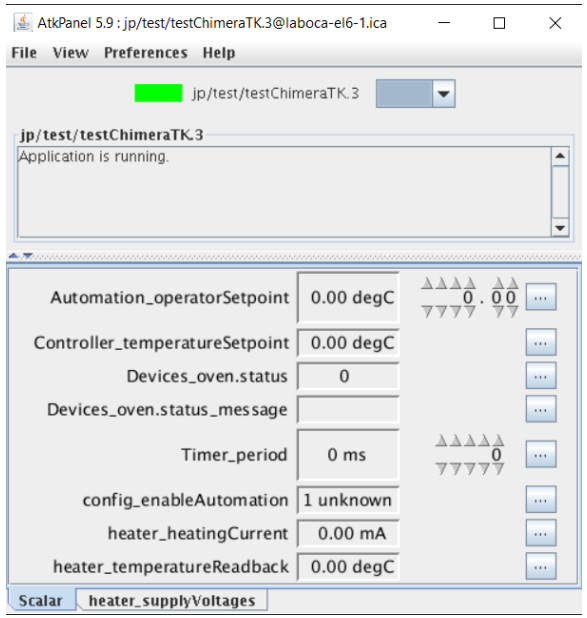
- Using ChimeraTK lib to communicate with MTCA FPGA over **PCIe-over-fiber** link
- Control system TangoAdapter lib adapts the variable to Tango device attributes
- Ongoing evaluation by Control system team

- Hot-swapping issue of PCIe-over-fiber is under investigation -> possible no go

MTCA integration strategy: CSA-TangoAdapter



- Create dynamic attributes by property configuration or auto-mode
  - –Scalar
  - –Spectrum
  - !Not support Image type
- Memory attributes and write hardware at init
  - – Scalar
  - – Spectrum (in progress– wait for correction in Tango)
- READ only / WRITE only attributes (correspoding to ChimeraTK process variable)
  - – *Inconvenient for Tango community who uses RW attributes*
- Cannot re-init the application

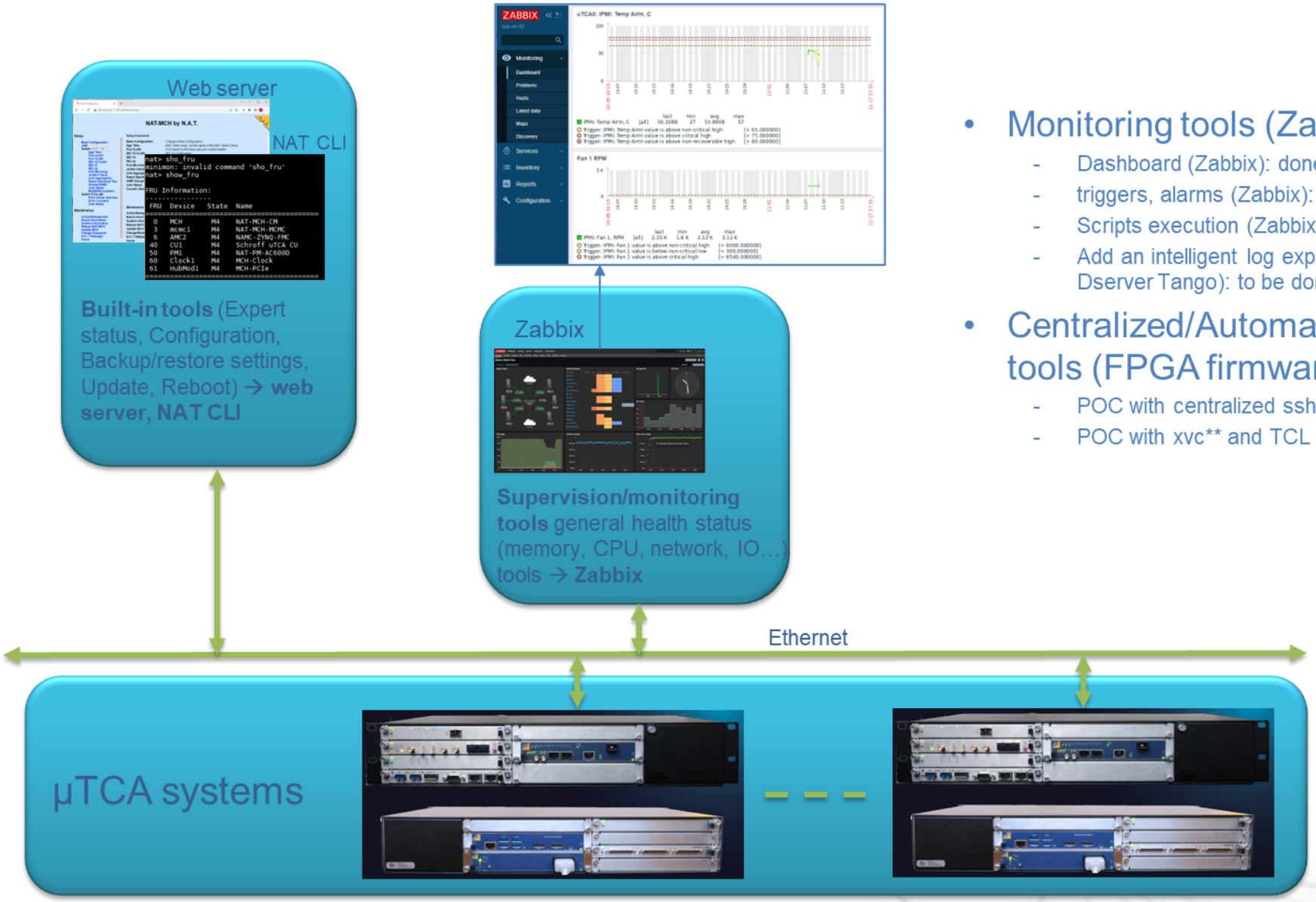


# name	nr of elements	address	size	bar	width	fracbits	signed	R/W
heater.temperatureReadback	1	0	4	0	32	16	0	RO
heater.heatingCurrent	1	4	4	0	32	16	0	RW
heater.supplyVoltages	4	11	16	0	32	16	0	RW

Property name	
AttributList	
DMapFilePath	/urs/Local/configFiles/example.dmap

❖ In collaboration with Desy

MicroTCA standardisation for SOLEIL - Monitoring/Administration Tools



- Monitoring tools (Zabbix): ongoing
  - Dashboard (Zabbix): done
  - triggers, alarms (Zabbix): done
  - Scripts execution (Zabbix): done
  - Add an intelligent log exploitation service (ELK*) (Zabbix, Dserver Tango): to be done
- Centralized/Automated Firmware update tools (FPGA firmwares …): ongoing
  - POC with centralized ssh scripts: ongoing
  - POC with xvc** and TCL scripts: ongoing

*: **E**lastik, **L**ogstash, **K**ibana
: **Xilinx **V**irtual **C**able

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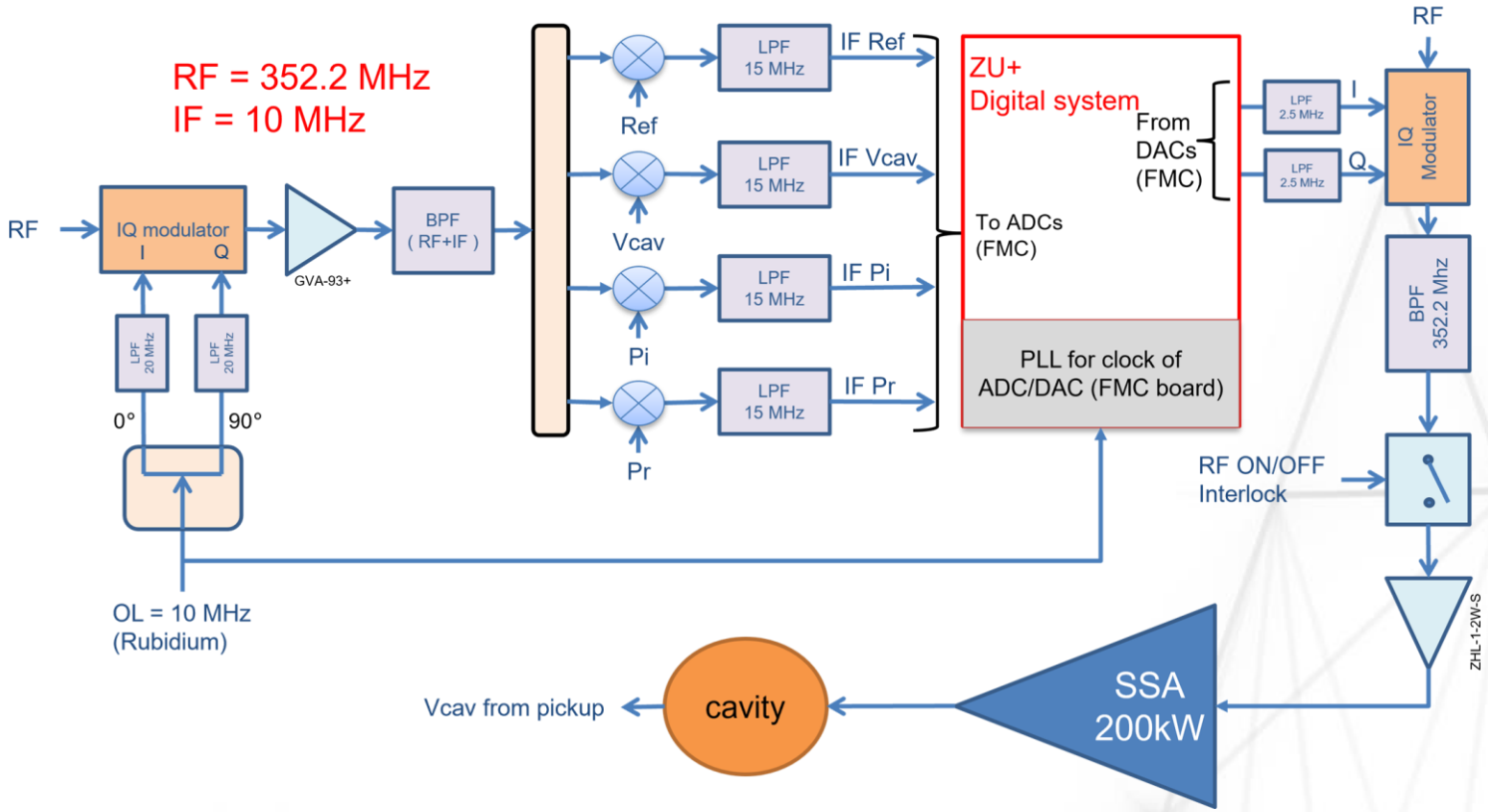
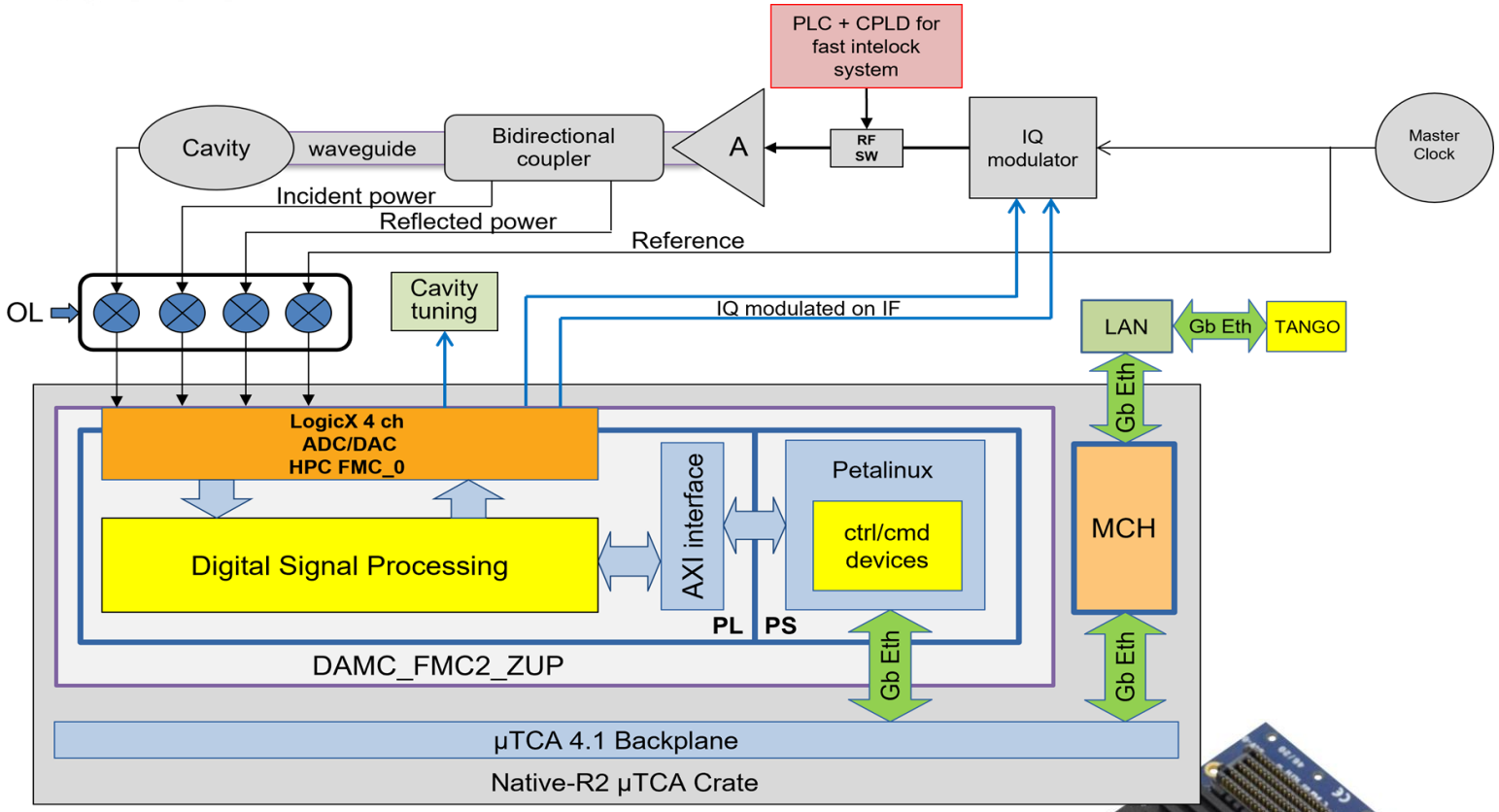
- Fast Orbit Feedback application at SOLEIL

MTCA for LLRF system

- Joined projects
  LUCRECE (LUNEX5: CW Linac)
  SOLEIL II
- LUCRECE specifications
  phase noise 0.01° rms
  amplitude precision 10^{-4}
- SOLEIL II specifications TDB
  Less demanding



LLRF tested and selected hardware



Tested

- ZC706 Zynq evaluation board
- Vadatech crate VT812: (8 AMCs + 4 RTMs + 2 MCHs + JSM + Telco Alarm)
- UTC002 (Vadatech MCH)
- AMC580 (Vadatech) => Zynq Ultrascale+ (ZU+) + 2 HPC FMCs
- FMC224 (Vadatech) => 4 CH DAC AC coupled (JESD204)
- FMC-4CH-125 (Techway)

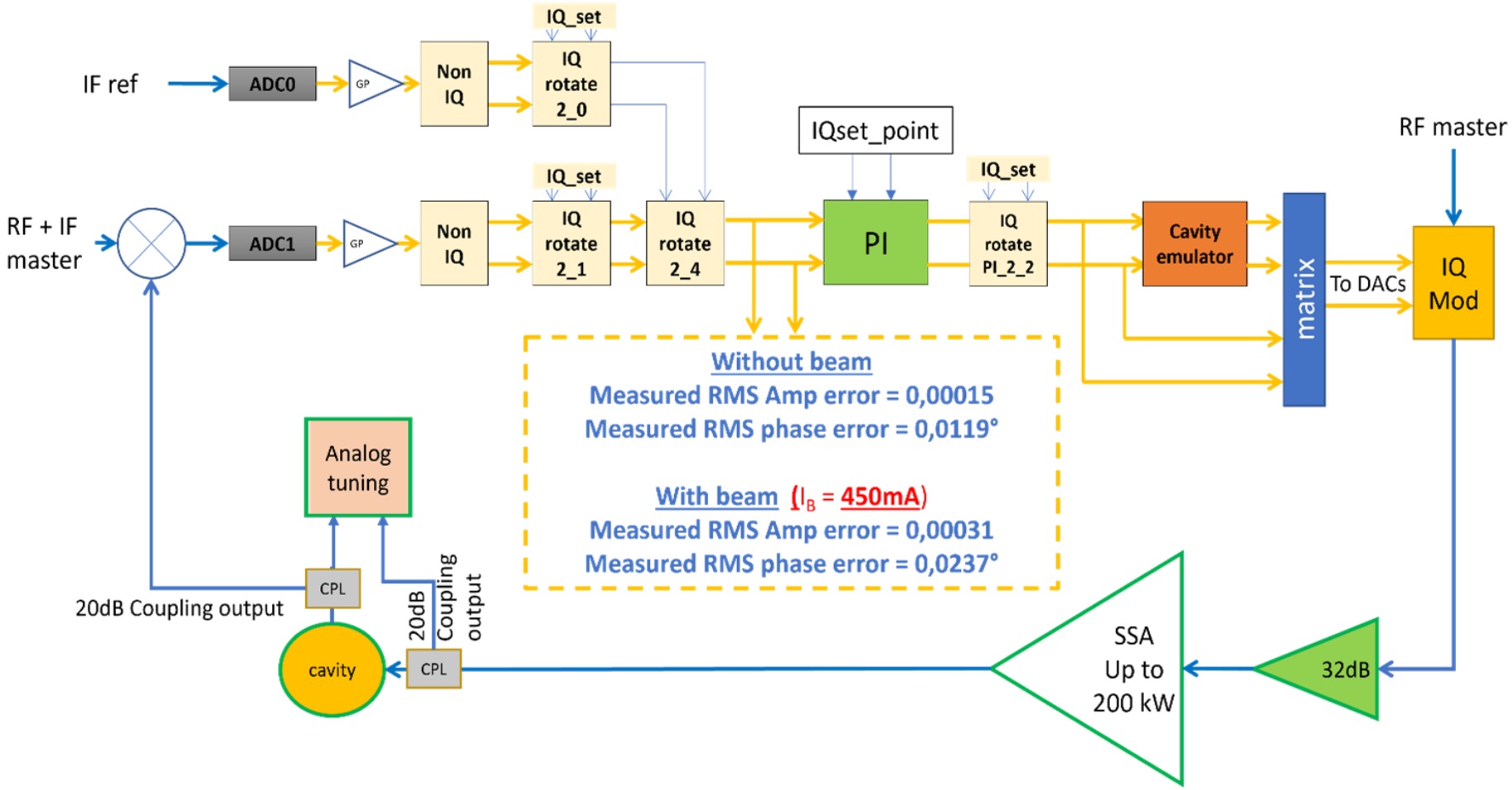
Digital systems

- Native-R2 µTCA platform, MCH-PHYS80 (Nat Europe)
- DAMC-FMC2ZUP (CAENels) => ZU+ + HPC FMC + HPC FMC+
- FMC LXD31K4-DC 4 channel 16-bit ADC/DAC (Logic-X)

RF analog components

- Mixer ADL5801 (Analog Devices)
- Amplifier GVA-93+, ZHL-1-2W-S (Mini-Circuits)
- PLL LTC6951 (implemented in the LXD31K4)
- IQ modulator LTC5598 (Analog Devices)
- Master clock synthetizer MXG5181B (Keysight)
- SRS Rubidium FS725 10 MHz Clock source

LLRF first tests at SOLEIL



Experimental results

First test on one of SOLEIL cavity with stored beam is a full success. The closed loop accuracy is :

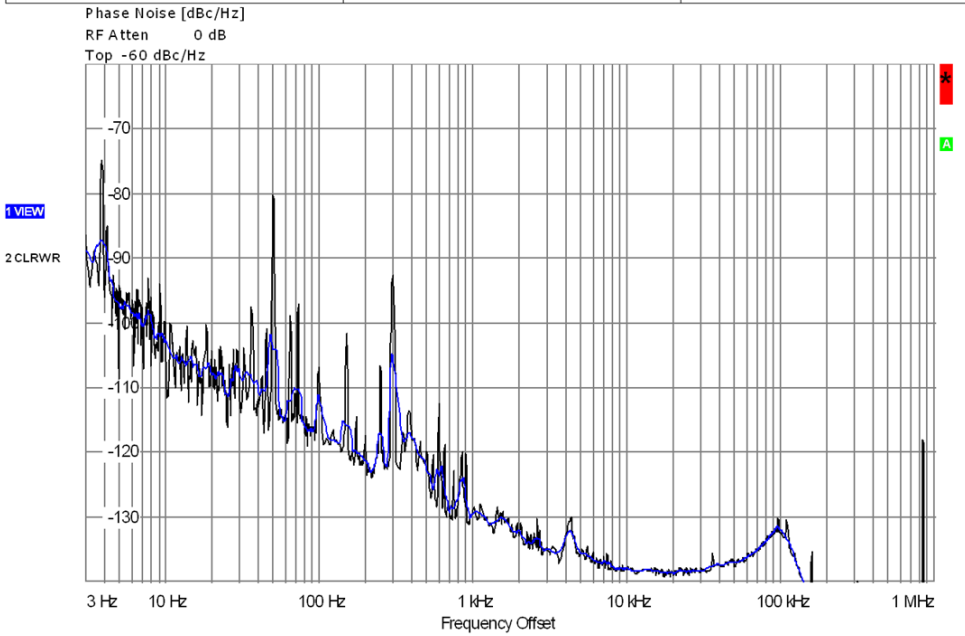
- 3×10^{-4} in amplitude
- 2.4×10^{-2}° rms in phase

LLRF results and next steps

Phase noise measurement on the cavity pickup (closed loop, Gain = 18) with 450 mA stored beam current

R&S FSUP 8 Signal Source Analyzer

Settings		Residual Noise [T1]		Spot Noise [T1]		
Signal Frequency:	352.197832 MHz	Int PHN (3.0 .. 1.0 M)	-80.1 dBc	1.000	kHz	-129.54 dBc/Hz
Signal Level:	-12.97 dBm	Residual PM	8.028 m°	10.000	kHz	-138.06 dBc/Hz
Analyzer Mode		Residual FM	18.49 Hz	100.000	kHz	-132.15 dBc/Hz
		RMS Jitter	0.0633 ps	1.000	MHz	-161.48 dBc/Hz



The phase noise of the cavity pickup signal is measured directly by the source analyzer. It corresponds to 0.06 ps, which is comparable to the present analog system.

Next steps

- Fixup on the ADC/DAC FMC : i2c for control
- Move analog cavity tuning to digital
- Add new feature for transfer function identification
- Integrate to control system

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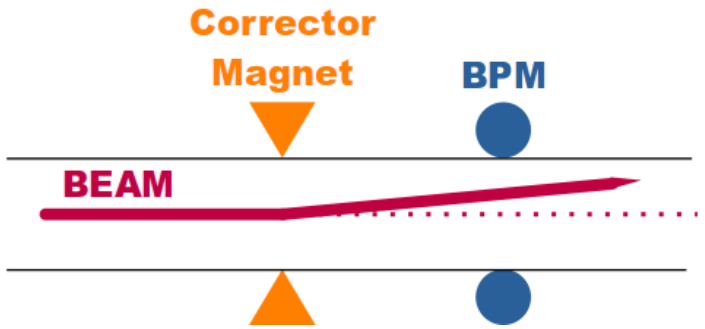
Fast Orbit Feedback application

- What's that ?
  - Measure position at 122 points (each plane)
  - Compute global compensation
  - Apply compensation at 50 points (each plane)
  - At 10kHz, minimize loop latency



- How to ?
  - CellNode: local interface for aggregation & distribution
  - CentralNode: computation, data acquisition

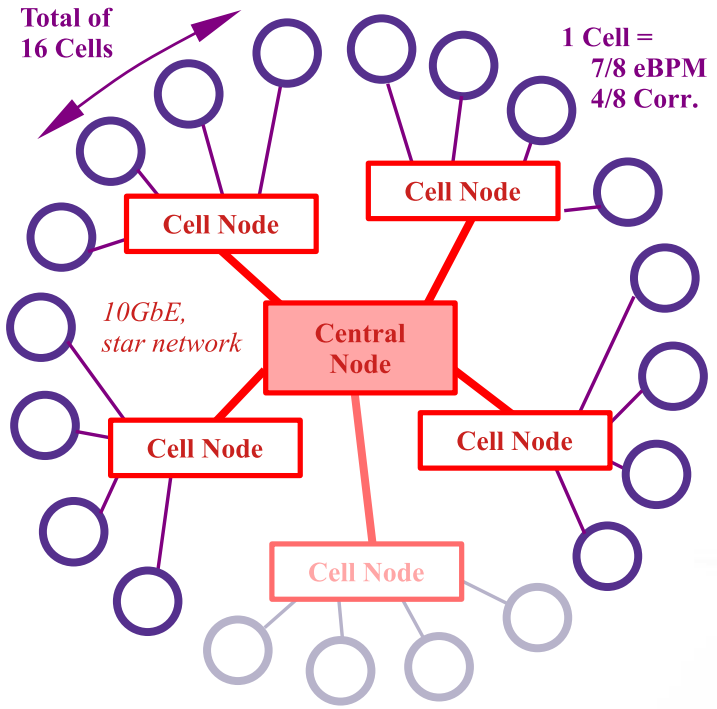
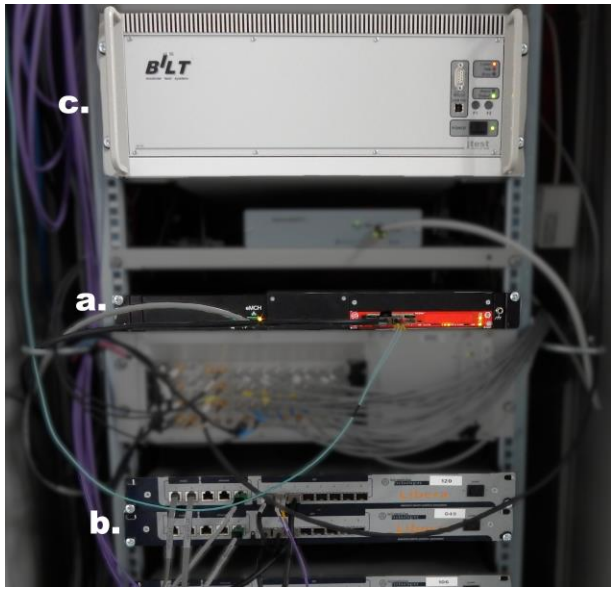
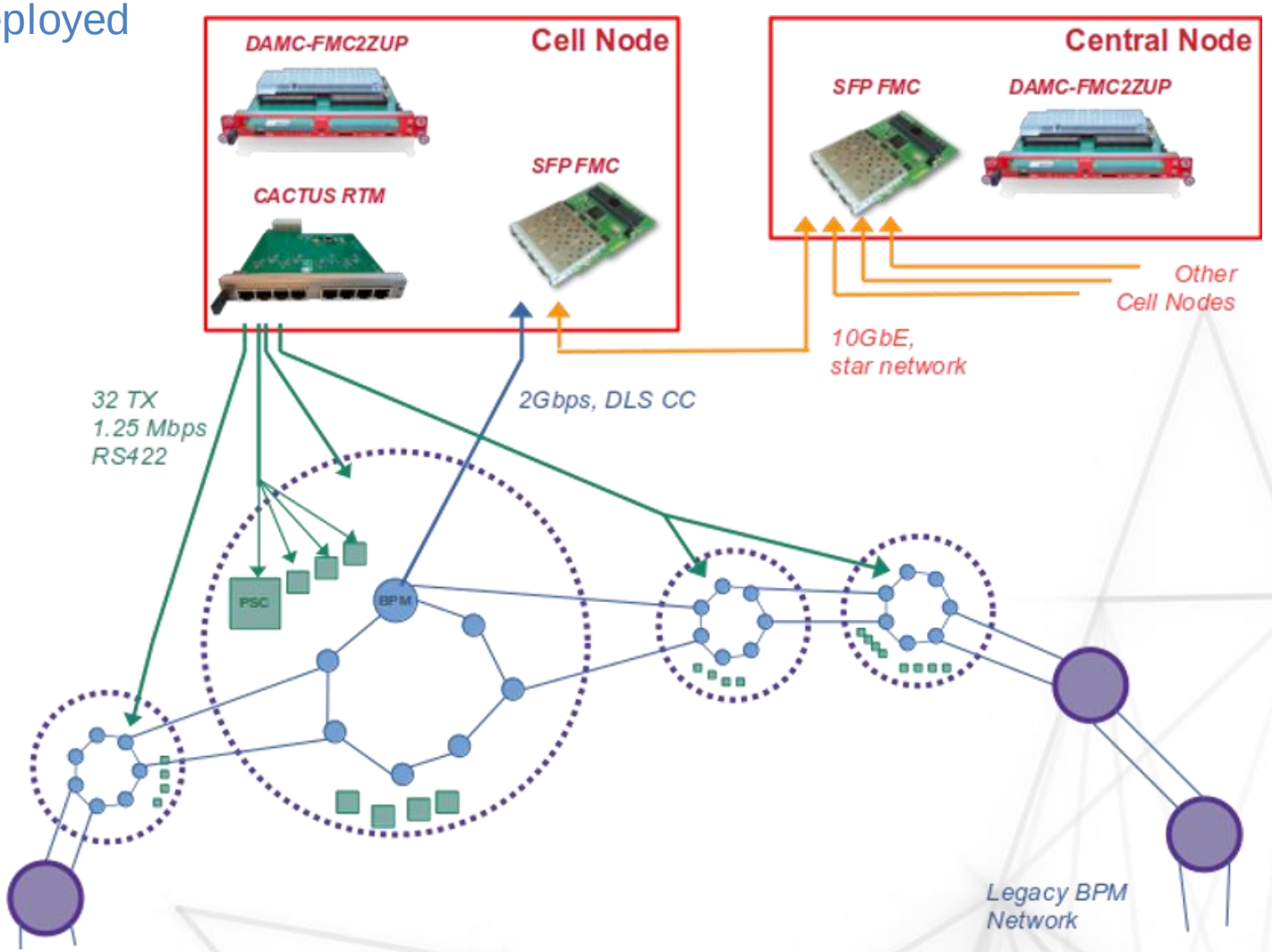


Figure 1 - Proposed two level star topology. As SOLEIL II increases the number of systems, the network will expand by adding a Cell Node.

System integration

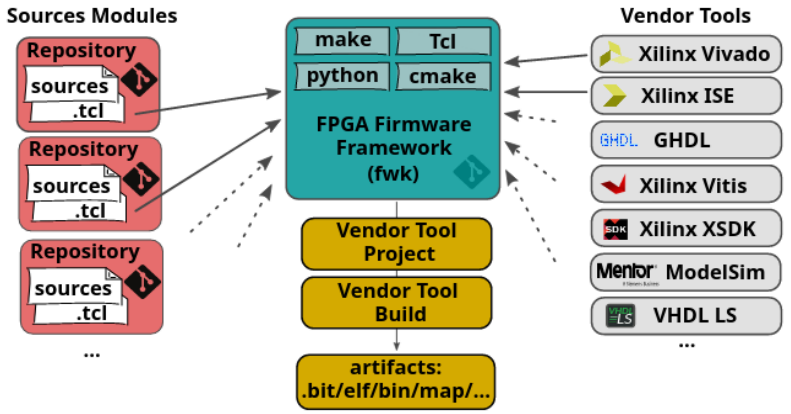
- Cell/Central Node base platform, 5 units deployed
  - nVent NATIVE-R1
  - CaenELS DAMC-FMC2ZUP
  - CaenELS 4SFP+ FMC
  - Custom RTM CACTUS (32 TX RS422)
- Dedicated networks
  - CellNodes tap in BPM ring network
  - Inter Node dedicated star network
  - CellNodes to PSC Star network

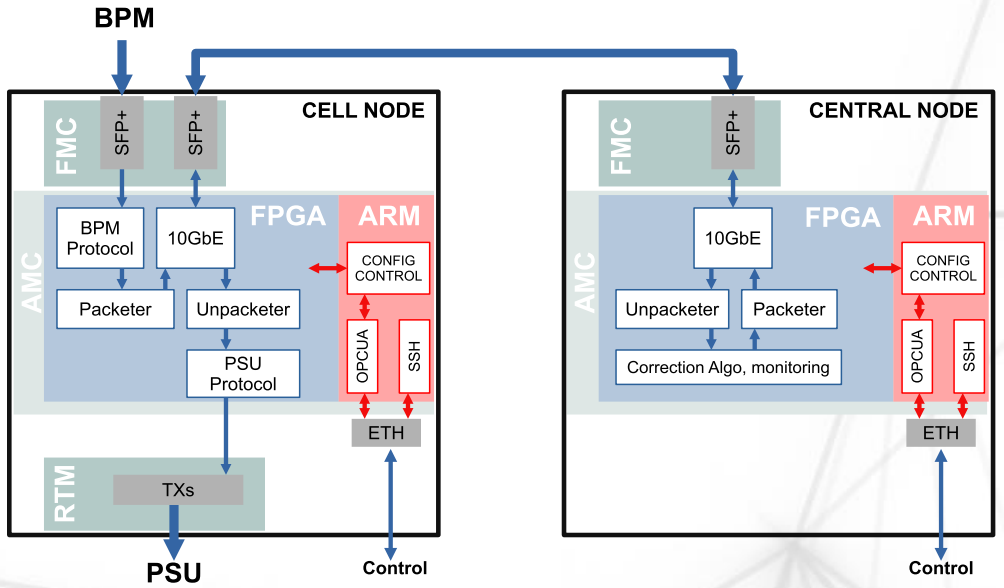




FPGA Firmware & Embedded linux

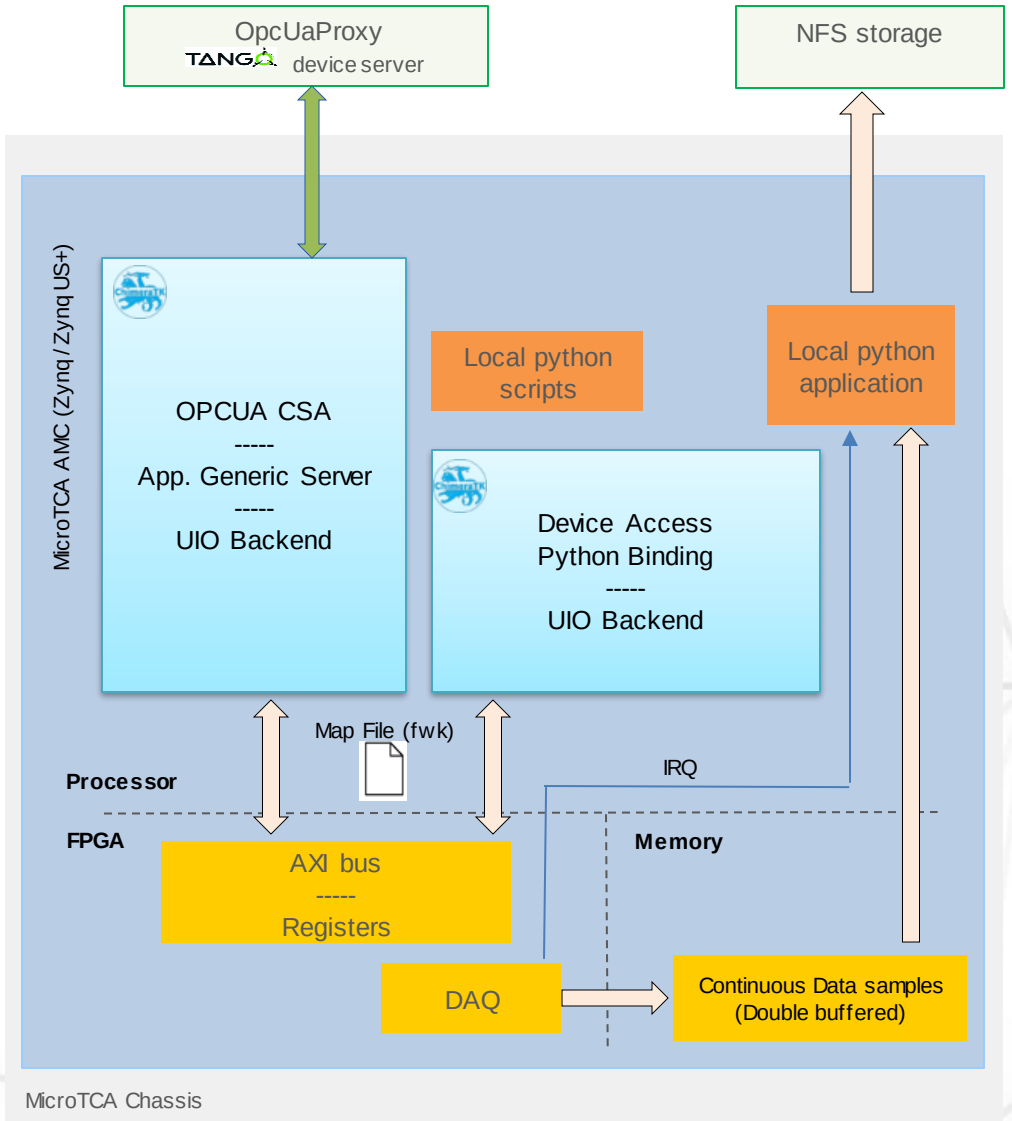
- FPGA FW made with DESY's FWK
  - 2 configurations: CellNode & CentralNode
  - Based on common blocks
    - 8 home made
  - BSP and DAQ from DESY MSK
    - Contribution on corrections and modifications no PCIe, DAQ IRQ signal, bugfixes...
- Embedded linux cross-compiled with Yocto/bitbake
  - Use meta-layers from Techlab and DESY MSK
    - DAMC-FMC2ZUP platform
    - ChimeraTK
  - Dedicated meta-layer for SOLEIL
    - Image wrap-up
    - Configuration & start at boot
    - Application





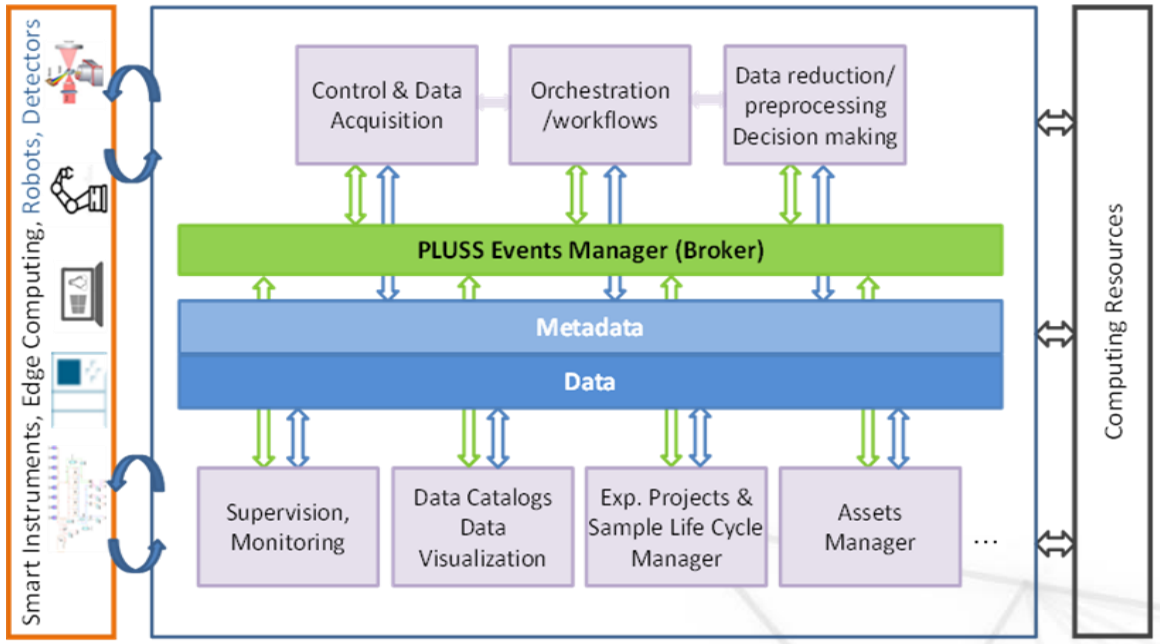
Interface to control system

- Local python prompt/script
  - ChimeraTK DeviceAccess binding
- OPCUA generic server
  - From DESY MSK
- FPGA register via Linux UIO
  - Register mapping obtained from FWK flow
- Prototype continuous capture
  - 2 DAQ regions push data samples to dual buffers
  - IRQ when buffer switch
  - Copy data from shared memory
  - Write to NFS storage (20 MBps)



Conclusion

- MTCA based systems are being installed at SOLEIL
  LLRF, FOFB
- Integration to Control System ongoing, relying on ChimeraTK and FWK
- All this work paves the way to SOLEIL II, Dark period is scheduled to start in October 2028
- The systems will be integrated in the SI target architecture



Core Data Architecture